2.1 Ω On Resistance, ±15 V/+12 V/±5 V *i*CMOS Dual SPST Switches

Data Sheet

ADG1421/ADG1422/ADG1423

FEATURES

2.1 Ω on resistance
0.5 Ω maximum on resistance flatness
Up to 250 mA continuous current
Fully specified at +12 V, ±15 V, ±5 V
No V_L supply required
3 V logic-compatible inputs
Rail-to-rail operation
10-lead MSOP and 10-lead, 3 mm × 3 mm LFCSP packages

APPLICATIONS

Automatic test equipment
Data acquisition systems
Relay replacements
Battery-powered systems
Sample-and-hold systems
Audio signal routing
Video signal routing
Communication systems

FUNCTIONAL BLOCK DIAGRAM

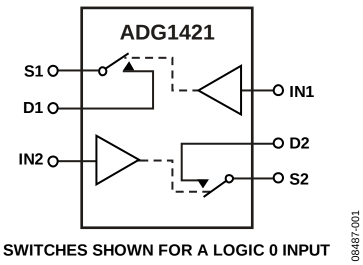

Figure 1. ADG1421 Functional Block Diagram

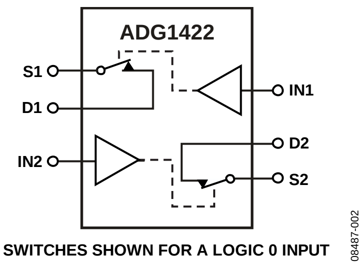

Figure 2. ADG1422 Functional Block Diagram

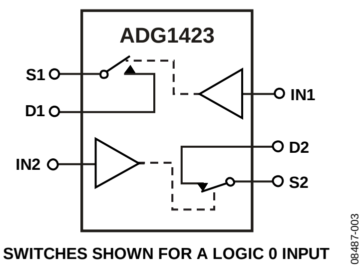

Figure 3. ADG1423 Functional Block Diagram

GENERAL DESCRIPTION

The ADG1421/ADG1422/ADG1423 contain two independent single-pole/single-throw (SPST) switches. The ADG1421 and ADG1422 differ only in that the digital control logic is inverted. The ADG1421 switches are turned on with Logic 1 on the appropriate control input, and Logic 0 is required for the ADG1422. The ADG1423 has one switch with digital control logic similar to that of the ADG1421; the logic is inverted on the other switch. The ADG1423 exhibits break-before-make switching action for use in multiplexer applications. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

The *i*CMOS® (industrial CMOS) modular manufacturing process combines high voltage, complementary metal-oxide semiconductor (CMOS) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no other generation of high voltage parts has achieved. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The on resistance profile is very flat over the full analog input range ensuring excellent linearity and low distortion when switching audio signals. The *i*CMOS construction ensures ultralow power dissipation, making the part ideally suited for portable and battery-powered instruments.

PRODUCT HIGHLIGHTS

1. 2.4 Ω maximum on resistance at 25°C.
2. Minimum distortion.
3. 3 V logic-compatible digital inputs: V_{INH} = 2.0 V, V_{INL} = 0.8 V.
4. No V_L logic power supply required.
5. 10-lead MSOP and 10-lead, 3 mm × 3 mm LFCSP packages.

Rev. A Document Feedback

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REVISION HISTORY

7/14—Rev. 0 to Rev. A

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10/09—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +105°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range				V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	2.1				Ω typ	V_S = ±10 V, I_S = −10 mA; see Figure 23
	2.4	2.8	2.95	3.2	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On Resistance Match Between Channels, ΔR_{ON}	0.02				Ω typ	V_S = ±10 V, I_S = −10 mA
	0.1	0.12	0.124	0.13	Ω max	
On Resistance Flatness, $R_{FLAT (ON)}$	0.4				Ω typ	V_S = ±10 V, I_S = −10 mA
	0.5	0.6	0.63	0.65	Ω max	
LEAKAGE CURRENTS						V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.1				nA typ	V_S = ±10 V, V_D = ±10 V; see Figure 24
	±0.5	±2	±9	±75	nA max	
Drain Off Leakage, I_D (Off)	±0.1				nA typ	V_S = ±10 V, V_D = ±10 V; see Figure 24
	±0.5	±2	±9	±75	nA max	
Channel On Leakage, I_D, I_S (On)	±0.2				nA typ	V_S = V_D = ±10 V; see Figure 25
	±1	±2	±9	±75	nA max	
DIGITAL INPUTS						
Input High Voltage, V_{INH}				2.0	V min	
Input Low Voltage, V_{INL}				0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005				μA typ	V_{IN} = V_{GND} or V_{DD}
				±0.1	μA max	
Digital Input Capacitance, C_{IN}	4				pF typ	
DYNAMIC CHARACTERISTICS[1]						
t_{ON}	115				ns typ	R_L = 300 Ω, C_L = 35 pF
	145	180		210	ns max	V_S = 10 V; see Figure 26
t_{OFF}	115				ns typ	R_L = 300 Ω, C_L = 35 pF
	145	165		190	ns max	V_S = 10 V; see Figure 26
Break-Before-Make Time Delay, t_D (ADG1423 Only)	45				ns typ	R_L = 300 Ω, C_L = 35 pF
				30	ns min	V_{S1} = V_{S2} = 10 V; see Figure 27
Charge Injection	−5				pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 28
Off Isolation	−64				dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
Channel-to-Channel Crosstalk	−74				dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 30
Total Harmonic Distortion + Noise	0.016				% typ	R_L = 10 kΩ, 5 V rms, f = 20 Hz to 20 kHz; see Figure 32
−3 dB Bandwidth	180				MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 31
Insertion Loss	0.12				dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 31
C_S (Off)	18				pF typ	f = 1 MHz; V_S = 0 V
C_D (Off)	22				pF typ	f = 1 MHz; V_S = 0 V
C_D, C_S (On)	86				pF typ	f = 1 MHz; V_S = 0 V
POWER REQUIREMENTS						V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	0.002				μA typ	Digital inputs = 0 V or V_{DD}
				1.0	μA max	
I_{DD}	120				μA typ	Digital inputs = 5 V
				190	μA max	
I_{SS}	0.002				μA typ	Digital inputs = 0 V, 5 V, or V_{DD}
				1.0	μA max	
V_{DD}/V_{SS}				±4.5/±16.5	V min/max	Ground = 0 V

[1] Guaranteed by design, not subject to production test.

+12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	4			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA; see Figure 23
	4.6	5.5	6.2	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On Resistance Match Between Channels, ΔR_{ON}	0.03			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	0.15	0.17	0.18	Ω max	
On Resistance Flatness, $R_{FLAT (ON)}$	1.2			Ω typ	V_S = 0V to 10 V, I_S = −10 mA
	1.5	1.75	1.9	Ω max	
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 24
	±0.5	±2	±75	nA max	
Drain Off Leakage, I_D (Off)	±0.05			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 24
	±0.5	±2	±75	nA max	
Channel On Leakage, I_D, I_S (On)	±0.1			nA typ	V_S = V_D = 1 V or 10 V; see Figure 25
	±1	±2	±75	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	180			ns typ	R_L = 300 Ω, C_L = 35 pF
	230	295	340	ns max	V_S = 8 V; see Figure 26
t_{OFF}	130			ns typ	R_L = 300 Ω, C_L = 35 pF
	165	205	235	ns max	V_S = 8 V; see Figure 26
Break-Before-Make Time Delay, t_D (ADG1423 Only)	70			ns typ	R_L = 300 Ω, C_L = 35 pF
			48	ns min	V_{S1} = V_{S2} = 8 V; see Figure 27
Charge Injection	30			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 28
Off Isolation	−60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
Channel-to-Channel Crosstalk	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 30
−3 dB Bandwidth	140			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 31
Insertion Loss	0.26			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 31
C_S (Off)	31			pF typ	f = 1 MHz; V_S = 6 V
C_D (Off)	36			pF typ	f = 1 MHz; V_S = 6 V
C_D, C_S (On)	90			pF typ	f = 1 MHz; V_S = 6 V
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
I_{DD}	120			μA typ	Digital inputs = 5 V
			190	μA max	
V_{DD}			5/16.5	V min/max	Ground = 0 V, V_{SS} = 0 V

[1] Guaranteed by design, not subject to production test.

±5 V DUAL SUPPLY

V_{DD} = +5 V ± 10%, V_{SS} = −5 V ± 10%, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	4.5			Ω typ	V_S = ±4.5 V, I_S = −10 mA; see Figure 23
	5.2	6.2	7	Ω max	V_{DD} = +4.5 V, V_{SS} = −4.5 V
On Resistance Match Between Channels, ΔR_{ON}	0.04			Ω typ	V_S = ±4.5V; I_S = −10 mA
	0.18	0.2	0.21	Ω max	
On Resistance Flatness, $R_{FLAT (ON)}$	1.3			Ω typ	V_S = ±4.5 V, I_S = −10 mA
	1.6	1.85	2	Ω max	
LEAKAGE CURRENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V; see Figure 24
	±0.5	±2	±75	nA max	
Drain Off Leakage, I_D (Off)	±0.05			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V; see Figure 24
	±0.5	±2	±75	nA max	
Channel On Leakage, I_D, I_S (On)	±0.1			nA typ	V_S = V_D = ±4.5 V; see Figure 25
	±1	±2	±75	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			µA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	µA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	285			ns typ	R_L = 300 Ω, C_L = 35 pF
	370	460	520	ns max	V_S = 3 V; see Figure 26
t_{OFF}	220			ns typ	R_L = 300 Ω, C_L = 35 pF
	295	350	395	ns max	V_S = 3 V; see Figure 26
Break-Before-Make Time Delay, t_D (ADG1423 Only)	85			ns typ	R_L = 300 Ω, C_L = 35 pF
			45	ns min	V_{S1} = V_{S2} = 3 V; see Figure 27
Charge Injection	82			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 28
Off Isolation	−60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
Channel-to-Channel Crosstalk	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 30
Total Harmonic Distortion + Noise	0.04			% typ	R_L = 10 kΩ, 5 V p-p, f = 20 Hz to 20 kHz; see Figure 32
−3 dB Bandwidth	150			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 31
Insertion Loss	0.25			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 31
C_S (Off)	25			pF typ	V_S = 0V, f = 1 MHz
C_D (Off)	30			pF typ	V_S = 0V, f = 1 MHz
C_D, C_S (On)	100			pF typ	V_S = 0V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 5.5 V, V_{SS} = −5.5 V
I_{DD}	0.001			µA typ	Digital inputs = 0 V or V_{DD}
			1.0	µA max	
I_{SS}	0.001			µA typ	Digital inputs = 0 V or V_{DD}
			1.0	µA max	
V_{DD}/V_{SS}			±4.5/±16.5	V min/max	Ground = 0 V

[1] Guaranteed by design, not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, S OR D

Table 4.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT PER CHANNEL[1]					
±15 V Dual Supply					V_{DD} = +13.5 V, V_{SS} = −13.5 V
10-Lead MSOP (θ_{JA} = 142°C/W)	185	120	75	mA maximum	
10-Lead LFCSP (θ_{JA} = 76°C/W)	250	155	85	mA maximum	
+12 V Single Supply					V_{DD} = 10.8 V, V_{SS} = 0 V
10-Lead MSOP (θ_{JA} = 142°C/W)	150	100	65	mA maximum	
10-Lead LFCSP (θ_{JA} = 76°C/W)	205	130	80	mA maximum	
±5 V Dual Supply					V_{DD} = +4.5 V, V_{SS} = −4.5 V
10-Lead MSOP (θ_{JA} = 142°C/W)	145	100	65	mA maximum	
10-Lead LFCSP (θ_{JA} = 76°C/W)	195	125	75	mA maximum	

[1] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	GND − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D (Pulsed at 1 ms, 10% Duty-Cycle Maximum)	
10-Lead MSOP (4-Layer Board)	300 mA
10-Lead LFCSP	400 mA
Continuous Current per Channel, S or D	Data in Table 4 + 15% mA
Operating Temperature Range	
Industrial	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Reflow Soldering Peak Temperature, Pb Free	260°C

[1] Over voltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
10-Lead MSOP (4-Layer Board)	142	44	°C/W
10-Lead LFCSP	76		°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

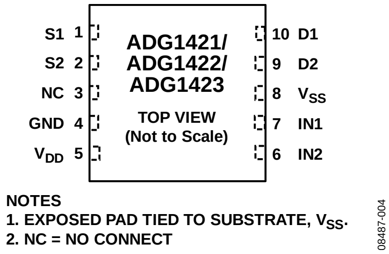

Figure 4. 10-Lead LFCSP Pin Configuration

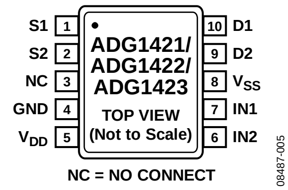

Figure 5. 10-Lead MSOP Pin Configuration

Table 7. 10-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	S1	Source Terminal. This pin can be an input or output.
2	S2	Source Terminal. This pin can be an input or output.
3	NC	No Connect.
4	GND	Ground (0 V) Reference.
5	V_{DD}	Most Positive Power Supply Potential.
6	IN2	Logic Control Input.
7	IN1	Logic Control Input.
8	V_{SS}	Most Negative Power Supply Potential.
9	D2	Drain Terminal. This pin can be an input or output.
10	D1	Drain Terminal. This pin can be an input or output.
	EPAD	Exposed pad tied to substrate, V_{SS}.

Table 8. 10-Lead MSOP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	S1	Source Terminal. This pin can be an input or output.
2	S2	Source Terminal. This pin can be an input or output.
3	NC	No Connect.
4	GND	Ground (0 V) Reference.
5	V_{DD}	Most Positive Power Supply Potential.
6	IN2	Logic Control Input.
7	IN1	Logic Control Input.
8	V_{SS}	Most Negative Power Supply Potential.
9	D2	Drain Terminal. This pin can be an input or output.
10	D1	Drain Terminal. This pin can be an input or output.

Table 9. ADG1421/ADG1422 Truth Table

ADG1421 INx	ADG1422 INx	Switch Condition
1	0	On
0	1	Off

Table 10. ADG1423 Truth Table

ADG1423 INx	Switch 1 Condition	Switch 2 Condition
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

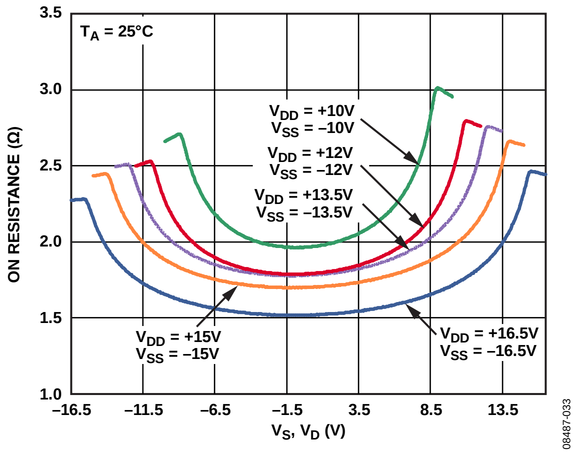

Figure 6. On Resistance as a Function of V_D (V_S) for Dual Supply

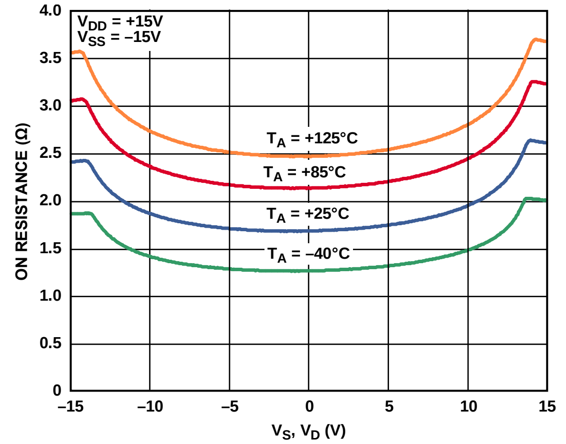

Figure 9. On Resistance as a Function of V_D (V_S) for Different Temperatures, ±15 V Dual Supply

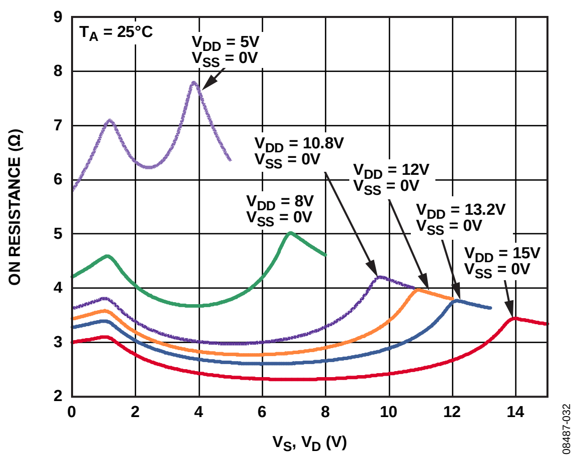

Figure 7. On Resistance as a Function of V_D (V_S) for Single Supply

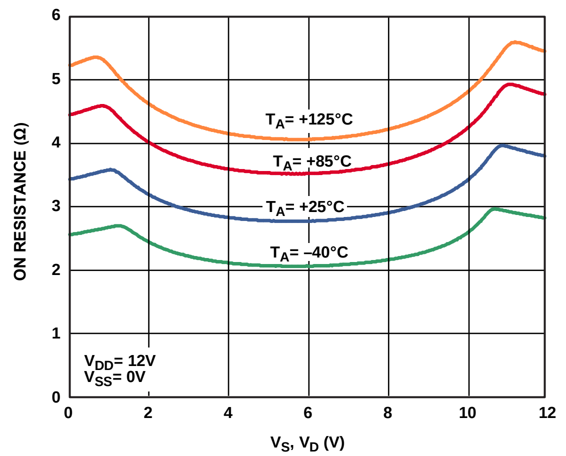

Figure 10. On Resistance as a Function of V_D (V_S) for Different Temperatures, +12 V Single Supply

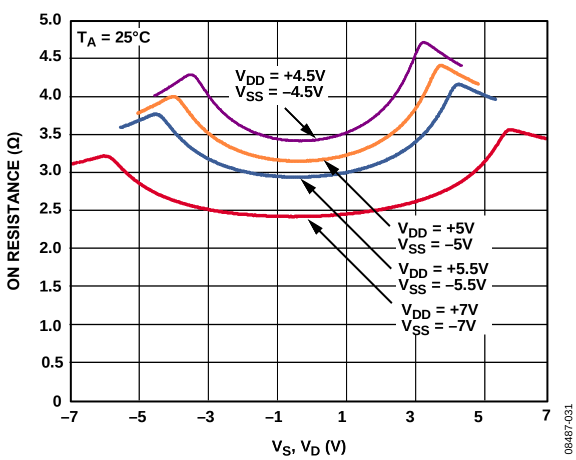

Figure 8. On Resistance as a Function of V_D (V_S) for Dual Supply

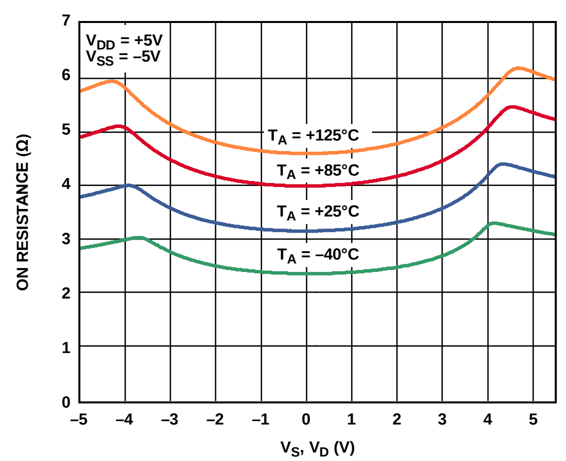

Figure 11. On Resistance as a Function of V_D (V_S) for Different Temperatures, ±5 V Dual Supply

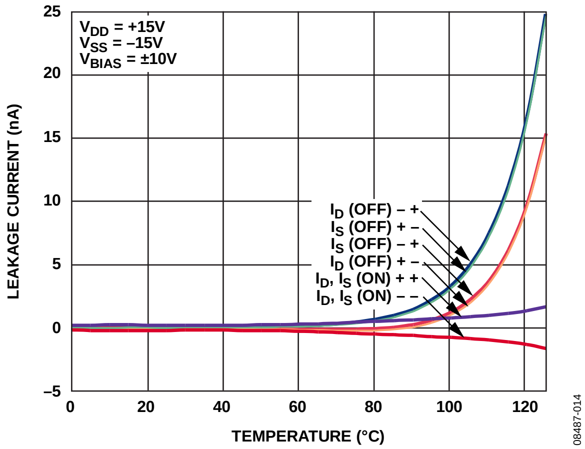

Figure 12. Leakage Currents as a Function of Temperature, ±15 V Dual Supply

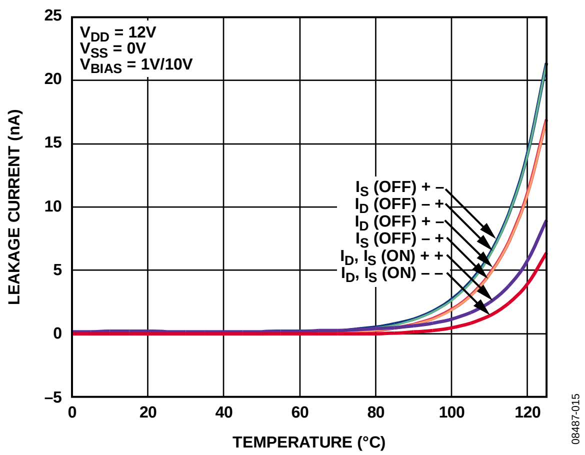

Figure 13. Leakage Currents as a Function of Temperature, +12 V Single Supply

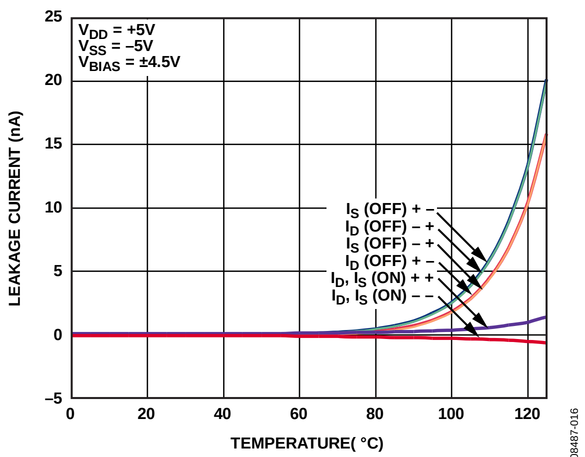

Figure 14. Leakage Currents as a Function of Temperature, ±5 V Dual Supply

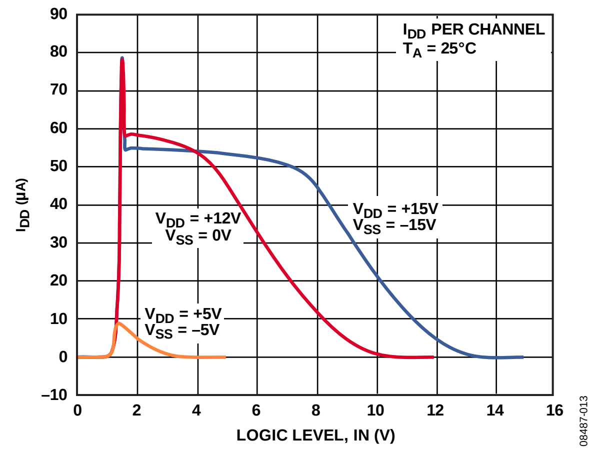

Figure 15. I_{DD} vs. Logic Level

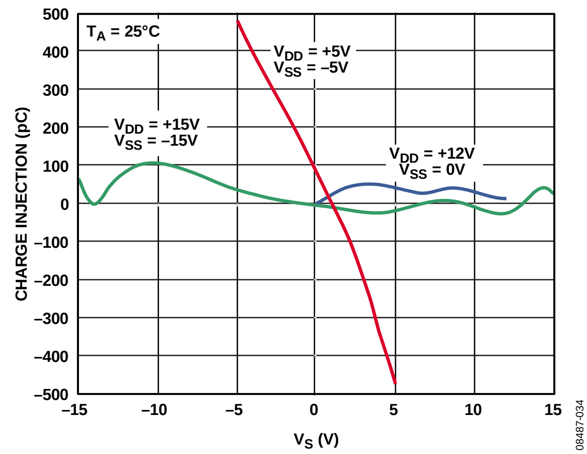

Figure 16. Charge Injection vs. Source Voltage

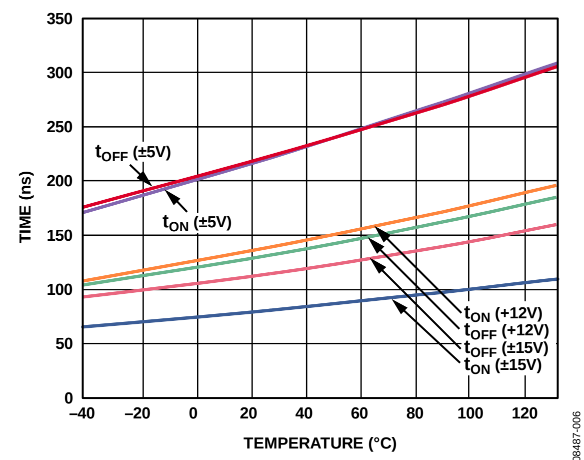

Figure 17. $t_{TRANSITION}$ Times vs. Temperature

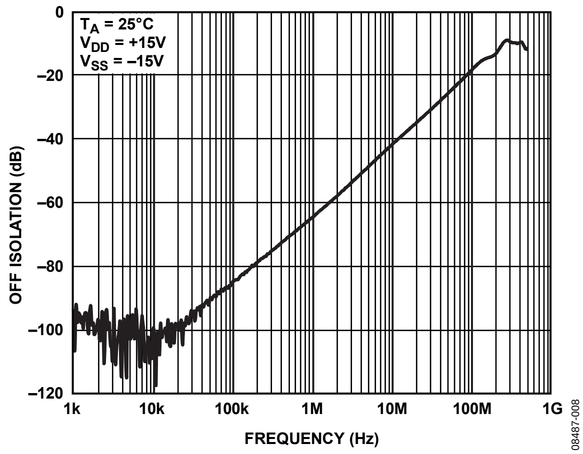

Figure 18. Off Isolation vs. Frequency

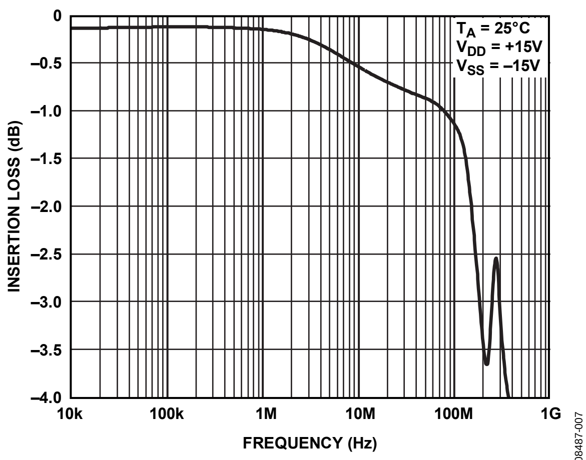

Figure 19. On Response vs. Frequency

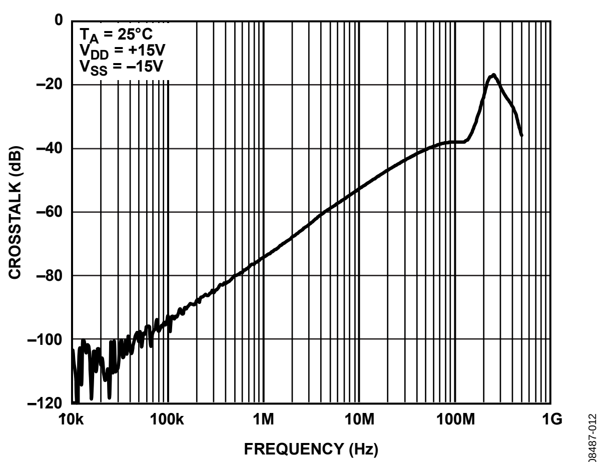

Figure 20. Crosstalk vs. Frequency

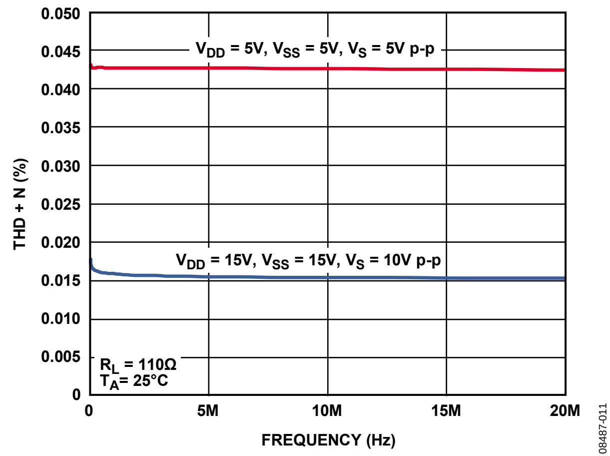

Figure 21. THD + N vs. Frequency

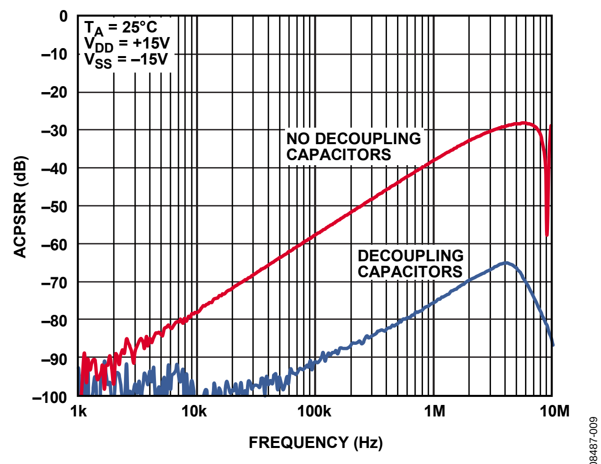

Figure 22. ACPSRR vs. Frequency

TEST CIRCUITS

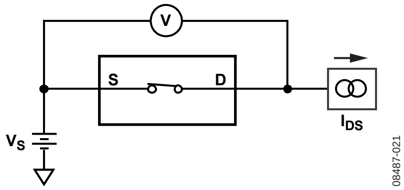

Figure 23. On Resistance

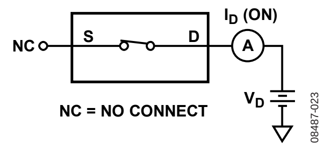

Figure 25. On Leakage

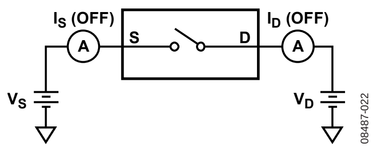

Figure 24. Off Leakage

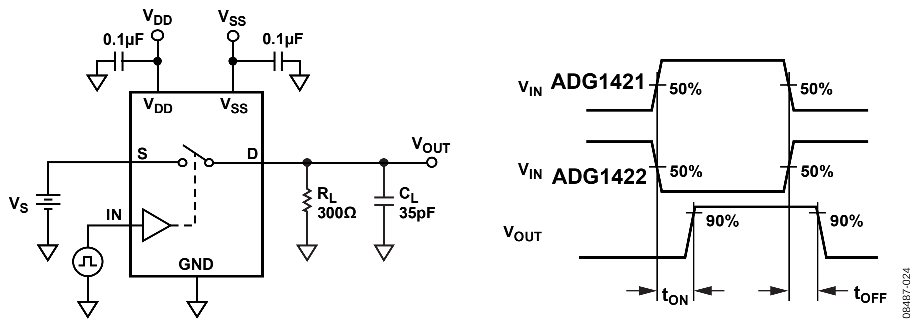

Figure 26. Switching Times

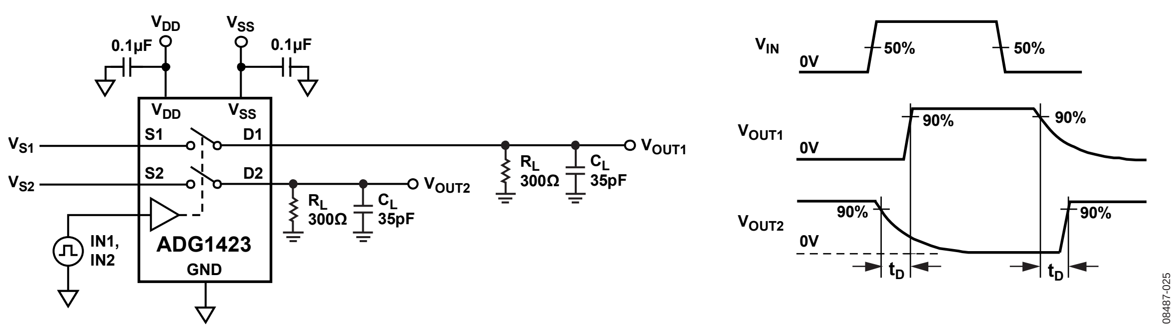

Figure 27. Break-Before-Make Time Delay

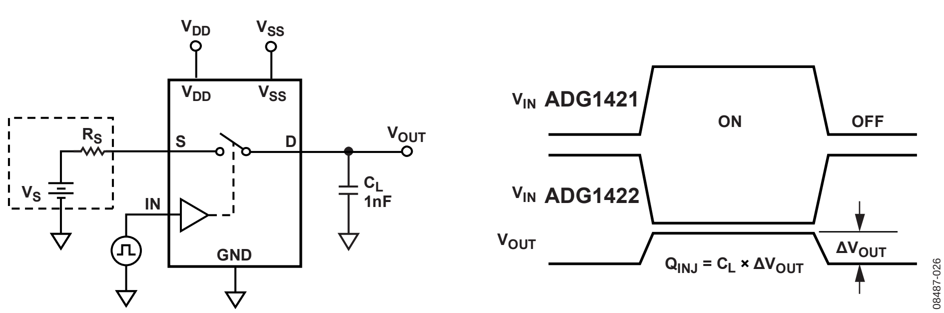

Figure 28. Charge Injection

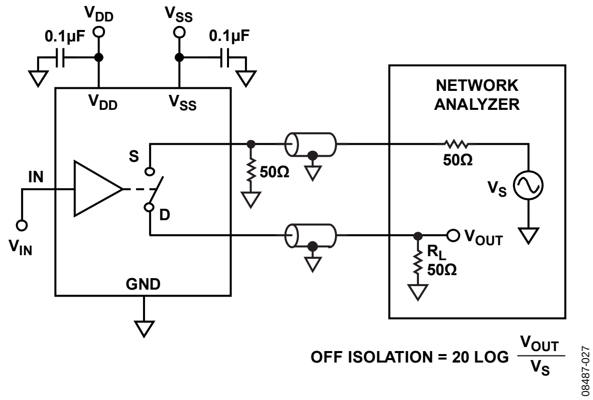

Figure 29. Off Isolation

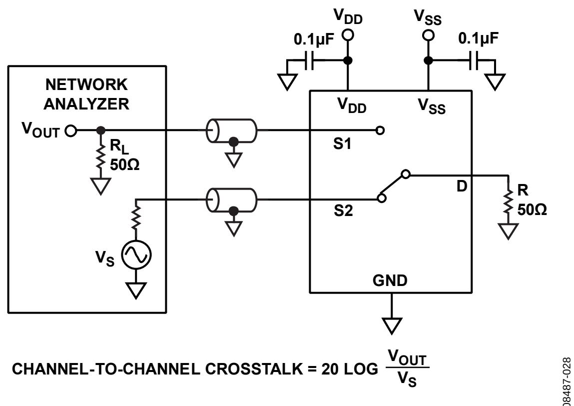

Figure 30. Channel-to-Channel Crosstalk

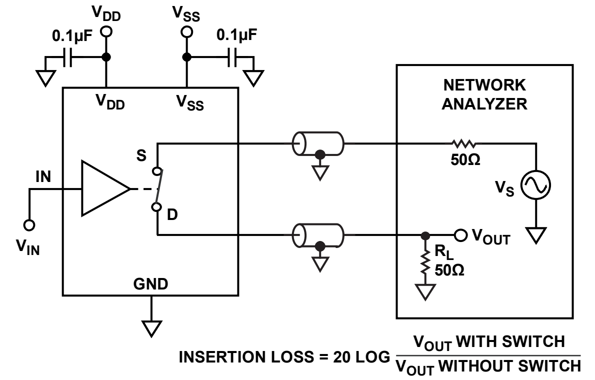

Figure 31. Bandwidth

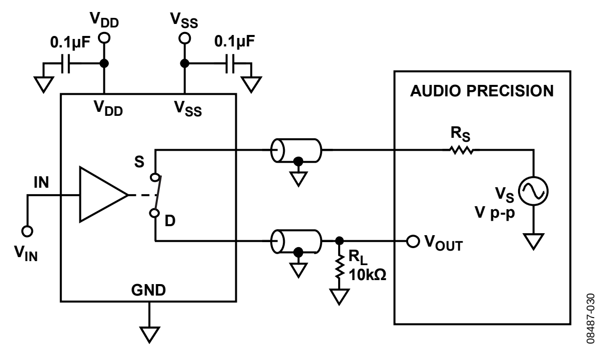

Figure 32. THD + N

TERMINOLOGY

I_{DD}
The positive supply current.

I_{SS}
The negative supply current.

V_D (V_S)
The analog voltage on Terminal D and Terminal S.

R_{ON}
The ohmic resistance between Terminal D and Terminal S.

$R_{FLAT (ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

I_S (Off)
The source leakage current with the switch off.

I_D (Off)
The drain leakage current with the switch off.

I_D, I_S (On)
The channel leakage current with the switch on.

V_{INL}
The maximum input voltage for Logic 0.

V_{INH}
The minimum input voltage for Logic 1.

I_{INL} (I_{INH})
The input current of the digital input.

C_S (Off)
The off switch source capacitance, measured with reference to ground.

C_D (Off)
The off switch drain capacitance, measured with reference to ground.

C_D, C_S (On)
The on switch capacitance, measured with reference to ground.

C_{IN}
The digital input capacitance.

t_{ON} (EN)
Delay time between the 50% and 90% points of the digital input and switch on condition. See Figure 26.

t_{OFF} (EN)
Delay time between the 50% and 90% points of the digital input and switch off condition. See Figure 26.

$t_{TRANSITION}$
Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

T_{BBM}
Off time measured between the 80% point of both switches when switching from one address state to another. See Figure 27.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching. See Figure 28.

Off Isolation
A measure of unwanted signal coupling through an off switch. See Figure 29.

Crosstalk
A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. See Figure 30.

Bandwidth
The frequency at which the output is attenuated by 3 dB. See Figure 31.

On Response
The frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch. See Figure 31.

THD + N
The ratio of the harmonic amplitude plus noise of the signal to the fundamental. See Figure 32.

AC Power Supply Rejection Ratio (ACPSRR)
ACPSRR measures the ability of a part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR. See Figure 22.

OUTLINE DIMENSIONS

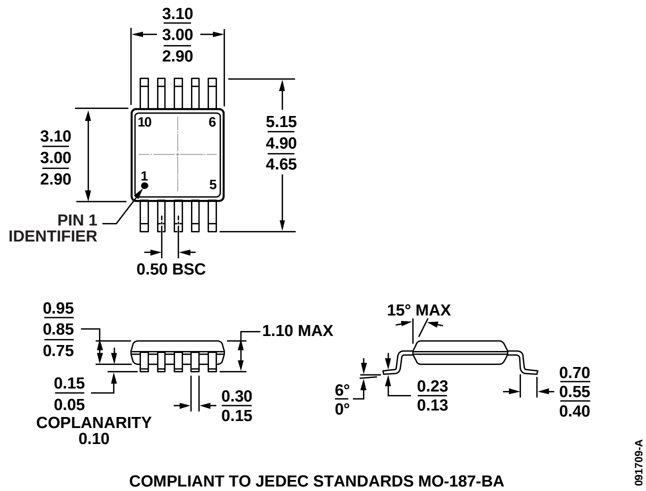

Figure 33. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

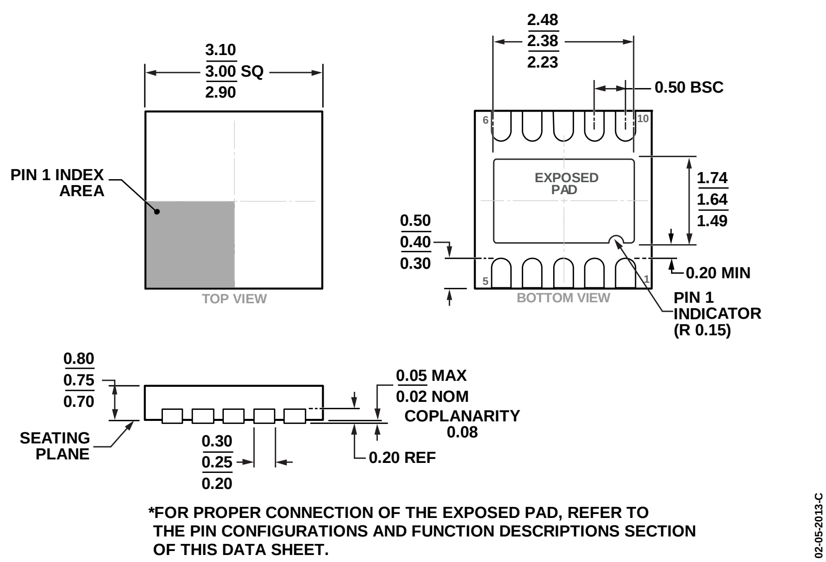

Figure 34. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADG1421BRMZ	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	S2V
ADG1421BRMZ-REEL7	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	S2V
ADG1421BCPZ-REEL7	−40°C to +125°C	10- Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	S2V
ADG1422BRMZ	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	S2W
ADG1422BRMZ-REEL7	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	S2W
ADG1422BCPZ-REEL7	−40°C to +125°C	10- Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	S2W
ADG1423BRMZ	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	S2X
ADG1423BRMZ-REEL7	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	S2X
ADG1423BCPZ-REEL7	−40°C to +125°C	10- Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	S2X

[1] Z = RoHS Compliant Part.