Evaluation Board User Guide
UG-472

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Evaluating the AD5142A Digital Potentiometer

FEATURES

Full featured evaluation board in conjunction with low voltage digiPOT motherboard (EVAL-MB-LV-SDZ)
Various test circuits
Various ac/dc input signals
PC control via a separately purchased system demonstration platform (SDP-B or SDP-S)
PC software for control

PACKAGE CONTENTS

EVAL-AD5142ADBZ board
EVAL-MB-LV-SDZ motherboard
CD that includes
- **Self-installing software that allows users to control the board and exercise all functions of the device**
- **Electronic version of the AD5142A data sheet**
- **Electronic version of the UG-472 user guide**

GENERAL DESCRIPTION

This user guide describes the evaluation board for evaluating the AD5142A—a quad-channel, 256-position, nonvolatile memory, digital potentiometer. With versatile programmability, the AD5142A allows multiple modes of operation, including read/write access in the RDAC and EEMEM registers, increment/decrement of resistance, resistance changes in ±6 dB scales, wiper setting readback, and extra EEMEM for storing user-defined information, such as memory data for other components or a lookup table.

The AD5142A supports a dual-supply ±2.25 V to ±2.75 V operation and a single-supply 2.3 V to 5.5 V operation, making the device suitable for battery-powered applications and many other applications. In addition, the AD5142A uses a versatile I^2C-compatible serial interface that operates in fast mode, allowing speeds of up to 400 kbps and supporting the selection of up to nine different I^2C addresses. The EVAL-AD5142DBZ can operate in single-supply or dual-supply mode and incorporates an internal power supply from the USB.

Complete specifications for the AD5142A part can be found in the AD5142A data sheet, which is available from Analog Devices, Inc., and should be consulted in conjunction with this user guide when using the evaluation board.

EVAL-AD5142ADBZ WITH MOTHERBOARD AND SDP-S

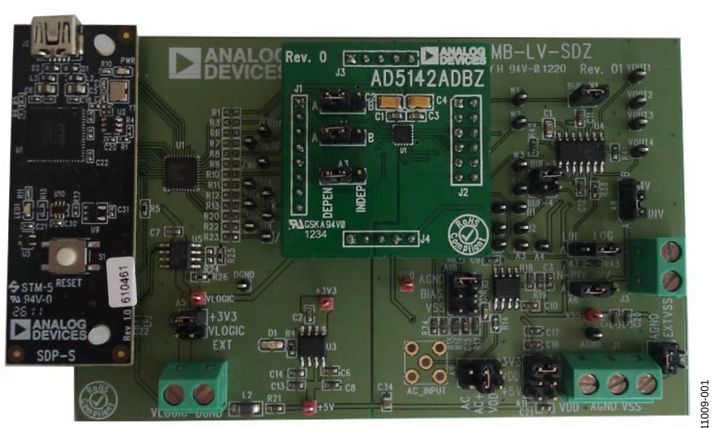

Figure 1. Digital Picture of Evaluation Board with Low Voltage DigiPOT Motherboard and System Demonstration Platform

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REVISION HISTORY

11/12—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The EVAL-MB-LV-SDZ motherboard supports using single and dual power supplies.

The EVAL-AD5142ADBZ evaluation board can be powered either from the SDP port or externally by the J1 and J2 connectors, as described in Table 1.

All supplies are decoupled to ground using 10 µF tantalum and 0.1 µF ceramic capacitors.

Table 1. Maximum and Minimum Voltages of the Connectors

Connector No.	Label	Voltage
J1-1	VDD	Analog positive power supply, V_{DD}. Single supply from 2.3 V to 5.5 V. Dual supply from 2.25 V to 2.75 V.
J1-2	AGND	Analog ground.
J1-3	VSS	Analog negative power supply, V_{SS}. Dual supply from −2.25 V to −2.75 V.
J2-1	VLOGIC	Digital supply, from 1.8 V to V_{DD}.
J2-2	DGND	Digital ground.

Link Options

Several link and switch options are incorporated in the EVAL-MB-LV-SDZ motherboard and should be set up before using the board. Table 2 describes the positions of the links to control the evaluation board via the SDP board using a PC. The functions of these link options are described in detail in Table 4 through Table 7.

Table 2. Link Options Setup for SDP Control (Default)

Link No.	Option
A5	+3V3
A11	3.3 V
A12	AGND

Linear Gain Setting Mode

The linear gain setting mode pin is controlled directly by Jumper A1. If the jumper is placed in DEPEN, the AD5142A powers up in potentiometer mode, and the linear gain setting mode can be controlled by software. If the jumper is placed in INDEP, the part powers up in linear gain setting mode, loading independent values for each resistor string—R_{AW1}, R_{WB1}, R_{AW2}, and R_{WB2}. The part cannot be placed in potentiometer mode again unless the jumper is manually placed in DEPEN.

I²C Address Selection

The I²C address can be selected by using Link A1 and Link A2 as described in Table 3.

Table 3. I²C Address Selection

Link A1	Link A2	I²C Address
Position A	Position A	0101111
	Position B	0100011
Position B	Position A	0101100
	Position B	0100000

Table 4. Link Functions

Link No.	Power Supply	Options
A5	V_{LOGIC}	This link selects one of the following as the digital supply: +3V3 (3.3 V from SDP). VLOGIC EXT (external supply from the J2 connector).
A11	V_{DD}	This link selects one of the following as the positive power supply: +5 V (5 V from SDP). 3V3 (3.3 V from SDP). VDD (external supply from the J1 connector).
A12	V_{SS}	This link selects one of the following as the negative power supply: AGND. EXTVSS (external supply from the J1 connector).

TEST CIRCUITS

The EVAL-AD5142ADBZ and EVAL-MB-LV-SDZ incorporate several test circuits to evaluate the performance of the AD5142A.

DAC

The digiPOT can be operated as a digital-to-analog converter (DAC), as shown in Figure 2. Table 5 describes the options available for the voltage references.

The output voltage is defined in Equation 1.

$$V_{OUT} = (V_A - V_B) \times \frac{RDAC1}{256} \quad (1)$$

where:
RDAC1 is the code loaded in the RDAC1 register.
V_A is the voltage applied to the A terminal (A9 link).
V_B is the voltage applied to the B terminal (A10 link).

However, by using the R34 and R35 external resistors, the user can reduce the voltage of the voltage references. In this case, use the A1 and B1 test points to measure the voltage applied to the A and B terminals and to recalculate V_A and V_B in Equation 1.

Table 5. DAC Voltage References

Terminal	Link	Options	Description
A1	A9	AC+	Connects Terminal A1 to $V_{DD}/2$
		VDD	Connects Terminal A1 to V_{DD}
W1	BUF-W1		Connects Terminal W1 to an output buffer
B1	A10	BIAS	Connects Terminal B1 to $V_{DD}/2$
		VSS	Connects Terminal B1 to V_{SS}
		AGND	Connects Terminal B1 to analog ground

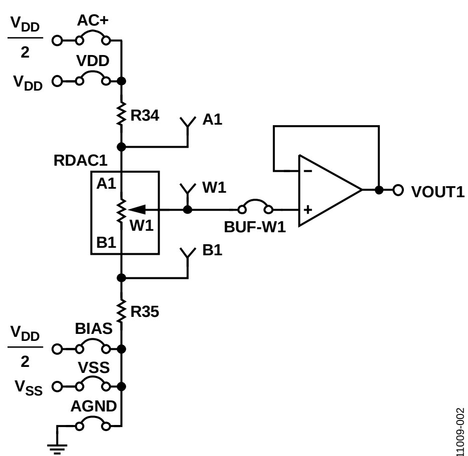

Figure 2. DAC

AC Signal Attenuation

The RDAC can be used to attenuate an ac signal, which must be provided externally using the AC_INPUT connector, as shown in Figure 3.

Depending on the voltage supply rails and the dc offset voltage of the ac signal, various configurations can be used as described in Table 6.

The signal attenuation is defined in Equation 2.

$$Attenuation\,(\text{dB}) = 20 \times \log\left(\frac{R_{WB1} + R_W}{R_{AB}}\right) \quad (2)$$

where:
R_W is the wiper resistance.
R_{AB} is the end-to-end resistance value.
R_{WB1} is the resistor between the W1 and B1 terminals.

Table 6. AC Signal Attenuation Link Options

Voltage Supply	Maximum AC Signal Amplitude	Link	Options	Conditions
Single	V_{DD}	A9	AC+	No dc offset voltage; the ac signal is outside the voltage supply rails due to the dc offset voltage; or the dc offset voltage ≠ V_{DD}/2.[1]
			AC	All other conditions.
		A10	BIAS	Use in conjunction with the AC+ link.
			GND	All other conditions.
Dual	V_{DD}/V_{SS}	A9	AC+	The ac signal is outside the voltage supply rails due to the dc offset voltage; the dc offset voltage ≠ 0 V.[1]
			AC	All other conditions.
		A10	GND	Use in conjunction with the AC+ link.
			VSS	All other conditions.

[1] Recommended to ensure optimal total harmonic distortion (THD) performance.

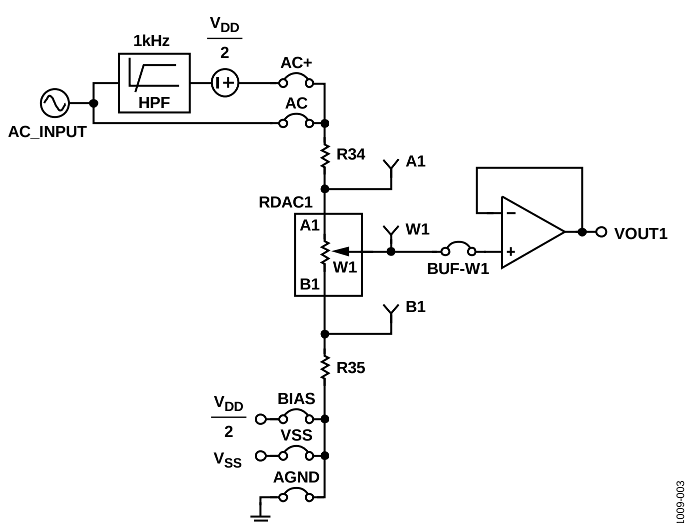

Figure 3. AC Signal Attenuator

Signal Amplifier

The RDAC can be operated as an inverting or noninverting signal amplifier supporting linear or pseudologarithmic gains. Table 7 shows the available configurations.

The noninverting amplifier with linear gain is shown in Figure 4, and the gain is defined in Equation 3.

$$G = 1 + \frac{R_{WB2}}{R_{AW2}} \quad (3)$$

where:
R_{WB2} is the code loaded for the R_{WB2} resistance.
R_{AW2} is the code loaded for the R_{AW2} resistance.

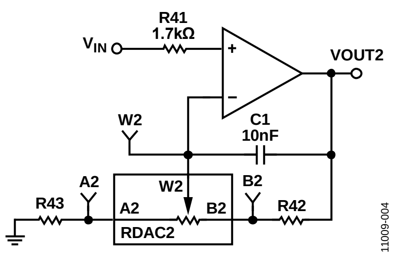

Figure 4. Linear Noninverting Amplifier

R43 and R42 can be used to set the maximum and minimum gain limits.

The noninverting amplifier with pseudologarithmic gain is shown in Figure 5, and the gain is defined in Equation 4.

$$G = 1 + \frac{RDAC2}{256 - RDAC2} \quad (4)$$

where:
RDAC2 is the code loaded in the RDAC2.

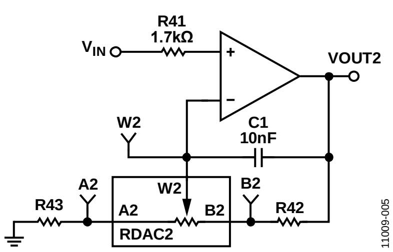

Figure 5. Pseudologarithmic Noninverting Amplifier

R43 and R42 can be used to set the maximum and minimum gain limits.

The inverting amplifier with linear gain is shown in Figure 6, and the gain is defined in Equation 5.

Note that the input signal, V_{IN}, must be negative.

$$G = -\frac{R_{WB2}}{R_{AW2}} \quad (5)$$

where:
R_{WB2} is the code loaded for the R_{WB2} resistance.
R_{AW2} is the code loaded for the R_{AW2} resistance.

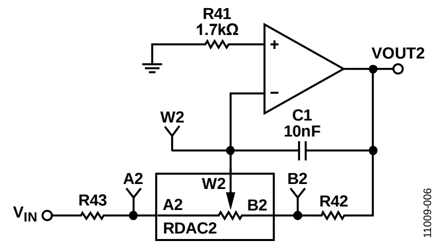

Figure 6. Linear Inverting Amplifier

R43 and R42 can be used to set the maximum and minimum gain limits.

The inverting amplifier with pseudologarithmic gain is shown in Figure 7, and the gain is defined in Equation 6.

$$G = -\frac{RDAC2}{256 - RDAC2} \quad (6)$$

where:
RDAC2 is the code loaded in the RDAC2.

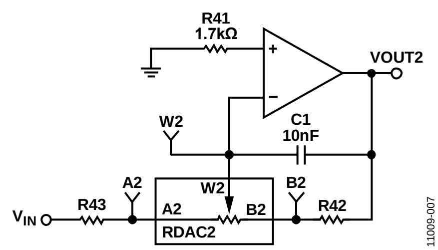

Figure 7. Pseudologarithmic Inverting Amplifier

R43 and R42 can be used to set the maximum and minimum gain limits.

Table 7. Amplifier Selection Link Options

Amplifier	Gain	Linear Setting Gain Mode Enabled	Link	Label
Noninverting	Linear	Yes	A7	LIN
			A6	N-INV
			A8	N-INV
	Pseudologarithmic	No	A7	LOG
			A6	N-INV
			A8	N-INV
Inverting	Linear	Yes	A7	LIN
			A6	INV
			A8	INV
	Pseudologarithmic	No	A7	LOG
			A6	INV
			A8	INV

EVALUATION BOARD SOFTWARE

INSTALLING THE SOFTWARE

The EVAL-AD5142ADBZ kit includes a CD containing the evaluation board software. The software is compatible with Windows® XP, Windows Vista, and Windows 7 (both 32 bits and 64 bits).

Install the software before connecting the SDP board to the USB port of the PC to ensure that the SDP board is recognized when it is connected to the PC.

To install the software,

1. Start the Windows operating system and insert the CD into the CD-ROM drive.
2. The installation software opens automatically. If it does not open automatically, run the **setup.exe** file from the CD.
3. After the installation is complete, power up the evaluation board as described in the Power Supplies section.
4. Connect the EVAL-AD5142ADBZ and EVAL-MB-LV-SDZ to the SDP board, and then connect the SDP board to the PC using the USB cable included with the SDP board.
5. When the software detects the evaluation board, follow the instructions that appear to finalize the installation.

To run the program, do the following:

1. Click **Start** > **All Programs** > **Analog Devices** > **AD5142A** > **AD5142A Eval Board**. To uninstall the program, click **Start** > **Control Panel** > **Add or Remove Programs** > **AD5142A Eval Board**.
2. If the SDP board is not connected to the USB port when the software is launched, a connectivity error displays (see Figure 8). Simply connect the evaluation board to the USB port of the PC, wait a few seconds, click **Rescan**, and follow the instructions.

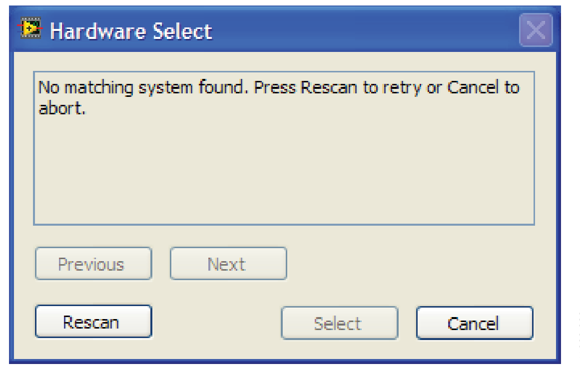

Figure 8. Pop-Up Window Error

The main window of the EVAL-AD5142ADBZ software then opens, as shown in Figure 9.

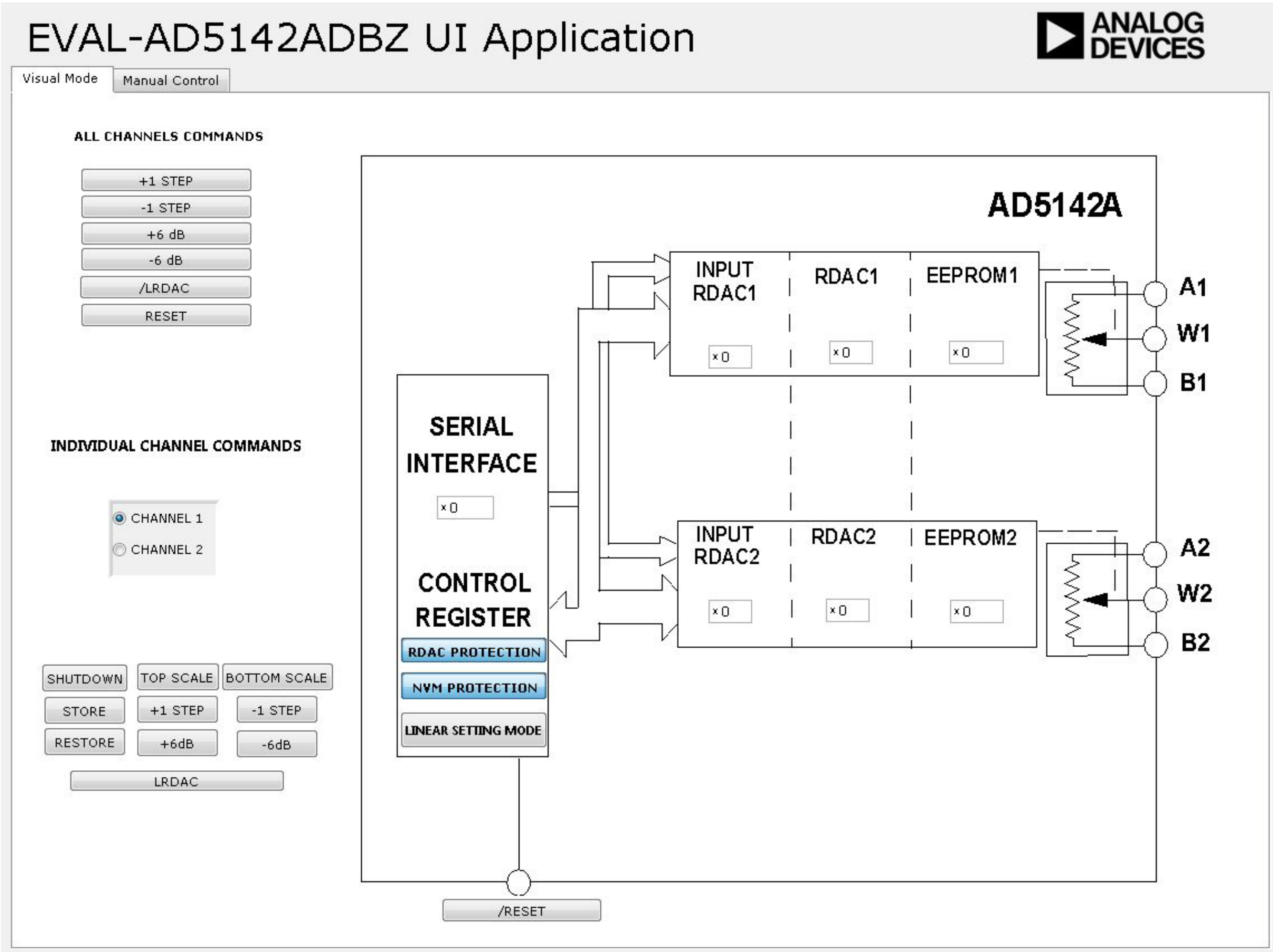

Figure 9. EVAL-AD5142ADBZ Software Main Window

SOFTWARE OPERATION

The main window of the EVAL-AD5142ADBZ software has two tabs, **Visual Mode** and **Manual Control**.

Visual Mode

The **Visual Mode** tab is divided into the following sections: **ALL CHANNELS COMMANDS**, **INDIVIDUAL CHANNEL COMMANDS**, and a block diagram that contains boxes for changing the control register values and buttons and for controlling the hardware pins.

The **ALL CHANNELS COMMANDS** section allows you to send quick commands directly to the AD5142A.

The **INDIVIDUAL CHANNEL COMMANDS** section allows you to send quick commands to only specific channels of the AD5142A.

The block diagram allows you to update the control register status. Each register value can be easily updated by changing the value in its respective block within the diagram. In addition, buttons are available that allow you to change the level of some hardware pins.

Manual Mode

The **Manual Mode** tab, as shown in Figure 10, allows you to customize an I^2C data-word by manually switching the scroll bars from 0 to 1 or from 1 to 0, as desired, and then clicking **SEND DATA**.

Figure 10. Manual Mode

EVALUATION BOARD SCHEMATICS AND ARTWORK

MOTHERBOARD

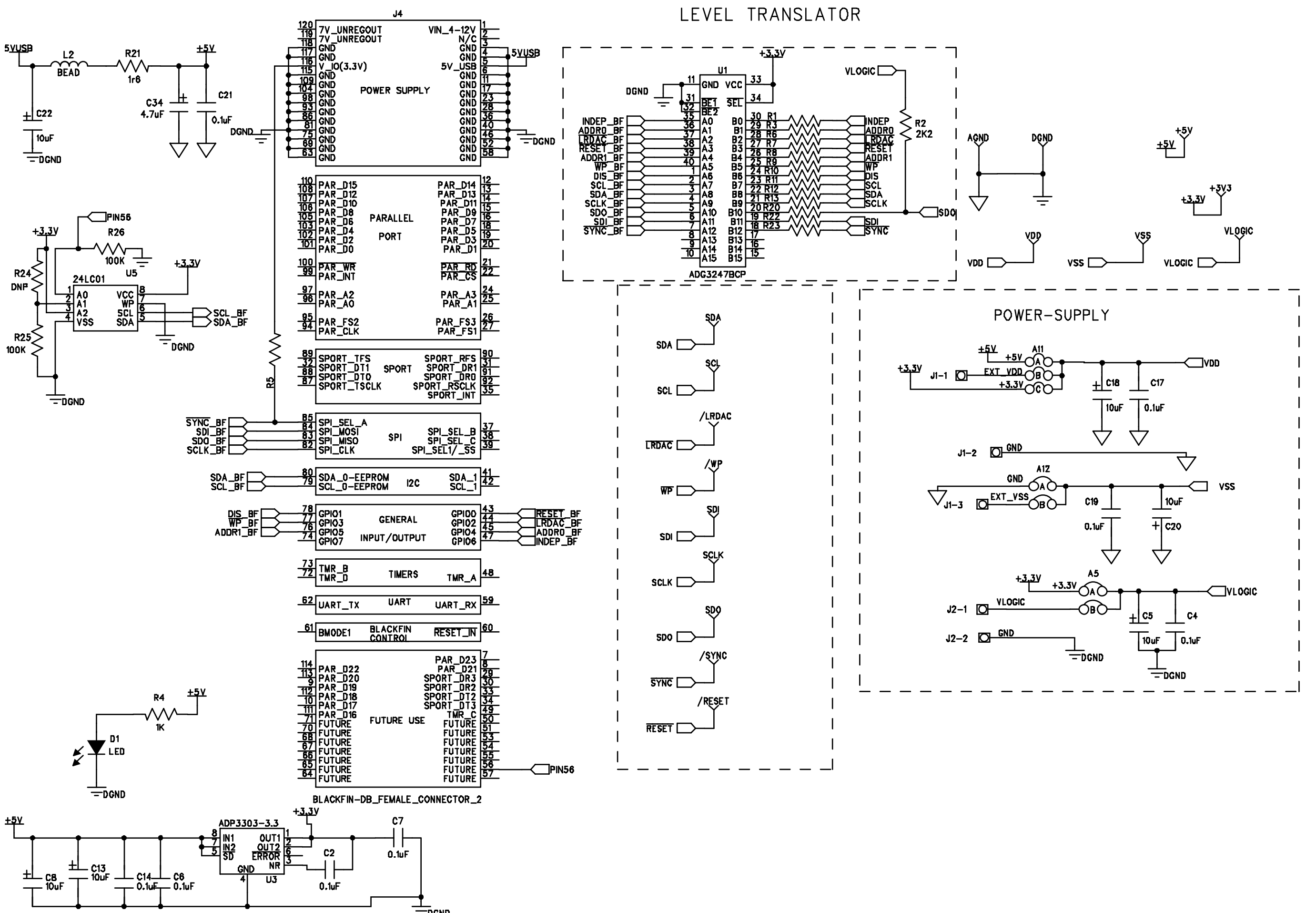

Figure 11. SDP Connector and Power Supply

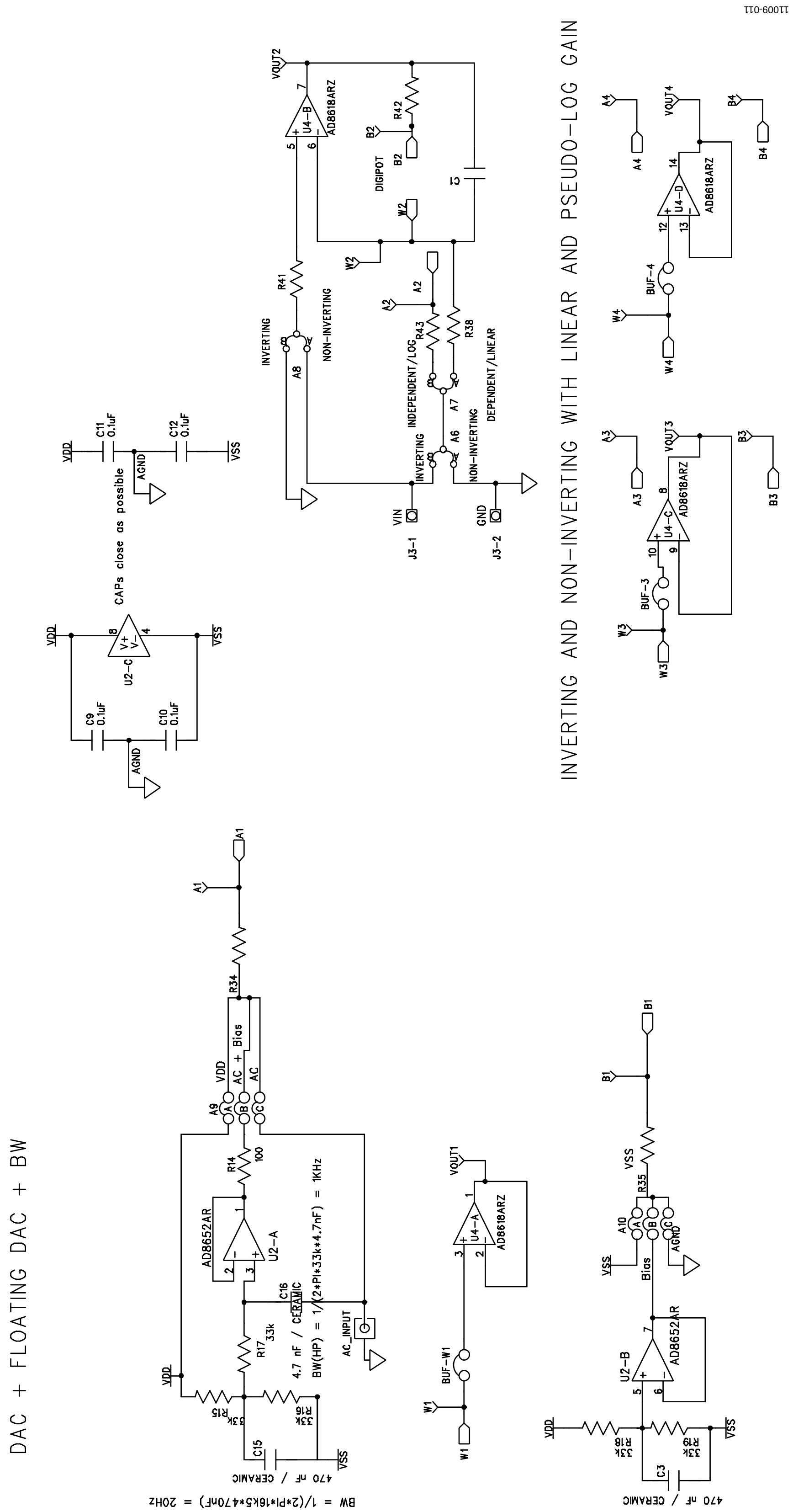

Figure 12. Schematic of Test Circuits

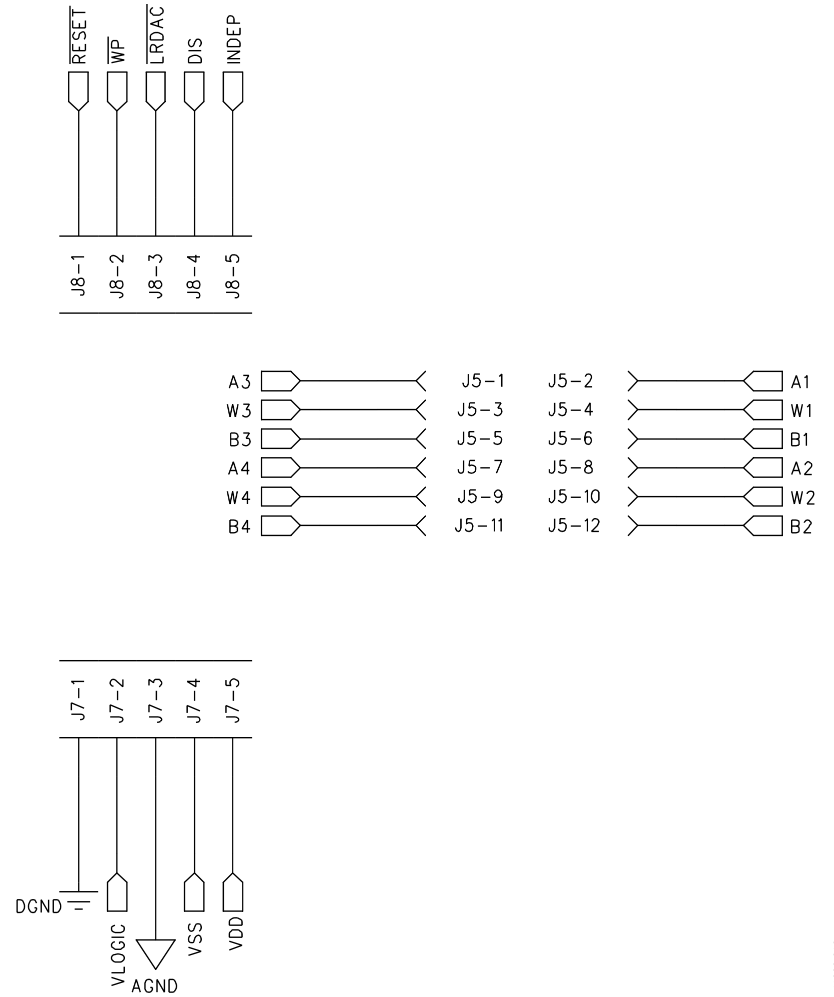

Figure 13. Schematic of Connectors to Daughter Board

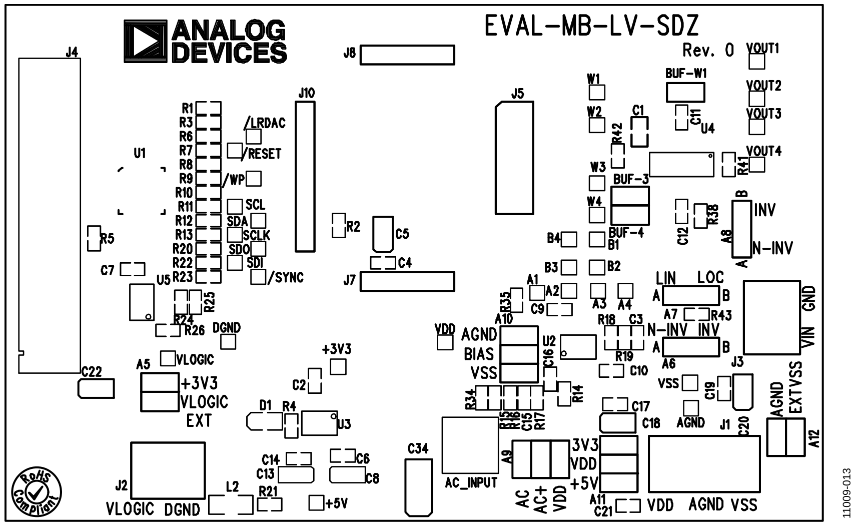

Figure 14. Component Side View of Motherboard

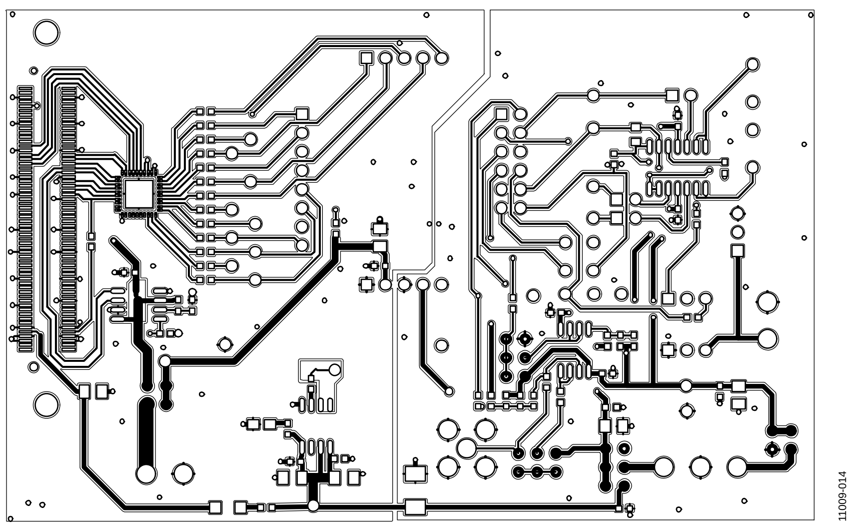

Figure 15. Component Placement Drawing of Motherboard

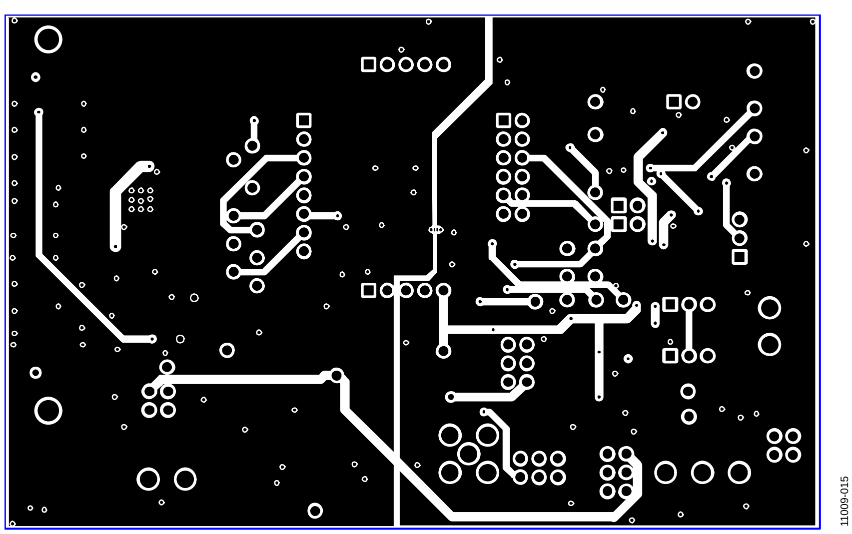

Figure 16. Layer 2 Side PCB Drawing of Motherboard

DAUGHTER BOARD

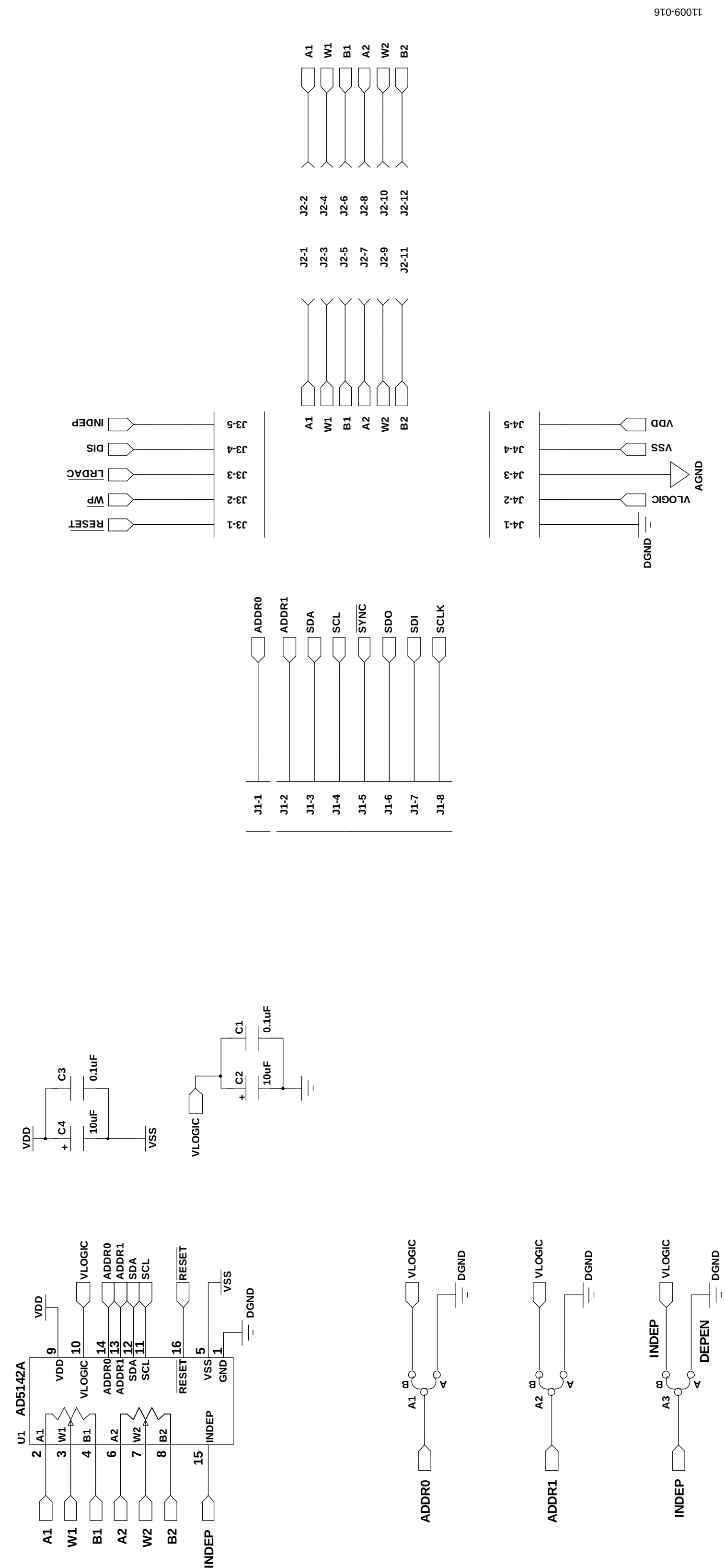

Figure 17. Schematic of Daughter Board

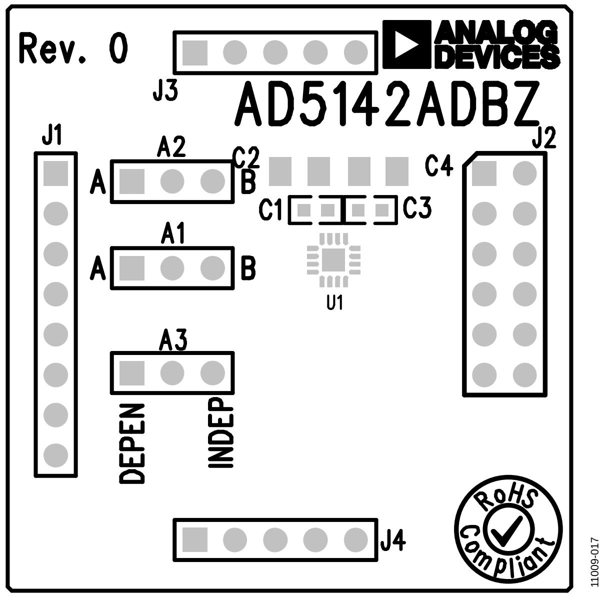

Figure 18. Component Side View of Daughter Board

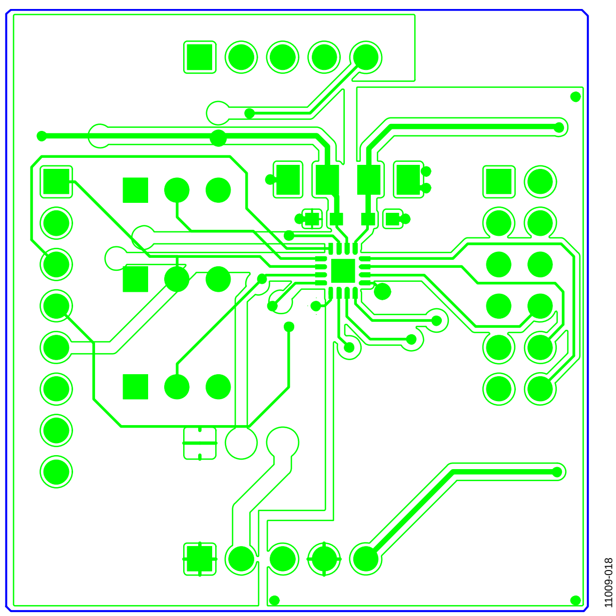

Figure 19. Component Placement Drawing of Daughter Board

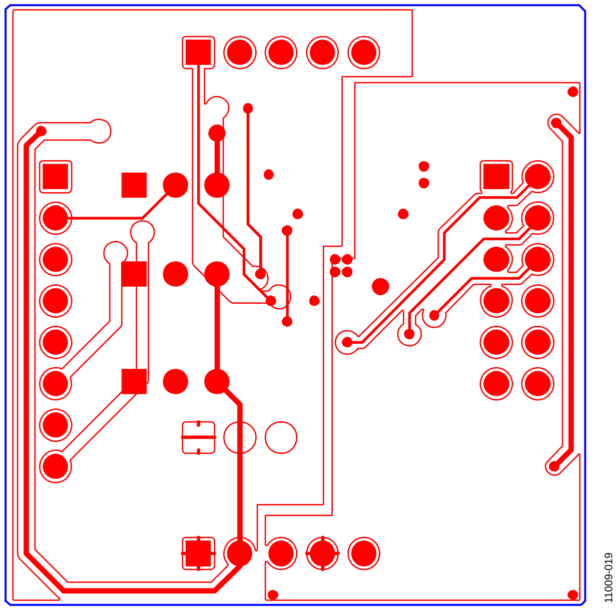

Figure 20. Layer 2 Side PCB Drawing of Daughter Board

ORDERING INFORMATION

BILL OF MATERIALS

Table 8. Motherboard

Qty	Reference Designator	Description	Supplier[1]/Part Number
3	BUF-3, BUF-4, BUF-W1	2-pin (0.1" pitch) header and shorting shunt	FEC 1022247 and 150411
3	A6, A7, A8	3-pin SIL header and shorting link	FEC 1022248 and 150410
5	A5, A9, A10, A11, A12	6-pin (3 × 2), 0.1" header and shorting block	FEC 672014 and 150411 (36-pin strip)
1	J1	3-pin terminal block (5 mm pitch)	FEC 151790
2	J7, J8	4-pin SIL header	FEC 1098035
1	J4	Receptacle, 0.6 mm, 120-way	Digi-Key H1219-ND
1	J10	8-pin in-line header; 100 mil centers	FEC 1098038
1	J5	12-pin (2 × 6), 0.1" pitch header	FEC 1098051
2	J2, J3	2-pin terminal block (5 mm pitch)	FEC 151789
17	R1, R3, R6, R7, R8, R9, R10, R11, R12, R13, R20, R22, R23, R34, R35, R42, R43	SMD resistor, 0 Ω, 0.01, 0603	FEC 9331662
1	R2	SMD resistor, 2.2 kΩ, 0.01, 0603	FEC 1750676
1	R41	SMD resistor, 1.7 kΩ, 1% ,0603	FEC 1170811
1	R21	Resistor, surge, 1.6 Ω, 1%, 0603	FEC 1627674
1	R38	SMD resistor, 2.7 kΩ, 1%, 0603	FEC 1750678
1	R14	SMD resistor, 100 Ω, 1%, 0603	FEC 9330364
1	R4	SMD resistor, 1 kΩ, 0.01, 0603	FEC 9330380
3	R5, R25, R26	SMD resistor, 100 kΩ, 1%, 0603	FEC 9330402
5	R15, R16, R17, R18, R19	SMD resistor, 33 kΩ, 1%, 0603	FEC 9331034
1	C1	SMD capacitor, 100 nF, 10%, 0805	FEC 1650863
8	C4, C9, C10, C11, C12, C17, C19, C21	SMD capacitor, 0.1 µF, ±10%, 0603	FEC 1759122
4	C2, C6, C7, C14	SMD capacitor, 0.1 µF, ±10%, 0603	FEC 3019482
2	C8, C13	SMD capacitor, 10 µF, ±10%	FEC 197130
4	C18, C20, C22, C5	Capacitor, 10 µF, ±20%	FEC 1190107
2	C3, C15	Capacitor, 470 nF, ±10%, 0603	FEC 1414037
1	C16	Capacitor, 4.7 nF, ±10%, 0603	FEC 1414642
1	C34	Capacitor, 4.7 nF, ±20%	FEC 1432350
1	L2	Inductor, SMD, 600Z	FEC 9526862
1	D1	Green SMD LED	FEC 5790852
1	U1	Two-port level translating bus switch	ADG3247BCPZ
1	U2	Dual op amp	AD8652ARZ
1	U3	Precision low dropout voltage regulator	ADP3303ARZ-3.3
1	U4	Operational amplifier	AD8618ARZ
1	U5	I^{2}C serial EEPROM 64k 2.5 V MSOP-8	FEC 1331335
18	$\overline{\text{LRDAC}}$, $\overline{\text{RESET}}$, $\overline{\text{SYNC}}$, $\overline{\text{WP}}$, A1, A2, A3, A4, AGND, B1, VOUT_C1, VOUT_C2, VOUT3, VOUT4, W1, W2, W3, W4	Terminal, PCB, black, PK100, test point	FEC 8731128
5	+3.3V , +5V, EXT_VDD, VLOGIC, EXT_VSS	Terminal, PCB, red, PK100, test point	FEC 8731144

[1] FEC refers to Farnell Electronic Component Distributors; Digi-Key refers to Digi-Key Corporation.

Table 9. Daughter Board

Qty	Reference Designator	Description	Supplier[1]/Part Number
1	U1	256-position digital potentiometer	AD5142ABCPZ10
3	A1, A2, A3	3-pin SIL header and shorting link	FEC 1022248 and 150410
2	C2, C4	6.3 V tantalum capacitor (Case A), 10 µF, ±20%	FEC 1190107
2	C1, C3	50 V, X7R ceramic capacitor, 0.1 µF, ±10%	FEC 1759122
1	J1	Header, 2.54 mm, PCB, 1 × 8-way	FEC 1766172
1	J2	12-pin (2 × 6), 0.1" pitch header	FEC 1804099
2	J3, J4	5-pin SIL header	FEC 1929016

[1] FEC refers to Farnell Electronic Component Distributors.

NOTES

I^2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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