

## FEATURES

- Single-channel, 1024-position resolution
- 20 k $\Omega$  nominal resistance
- Maximum  $\pm 1\%$  nominal resistor tolerance error (resistor performance mode)
- 20-times programmable wiper memory
- Rheostat mode temperature coefficient: 35 ppm/ $^{\circ}\text{C}$
- Voltage divider temperature coefficient: 5 ppm/ $^{\circ}\text{C}$
- +9 V to +33 V single-supply operation
- $\pm 9$  V to  $\pm 16.5$  V dual-supply operation
- SPI-compatible serial interface
- Wiper setting readback
- Power-on refreshed from 20-TP memory

## ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC)
- Temperature range:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Controlled manufacturing baseline
- 1 assembly/test site
- 1 fabrication site
- Product change notification
- Qualification data available on request

## APPLICATIONS

- Mechanical potentiometer replacement
- Instrumentation: gain and offset adjustment
- Programmable voltage-to-current conversion
- Programmable filters, delays, and time constants
- Programmable power supply
- Low resolution DAC replacement
- Sensor calibration

## GENERAL DESCRIPTION

The AD5292-EP is a single-channel, 1024-position digital potentiometer<sup>1</sup> that combines industry leading variable resistor performance with nonvolatile memory (NVM) in a compact package. This device is capable of operating across a wide voltage range, supporting both dual supply operation at  $\pm 10.5$  V to  $\pm 16.5$  V and single-supply operation at +21 V to +33 V, while ensuring less than 1% end-to-end resistor tolerance error and offering 20-time programmable (20-TP) memory.

The guaranteed industry leading low resistor tolerance error feature simplifies open-loop applications as well as precision calibration and tolerance matching applications.

<sup>1</sup> The terms digital potentiometer and RDAC are used interchangeably.

Rev. A

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## FUNCTIONAL BLOCK DIAGRAM

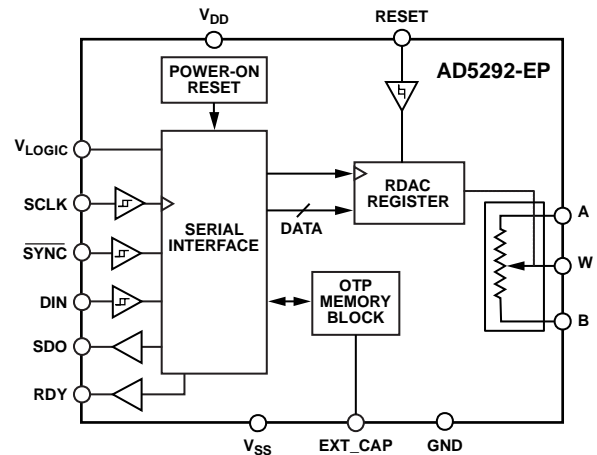


Figure 1.

The AD5292-EP device wiper settings are controllable through the SPI digital interface. Unlimited adjustments are allowed before programming the resistance value into the 20-TP memory. The AD5292-EP does not require any external voltage supply to facilitate fuse blow, and there are 20 opportunities for permanent programming. During 20-TP activation, a permanent blow fuse command freezes the wiper position (analogous to placing epoxy on a mechanical trimmer).

The AD5292-EP is available in a compact 14-lead TSSOP package. The part is guaranteed to operate over the extended industrial temperature range of  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

Additional application and technical information can be found in the [AD5292](#) data sheet.

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**REVISION HISTORY**

**4/2018—Rev. 0 to Rev. A**

Change to Enhanced Product Features Section .....	1
Changes to Ordering Guide .....	15

**9/2011—Revision 0: Initial Version**

## SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS—AD5292-EP

$V_{DD} = 21\text{ V to }33\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ;  $V_{DD} = 10.5\text{ V to }16.5\text{ V}$ ,  $V_{SS} = -10.5\text{ V to }-16.5\text{ V}$ ;  $V_{LOGIC} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_A = V_{DD}$ ,  $V_B = V_{SS}$ ,  
 $-55^\circ\text{C} < T_A < +125^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resolution	N		10			Bits
Resistor Differential Nonlinearity <sup>2</sup>	R-DNL	$R_{WB}$ , $V_A = NC$	-1		+1	LSB
Resistor Integral Nonlinearity <sup>2</sup>	R-INL	$R_{AB} = 20\text{ k}\Omega$ , $ V_{DD} - V_{SS}  = 26\text{ V to }33\text{ V}$	-2		+2	LSB
	R-INL	$R_{AB} = 20\text{ k}\Omega$ , $ V_{DD} - V_{SS}  = 21\text{ V to }26\text{ V}$	-3		+3	LSB
Nominal Resistor Tolerance (R-Perf Mode) <sup>3</sup>	$\Delta R_{AB}/R_{AB}$	See Table 2	-1	$\pm 0.5$	+1	%
Nominal Resistor Tolerance (Normal Mode) <sup>4</sup>	$\Delta R_{AB}/R_{AB}$			$\pm 7$		%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$	Code = full scale; see Figure 14		35		ppm/°C
Wiper Resistance	$R_W$	Code = zero scale		60	100	$\Omega$
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE						
Resolution	N		10			Bits
Differential Nonlinearity <sup>5</sup>	DNL		-1		+1	LSB
Integral Nonlinearity <sup>5</sup>	INL		-2.5		+2.5	LSB
Voltage Divider Temperature Coefficient <sup>4</sup>	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale; see Figure 17		5		ppm/°C
Full-Scale Error	$V_{WFSE}$	Code = full scale	-8		+1	LSB
Zero-Scale Error	$V_{WZSE}$	Code = zero scale	0		10	LSB
RESISTOR TERMINALS						
Terminal Voltage Range <sup>6</sup>	$V_A, V_B, V_W$		$V_{SS}$		$V_{DD}$	V
Capacitance A, Capacitance B <sup>4</sup>	$C_A, C_B$	$f = 1\text{ MHz}$ , measured to GND, code = half scale		85		pF
Capacitance W <sup>4</sup>	$C_W$	$f = 1\text{ MHz}$ , measured to GND, code = half scale		65		pF
Common-Mode Leakage Current <sup>4</sup>	$I_{CM}$	$V_A = V_B = V_W$	-120	$\pm 1$	120	nA
DIGITAL INPUTS						
Input Logic High <sup>4</sup>	$V_{IH}$	JEDEC compliant $V_{LOGIC} = 2.7\text{ V to }5.5\text{ V}$	2.0			V
Input Logic Low <sup>4</sup>	$V_{IL}$	$V_{LOGIC} = 2.7\text{ V to }5.5\text{ V}$			0.8	V
Input Current	$I_{IL}$	$V_{IN} = 0\text{ V or }V_{LOGIC}$			$\pm 1$	$\mu\text{A}$
Input Capacitance <sup>4</sup>	$C_{IL}$			5		pF
DIGITAL OUTPUTS (SDO and RDY)						
Output High Voltage <sup>4</sup>	$V_{OH}$	$R_{PULL\_UP} = 2.2\text{ k}\Omega$ to $V_{LOGIC}$	$V_{LOGIC} - 0.4$			V
Output Low Voltage <sup>4</sup>	$V_{OL}$	$R_{PULL\_UP} = 2.2\text{ k}\Omega$ to $V_{LOGIC}$			GND + 0.4	V
Three-State Leakage Current			-1		+1	$\mu\text{A}$
Output Capacitance <sup>4</sup>	$C_{OL}$			5		pF
POWER SUPPLIES						
Single-Supply Power Range	$V_{DD}$	$V_{SS} = 0\text{ V}$	9		33	V
Dual-Supply Power Range	$V_{DD}/V_{SS}$		$\pm 9$		$\pm 16.5$	V
Positive Supply Current	$I_{DD}$	$V_{DD}/V_{SS} = \pm 16.5\text{ V}$		0.1	2	$\mu\text{A}$
Negative Supply Current	$I_{SS}$	$V_{DD}/V_{SS} = \pm 16.5\text{ V}$	-2	-0.1		$\mu\text{A}$
Logic Supply Range	$V_{LOGIC}$		2.7		5.5	V
Logic Supply Current	$I_{LOGIC}$	$V_{LOGIC} = 5\text{ V}$ , $V_{IH} = 5\text{ V or }V_{IL} = \text{GND}$		1	10	$\mu\text{A}$
OTP Store Current <sup>4,7</sup>	$I_{LOGIC\_PROG}$	$V_{IH} = 5\text{ V or }V_{IL} = \text{GND}$		25		mA
OTP Read Current <sup>4,8</sup>	$I_{LOGIC\_FUSE\_READ}$	$V_{IH} = 5\text{ V or }V_{IL} = \text{GND}$		25		mA
Power Dissipation <sup>9</sup>	$P_{DISS}$	$V_{IH} = 5\text{ V or }V_{IL} = \text{GND}$		8	110	$\mu\text{W}$
Power Supply Rejection Ratio	PSRR	$\Delta V_{DD}/\Delta V_{SS} = \pm 15\text{ V} \pm 10\%$		0.103		%/%

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
DYNAMIC CHARACTERISTICS <sup>5, 10</sup>						
Bandwidth	BW	−3 dB		520		kHz
Total Harmonic Distortion	THD <sub>W</sub>	V <sub>A</sub> = 1 V rms, V <sub>B</sub> = 0 V, f = 1 kHz		−93		dB
V <sub>W</sub> Settling Time	t <sub>S</sub>	V <sub>A</sub> = 30 V, V <sub>B</sub> = 0 V, ±0.5 LSB error band, initial code = zero scale, board capacitance = 170 pF				
		Code = full-scale, normal mode		750		ns
		Code = full-scale, R-Perf mode		2.5		μs
		Code = half-scale, normal mode		2.5		μs
		Code = half-scale, R-Perf mode		5		μs
Resistor Noise Density	e <sub>N, WB</sub>	Code = half-scale, T <sub>A</sub> = 25°C, 0 kHz to 200 kHz		10		nV/√Hz

<sup>1</sup> Typical values represent average readings at 25°C, V<sub>DD</sub> = 15 V, V<sub>SS</sub> = −15 V, and V<sub>LOGIC</sub> = 5 V.

<sup>2</sup> Resistor position nonlinearity error. R-INL is the deviation from an ideal value measured between R<sub>WB</sub> at Code 0x00B and Code 0x3FF or between R<sub>WA</sub> at Code 0x3F3 and Code 0x000. R-DNL measures the relative step change from ideal between successive tap positions. The specification is guaranteed in resistor performance mode, with a wiper current of 1 mA for V<sub>A</sub> < 12 V and 1.2 mA for V<sub>A</sub> ≥ 12 V.

<sup>3</sup> Resistor performance mode. The terms resistor performance mode and R-Perf mode are used interchangeably.

<sup>4</sup> Guaranteed by design and characterization, not subject to production test.

<sup>5</sup> INL and DNL are measured at V<sub>W</sub> with the RDAC configured as a potentiometer divider similar to a voltage output DAC. V<sub>A</sub> = V<sub>DD</sub> and V<sub>B</sub> = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.

<sup>6</sup> Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground-referenced bipolar signal adjustment.

<sup>7</sup> Different from operating current; supply current for fuse program lasts approximately 550 μs.

<sup>8</sup> Different from operating current; supply current for fuse read lasts approximately 550 μs.

<sup>9</sup> P<sub>DISS</sub> is calculated from (I<sub>DD</sub> × V<sub>DD</sub>) + (I<sub>SS</sub> × V<sub>SS</sub>) + (I<sub>LOGIC</sub> × V<sub>LOGIC</sub>).

<sup>10</sup> All dynamic characteristics use V<sub>DD</sub> = 15 V, V<sub>SS</sub> = −15 V, and V<sub>LOGIC</sub> = 5 V.

## RESISTOR PERFORMANCE MODE CODE RANGE

Table 2.

Resistor Tolerance per Code	−55°C < T <sub>A</sub> < +125°C							
	V <sub>DD</sub> − V <sub>SS</sub>   = 30 V to 33 V		V <sub>DD</sub> − V <sub>SS</sub>   = 26 V to 30 V		V <sub>DD</sub> − V <sub>SS</sub>   = 22 V to 26 V		V <sub>DD</sub> − V <sub>SS</sub>   = 21 V to 22 V	
	R <sub>WB</sub>	R <sub>WA</sub>	R <sub>WB</sub>	R <sub>WA</sub>	R <sub>WB</sub>	R <sub>WA</sub>	R <sub>WB</sub>	R <sub>WA</sub>
1% R-Tolerance	From 0x1EF to 0x3FF	From 0x000 to 0x210	From 0x1F4 to 0x3FF	From 0x000 to 0x20B	From 0x1F4 to 0x3FF	From 0x000 to 0x20B	N/A	N/A
2% R-Tolerance	From 0x0C3 to 0x3FF	From 0x000 to 0x33C	From 0x0E6 to 0x3FF	From 0x000 to 0x319	From 0x131 to 0x3FF	From 0x000 to 0x2CE	From 0x131 to 0x3FF	From 0x000 to 0x2CE
3% R-Tolerance	From 0x073 to 0x3FF	From 0x000 to 0x38C	From 0x087 to 0x3FF	From 0x000 to 0x378	From 0x0AF to 0x3FF	From 0x000 to 0x350	From 0x0AF to 0x3FF	From 0x000 to 0x350

**INTERFACE TIMING SPECIFICATIONS**

$V_{DD}/V_{SS} = \pm 15\text{ V}$ ,  $V_{LOGIC} = 2.7\text{ V to } 5.5\text{ V}$ ,  $-55^{\circ}\text{C} < T_A < +125^{\circ}\text{C}$ . All specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

**Table 3.**

Parameter	Limit <sup>1</sup>	Unit	Description
$t_1^2$	20	ns min	SCLK cycle time
$t_2$	10	ns min	SCLK high time
$t_3$	10	ns min	SCLK low time
$t_4$	10	ns min	$\overline{\text{SYNC}}$ to SCLK falling edge setup time
$t_5$	5	ns min	Data setup time
$t_6$	5	ns min	Data hold time
$t_7$	1	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge
$t_8$	400 <sup>3</sup>	ns min	Minimum $\overline{\text{SYNC}}$ high time
$t_9$	14	ns min	$\overline{\text{SYNC}}$ rising edge to next SCLK fall ignore
$t_{10}^4$	1	ns min	RDY rising edge to $\overline{\text{SYNC}}$ falling edge
$t_{11}^4$	40	ns max	$\overline{\text{SYNC}}$ rising edge to RDY fall time
$t_{12}^4$	2.4	$\mu\text{s max}$	RDY low time, RDAC register write command execute time (R-Perf mode)
$t_{12}^4$	410	ns max	RDY low time, RDAC register write command execute time (normal mode)
$t_{12}^4$	8	ms max	RDY low time, memory program execute time
$t_{12}^4$	1.5	ms min	Software/hardware reset
$t_{13}^4$	450	ns max	RDY low time, RDAC register readback execute time
$t_{13}^4$	1.3	ms max	RDY low time, memory readback execute time
$t_{14}^4$	450	ns max	SCLK rising edge to SDO valid
$t_{\text{RESET}}$	20	ns min	Minimum $\overline{\text{RESET}}$ pulse width (asynchronous)
$t_{\text{POWER-UP}}^5$	2	ms max	Power-on OTP restore time

<sup>1</sup> All input signals are specified with  $t_r = t_f = 1\text{ ns/V}$  (10% to 90% of  $V_{DD}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH})/2$ .

<sup>2</sup> Maximum SCLK frequency is 50 MHz.

<sup>3</sup> Refer to  $t_{12}$  and  $t_{13}$  for RDAC register and memory commands operations.

<sup>4</sup>  $R_{\text{PULL-UP}} = 2.2\text{ k}\Omega$  to  $V_{LOGIC}$ , with a capacitance load of 168 pF.

<sup>5</sup> Maximum time after  $V_{LOGIC}$  is equal to 2.5 V.

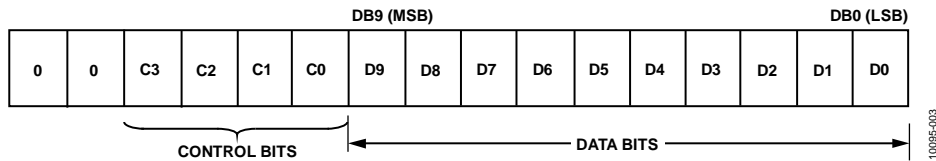


Figure 2. Shift Register Content

Timing Diagrams

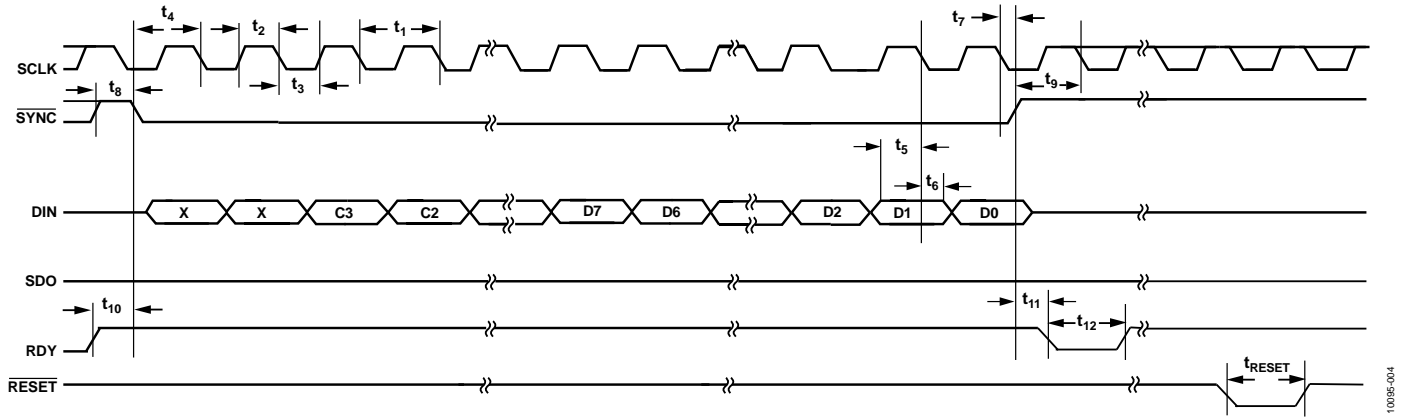


Figure 3. Write Timing Diagram, CPOL = 0, CPHA = 1

10095-004

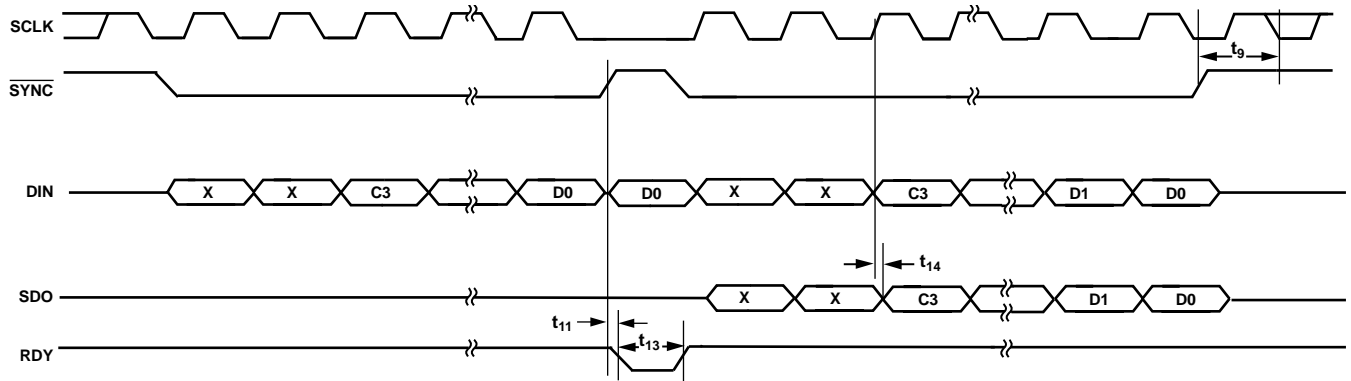


Figure 4. Read Timing Diagram, CPOL = 0, CPHA = 1

10095-005

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 4.**

Parameter	Rating
$V_{DD}$ to GND	-0.3 V to +35 V
$V_{SS}$ to GND	+0.3 V to -25 V
$V_{LOGIC}$ to GND	-0.3 V to +7 V
$V_{DD}$ to $V_{SS}$	35 V
$V_A, V_B, V_W$ to GND	$V_{SS} - 0.3\text{ V}, V_{DD} + 0.3\text{ V}$
Digital Input and Output Voltage to GND	-0.3 V to $V_{LOGIC} + 0.3\text{ V}$
EXT_CAP Voltage to GND	-0.3 V to +7 V
$I_A, I_B, I_W$	
Continuous	$\pm 3\text{ mA}$
Pulsed <sup>1</sup>	
Frequency > 10 kHz	$\pm 3/d^2$
Frequency $\leq 10\text{ kHz}$	$\pm 3/\sqrt{d^2}$
Operating Temperature Range <sup>3</sup>	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
Maximum Junction Temperature ( $T_J$ max)	$150^\circ\text{C}$
Storage Temperature Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Reflow Soldering	
Peak Temperature	$260^\circ\text{C}$
Time at Peak Temperature	20 sec to 40 sec
Package Power Dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$

<sup>1</sup> Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

<sup>2</sup> Pulse duty factor.

<sup>3</sup> Includes programming of OTP memory.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is defined by JEDEC specification JESD-51 and the value is dependent on the test board and test environment.

**Table 5. Thermal Resistance**

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
14-Lead TSSOP	93 <sup>1</sup>	20	$^\circ\text{C}/\text{W}$

<sup>1</sup> JEDEC 2S2P test board, still air (0 m/sec to 1 m/sec air flow).

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

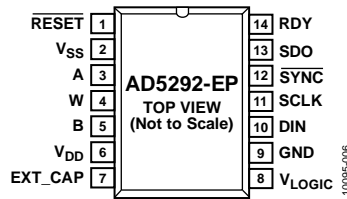


Figure 5. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RESET	Hardware Reset Pin. Refreshes the RDAC register with the contents of the 20-TP memory register. Factory default loads midscale until the first 20-TP wiper memory location is programmed. RESET is activated at the logic high transition. Tie RESET to V <sub>LOGIC</sub> if not used.
2	V <sub>SS</sub>	Negative Supply. Connect to 0 V for single-supply applications. This pin should be decoupled with 0.1 μF ceramic capacitors and 10 μF capacitors.
3	A	Terminal A of RDAC. $V_{SS} \leq V_A \leq V_{DD}$ .
4	W	Wiper Terminal of RDAC. $V_{SS} \leq V_W \leq V_{DD}$ .
5	B	Terminal B of RDAC. $V_{SS} \leq V_B \leq V_{DD}$ .
6	V <sub>DD</sub>	Positive Power Supply. This pin should be decoupled with 0.1 μF ceramic capacitors and 10 μF capacitors.
7	EXT_CAP	External Capacitor. Connect a 1 μF capacitor to EXT_CAP. This capacitor must have a voltage rating of ≥7 V.
8	V <sub>LOGIC</sub>	Logic Power Supply; 2.7 V to 5.5 V. This pin should be decoupled with 0.1 μF ceramic capacitors and 10 μF capacitors.
9	GND	Ground Pin, Logic Ground Reference.
10	DIN	Serial Data Input. The AD5292-EP has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
11	SCLK	Serial Clock Input. Data is clocked into the shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 50 MHz.
12	SYNC	Falling Edge Synchronization Signal. This is the frame synchronization signal for the input data. When SYNC goes low, it enables the shift register and data is transferred in on the falling edges of the following clocks. The selected register is updated on the rising edge of SYNC following the 16 <sup>th</sup> clock cycle. If SYNC is taken high before the 16 <sup>th</sup> clock cycle, the rising edge of SYNC acts as an interrupt, and the write sequence is ignored by the DAC.
13	SDO	Serial Data Output. This open-drain output requires an external pull-up resistor. SDO can be used to clock data from the shift register in daisy-chain mode or in readback mode.
14	RDY	Ready Pin. This active-high open-drain output identifies the completion of a write or read operation to or from the RDAC register or memory.



### TYPICAL PERFORMANCE CHARACTERISTICS

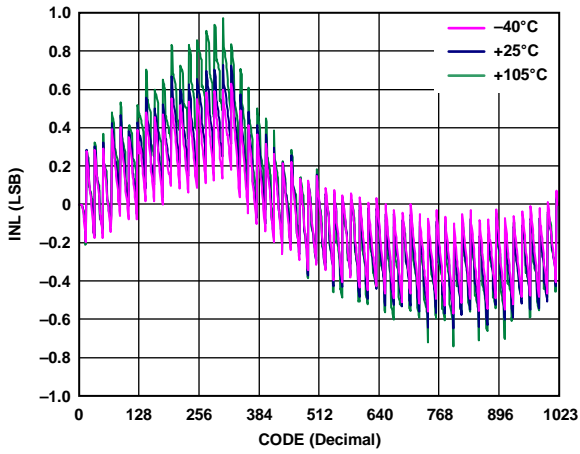


Figure 6. R-INL in R-Perf Mode vs. Code

10095-106

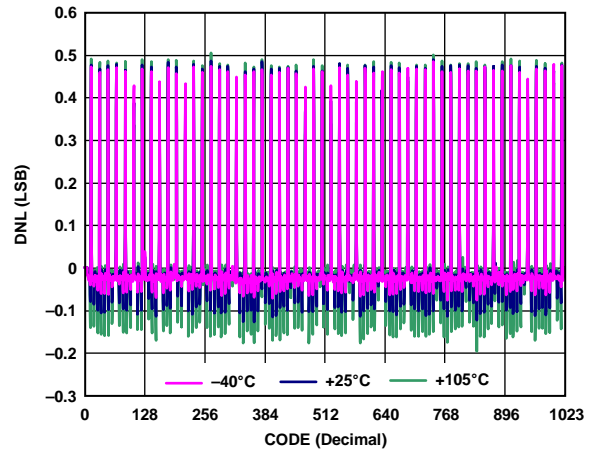


Figure 9. R-DNL in R-Perf Mode vs. Code

10095-007

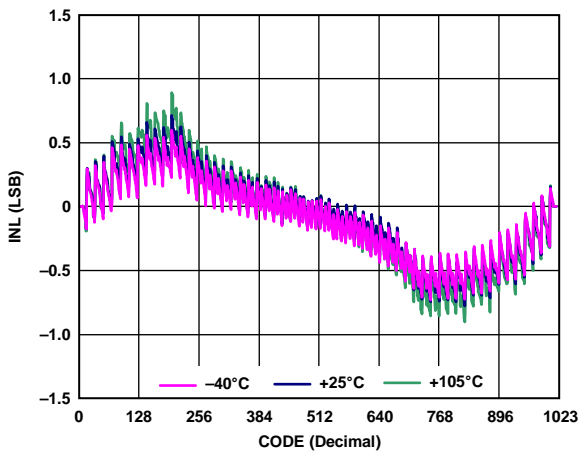


Figure 7. INL in R-Perf Mode vs. Code

10095-014

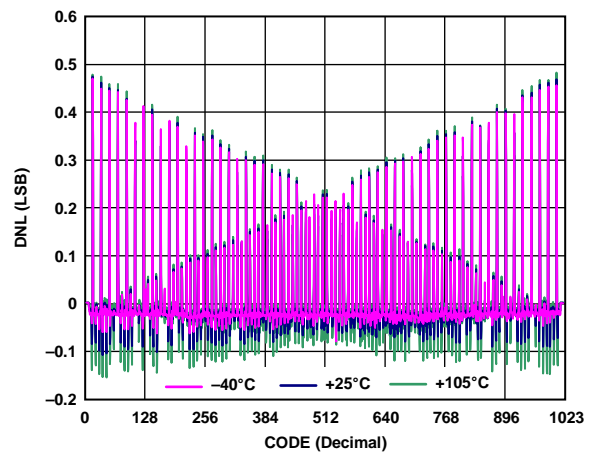


Figure 10. DNL in R-Perf Mode vs. Code

10095-015

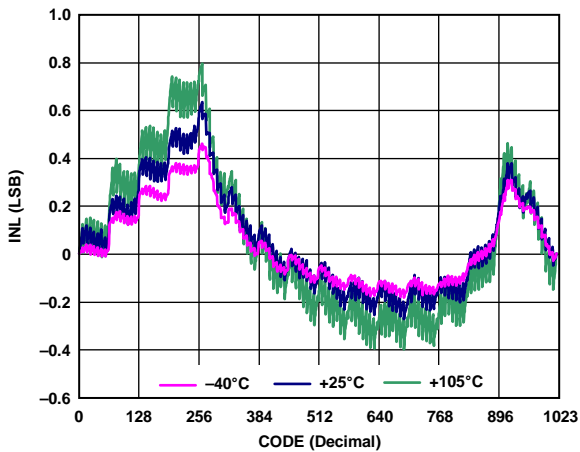


Figure 8. R-INL in Normal Mode vs. Code

10095-010

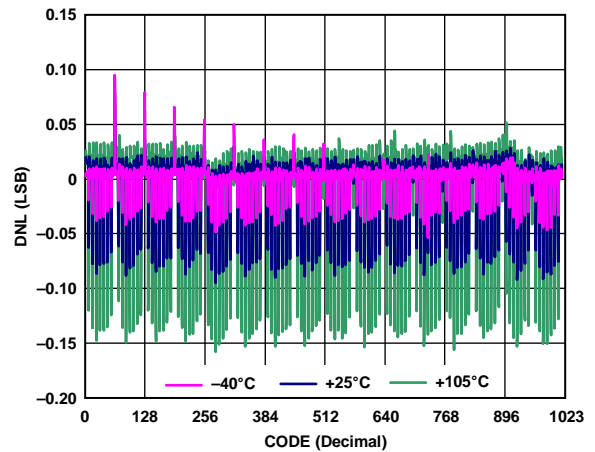


Figure 11. R-DNL in Normal Mode vs. Code

10095-011

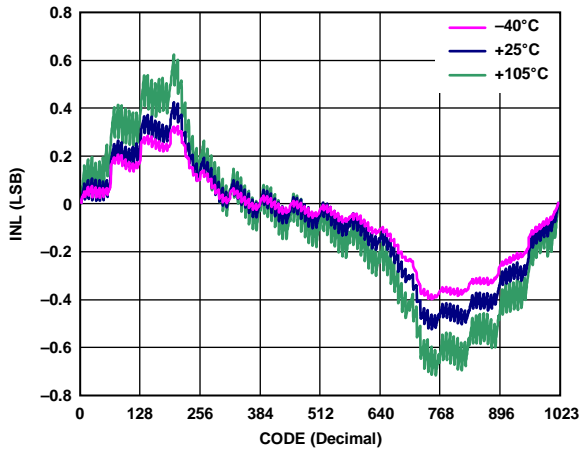


Figure 12. INL in Normal Mode vs. Code

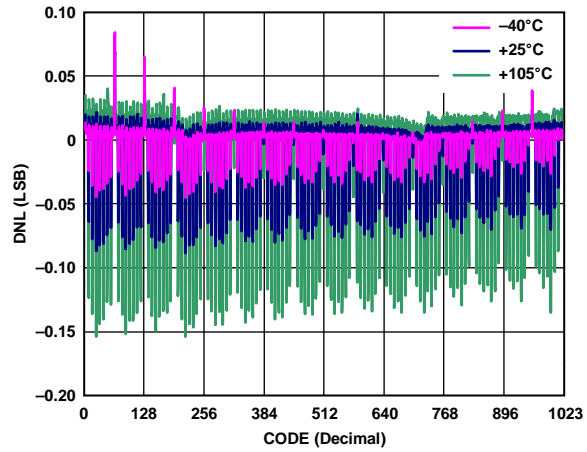


Figure 15. DNL in Normal Mode vs. Code

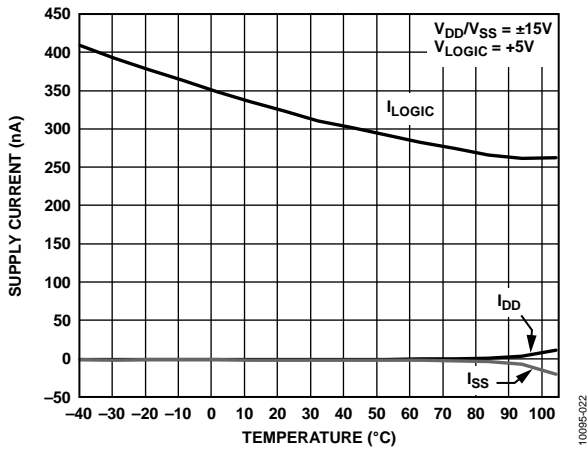


Figure 13. Supply Current ( $I_{DD}$ ,  $I_{SS}$ ,  $I_{LOGIC}$ ) vs. Temperature

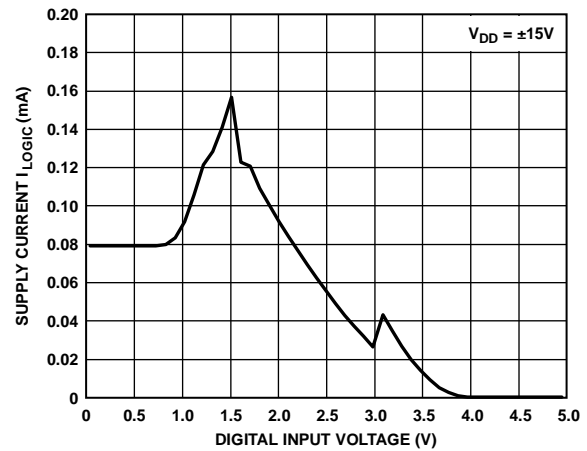


Figure 16. Supply Current  $I_{LOGIC}$  vs. Digital Input Voltage

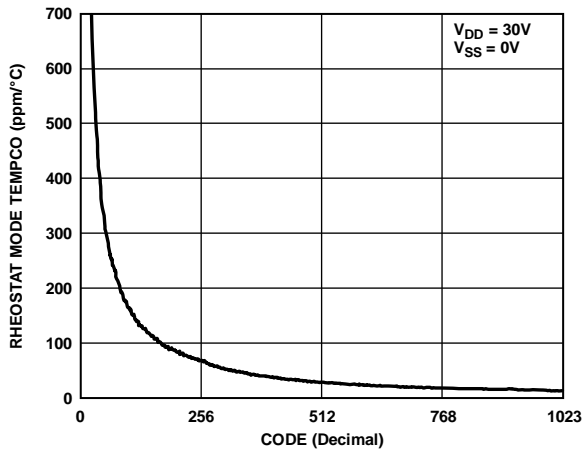


Figure 14. Rheostat Mode Tempco  $\Delta R_{WB}/\Delta T$  vs. Code

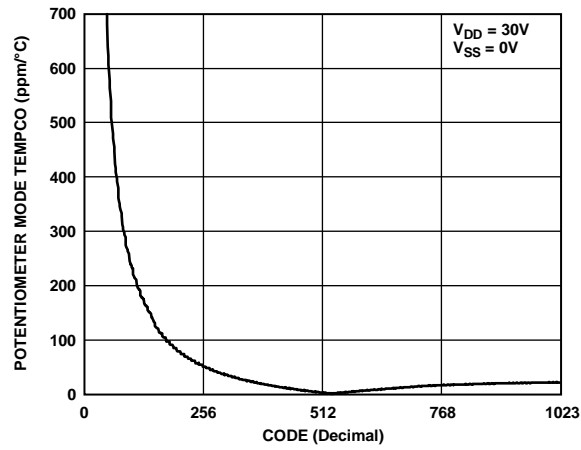


Figure 17. Potentiometer Mode Tempco  $\Delta R_{WB}/\Delta T$  vs. Code

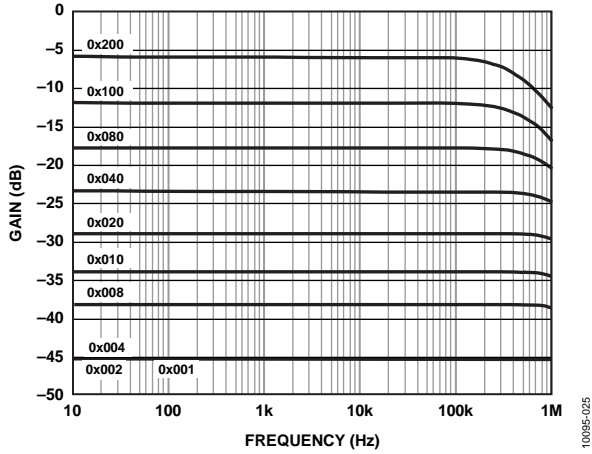


Figure 18. 20 kΩ Gain vs. Frequency vs. Code

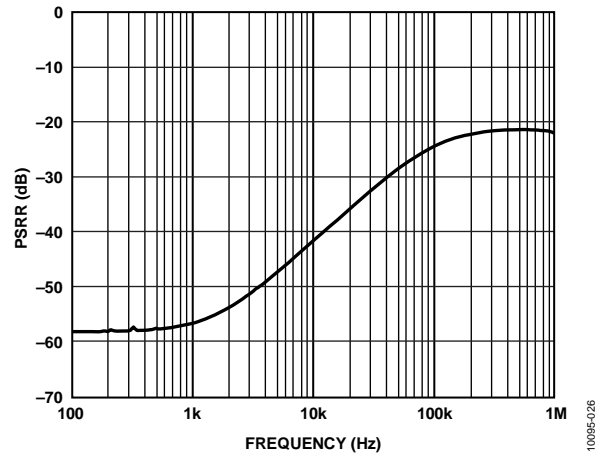


Figure 21. Power Supply Rejection Ratio vs. Frequency

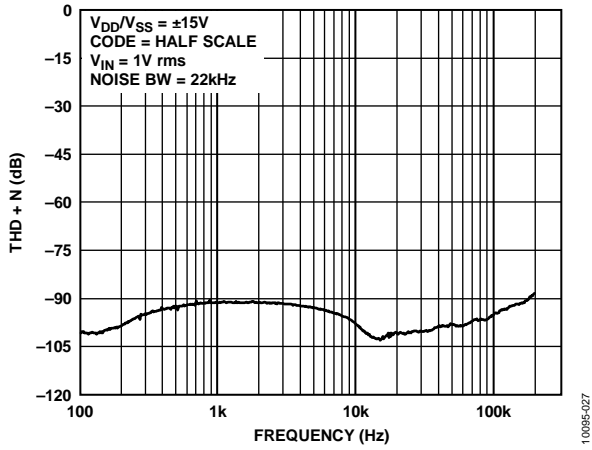


Figure 19. THD + Noise vs. Frequency

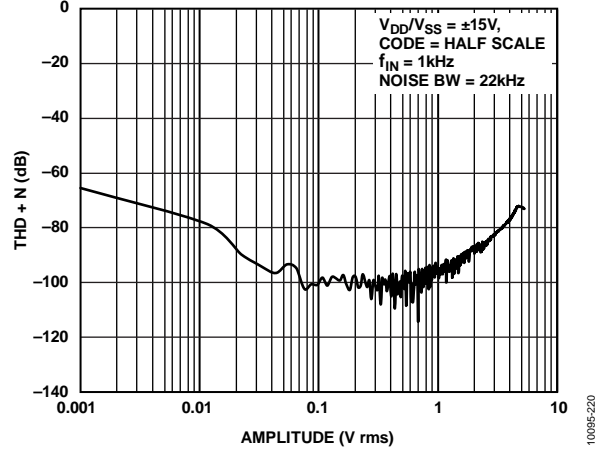


Figure 22. THD + Noise vs. Amplitude

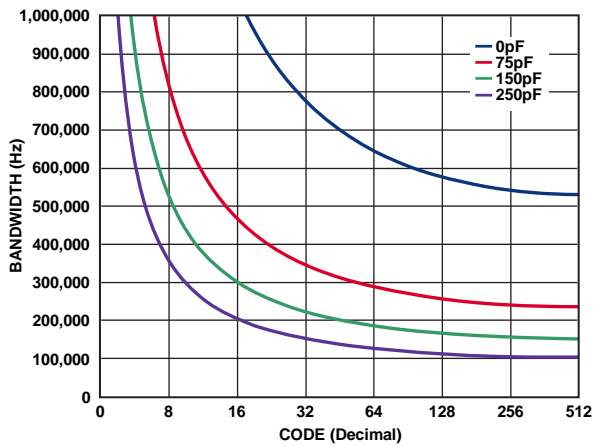


Figure 20. Bandwidth vs. Code vs. Net Capacitance

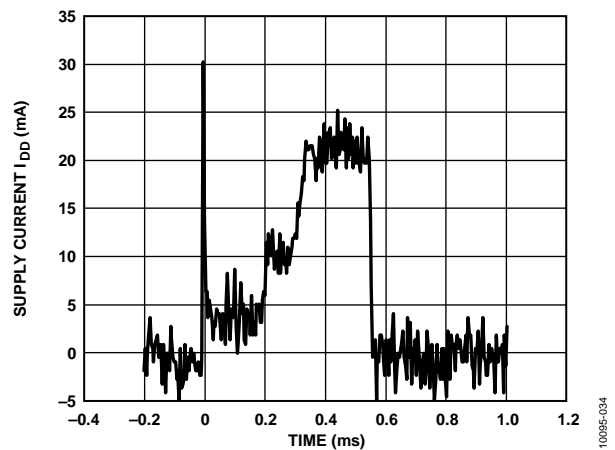


Figure 23.  $I_{DD}$  Waveform While Blowing/Reading Fuse

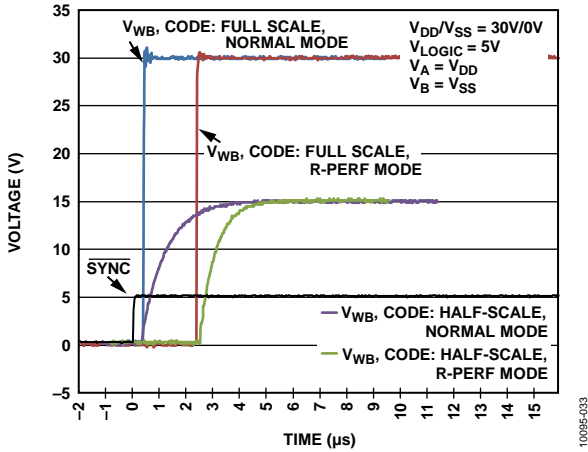


Figure 24. Large-Signal Settling Time from Code Zero Scale

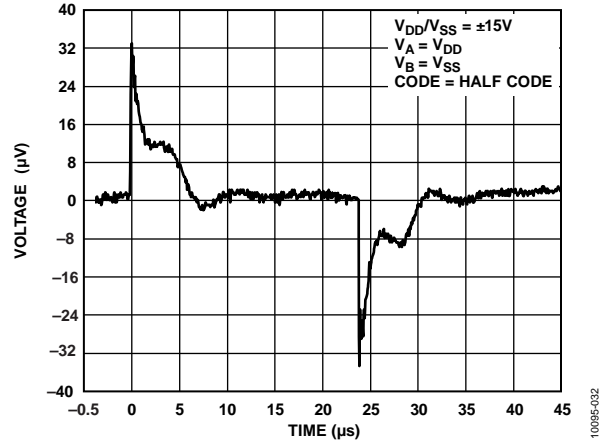


Figure 27. Digital Feedthrough

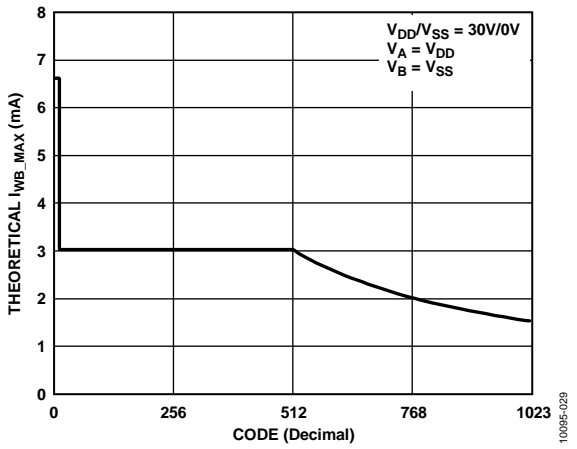


Figure 25. Theoretical Maximum Current vs. Code

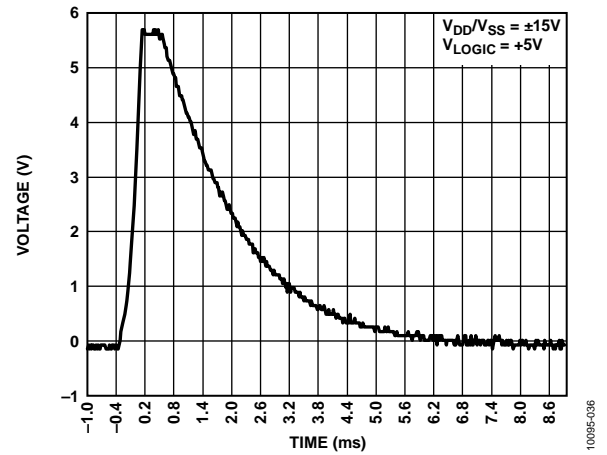


Figure 28.  $V_{EXT\_CAP}$  Waveform While Reading Fuse Or Calibration

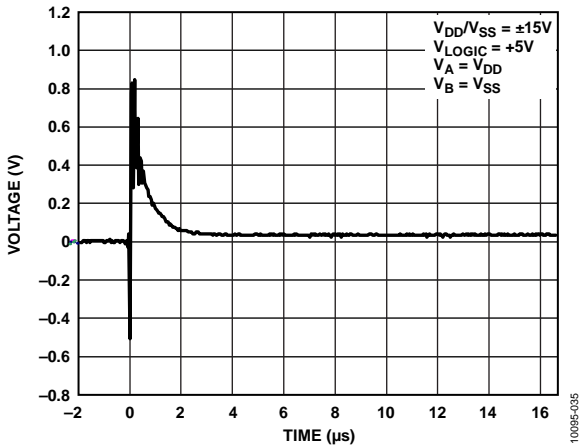


Figure 26. Maximum Transition Glitch

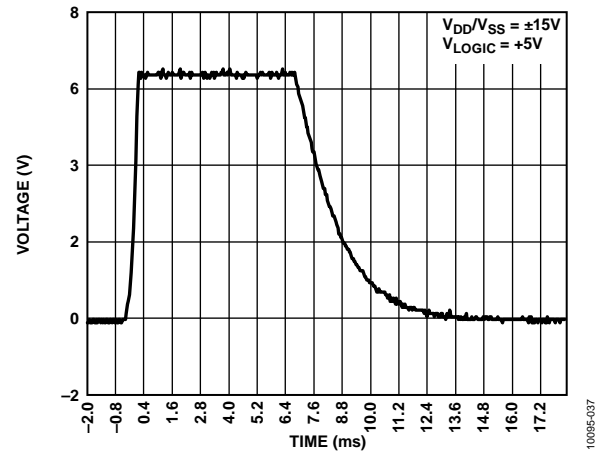


Figure 29.  $V_{EXT\_CAP}$  Waveform While Writing Fuse

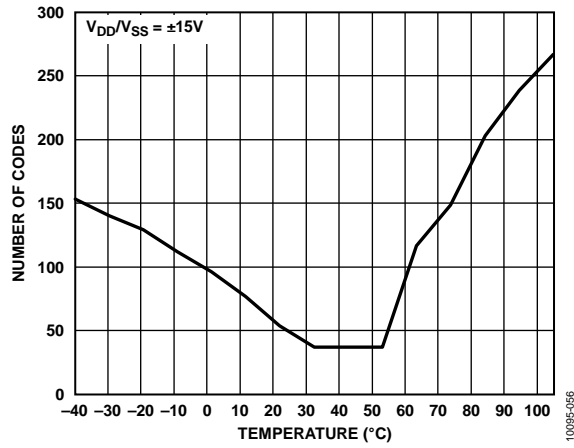


Figure 30. Code Range > 1% R-Tolerance Error vs. Temperature

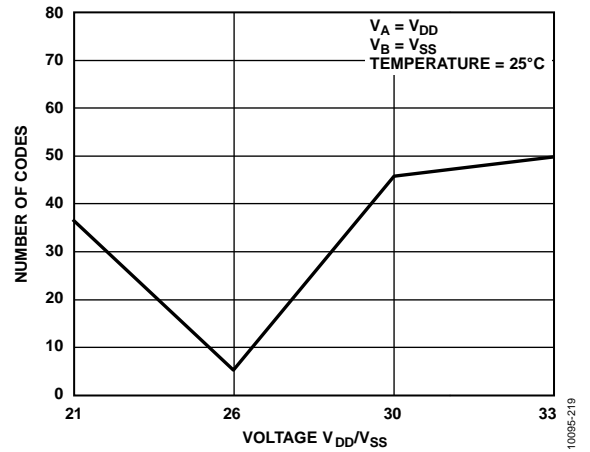


Figure 31. Code Range > 1% R-Tolerance Error vs. Voltage

TEST CIRCUITS

Figure 32 to Figure 37 define the test conditions used in the Specifications section.

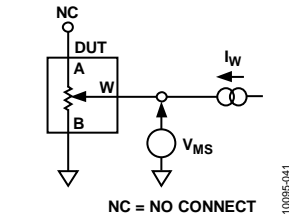


Figure 32. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

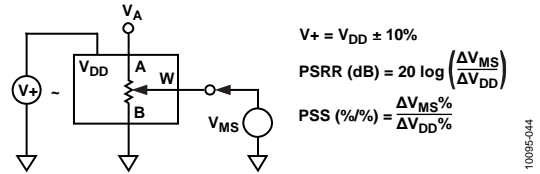


Figure 35. Power Supply Sensitivity (PSS, PSRR)

$$V_+ = V_{DD} \pm 10\%$$

$$PSRR \text{ (dB)} = 20 \log \left( \frac{\Delta V_{MS}}{\Delta V_{DD}} \right)$$

$$PSS \text{ (%/%) } = \frac{\Delta V_{MS}\%}{\Delta V_{DD}\%}$$

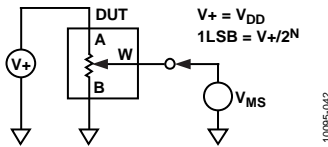


Figure 33. Potentiometer Divider Nonlinearity Error (INL, DNL)

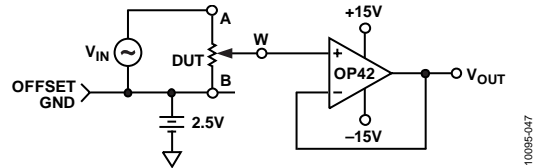


Figure 36. Gain vs. Frequency

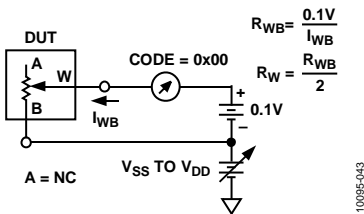


Figure 34. Wiper Resistance

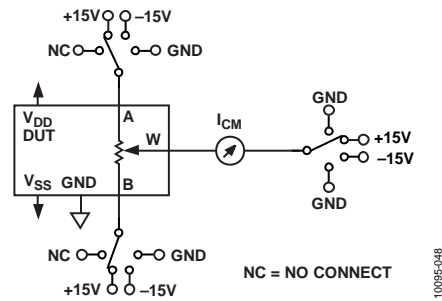
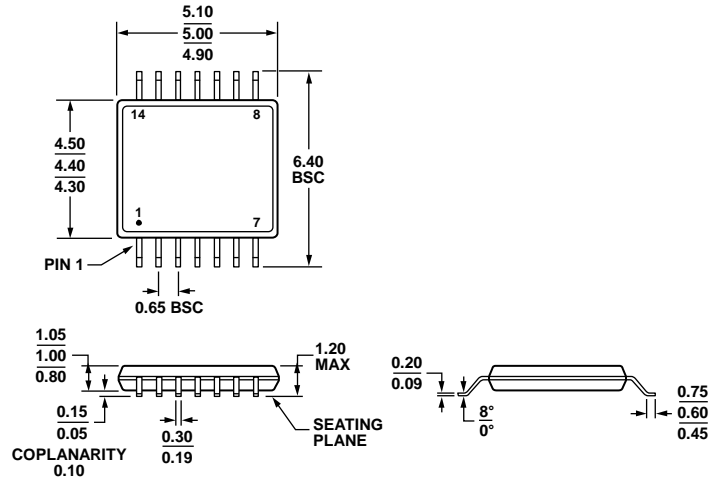


Figure 37. Common-Mode Leakage Current

### OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 38. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)  
 Dimensions shown in millimeters

061908-A

### ORDERING GUIDE

Model <sup>1</sup>	R <sub>AB</sub> (kΩ)	Resolution	Memory	Temperature Range	Package Description	Package Option
AD5292SRU-20-EP	20	1024	20-TP	-55°C to +125°C	14-Lead TSSOP	RU-14
AD5292SRUZ-20-EP	20	1024	20-TP	-55°C to +125°C	14-Lead TSSOP	RU-14

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**



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