One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

### Evaluating the AD7606C-18 8-Channel DAS with 18-Bit, 1 MSPS Bipolar Input, Simultaneous Sampling ADC

#### FEATURES

Fully featured evaluation board for the AD7606C-18 On-board power supplies Standalone capability SDP-H1 compatible PC software for control and data analysis Time and frequency domain

#### EVALUATION KIT CONTENTS EVAL-AD7606C18FMCZ evaluation board

#### ADDITIONAL EQUIPMENT NEEDED

EVAL-SDP-CH1Z (SDP-H1) high speed controller board PC running Windows Vista SP2 (32-bit or 64-bit), Windows 7 SP1 (32-bit or 64-bit), Windows 8.1 (32-bit or 64-bit), or Windows 10 (32-bit or 64-bit) with a USB 2.0 port DC and ac signal source SMB and USB cables External supply (optional)

#### DOCUMENTS NEEDED

AD7606C-18 data sheet

#### **ONLINE RESOURCES**

ACE software AD7606C-18 ACE plugin (provided in the ACE software) AD7606x Family Software Model

#### **EVALUATION BOARD DESCRIPTION**

The EVAL-AD7606C18FMCZ is a fully featured evaluation board that allows users to evaluate the features of the AD7606C-18 analog-to-digital converter (ADC). The EVAL-AD7606C18FMCZ is controlled by the EVAL-SDP-CH1Z (SDP-H1) system demonstration platform (SDP). The SDP-H1 controls the EVAL-AD7606C18FMCZ through the USB port of a PC using the Analysis | Control | Evaluation (ACE) software, which is available to download from the ACE software page or the AD7606C-18 product page.

The on-board components include the ADP7118 5 V and 3.3 V low noise, low dropout (LDO) linear regulators and an ADR4525 high precision, band gap voltage reference.

Figure 1 shows the evaluation board photograph. The printed model number on the evaluation board is EVAL-AD7606CFMCZ.

For full details on the AD7606C-18, see the AD7606C-18 data sheet, which must be consulted in conjunction with this user guide when using the EVAL-AD7606C18FMCZ. In addition, full details on the SDP-H1 are available on the SDP-H1 product page.



#### **EVALUATION BOARD PHOTOGRAPH**

PLEASE SEE THE LAST PAGE FOR AN IMPORTANT WARNING AND LEGAL TERMS AND CONDITIONS.

### TABLE OF CONTENTS

Features
Evaluation Kit Contents 1
Additional Equipment Needed 1
Documents Needed 1
Online Resources
Evaluation Board Description1
Evaluation Board Photograph1
Revision History
Evaluation Board Quick Start Guide 3
Evaluation Board Hardware 4
Device Description
Hardware Link Options 4
Connectors and Sockets 4
Power Supplies 4
Channel Input4

6
6
8
9
9
9
11
12
12
13
13
13
13

#### **REVISION HISTORY**

10/2020—Revision 0: Initial Version

### **EVALUATION BOARD QUICK START GUIDE**

To quickly evaluate the AD7606C-18 ADC, take the following steps:

- Download and install the ACE software from the AD7606C-18 product page or the ACE software page. When installing the ACE software, ensure that the SDP-H1 is disconnected from the USB port of the PC. Restart the PC after the installation process completes. For complete software installation instructions, see the Software Installation section.
- 2. Ensure that the link options are configured as detailed in Table 2.
- 3. Connect the SDP-H1 to the EVAL-AD7606C18FMCZ. By default, the power for the EVAL-AD7606C18FMCZ is

supplied by the SDP-H1. See the Power Supplies section for the available power options.

- 4. Connect the SDP-H1 to the 12 V supply (included in the SDP-H1 kit) and to the PC via the USB cable. If prompted by the operating system, choose to automatically search for the drivers for the SDP-H1.
- Launch the ACE software from the following location: C:\Program Files (x86)\Analog Devices\ACE.
- 6. Connect an input signal via the Channel 1 to Channel 8 terminal blocks or the Subminiature Version B (SMB) connectors, J1 to J8.

### **EVALUATION BOARD HARDWARE** DEVICE DESCRIPTION

The AD7606C-18 is an 18-bit, 8-channel, simultaneous sampling, successive approximation register (SAR) ADC. The device operates from a single 4.75 V to 5.25 V power supply and features throughput rates of up to 1 MSPS. The device has 1 M $\Omega$  input impedance for direct connection from the user sensor outputs to the ADC.

#### HARDWARE LINK OPTIONS

Table 2 details the link option functions and the default power link options. The EVAL-AD7606C18FMCZ can be powered by different sources, as described in the Power Supplies section. By default, the power supply required for the EVAL-

AD7606C18FMCZ comes from the SDP-H1. The power supply is regulated by the on-board ADP7118 LDO linear regulators, which generate the 5 V and 3.3 V supplies.

#### **CONNECTORS AND SOCKETS**

The connectors and sockets on the EVAL-AD7606C18FMCZ are detailed in Table 1.

#### Table 1. On-Board Connectors

Connector	Function
J1 to J8	Analog input SMB connectors to Channel 1
	through Channel 8
J9	Analog input SMB connector to external reference
P1, P2, P3	General connectors for debugging purposes or to
	connect an external controller
P4	External power terminal block, 7 V to 9 V dc input
P5	External reference connection
P6, P8	8-pin connectors for input to Channel 1 through
	Channel 4
P7, P11	Channel 8 surfboard evaluation headers
P9, P10	8-pin connectors for input to Channel 5 through
	Channel 8
P12	FMC connector

#### Table 2. Link Options

The default interface to the EVAL-AD7606C18FMCZ is achieved via the field programmable gate array (FPGA) mezzanine card (FMC) connector, which connects the EVAL-AD7606C18FMCZ to the SDP-H1.

#### **POWER SUPPLIES**

Before applying power and signals to the EVAL-AD7606C18FMCZ, ensure that all link positions are set according to the required operating mode. See Table 2 for the complete list of link options.

The supply required for the EVAL-AD7606C18FMCZ comes from the SDP-H1. Alternatively, the EVAL-AD7606C18FMCZ can also be supplied with a dc power supply connected to the P4 terminal block. Select the external power supply or the SDP-H1 supply through JP2. The power supply is then connected to the on-board ADP7118 5 V and 3.3 V LDO linear regulators that supply the proper bias to each of the various sections on the EVAL-AD7606C18FMCZ.

#### **CHANNEL INPUT**

The J1 to J8 connectors allow the user to connect external signals to the ADC channel inputs through the SMB inputs. The EVAL-AD7606C18FMCZ is supplied with the AD7606C-18 mounted (U4, see Figure 1). The AD7606C-18 is an 8-channel data acquisition system (DAS) with a simultaneous sampling ADC. External signals can be applied to the P6, P8, P9, and P10 connectors on the EVAL-AD7606C18FMCZ.

Link	Default Position	Function
JP1	А	The ACE software controls the STBY pin. When using the EVAL-AD7606C18FMCZ in standalone mode
		without running the ACE software, JP1 allows the selection of standby mode. In this case, change the R8 and R10 resistors to 0 $\Omega$ links.
		In Position A, the $\overline{\text{STBY}}$ pin is tied to $V_{DRIVE}$ .
		In Position B, the STBY pin is tied to AGND.
JP2	А	JP2 selects the power supply source for the EVAL-AD7606C18FMCZ.
		In Position A, the unregulated supply to the on-board LDOs is taken from the SDP-H1 12 V supply.
		In Position B, the unregulated external supply to the on-board LDOs is taken from the P4 terminal block connector.

Link	<b>Default Position</b>	Function
JP3	A	Use JP3 to select the V <sub>DRIVE</sub> source for the AD7606C-18.
		In Position A, the AD7606C-18 is supplied with 3.3 V from the ADP7118.
		In Position B, the AD7606C-18 is supplied with 3.3 V from the SDP-H1.
JP4	А	The ACE software controls the RANGE pin. If using the EVAL-AD7606C18FMCZ in standalone mode, JP4
		allows the selection of the analog input range in hardware mode. In this case, change the R20 resistor to a
		$0 \Omega$ link.
		In Position A, the RANGE pin is tied to $V_{DRIVE}$ , and the ±10 V range is selected.
		In Position B, the RANGE pin is tied to AGND, and the $\pm 5$ V range is selected.
		In software mode, the RANGE pin is ignored.
JP5	А	The ACE software controls the PAR/SER SEL pin. If using the EVAL-AD7606C18FMCZ in standalone mode,
		JPS allows the selection of the digital interface. In this case, change the RT9 and R2T resistors to 0 $\Omega$ links
		In Position A, the PAR/SER SEL pin is tied to $v_{DRIVE}$ , and the serial interface is selected.
		In Position B, the PAR/SER SEL pin is tied to AGND, and the parallel interface is selected.
JP6	A	The ACE software controls the REF SELECT pin. By default, the internal reference is selected. If switching to
		the external reference is required through the ACE software, P5 must be inserted. If using the EVAL-
		R13 resistor to a 0 $\Omega$ link.
		In Position A, the REF SELECT pin is tied to VDRIVE, and the internal reference is enabled and selected. P5
		must be unpopulated.
		In Position B, the REF SELECT pin is tied to AGND, the internal reference is disabled, and the external
		reference is selected. P5 must be inserted if using the on-board U1 devices, and must not be inserted if
107		using the J9 SMB connector.
JP7	В	JP7 selects the VI – line to be connected to ground (single-ended operation) or to the SMB connector (differential operation)
		Position A connects the V1- line to ground for single-ended operation.
		Position B connects the V1– line to the J5 SMB connector and disconnects the V1– line from ground.
JP8, JP10	A	Position A bypasses the amplifier mezzanine card (AMC).
		Position B enables the AMC to be connected on the P7 and P11 headers.
JP9, JP11	A	Position A bypasses the AMC.
		Position B enables the AMC to be connected on the P7 and P11 headers.
JP12	В	JP12 selects the V2– line to be connected to ground (single-ended operation) or to the SMB connector
		(differential operation).
		Position A connects the $V_2$ line to ground for single-ended operation.
1010	<b>D</b>	Position B connects the $V_2$ – line to the J6 SMB connector and disconnects the $V_2$ – line from ground.
JP13	В	(differential operation).
		Position A connects the V3– line to ground for single-ended operation.
		Position B connects the V3– line to the J7 SMB connector and disconnects the V3– line from ground.
JP14	В	JP14 selects the V4- line to be connected to ground (single-ended operation) or to the SMB connector
		(differential operation).
		Position A connects the V4– line to ground for single-ended operation.
		Position B connects the V4– line to the J8 SMB connector and disconnects the V4– line from ground.
P13	Not inserted	Inserting P13 connects the V5– line to ground.
P14	Not inserted	Inserting P14 connects the V8– line to ground.
P15	Not inserted	Inserting P15 connects the V6– line to ground.
P16	Not inserted	Inserting P16 connects the V7– line to ground.
S1	Open	The ACE software controls the OS0, OS1, and OS2 pins. If using the EVAL-AD7606C18FMCZ in standalone mode, these switches select the logic level on the OS0, OS1, and OS2 pins.

### **EVALUATION BOARD SOFTWARE** software installation

Download the ACE software from the ACE software page or the AD7606C-18 product page. Both the ACE software and the SDP-H1 board drivers must be installed.

#### Warning

The ACE software and SDP-H1 drivers must be installed before connecting the EVAL-AD7606C18FMCZ and the SDP-H1 to the USB port of the PC to ensure that the evaluation system is properly recognized when it is connected to the PC.

#### Installing the ACE Software

To install the ACE software, take the following steps:

- 1. Download the ACE software to a Windows® based PC.
- Double click the ACEInstall.exe file to begin the installation. By default, the software is saved to the following location: C:\Program Files (x86)\Analog Devices\ACE.
- 3. A dialog box opens asking for permission to allow the program to make changes to the PC. Click **Yes** to begin the installation process.
- 4. In the **ACE Setup** window, click **Next** > to continue the installation (see Figure 2).



Figure 2. ACE Software Installation Confirmation

5. Read the software license agreement and click **I Agree** (see Figure 3).



Figure 3. License Agreement

6. Click **Browse...** to choose the installation location and then click **Next** > (see Figure 4).

🛗 ACE Setup	
Choose Install Location Choose the folder in which to install ACE.	
Setup will install ACE in the following folder. To install in a different folder select another folder. Click Next to continue.	; click Browse and
Destination Folder           C:\Program Files (x86)\Analog Devices\ACE	Browse
Space required: 93.1MB Space available: 15.1GB Nullsoft Install System v3.01 <back next=""></back>	Cancel

Figure 4. Choose Installation Location

25052-004

### UG-1870

25052-008

7. The ACE software components to install are preselected (see Figure 5). Click **Install**.



Figure 5. Choose Components

8. The **Windows Security** window opens (see Figure 6). Click **Install**. Figure 7 shows the installation in progress. No action is required.



Figure 6. Windows Security Window

1:	stalling
P	lease wait while ACE is being installed.
F	xtrart: AnalooDevices.Csa.Ann.Installers.dll 100%
ī	Extract: AD9680Fs1GFin173Full8W.txt 100%
	Extract: AD9680SampleDDC500.txt 100%
	Extract: adianalysis.dll 100%
	Extract: AnalogDevices.Csa.Analysis.dll 100%
	Extract: AnalogDevices.Csa.Analysis.pdb 100%
	Extract: AnalogDevices.Csa.Analysis.Test.pdb 100%
	Extract: AnalogDevices.Csa.App.DataInstallers.dll 100%
	Extract: AnalogDevices.Csa.App.DataInstallers.dll.config 100%
	Extract: AnalogDevices.Csa.App.DataInstallers.pdb 100%
	Extract: AnalogDevices.Csa.App.Installers.dll 100%
19	soft Install System v3.01
	< Back Next > Cancel

9. When the installation is complete, click **Next** > (see Figure 8), and then click **Finish** to complete the installation process.

🔜 ACE Setup	
Installation Complete Setup was completed successfully.	
Completed	
Extract: Chip.ADF4355.1.1.1.nupkg 100% Extract: Chip.ADGS1412.1.0.7.nupkg 100% Extract: Chip.ADRF6780.1.1.0.nupkg 100% Extract: Chip.Generic.1.6.2542.0.nupkg 100% Extract: Chip.GenericFpga.1.6.2542.0.nupkg 100% Extract: Hardware.ClockSupport.1.6.2542.0.nupkg 100% Extract: Hardware.SdpSupport.1.6.2542.0.nupkg 100% Extract: Hardware.SdpSupport.1.6.2542.0.nupkg 100% Extract: Hardware.SdpSupport.1.6.2542.0.nupkg 100% Extract: Hardware.SdpSupport.1.6.2542.0.nupkg 100%	ckages
Nullsoft Install System v3.01 < Back Next >	Cancel
Figure 8. Installation Complete	

#### **EVALUATION BOARD SETUP PROCEDURES**

The EVAL-AD7606C18FMCZ connects to the SDP-H1. The SDP-H1 is the communication link between the PC and the EVAL-AD7606C18FMCZ.

### Connecting the EVAL-AD7606C18FMCZ and the SDP-H1 to a PC

After the ACE software is installed, take the following steps to set up the EVAL-AD7606C18FMCZ and the SDP-H1:

- 1. Ensure that all configuration links are in the appropriate positions, as detailed in Table 2.
- 2. Connect the EVAL-AD7606C18FMCZ to the 160-way connector on the SDP-H1. The EVAL-AD7606C18FMCZ does not require an external power supply adapter.
- 3. To power up the SDP-H1, insert the 12 V, dc barrel jack (provided in the SDP-H1 kit) into the barrel connector labeled +12V\_VIN on the SDP-H1.
- 4. Connect the SDP-H1 to the PC via the USB cable included in the SDP-H1 kit.

#### Verifying the Board Connection

After connecting the power and the USB cable from the SDP-H1 to the PC, take the following steps to verify the SDP-H1 connection:

- After connecting the SDP-H1 to the PC, allow the Found New Hardware Wizard to run. Choose to automatically search for the drivers for the SDP-H1 if prompted by the operating system.
- 2. Navigate to the **Device Manager** window on the PC (see Figure 9).

- 3. A dialog box may open asking for permission to allow the program to make changes to the computer. Click **Yes**.
- 4. The Computer Management window opens. From the list labeled System Tools, click Device Manager. If the SDP-H1 driver is installed and the SDP-H1 is properly connected to the PC, Analog Devices SDP-H1 is shown in the ADI Development Tools list in the Device Manager window, as shown in Figure 9.

🚔 Device Manager	
<u>File Action View H</u> elp	
🗢 🔿   📧   🚺 🖬	
BSOMERS-L03	*
🖌 👰 ADI Development Tools	
Analog Devices SDP-H1	
Batteries	=
Bluetooth Radios	
⊳ nter Computer	
Disk drives	
🔈 🖳 Display adapters	
DVD/CD-ROM drives	
Human Interface Devices	
Imaging devices	
	•

Figure 9. Device Manager Window

#### Disconnecting the EVAL-AD7606C18FMCZ

Disconnect power from the SDP-H1, or press the reset tact switch located alongside the mini USB port on the SDP-H1 before disconnecting the EVAL-AD7606C18FMCZ from the SDP-H1.

# ACE SOFTWARE OPERATION LAUNCHING THE SOFTWARE

After the EVAL-AD7606C18FMCZ and SDP-H1 are properly connected to the PC, launch the ACE software by taking the following steps:

- From the Start menu of the PC, select All Programs > Analog Devices > ACE> ACE.exe to open the ACE software main window shown in Figure 10.
- 2. If the EVAL-AD7606C18FMCZ is not connected to the USB port via the SDP-H1 when the ACE software launches, the AD7606C-18 Board icon does not appear in the Attached Hardware section in ACE (see Figure 10). To make the AD7606C-18 Board icon appear, connect the EVAL-AD7606C18FMCZ and the SDP-H1 to the USB port of the PC, wait a few seconds, and then follow the instructions in the dialog box that opens.
- 3. Double click the **AD7606C-18 Board** icon to open the **AD7606C-18 Board** view window shown in Figure 11.
- Double click the AD7606C-18 chip icon in the AD7606C-18 Board view window to open the AD7606C-18 chip view window shown in Figure 12.
- 5. Click **Software Defaults** and then click **Apply Changes** to apply the default settings to the AD7606C-18.

#### **DESCRIPTION OF CHIP VIEW WINDOW**

After completing the steps in the Software Installation section, set up the system for data capture.

Block icons that are dark blue are programmable blocks. Clicking a dark blue block icon opens a configurable pop-up window that allows customization for the data capture, as shown for the Channel 1 input range in Figure 13.

The available programmable blocks in the **AD7606C-18** chip view window are as follows:

- Analog input range, on a per channel basis, through the icon located on each **PGA** block.
- Bandwidth mode, on a per channel basis, through each low-pass filter (LPF) block.
- System gain, offset, and phase calibration settings, on a per channel basis.
- Diagnostic multiplexer.
- Oversampling ratio lines. By setting all the oversampling ratio lines high, the AD7606C-18 enters software mode, and the oversampling ratio is set through the memory map. In hardware mode, these lines select the oversampling ratio.
- Data interface, either serial or parallel.
- Reference selection, either internal or external, through the REF SELECT switch.

	Start			
AVEAD OF WHAT'S POSSIBLE*	Start X			
Systems	Load plug-ins from: %ALLUSERSPROFILE%\Analog Devices\	CE (internal)\Pluging	P	
Plug-in Manager	Attached Hardware			
Remoting Console	AD7606C-18 Board			
Vector Generator	Version 1.2020.13502-dev			
📑 Recent Sessions 🔹				
S Tools	Wanually Add Subsystem	m		
	Explore Without Hardware			
	Plugin ID	Version	Compatible Controllers	
	AD7380 Eval Board	1.2019.49500-dev0029	SDPH1	
	AD7380-4 Eval Board	1.2019.49500-dev0029	SDPH1	010
	AD7381 Eval Board	1.2019.49500-dev0029	SDPH1	052-(
	A/97283 Eval Roard	1.2019.49500dev0029	SDPH1	25

Figure 10. ACE Software Main Window

### UG-1870

### **EVAL-AD7606C18FMCZ** Evaluation Board User Guide

≡, [	ANALOG DEVICES	Start > System > Sul	system_1 > AD7606C-18 Bo	ard >						
All Hom	HEAD OF WHAT'S POSSIBLE*	Start 🗙 System 🗙	O AD7606C-18 Board X							
Syste	ems		N≡							
Plug	-in Manager	Reset Board Poll Device	Auto Apply							
Rem	oting Console									
Vecto	or Generator									
Rece	ent Sessions 🛛 🗸 🗸									
💕 Tool				V1+ 0	<b>○v</b> 1- <b>v</b> 1+○	<b>(5</b> )	2 SV	[11:00:00] SV	(T1/05/00) 2 21/	
				V2+0	<b>○ v2- v2+</b> ○	ADR4	525	ADP7118	ADP7118	
				V3+0			_			
				V3- 0 V4+ 0	O v3- v3+○			IT ANALOG		
				V4-0				La DEVICES		
				V5+	0 v4- v4+0			AD7606C-18	FMC	
				V5- V6+		0				
				V6- Ø V7+ Ø		00				
				V7- Ø		0				
				V8-0		ŏ	EVAL	-AD7606CF	MCZ ii	
~				L						
() Repi	ort Issue									
V Requ	uest Feature									
Appl	lication Usage Logging	ļ								

#### Figure 11. AD7606C-18 Board View



#### Figure 12. AD7606C-18 Chip View Window



Figure 13. Configurable Pop-Up Window

AT OF WARTS PROPERTY						
s. Manuar	Start X Spriter X O ADTOIC-18 Social X ADTOI ADDY AD	ec-so >	ADROSC 15 Memory Map X	of ChaView Steed-Scher		
	Select View	Registers				
a course	A benting O bit facts	+1.	Address (Hea)	None	Data (Hex)	Data (Einary)
	a agent of an age		00003001	* STATUS	¢i.	1 0 0 1 0 0 0
	is Carly Film		00000002	conng	08	8008180
	Dry Show Registers To Apply O	1.1	0000001	* RANGE_0H3_012	31	0 0 1 ± 0 0 1
	Revision Mars (Davi	100	00000004	* RANGE, OH2, OH4	33	0 0 1 1 0 0 1
		1.4	00001005	* RANGE_OHS_OHS	33	0 0 1 t 0 0 1
	Functional George Titler 🗸 🗸 🗸	1.0	00001006	* RANGE_OH7_CHS	33	0 0 1 1 0 0 1
	Attink lands A	14	00000007	Bandwidth	00	0 0 0 8 0 0 0
		1.0	00000008	OVERSMARTING	01	0000000
	Search 61 Fields		00000009	- CHI_GAN	00-1	0 0 0 0 0 0 0
	Results	1.4	00003064	- 0-0_00a	08	8 0 0 0 0 0
	0x0001 DIGTAL BISIOR		00000008	• 04,000	01	0 0 0 0 0 0
	0x0001: RESET_DETECT	14	00000000	* OHLGAB	01	<b>X R D B D D D</b>
	6x0000 EOUT_FORMAT		00001000	· CHE, GAIN	00	8 0 0 8 0 0 0
	Ox0000: ENT, OS, CLOCK	1	0000000E	* CHE_GAIR	00	8 8 0 8 0 0 0
	0x0002: SIARDS_HEADER 0x0002: CH1, RANGE		0000100F	· CHT_GAIN	00	0 0 0 0 0 0
	0x0000 CHQ_RANGE		00000010	* CHE_GAIN	00	8 8 0 8 0 0 0
	0x00xx CH1_RANGE		00000011	CH1_DHSET	80	100000
	0x0005 CH5 RANGE		000090\2	crg_orrset	01	1000000
	0x0006 CHT_RANGE		00003013	cid_priset	00	1 0 0 0 0 0
	DNDDDE: CHE_RANGE	14	00003014	CHI, DIFST	81	1 0 0 0 0 0 0
	0x0007: wide_bw_ch0 0x0007: wide_bw_ch1		00000015	cie_ousit	81	1000000
	0x0007 wide_bw_ch2		00000016	CHE_DIFSIT	82	100800
	0x0007: wide_bw_014		000000/17	CHT OFFSET	81	100200
	0x0007 wide_bw,xh5		00000018	CHE_OFFSET	80	1000000
	CHOIDCT: WILDE, DW, CT.7		000000/9	CHT, PHISE	01	2002200
	0x0000 cs_satio		000000A	CH2, PHASE	00	0000000
	0x0006 CH1_CAIN		000000-18	CP0, PHISE	OT .	20022000
	0x000A: CH2_GAIN 0x000B: CH2_GAIN		000000-0	CTH_PHASE	E OII	0 0 0 0 0 0 0
estare	DIODOCI CH4, GAIN		00000010	CHLINKE	01	

Figure 14. AD7606C-18 Memory Map View Window

#### **DESCRIPTION OF MEMORY MAP VIEW WINDOW**

Click **Proceed to Memory Map** in the **AD7606C-18** chip view window (see Figure 12) to open the **AD7606C-18 Memory Map** view window shown in Figure 14. The **AD7606C-18 Memory Map** view window shows all registers of the AD7606C-18.

The registers of the AD7606C-18 are populated with default values when powered up. To implement the values changed in all of the registers, click **Apply Changes** to write to the registers.

In some cases, the values of every register have been changed, but the user wants to implement changes on a selected register only. Click **Apply Selected** to write the new value on the selected register to the AD7606C-18.

Click **Read All** to read the values of all the registers from the chip.

Click **Read Selected** to read the selected register from the chip.

Click Reset Chip to prompt the software to reset the AD7606C-18.

Click **Diff** to check for differences in register values between the software and the chip.

To revert all the register values back to their defaults, click **Software Defaults**, and then click **Apply Changes** to write to the AD7606C-18.

### UG-1870

### EVAL-AD7606C18FMCZ Evaluation Board User Guide

	-	CADTURE		0000070	
	M	CAPTURE (	ANALYSIS (	RESULIS	
Menager	(m)	Restore Software Delauits	Restore Active Settings Restore Defaults	(Andread ) ( Andread	Waveform
ng Console	intogram	General Capture Settings	General Settings.	Oliptay Chamble	30
ienetatar 🗸		Throughput (KSPS): 200	Prefer dBFS Two Tone Eastler: Single Tone V	Control Data Sec.	
iessiens 🐱	HT	Sample Count: 131072 V	Set Fundamental: Manually		*
~		Device Configuration	Windowing		
		Made: Software V	Window: Blackman Harris 4 🗸		8
		Resteutorial Capture Patallel V	Number of Harmonics 5		
		Oversampling Ratio Coftwaret: Cff 🛛 👻	Fundamental Bins: 10		÷
		Toggle Reset Pin: Toggle Reset Pin	Harmonic Bris: 5		8.
			DC Bing 6		9
			Worst Other Bins: 2		2
			Single Tone Analysis		Get started by importing some data or running
			Single Tane Fundamental (MP4) 0 MP42 *		g s capturel
			Two Tone Analysis		tengal (
			First Fundamental (MPIp 0 MPIp 1		* · · · · · · · · · · · · · · · · · · ·
			Second Fundamental (NHc) 0 MHz 1		
					3
					2
					0 1 2 3 4 5 6 7 8 9
rature		and an and a second sec		and a second second second second second	Time (ms)

Figure 15. AD7606C-18 Analysis View Window

#### **DESCRIPTION OF ANALYSIS WINDOW**

Click **Proceed to Analysis** in the **AD7606C-18** chip view window (see Figure 12) to open the **AD7606C-18 Analysis** view window shown in Figure 15. The analysis view window contains the **Waveform** tab, **Histogram** tab, and **FFT** tab.

#### **WAVEFORM TAB**

The **Waveform** tab displays data in the form of time vs. discrete data values with the results, as shown in Figure 16.

#### **CAPTURE** Pane

The **CAPTURE** pane contains the capture settings, which reflect onto the registers automatically before data capture.

The **Sample Count** pulldown menu in the **General Capture Settings** section allows the user to select the number of samples per channel per capture (see Figure 16).

The user can enter the input sample frequency in kSPS in the **Throughput (kSPS)** box in the **General Capture Settings** section (see Figure 16). Refer to the AD7606C-18 data sheet to determine the maximum sampling frequency for the selected oversampling ratio and data interface mode.

The **Mode** pulldown menu in the **Device Configuration** section can be set as either **Hardware**, meaning that the device is configured through digital input pins, or **Software**, which allows reading and writing of the memory map and enables a wider range of features (see Figure 16). Refer to the AD7606C-18 data sheet to determine the benefits of hardware and software mode.

The **Parallel/Serial Capture** pulldown menu in the **Device Configuration** section allows the user to select the data interface as either **Parallel** or **Serial** (see Figure 16). If **Serial** is selected, the number of data lines can be selected through the **DOUT Configuration** pulldown menu. The **Oversampling Ratio (Software)** pulldown menu in the **Device Configuration** section can be set between 2 and 64 (in hardware mode) or 256 (in software mode) and provides improved signal-to-noise ratio (SNR) performance (see Figure 16). Refer to the AD7606C-18 data sheet to determine the maximum oversampling ratio for the selected oversampling mode.

When hardware mode is enabled, the **Input Range** pulldown menu allows the user to select an input span between  $\pm 10$  V and  $\pm 5$  V. In software mode, the input span is selected either in the **AD7606C-18 Memory Map** or a configurable pop-up window in the **AD7606C-18** chip view window, as shown in Figure 13.

The **Toggle Reset Pin** button in the **Device Configuration** section issues a full reset to the AD7606C-18 (see Figure 16). Refer to the AD7606C-18 data sheet for the different reset options available on the AD7606C-18.

Click **Run Once** to start a data capture of the samples at the sample rate specified in the **Throughput (kSPS)** pulldown menu for the number of samples specified in the **Sample Count** pulldown menu (see Figure 16). These samples are stored on the FPGA device and are only transferred to the PC when the sample frame is complete.

Click **Run Continuously** to start a data capture that gathers samples continuously with one batch of data at a time (see Figure 16). This operation runs the **Run Once** operation continuously.

#### **RESULTS** Pane

The **Display Channels** section allows the user to select the channels to capture (see Figure 16). The channel data is shown only if that channel is selected before the capture.

The **Waveform Results (Codes)** and **Waveform Results (Volts)** sections display the amplitude, sample frequency, and noise analysis data for the selected channels (see Figure 16).

Click **Export** to export the captured data (see Figure 16). The waveform, histogram, and FFT data is stored in .xml files along with the values of parameters at capture.

The data **Waveform** graph shows each successive sample of the ADC output (see Figure 16). The user can zoom in and out and pan over the **Waveform** graph using the embedded waveform tools above the graph. Select the channels to display in the **Display Channels** section.

Under the **Display Units** pulldown menu, select **Codes** above the **Waveform** graph (see Figure 16) to select whether the **Waveform** graph displays in units of **Codes**, **Hex**, or **Volts**. The axis controls are dynamic.

When selecting either **y-scale dynamic** or **x-scale dynamic**, the corresponding axis width automatically adjusts to show the entire range of the ADC results after each batch of samples. Select the dynamic using the **XYDirection** tool (see Figure 16).

#### **HISTOGRAM TAB**

The **Histogram** tab contains the **Histogram** graph and the **RESULTS** pane, as shown in Figure 17.

The **RESULTS** pane displays the information related to the dc performance.

The **Histogram** graph displays the number of hits per code within the sampled data (see Figure 17). The **Histogram** graph is useful for dc analysis and indicates the noise performance of the AD7606C-18.

#### **FFT TAB**

The **FFT** tab displays the fast Fourier transform (FFT) information for the last batch of samples gathered (see Figure 18).

#### ANALYSIS Pane

The **General Settings** section allows the user to set up the preferred configuration of the FFT analysis, including how many tones are analyzed. The fundamental is set manually.

The **Windowing** section allows the user to select the windowing type used in the FFT analysis, the number of **Harmonic Bins**, and the number of **Fundamental Bins** that must be included.

The **Single Tone Analysis** and **Two Tone Analysis** sections allow the user to select the fundamental frequency included in the FFT analysis. Use the **Two Tone Analysis** settings when analyzing two frequencies.

#### **RESULTS** Pane

The **Signal** section displays the **Fund Frequency** and **Fund Power** (see Figure 18).

The **Noise** section displays the **SNR** and other noise performance results (see Figure 18).

The **Distortion** section displays the harmonic content of the sampled signal and dc power when viewing the FFT analysis (see Figure 18).

#### **AUTOMATED TEST OPERATION**

To perform the automated test for the AD7606C-18, see the AD7606C ACE Remote Control page on the Analog Devices, Inc., website and follow the instructions to operate the hardware and software, set up the Python/MATLAB environment, and begin communication between the ACE software and the Python/MATLAB script.

#### **EXITING THE SOFTWARE**

To exit the software, click File and then click Exit.



UG-1870

Figure 16. Waveform Tab



Figure 17. Histogram Tab



Figure 18. **FFT** Tab

#### ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

#### Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer, all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NONINFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS. DELAY COSTS. LABOR COSTS OR LOSS OF GOODWILL, ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS (\$100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.

©2020 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners. UG25052-10/20(0)



www.analog.com

### **X-ON Electronics**

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Data Conversion IC Development Tools category:

Click to view products by Analog Devices manufacturer:

Other Similar products are found below :

EVAL-AD5063EBZ EVAL-AD5422LFEBZ EVAL-AD7265EDZ EVAL-AD7641EDZ EVAL-AD7674EDZ EVAL-AD7719EBZ EVAL-AD7767-1EDZ EVAL-AD7995EBZ AD9114-DPG2-EBZ AD9211-200EBZ AD9251-20EBZ AD9251-65EBZ AD9255-125EBZ AD9284-250EBZ AD9613-170EBZ AD9627-125EBZ AD9629-20EBZ AD9709-EBZ AD9709-EBZ AD9716-DPG2-EBZ AD9737A-EBZ AD9787-DPG2-EBZ AD9993-EBZ DAC8555EVM ADS5482EVM ADS8372EVM EVAL-AD5061EBZ EVAL-AD5062EBZ EVAL-AD5443-DBRDZ EVAL-AD5570SDZ EVAL-AD7450ASDZ EVAL-AD7677EDZ EVAL-AD7992EBZ EVAL-AD7994EBZ AD9119-MIX-EBZ AD9148-M5375-EBZ AD9204-80EBZ AD9233-125EBZ AD9265-105EBZ AD9265-80EBZ AD9608-125EBZ AD9629-80EBZ AD9648-125EBZ AD9649-20EBZ AD9650-80EBZ AD9765-EBZ AD9767-EBZ AD9778A-DPG2-EBZ ADS8322EVM LM96080EB/NOPB EVAL-AD5445SDZ