ANALOG DEVICES

Ultrafast SiGe Voltage Comparators

Data Sheet

ADCMP580/ADCMP581/ADCMP582

FEATURES

180 ps propagation delay
25 ps overdrive and slew rate dispersion
8 GHz equivalent input rise time bandwidth
100 ps minimum pulse width
37 ps typical output rise/fall
10 ps deterministic jitter (DJ)
200 fs random jitter (RJ)
−2 V to +3 V input range with +5 V/−5 V supplies
On-chip terminations at both input pins
Resistor-programmable hysteresis
Differential latch control
Power supply rejection > 70 dB

APPLICATIONS

Automatic test equipment (ATE)
High speed instrumentation
Pulse spectroscopy
Medical imaging and diagnostics
High speed line receivers
Threshold detection
Peak and zero-crossing detectors
High speed trigger circuitry
Clock and data signal restoration

FUNCTIONAL BLOCK DIAGRAM

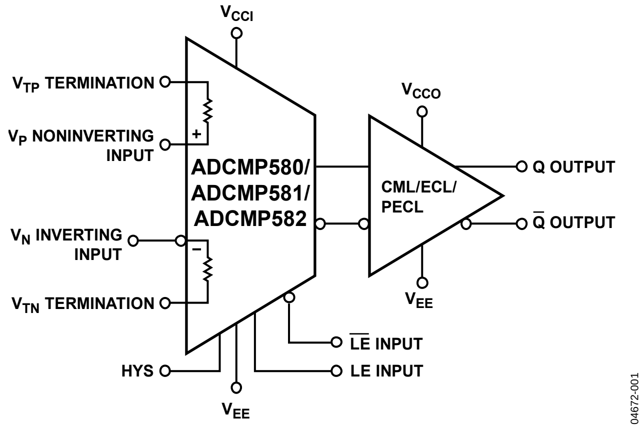

Figure 1.

GENERAL DESCRIPTION

The ADCMP580/ADCMP581/ADCMP582 are ultrafast voltage comparators fabricated on the Analog Devices, Inc. proprietary XFCB3 Silicon Germanium (SiGe) bipolar process. The ADCMP580 features CML output drivers, the ADCMP581 features reduced swing ECL (negative ECL) output drivers, and the ADCMP582 features reduced swing PECL (positive ECL) output drivers.

All three comparators offer 180 ps propagation delay and 100 ps minimum pulse width for 10 Gbps operation with 200 fs random jitter (RJ). Overdrive and slew rate dispersion are typically less than 15 ps.

The ±5 V power supplies enable a wide −2 V to +3 V input range with logic levels referenced to the CML/NECL/PECL outputs. The inputs have 50 Ω on-chip termination resistors with the optional capability to be left open (on an individual pin basis) for applications requiring high impedance input.

The CML output stage is designed to directly drive 400 mV into 50 Ω transmission lines terminated to ground. The NECL output stages are designed to directly drive 400 mV into 50 Ω terminated to −2 V. The PECL output stages are designed to directly drive 400 mV into 50 Ω terminated to V_{CCO} − 2 V. High speed latch and programmable hysteresis are also provided. The differential latch input controls are also 50 Ω terminated to an independent V_{TT} pin to interface to either CML or ECL or to PECL logic.

The ADCMP580/ADCMP581/ADCMP582 are available in a 16-lead LFCSP.

Rev. B Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

4/16—Rev. A to Rev. B

Deleted Figure 4; Renumbered Sequentially ... 7
Changes to Figure 3 and Table 4 ... 7
Changes to Figure 4 ... 8
Added Table 5; Renumbered Sequentially ... 8
Updated Outline Dimensions ... 14
Changes to Ordering Guide ... 14

8/07—Rev. 0 to Rev. A

Changes to Figure 1 ... 1
Changes to Table 4 ... 7
Changes to Figure 9 ... 8
Changes to Figure 21, Figure 22, and Figure 23 ... 10
Changes to Using/Disabling the Latch Feature ... 11
Changes to Comparator Hysteresis Section and Figure 29 ... 13
Changes to Ordering Guide ... 14

7/05—Revision 0: Initial Version

SPECIFICATIONS

V_{CCI} = 5.0 V; V_{EE} = −5.0 V; V_{CCO} = 3.3 V; T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DC INPUT CHARACTERISTICS						
Input Voltage Range	V_P, V_N		−2.0		+3.0	V
Input Differential Range			−2.0		+2.0	V
Input Offset Voltage	V_{OS}		−10.0	±4	+10.0	mV
Offset Voltage Temperature Coefficient	$\Delta V_{OS}/d_T$			10		µV/°C
Input Bias Current	I_P, I_N	Open termination		15	30.0	µA
Input Bias Current Temperature Coefficient	$\Delta I_B/d_T$			50		nA/°C
Input Offset Current				+2	±5.0	µA
Input Resistance				47 to 53		Ω
Input Resistance, Differential Mode		Open termination		50		kΩ
Input Resistance, Common Mode		Open termination		500		kΩ
Active Gain	A_V			48		dB
Common-Mode Rejection Ratio	CMRR	V_{CM} = −2.0 V to +3.0 V		60		dB
Hysteresis		R_{HYS} = ∞		1		mV
LATCH ENABLE CHARACTERISTICS						
Latch Enable Input Impedance	Z_{IN}	Each pin, V_{TT} at ac ground		47 to 53		Ω
Latch-to-Output Delay	t_{PLOH}, t_{PLOL}	V_{OD} = 200 mV		175		ps
Latch Minimum Pulse Width	t_{PL}	V_{OD} = 200 mV		100		ps
ADCMP580 (CML)						
Latch Enable Input Range			−0.8		0	V
Latch Enable Input Differential			0.2	0.4	0.5	V
Latch Setup Time	t_S	V_{OD} = 200 mV		95		ps
Latch Hold Time	t_H	V_{OD} = 200 mV		−90		ps
ADCMP581 (NECL)						
Latch Enable Input Range			−1.8		+0.8	V
Latch Enable Input Differential			0.2	0.4	0.5	V
Latch Setup Time	t_S	V_{OD} = 200 mV		70		ps
Latch Hold Time	t_H	V_{OD} = 200 mV		−65		ps
ADCMP582 (PECL)						
Latch Enable Input Range			V_{CCO} − 1.8		V_{CCO} − 0.8	V
Latch Enable Input Differential			0.2	0.4	0.5	V
Latch Setup Time	t_S	V_{OD} = 200 mV		30		ps
Latch Hold Time	t_H	V_{OD} = 200 mV		−25		ps
DC OUTPUT CHARACTERISTICS						
ADCMP580 (CML)						
Output Impedance	Z_{OUT}			50		Ω
Output Voltage High Level	V_{OH}	50 Ω to GND	−0.10	0	+0.03	V
Output Voltage Low Level	V_{OL}	50 Ω to GND	−0.50	−0.40	−0.35	V
Output Voltage Differential		50 Ω to GND	340	395	450	mV
ADCMP581 (NECL)						
Output Voltage High Level	V_{OH}	50 Ω to −2 V, T_A = 125°C	−0.99	−0.87	−0.75	V
Output Voltage High Level	V_{OH}	50 Ω to −2 V, T_A = 25°C	−1.06	−0.94	−0.82	V
Output Voltage High Level	V_{OH}	50 Ω to −2 V, T_A = −55°C	−1.11	−0.99	−0.87	V
Output Voltage Low Level	V_{OL}	50 Ω to −2 V, T_A = 125°C	−1.43	−1.26	−1.13	V
Output Voltage Low Level	V_{OL}	50 Ω to −2 V, T_A = 25°C	−1.50	−1.33	−1.20	V
Output Voltage Low Level	V_{OL}	50 Ω to −2 V, T_A = −55°C	−1.55	−1.38	−1.25	V
Output Voltage Differential		50 Ω to −2.0 V	340	395	450	mV

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
ADCMP582 (PECL)		V_{CCO} = 3.3 V				
Output Voltage High Level	V_{OH}	50 Ω to V_{CCO} − 2 V, T_A = 125°C	V_{CCO} − 0.99	V_{CCO} − 0.87	V_{CCO} − 0.75	V
Output Voltage High Level	V_{OH}	50 Ω to V_{CCO} − 2 V, T_A = 25°C	V_{CCO} − 1.06	V_{CCO} − 0.94	V_{CCO} − 0.82	V
Output Voltage High Level	V_{OH}	50 Ω to V_{CCO} − 2 V, T_A = −55°C	V_{CCO} − 1.11	V_{CCO} − 0.99	V_{CCO} − 0.87	V
Output Voltage Low Level	V_{OL}	50 Ω to V_{CCO} − 2 V, T_A = 125°C	V_{CCO} − 1.43	V_{CCO} − 1.26	V_{CCO} − 1.13	V
Output Voltage Low Level	V_{OL}	50 Ω to V_{CCO} − 2 V, T_A = 25°C	V_{CCO} − 1.50	V_{CCO} − 1.33	V_{CCO} − 1.20	V
Output Voltage Low Level	V_{OL}	50 Ω to V_{CCO} − 2 V, T_A = −55°C	V_{CCO} − 1.55	V_{CCO} − 1.35	V_{CCO} − 1.25	V
Output Voltage Differential		50 Ω to V_{CCO} − 2.0 V	340	395	450	mV
AC PERFORMANCE						
Propagation Delay	t_{PD}	V_{OD} = 500 mV		180		ps
Propagation Delay Temperature Coefficient	$\Delta t_{PD}/d_T$			0.25		ps/°C
Propagation Delay Skew—Rising Transition to Falling Transition		V_{OD} = 500 mV, 5 V/ns		10		ps
Overdrive Dispersion		50 mV < V_{OD} < 1.0 V		10		ps
		10 mV < V_{OD} < 200 mV		15		ps
Slew Rate Dispersion		2 V/ns to 10 V/ns		15		ps
Pulse Width Dispersion		100 ps to 5 ns		15		ps
Duty Cycle Dispersion 5% to 95%		1.0 V/ns, 15 MHz, V_{CM} = 0.0 V		10		ps
Common-Mode Dispersion		V_{OD} = 0.2 V, −2 V < V_{CM} < 3 V		5		ps/V
Equivalent Input Bandwidth[1]	BW_{EQ}	0.0 V to 400 mV input, t_R = t_F = 25 ps, 20/80		8		GHz
Toggle Rate		>50% output swing		12.5		Gbps
Deterministic Jitter	DJ	V_{OD} = 500 mV, 5 V/ns, $PRBS^{31}$ − 1 NRZ, 5 Gbps		15		ps
Deterministic Jitter	DJ	V_{OD} = 200 mV, 5 V/ns, $PRBS^{31}$ − 1 NRZ, 10 Gbps		25		ps
RMS Random Jitter	RJ	V_{OD} = 200 mV, 5 V/ns, 1.25 GHz		0.2		ps
Minimum Pulse Width	PW_{MIN}	Δt_{PD} < 5 ps		100		ps
Minimum Pulse Width	PW_{MIN}	Δt_{PD} < 10 ps		80		ps
Rise/Fall Time	t_R, t_F	20/80		37		ps
POWER SUPPLY						
Positive Supply Voltage	V_{CCI}		+4.5	+5.0	+5.5	V
Negative Supply Voltage	V_{EE}		−5.5	−5.0	−4.5	V
ADCMP580 (CML)						
Positive Supply Current	I_{VCCI}	V_{CCI} = 5.0 V, 50 Ω to GND		6	8	mA
Negative Supply Current	I_{VEE}	V_{EE} = −5.0 V, 50 Ω to GND	−50	−40	−34	mA
Power Dissipation	P_D	50 Ω to GND		230	260	mW
ADCMP581 (NECL)						
Positive Supply Current	I_{VCCI}	V_{CCI} = 5.0 V, 50 Ω to −2 V		6	8	mA
Negative Supply Current	I_{VEE}	V_{EE} = −5.0 V, 50 Ω to −2 V	−35	−25	−19	mA
Power Dissipation	P_D	50 Ω to −2 V		155	200	mW
ADCMP582 (PECL)						
Logic Supply Voltage	V_{CCO}		+2.5	+3.3	+5.0	V
Input Supply Current	I_{VCCI}	V_{CCI} = 5.0 V, 50 Ω to V_{CCO} − 2 V		6	8	mA
Output Supply Current	I_{VCCO}	V_{CCO} = 5.0 V, 50 Ω to V_{CCO} − 2 V		44	55	mA
Negative Supply Current	I_{VEE}	V_{EE} = −5.0 V, 50 Ω to V_{CCO} − 2 V	−35	−25	−19	mA
Power Dissipation	P_D	50 Ω to V_{CCO} − 2 V		310	350	mW
Power Supply Rejection (V_{CCI})	PSR_{VCCI}	V_{CCI} = 5.0 V + 5%		−75		dB
Power Supply Rejection (V_{EE})	PSR_{VEE}	V_{EE} = −5.0 V + 5%		−60		dB
Power Supply Rejection (V_{CCO})	PSR_{VCCO}	V_{CCO} = 3.3 V + 5% (ADCMP582)		−75		dB

[1] Equivalent input bandwidth assumes a simple first-order input response and is calculated with the following formula: $BW_{EQ} = 0.22/\sqrt{(tr_{COMP}^2 - tr_{IN}^2)}$, where tr_{IN} is the 20/80 transition time of a quasi-Gaussian input edge applied to the comparator input and tr_{COMP} is the effective transition time digitized by the comparator.

TIMING INFORMATION

Figure 2 shows the ADCMP580/ADCMP581/ADCMP582 compare and latch timing relationships. Table 2 provides the definitions of the terms shown in Figure 2.

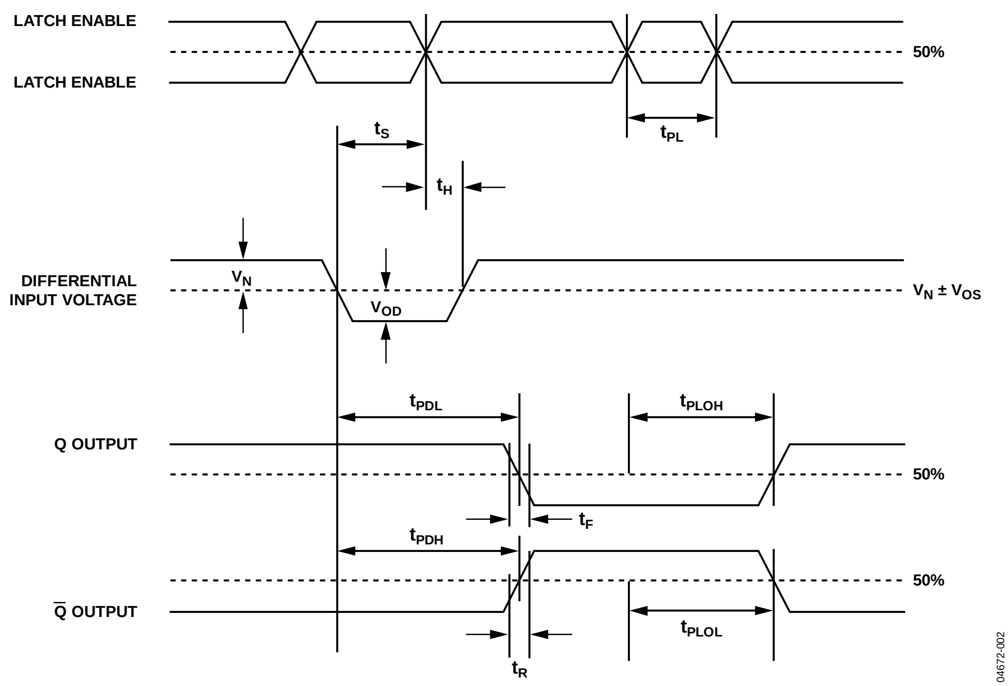


Figure 2. Comparator Timing Diagram

Table 2. Timing Descriptions

Symbol	Symbol Description	Timing Description
t_{PDH}	Input-to-Output High Delay	Propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output low-to-high transition.
t_{PDL}	Input-to-Output Low Delay	Propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output high-to-low transition.
t_{PLOH}	Latch Enable-to-Output High Delay	Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output low-to-high transition.
t_{PLOL}	Latch Enable-to-Output Low Delay	Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output high-to-low transition.
t_H	Minimum Hold Time	Minimum time after the negative transition of the latch enable signal that the input signal must remain unchanged to be acquired and held at the outputs.
t_{PL}	Minimum Latch Enable Pulse Width	Minimum time that the latch enable signal must be high to acquire an input signal change.
t_S	Minimum Setup Time	Minimum time before the negative transition of the latch enable signal that an input signal change must be present to be acquired and held at the outputs.
t_R	Output Rise Time	Amount of time required to transition from a low to a high output as measured at the 20% and 80% points.
t_F	Output Fall Time	Amount of time required to transition from a high to a low output as measured at the 20% and 80% points.
V_N	Normal Input Voltage	Difference between the input voltages V_P and V_N for output true.
V_{OD}	Voltage Overdrive	Difference between the input voltages V_P and V_N for output false.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
SUPPLY VOLTAGES	
Positive Supply Voltage (V_{CCI} to GND)	−0.5 V to +6.0 V
Negative Supply Voltage (V_{EE} to GND)	−6.0 V to +0.5 V
Logic Supply Voltage (V_{CCO} to GND)	−0.5 V to +6.0 V
INPUT VOLTAGES	
Input Voltage	−3.0 V to +4.0 V
Differential Input Voltage	−2 V to +2 V
Input Voltage, Latch Enable	−2.5 V to +5.5 V
HYSTERESIS CONTROL PIN	
Applied Voltage (HYS to V_{EE})	−5.5 V to +0.5 V
Maximum Input/Output Current	1 mA
OUTPUT CURRENT	
ADCMP580 (CML)	−25 mA
ADCMP581 (NECL)	−40 mA
ADCMP582 (PECL)	−40 mA
TEMPERATURE	
Operating Temperature Range, Ambient	−40°C to +125°C
Operating Temperature, Junction	125°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CONSIDERATIONS

The ADCMP580/ADCMP581/ADCMP582 16-lead LFCSP option has a junction-to-ambient thermal resistance (θ_{JA}) of 70°C/W in still air.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

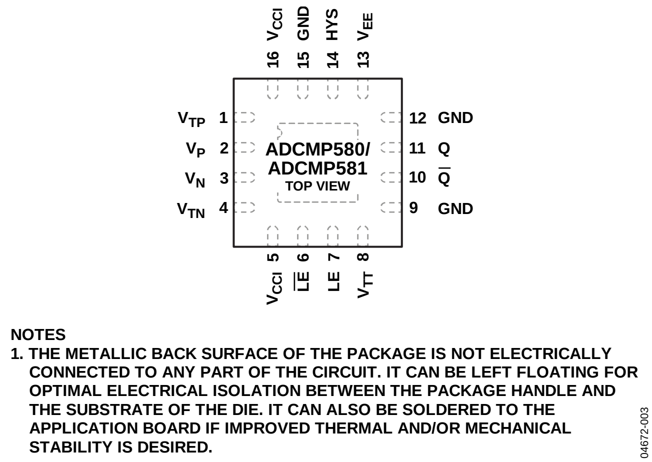
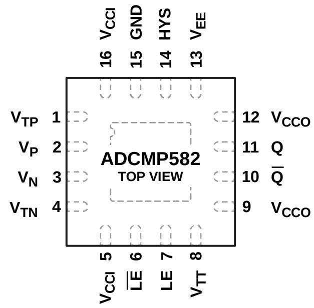


Figure 3. ADCMP580/ADCMP581 Pin Configuration

Table 4. ADCMP580/ADCMP581 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{TP}	Termination Resistor Return Pin for V_P Input.
2	V_P	Noninverting Analog Input.
3	V_N	Inverting Analog Input.
4	V_{TN}	Termination Resistor Return Pin for V_N Input.
5, 16	V_{CCI}	Positive Supply Voltage.
6	$\overline{LE}$	Latch Enable Input Pin, Inverting Side. In compare mode ($\overline{LE}$ = low), the output tracks changes at the input of the comparator. In latch mode ($\overline{LE}$ = high), the output reflects the input state just prior to the comparator being placed into latch mode. $\overline{LE}$ must be driven in complement with LE.
7	LE	Latch Enable Input Pin, Noninverting Side. In compare mode (LE = high), the output tracks changes at the input of the comparator. In latch mode (LE = low), the output reflects the input state just prior to the comparator being placed into latch mode. LE must be driven in complement with $\overline{LE}$.
8	V_{TT}	Termination Return Pin for the LE/$\overline{LE}$ Input Pins. For the ADCMP580 (CML output stage), this pin must be connected to ground. For the ADCMP581 (ECL output stage), connect this pin to the −2 V termination potential.
9, 12	GND	Digital Ground Pin/Positive Logic Power Supply Terminal. This pin must be connected to the GND pin.
10	$\overline{Q}$	Inverting Output. $\overline{Q}$ is logic low if the analog voltage at the noninverting input, V_P, is greater than the analog voltage at the inverting input, V_N, provided that the comparator is in compare mode. See the LE/$\overline{LE}$ descriptions (Pin 6 to Pin 7) for more information.
11	Q	Noninverting Output. Q is logic high if the analog voltage at the noninverting input, V_P, is greater than the analog voltage at the inverting input, V_N, provided that the comparator is in compare mode. See the LE/$\overline{LE}$ descriptions (Pin 6 to Pin 7) for more information.
13	V_{EE}	Negative Power Supply.
14	HYS	Hysteresis Control. Leave this pin disconnected for zero hysteresis. Connect this pin to the V_{EE} supply with a suitably sized resistor to add the desired amount of hysteresis. Refer to Figure 8 for proper sizing of the HYS hysteresis control resistor.
15	GND	Analog Ground.
	EPAD	Exposed Pad. The metallic back surface of the package is not electrically connected to any part of the circuit. It can be left floating for optimal electrical isolation between the package handle and the substrate of the die. It can also be soldered to the application board if improved thermal and/or mechanical stability is desired.



NOTES
1. THE METALLIC BACK SURFACE OF THE PACKAGE IS NOT ELECTRICALLY CONNECTED TO ANY PART OF THE CIRCUIT. IT CAN BE LEFT FLOATING FOR OPTIMAL ELECTRICAL ISOLATION BETWEEN THE PACKAGE HANDLE AND THE SUBSTRATE OF THE DIE. IT CAN ALSO BE SOLDERED TO THE APPLICATION BOARD IF IMPROVED THERMAL AND/OR MECHANICAL STABILITY IS DESIRED.

04672-004

Figure 4. ADCMP582 Pin Configuration

Table 5. ADCMP582 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{TP}	Termination Resistor Return Pin for V_P Input.
2	V_P	Noninverting Analog Input.
3	V_N	Inverting Analog Input.
4	V_{TN}	Termination Resistor Return Pin for V_N Input.
5, 16	V_{CCI}	Positive Supply Voltage.
6	$\overline{LE}$	Latch Enable Input Pin, Inverting Side. In compare mode ($\overline{LE}$ = low), the output tracks changes at the input of the comparator. In latch mode ($\overline{LE}$ = high), the output reflects the input state just prior to the comparator being placed into latch mode. $\overline{LE}$ must be driven in complement with LE.
7	LE	Latch Enable Input Pin, Noninverting Side. In compare mode (LE = high), the output tracks changes at the input of the comparator. In latch mode (LE = low), the output reflects the input state just prior to the comparator being placed into latch mode. LE must be driven in complement with $\overline{LE}$.
8	V_{TT}	Termination Return Pin for the LE/$\overline{LE}$ Input Pins. For the ADCMP582 (PECL output stage), connect this pin to the V_{CCO} −2 V termination potential.
9, 12	V_{CCO}	Digital Ground Pin/Positive Logic Power Supply Terminal. This pin must be connected to the positive logic power V_{CCO} supply.
10	$\overline{Q}$	Inverting Output. $\overline{Q}$ is logic low if the analog voltage at the noninverting input, V_P, is greater than the analog voltage at the inverting input, V_N, provided that the comparator is in compare mode. See the LE/$\overline{LE}$ descriptions (Pin 6 to Pin 7) for more information.
11	Q	Noninverting Output. Q is logic high if the analog voltage at the noninverting input, V_P, is greater than the analog voltage at the inverting input, V_N, provided that the comparator is in compare mode. See the LE/$\overline{LE}$ descriptions (Pin 6 to Pin 7) for more information.
13	V_{EE}	Negative Power Supply.
14	HYS	Hysteresis Control. Leave this pin disconnected for zero hysteresis. Connect this pin to the V_{EE} supply with a suitably sized resistor to add the desired amount of hysteresis. Refer to Figure 8 for proper sizing of the HYS hysteresis control resistor.
15	GND	Analog Ground.
	EPAD	Exposed Pad. The metallic back surface of the package is not electrically connected to any part of the circuit. It can be left floating for optimal electrical isolation between the package handle and the substrate of the die. It can also be soldered to the application board if improved thermal and/or mechanical stability is desired.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CCI} = 5.0 V, V_{EE} = −5.0 V, V_{CCO} = 3.3 V, T_A = 25°C, unless otherwise noted.

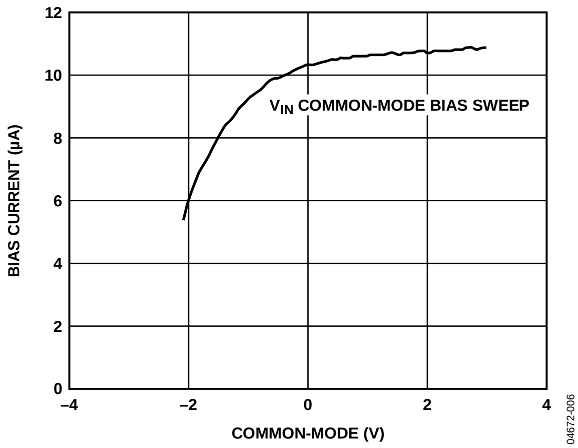


Figure 5. Bias Current vs. Common-Mode Voltage

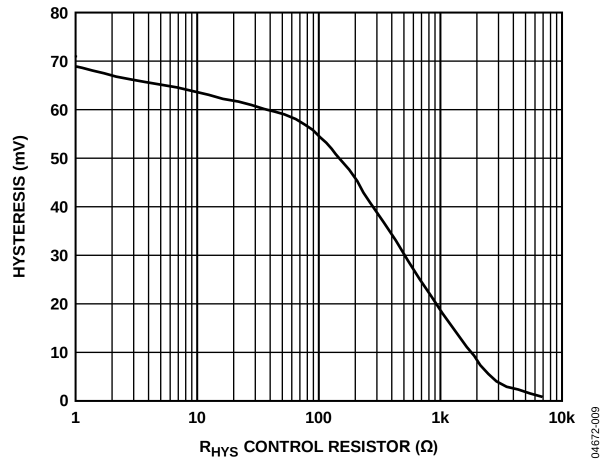


Figure 8. Hysteresis vs. R_{HYS} Control Resistor

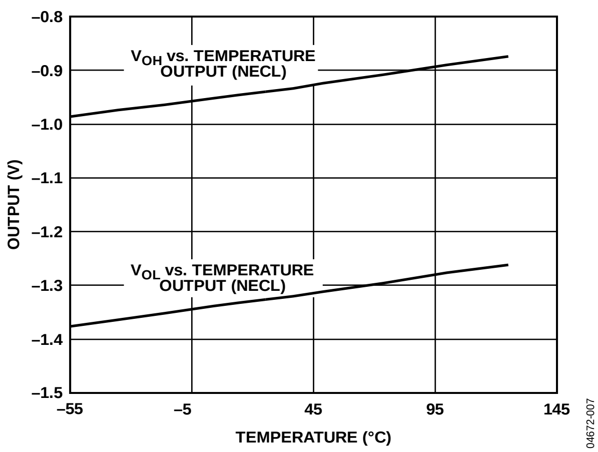


Figure 6. ADCMP581 Output Voltage vs. Temperature

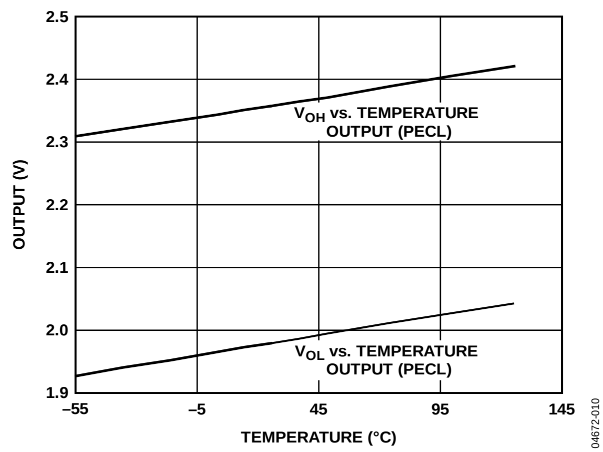


Figure 9. ADCMP582 Output Voltage vs. Temperature

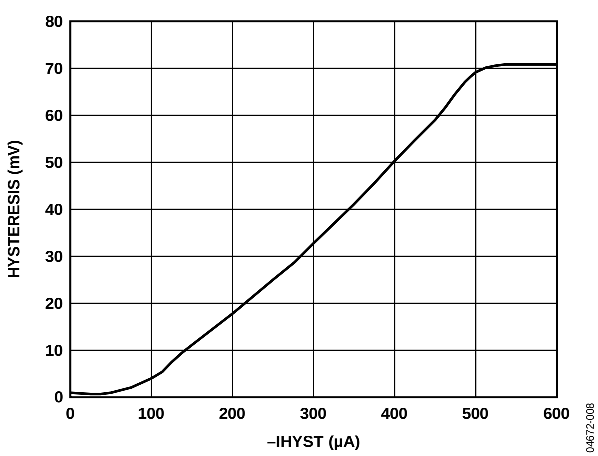


Figure 7. Hysteresis vs. –IHYST

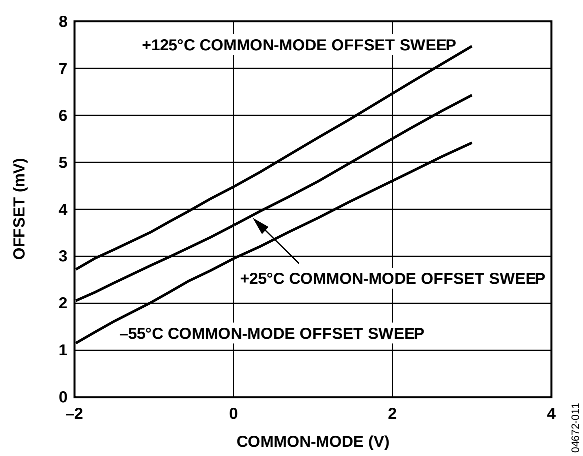


Figure 10. A Typical V_{OS} vs. Common-Mode Voltage

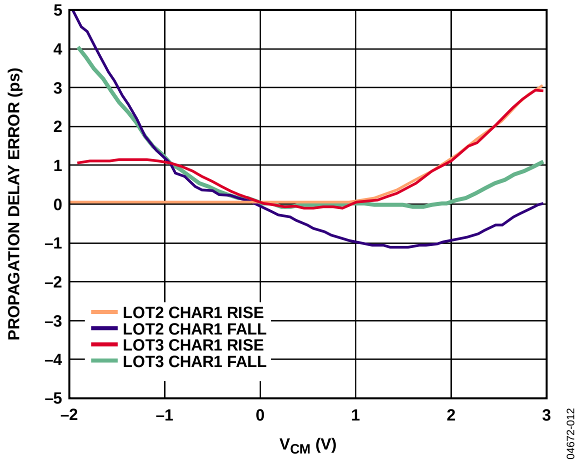


Figure 11. ADCMP580 Propagation Delay Error vs. Common-Mode Voltage

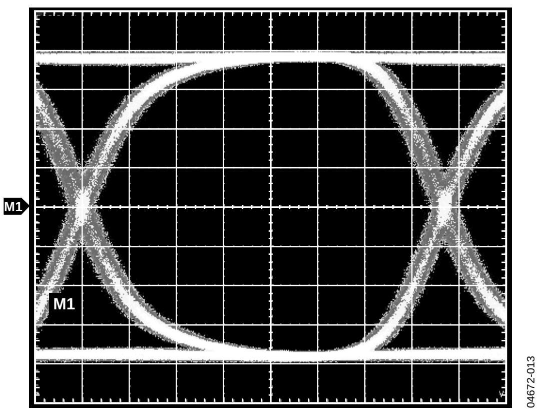


Figure 12. ADCMP580 Eye Diagram at 7.5 Gbps

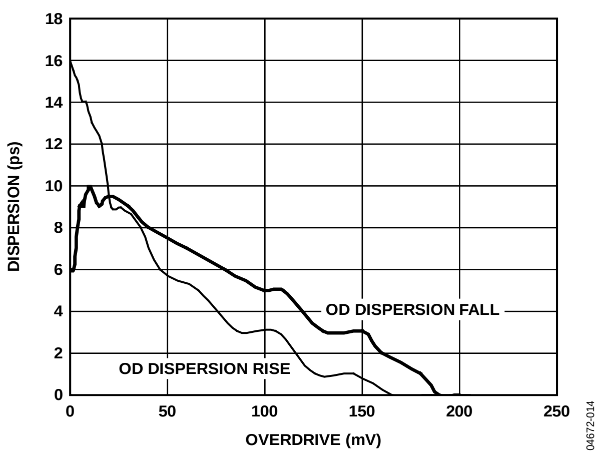


Figure 13. Dispersion vs. Overdrive

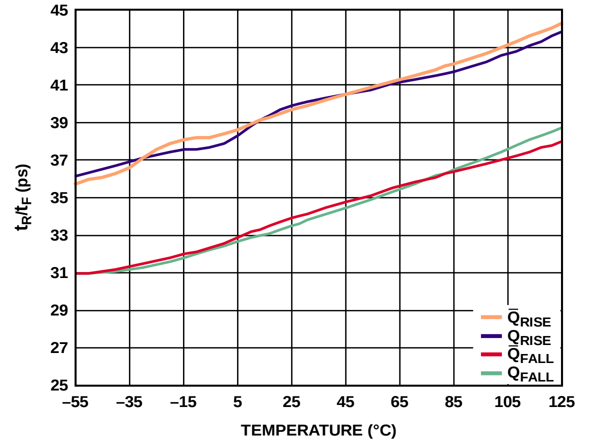


Figure 14. ADCMP581 t_R/t_F vs. Temperature

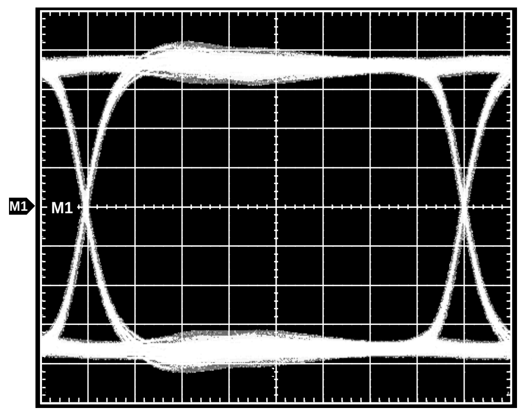


Figure 15. ADCMP582 Eye Diagram at 2.5 Gbps

TYPICAL APPLICATION CIRCUITS

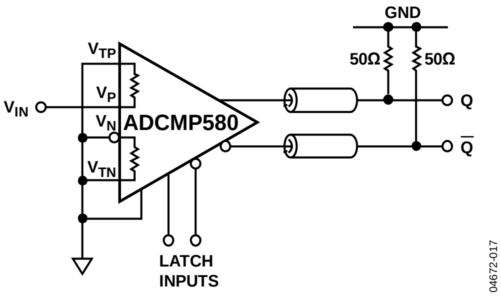


Figure 16. Zero-Crossing Detector with CML Outputs on the ADCMP580

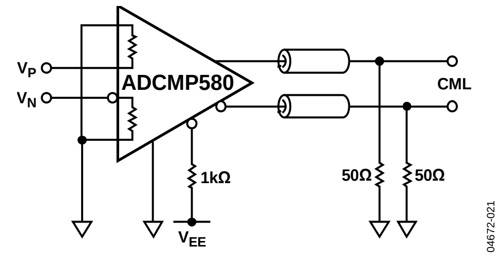


Figure 20. Disabling the Latch Feature on the ADCMP580

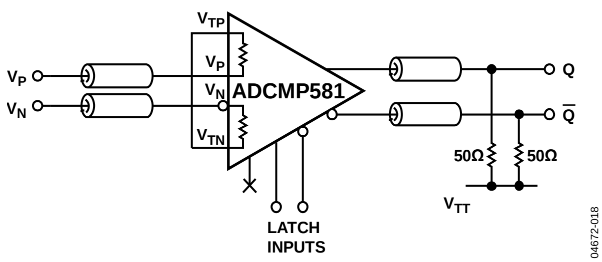


Figure 17. LVDS to a 50 Ω Back-Terminated (RS) ECL Receiver on the ADCMP581

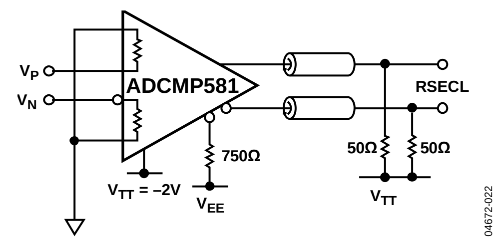


Figure 21. Disabling the Latch Feature on the ADCMP581

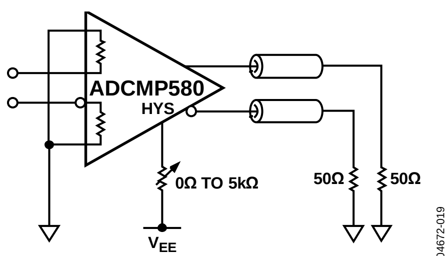


Figure 18. Adding Hysteresis Using the HYS Control on the ADCMP580

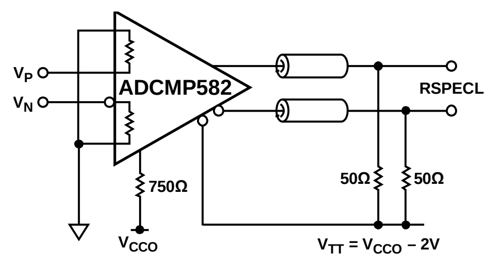


Figure 22. Disabling the Latch Feature on the ADCMP582

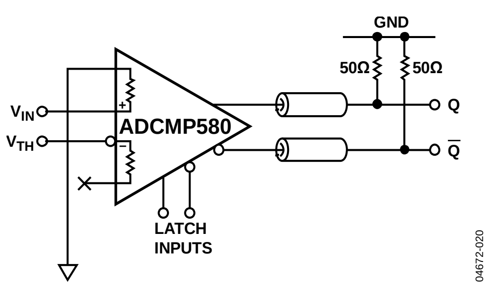


Figure 19. Comparator with −2 to +3 V Input Range on the ADCMP580

APPLICATIONS INFORMATION

POWER/GROUND LAYOUT AND BYPASSING

The ADCMP580/ADCMP581/ADCMP582 family of comparators is designed for very high speed applications. Consequently, high speed design techniques must be used to achieve the specified performance. It is critically important to use low impedance supply planes, particularly for the negative supply (V_{EE}), the output supply plane (V_{CCO}), and the ground plane (GND). Individual supply planes are recommended as part of a multilayer board. Providing the lowest inductance return path for the switching currents ensures the best possible performance in the target application.

It is also important to adequately bypass the input and output supplies. A 1 μF electrolytic bypass capacitor must be placed within several inches of each power supply pin to ground. In addition, multiple high quality 0.1 μF bypass capacitors must be placed as close as possible to each of the V_{EE}, V_{CCI}, and V_{CCO} supply pins and must be connected to the GND plane with redundant vias. High frequency bypass capacitors must be carefully selected for minimum inductance and ESR. Parasitic layout inductance must be strictly avoided to maximize the effectiveness of the bypass at high frequencies.

ADCMP580/ADCMP581/ADCMP582 FAMILY OF OUTPUT STAGES

Specified propagation delay dispersion performance is achieved by using proper transmission line terminations. The outputs of the ADCMP580 family comparators are designed to directly drive 400 mV into 50 Ω cable or microstrip/stripline transmission lines terminated with 50 Ω referenced to the proper return. The CML output stage for the ADCMP580 is shown in the simplified schematic diagram in Figure 23. Each output is back-terminated with 50 Ω for best transmission line matching. The outputs of the ADCMP581/ADCMP582 are illustrated in Figure 24; they must be terminated to −2 V for ECL outputs of ADCMP581 and V_{CCO} − 2 V for PECL outputs of ADCMP582. As an alternative, Thevenin equivalent termination networks can also be used. If these high speed signals must be routed more than a centimeter, either microstrip or stripline techniques are required to ensure proper transition times and to prevent excessive output ringing and pulse width-dependent propagation delay dispersion.

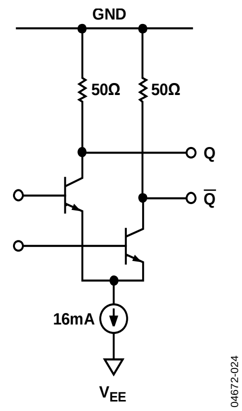


Figure 23. Simplified Schematic Diagram of the ADCMP580 CML Output Stage

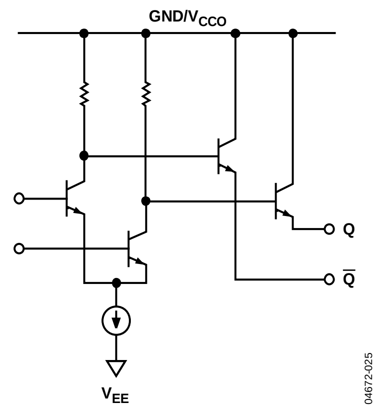


Figure 24. Simplified Schematic Diagram of the ADCMP581/ADCMP582 ECL/PECL Output Stage

USING/DISABLING THE LATCH FEATURE

The latch inputs (LE/$\overline{\text{LE}}$) are active low for latch mode and are internally terminated with 50 Ω resistors to the V_{TT} pin. When using the ADCMP580, V_{TT} must be connected to ground. When using the ADCMP581, V_{TT} must be connected to −2 V. When using the ADCMP582, V_{TT} must be connected externally to V_{CCO} − 2 V, preferably with its own low inductance plane.

When using the ADCMP580, the latch function can be disabled by connecting the $\overline{\text{LE}}$ pin to V_{EE} with an external pull-down resistor and by leaving the LE pin to ground. To prevent excessive power dissipation, the resistor must be 1 kΩ for the ADCMP580. When using the ADCMP581 comparators, the latch can be disabled by connecting the $\overline{\text{LE}}$ pin to V_{EE} with an external 750 Ω resistor and leaving the LE pin connected to −2 V. The idea is to create an approximate 0.5 V offset using the internal resistor as half of the voltage divider. Connect the V_{TT} pin as recommended.

OPTIMIZING HIGH SPEED PERFORMANCE

As with any high speed comparator, proper design and layout techniques are essential to obtaining the specified performance. Stray capacitance, inductance, inductive power, and ground impedances or other layout issues can severely limit performance and can cause oscillation. Discontinuities along input and output transmission lines can also severely limit the specified pulse width dispersion performance.

For applications in a 50 Ω environment, input and output matching have a significant impact on data-dependent (or deterministic) jitter (DJ) and pulse width dispersion performance. The ADCMP580/ADCMP581/ADCMP582 family of comparators provides internal 50 Ω termination resistors for both V_P and V_N inputs. The return side for each termination is pinned out separately with the V_{TP} and V_{TN} pins, respectively. If a 50 Ω termination is desired at one or both of the V_P/V_N inputs, the V_{TP} and V_{TN} pins can be connected (or disconnected) to (from) the desired termination potential as appropriate. The termination potential must be carefully bypassed using ceramic capacitors as discussed previously to prevent undesired aberrations on the input signal due to parasitic inductance in the termination return path. If a 50 Ω termination is not desired, either one or both of the V_{TP}/V_{TN} termination pins can be left disconnected. In this case, the open pins must be left floating with no external pull downs or bypassing capacitors.

For applications that require high speed operation but do not have on-chip 50 Ω termination resistors, some reflections must be expected, because the comparator inputs can no longer provide matched impedance to the input trace leading up to the device. It then becomes important to back-match the drive source impedance to the input transmission path leading to the input to minimize multiple reflections. For applications in which the comparator is less than 1 cm from the driving signal source, the source impedance must be minimized. High source impedance in combination with parasitic input capacitance of the comparator could cause undesirable degradation in bandwidth at the input, thus degrading the overall response. It is therefore recommended that the drive source impedance be no more than 50 Ω for best high speed performance.

COMPARATOR PROPAGATION DELAY DISPERSION

The ADCMP580/ADCMP581/ADCMP582 family of comparators has been specifically designed to reduce propagation delay dispersion over a wide input overdrive range of 5 mV to 500 mV. Propagation delay dispersion is a change in propagation delays that results from a change in the degree of overdrive or slew rate (how far or how fast the input signal exceeds the switching threshold). The overall result is a higher degree of timing accuracy.

Propagation delay dispersion is a specification that becomes important in critical timing applications, such as data communications, automatic test and measurement, instrumentation, and event-driven applications, such as pulse spectroscopy, nuclear instrumentation, and medical imaging. Dispersion is defined as the variation in the overall propagation delay as the input overdrive conditions are changed (see Figure 25 and Figure 26). For the ADCMP580/ADCMP581/ADCMP582 family of comparators, dispersion is typically <25 ps, because the overdrive varies from 5 mV to 500 mV, and the input slew rate varies from 1 V/ns to 10 V/ns. This specification applies for both positive and negative signals because the ADCMP580/ADCMP581/ADCMP582 family of comparators has almost equal delays for positive- and negative-going inputs.

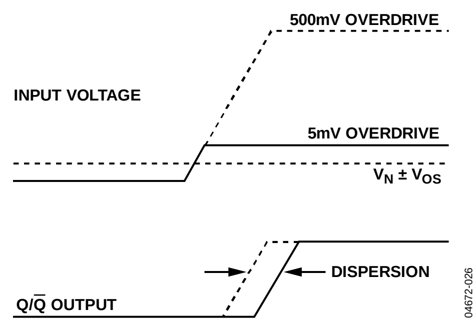


Figure 25. Propagation Delay—Overdrive Dispersion

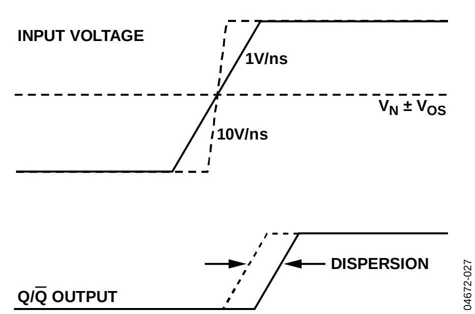


Figure 26. Propagation Delay—Slew Rate Dispersion

COMPARATOR HYSTERESIS

Adding hysteresis to a comparator is often desirable in a noisy environment or when the differential inputs are very small or slow moving. The transfer function for a comparator with hysteresis is shown in Figure 27. If the input voltage approaches the threshold from the negative direction, the comparator switches from a low to a high when the input crosses $+V_H/2$. The new switching threshold becomes $-V_H/2$. The comparator remains in the high state until the threshold $-V_H/2$ is crossed from the positive direction. In this manner, noise centered on 0 V input does not cause the comparator to switch states unless it exceeds the region bounded by $\pm V_H/2$.

The customary technique for introducing hysteresis into a comparator uses positive feedback from the output back to the input. A limitation of this approach is that the amount of hysteresis varies with the output logic levels, resulting in hysteresis that is not symmetric about the threshold. The external feedback network can also introduce significant parasitics that reduce high speed performance and can even reduce overall stability in some cases.

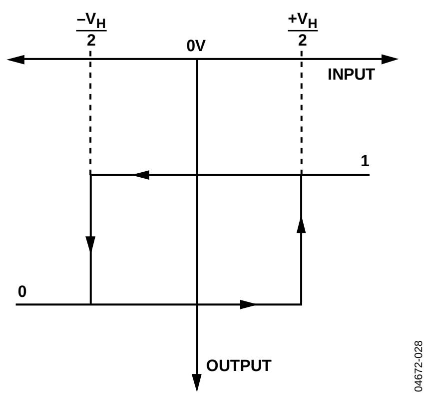


Figure 27. Comparator Hysteresis Transfer Function

The ADCMP580/ADCMP581/ADCMP582 family of comparators offers a programmable hysteresis feature that can significantly improve the accuracy and stability of the desired hysteresis. By connecting an external pull-down resistor from the HYS pin to V_{EE}, a variable amount of hysteresis can be applied. Leaving the HYS pin disconnected disables the feature, and hysteresis is then less than 1 mV, as specified. The maximum range of hysteresis that can be applied by using this method is approximately ±70 mV.

Figure 28 illustrates the amount of applied hysteresis as a function of the external resistor value. The advantage of applying hysteresis in this manner is improved accuracy, stability, and reduced component count. An external bypass capacitor is not required on the HYS pin, and it would likely degrade the jitter performance of the device.

The hysteresis pin can also be driven by a current source. It is biased approximately 400 mV above V_{EE} and has an internal series resistance of approximately 600 Ω.

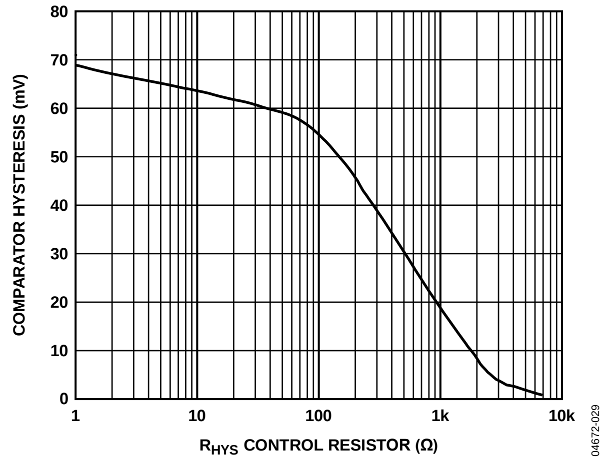


Figure 28. Comparator Hysteresis vs. R_{HYS} Control Resistor

MINIMUM INPUT SLEW RATE REQUIREMENT

As with many high speed comparators, a minimum slew rate requirement must be met to ensure that the device does not oscillate as the input signal crosses the threshold. This oscillation is due in part to the high input bandwidth of the comparator and the feedback parasitics inherent in the package. A minimum slew rate of 50 V/µs must ensure clean output transitions from the ADCMP580/ADCMP581/ADCMP582 family of comparators.

The slew rate may be too slow for other reasons. The extremely high bandwidth of these devices means that broadband noise can be a significant factor when input slew rates are low. There is 120 µV of thermal noise generated over the bandwidth of the comparator by the two 50 Ω terminations at room temperature. With a slew rate of only 50 V/µs, the inputs are inside this noise band for over 2 ps, rendering the comparator's jitter performance of 200 fs irrelevant. Raising the slew rate of the input signal and/or reducing the bandwidth over which that resistance is seen at the input can greatly reduce jitter. Devices are not characterized this way but simply bypassing a reference input close to the package can reduce jitter 30% in low slew rate applications.

OUTLINE DIMENSIONS

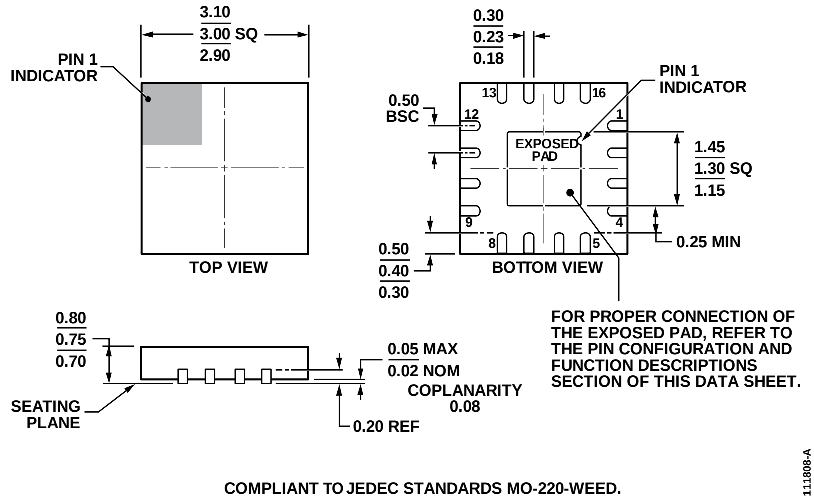


Figure 29. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-21)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADCMP580BCPZ-WP	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-21	G12
ADCMP580BCPZ-R2	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-21	G12
ADCMP580BCPZ-RL7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-21	G12
ADCMP581BCPZ-WP	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-21	G11
ADCMP581BCPZ-R2	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-21	G11
ADCMP581BCPZ-RL7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-21	G11
ADCMP582BCPZ-WP	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-21	G10
ADCMP582BCPZ-R2	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-21	G10
ADCMP582BCPZ-RL7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-21	G10
EVAL-ADCMP580BCPZ		Evaluation Board		
EVAL-ADCMP581BCPZ		Evaluation Board		
EVAL-ADCMP582BCPZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

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