ANALOG DEVICES

2.5 Ω, 1.8 V to 5.5 V, ±2.5 V Triple/Quad SPDT Switches in Chip Scale Packages

ADG786/ADG788

FEATURES
1.8 V to 5.5 V Single Supply
±2.5 V Dual Supply
2.5 Ω On Resistance
0.5 Ω On Resistance Flatness
100 pA Leakage Currents
19 ns Switching Times
Triple SPDT: ADG786
Quad SPDT: ADG788
20-Lead 4 mm × 4 mm Chip Scale Packages
Low Power Consumption
TTL/CMOS-Compatible Inputs
For Functionally-Equivalent Devices in 16-Lead TSSOP
  Packages, See ADG733/ADG734
Qualified for automotive applications

APPLICATIONS
Data Acquisition Systems
Communication Systems
Relay Replacement
Audio and Video Switching
Battery-Powered Systems

FUNCTIONAL BLOCK DIAGRAMS

SWITCHES SHOWN FOR A LOGIC "1" INPUT
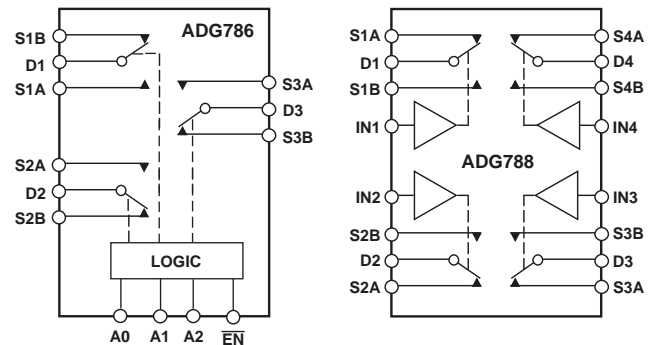
GENERAL DESCRIPTION
The ADG786 and ADG788 are low voltage, CMOS devices comprising three independently selectable SPDT (single pole, double throw) switches and four independently selectable SPDT switches respectively.

Low power consumption and operating supply range of 1.8 V to 5.5 V and dual ±2.5 V make the ADG786 and ADG788 ideal for battery powered, portable instruments and many other applications. All channels exhibit break-before-make switching action preventing momentary shorting when switching channels. An $\overline{EN}$ input on the ADG786 is used to enable or disable the device. When disabled, all channels are switched OFF.

These multiplexers are designed on an enhanced submicron process that provides low power dissipation yet gives high switching speed, very low on resistance, high signal bandwidths and low leakage currents. On resistance is in the region of a few ohms, is closely matched between switches and very flat over the full signal range. These parts can operate equally well in either direction and have an input signal range which extends to the supplies.

The ADG786 and ADG788 are available in small 20-lead chip scale packages.

PRODUCT HIGHLIGHTS
1. Small 20-Lead 4 mm × 4 mm Chip Scale Packages (CSP).

2. Single/Dual Supply Operation. The ADG786 and ADG788 are fully specified and guaranteed with 3 V ± 10% and 5 V ± 10% single supply rails, and ±2.5 V ± 10% dual supply rails.

3. Low On Resistance (2.5 Ω typical).

4. Low Power Consumption (<0.01 μW).

5. Guaranteed Break-Before-Make Switching Action.

ADG786/ADG788–SPECIFICATIONS[1]

ADG786/ADG788–SPECIFICATIONS[1] (V_{DD} = 5 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.)

Parameter	B Version +25°C	B Version −40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	2.5		Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA;
	4.5	5.0	Ω max	Test Circuit 1
On-Resistance Match between		0.1	Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA
Channels (ΔR_{ON})		0.4	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.5		Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA
		1.2	Ω max	
LEAKAGE CURRENTS				V_{DD} = 5.5 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V;
	±0.1	±0.3	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	V_D = V_S = 1 V, or 4.5 V;
	±0.1	±0.5	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	µA max	
C_{IN}, Digital Input Capacitance	4		pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	19		ns typ	R_L = 300 Ω, C_L = 35 pF;
		34	ns max	V_{S1A} = 3 V, V_{S1B} = 0 V, Test Circuit 4
t_{OFF}	7		ns typ	R_L = 300 Ω, C_L = 35 pF;
		12	ns max	V_S = 3 V, Test Circuit 4
ADG786 $t_{ON}(\overline{EN})$	20		ns typ	R_L = 300 Ω, C_L = 35 pF;
		40	ns max	V_S = 3 V, Test Circuit 5
$t_{OFF}(\overline{EN})$	7		ns typ	R_L = 300 Ω, C_L = 35 pF;
		12	ns max	V_S = 3 V, Test Circuit 5
Break-Before-Make Time Delay, t_D	13		ns typ	R_L = 300 Ω, C_L = 35 pF;
		1	ns min	V_S = 3 V, Test Circuit 6
Charge Injection	±3		pC typ	V_S = 2 V, R_S = 0 Ω, C_L = 1 nF;
				Test Circuit 7
Off Isolation	−80		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz;
				Test Circuit 8
Channel-to-Channel Crosstalk	−80		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz;
				Test Circuit 9
−3 dB Bandwidth	160		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 10
C_S (OFF)	11		pF typ	f = 1 MHz
C_D, C_S (ON)	34		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = 5.5 V
I_{DD}	0.001		µA typ	Digital Inputs = 0 V or 5.5 V
		1.0	µA max	

NOTES
[1]Temperature range is as follows: B Version: −40°C to +85°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

SPECIFICATIONS[1] (V_{DD} = 3 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.)

Parameter	B Version +25°C	B Version −40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	6		Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA;
	11	12	Ω max	Test Circuit 1
On-Resistance Match between		0.1	Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA
Channels (ΔR_{ON})		0.5	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)		3	Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA
LEAKAGE CURRENTS				V_{DD} = 3.3 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V;
	±0.1	±0.3	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	V_S = V_D = 1 V or 3 V;
	±0.1	±0.5	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	µA max	
C_{IN}, Digital Input Capacitance	4		pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	28		ns typ	R_L = 300 Ω, C_L = 35 pF;
		55	ns max	V_{S1A} = 2 V, V_{S1B} = 0 V, Test Circuit 4
t_{OFF}	9		ns typ	R_L = 300 Ω, C_L = 35 pF;
		16	ns max	V_S = 2 V, Test Circuit 4
ADG786 $t_{ON}(\overline{EN})$	29		ns typ	R_L = 300 Ω, C_L = 35 pF;
		60	ns max	V_S = 2 V, Test Circuit 5
$t_{OFF}(\overline{EN})$	9		ns typ	R_L = 300 Ω, C_L = 35 pF;
		16	ns max	V_S = 2 V, Test Circuit 5
Break-Before-Make Time Delay, t_D	22		ns typ	R_L = 300 Ω, C_L = 35 pF;
		1	ns min	V_S = 2 V, Test Circuit 6
Charge Injection	±3		pC typ	V_S = 1 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 7
Off Isolation	−80		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
Channel-to-Channel Crosstalk	−80		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 9
−3 dB Bandwidth	160		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 10
C_S (OFF)	11		pF typ	f = 1 MHz
C_D, C_S (ON)	34		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = 3.3 V
I_{DD}	0.001		µA typ	Digital Inputs = 0 V or 3.3 V
		1.0	µA max	

NOTES
[1]Temperature ranges are as follows: B Version: −40°C to +85°C.
[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG786/ADG788–SPECIFICATIONS[1]

DUAL SUPPLY (V_{DD} = +2.5 V ± 10%, V_{SS} = −2.5 V ± 10%, GND = 0 V, unless otherwise noted.)

Parameter	B Version +25°C	−40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
On Resistance (R_{ON})	2.5		Ω typ	$V_S = V_{SS}$ to V_{DD}, I_{DS} = 10 mA;
	4.5	5.0	Ω max	Test Circuit 1
On-Resistance Match between		0.1	Ω typ	$V_S = V_{SS}$ to V_{DD}, I_{DS} = 10 mA
Channels (ΔR_{ON})		0.4	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.5		Ω typ	$V_S = V_{SS}$ to V_{DD}, I_{DS} = 10 mA
		1.2	Ω max	
LEAKAGE CURRENTS				V_{DD} = +2.75 V, V_{SS} = −2.75 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_S = +2.25 V/−1.25 V, V_D = −1.25 V/+2.25 V;
	±0.1	±0.3	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	$V_S = V_D$ = +2.25 V/−1.25 V, Test Circuit 3
	±0.1	±0.5	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		1.7	V min	
Input Low Voltage, V_{INL}		0.7	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	$V_{IN} = V_{INL}$ or V_{INH}
		±0.1	µA max	
C_{IN}, Digital Input Capacitance	4		pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	21		ns typ	R_L = 300 Ω, C_L = 35 pF;
		35	ns max	V_{S1A} = 1.5 V, V_{S1B} = 0 V, Test Circuit 4
t_{OFF}	10		ns typ	R_L = 300 Ω, C_L = 35 pF;
		16	ns max	V_S = 1.5 V, Test Circuit 4
ADG786 $t_{ON}(\overline{EN})$	21		ns typ	R_L = 300 Ω, C_L = 35 pF;
		40	ns max	V_S = 1.5 V, Test Circuit 5
$t_{OFF}(\overline{EN})$	10		ns typ	R_L = 300 Ω, C_L = 35 pF;
		16	ns max	V_S = 1.5 V, Test Circuit 5
Break-Before-Make Time Delay, t_D	13		ns typ	R_L = 300 Ω, C_L = 35 pF;
		1	ns min	V_S = 1.5 V, Test Circuit 6
Charge Injection	±5		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 7
Off Isolation	−80		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
Channel-to-Channel Crosstalk	−80		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 9
−3 dB Bandwidth	160		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 10
C_S (OFF)	11		pF typ	f = 1 MHz
C_D, C_S (ON)	34		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = +2.75 V
I_{DD}	0.001		µA typ	Digital Inputs = 0 V or 2.75 V
		1.0	µA max	
I_{SS}	0.001		µA typ	V_{SS} = −2.75 V
		1.0	µA max	Digital Inputs = 0 V or 2.75 V

NOTES
[1]Temperature range is as follows: B Version: −40°C to +85°C.
[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

REV. C

ABSOLUTE MAXIMUM RATINGS[1]

($T_A = 25°C$ unless otherwise noted)

V_{DD} to V_{SS} . . . . 7 V
V_{DD} to GND . . . . –0.3 V to +7 V
V_{SS} to GND . . . . +0.3 V to –3.5 V
Analog Inputs[2] . . . . V_{SS} – 0.3 V to V_{DD} + 0.3 V or
30 mA, Whichever Occurs First
Digital Inputs[2] . . . . –0.3 V to V_{DD} + 0.3 V or
30 mA, Whichever Occurs First
Peak Current, S or D . . . . 100 mA
(Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, S or D . . . . 30 mA
Operating Temperature Range
Industrial (A, B Versions) . . . . –40°C to +85°C

Storage Temperature Range . . . . –65°C to +150°C
Junction Temperature . . . . 150°C
20 Lead CSP, θ_{JA} Thermal Impedance . . . . 32°C/W
Lead Temperature, Soldering (10 sec) . . . . 300°C
IR Reflow, Peak Temperature . . . . 220°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause perma-
nent damage to the device. This is a stress rating only; functional operation of the
device at these or any other conditions above those listed in the operational
sections of this specification is not implied. Exposure to absolute maximum rating
conditions for extended periods may affect device reliability. Only one absolute
maximum rating may be applied at any one time.
[2]Overvoltages at A, EN, IN, S, or D will be clamped by internal diodes. Current
should be limited to the maximum ratings given.

CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily
accumulate on the human body and test equipment and can discharge without detection. Although
the ADG786/ADG788 features proprietary ESD protection circuitry, permanent damage may
occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions
are recommended to avoid performance degradation or loss of functionality.

WARNING!

ESD SENSITIVE DEVICE

PIN CONFIGURATIONS
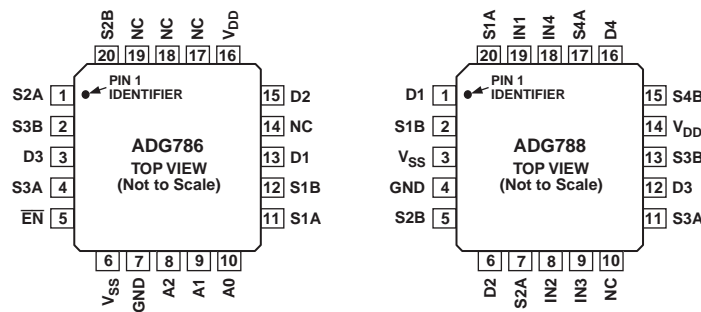
NC = NO CONNECT
EXPOSED PAD TIED TO SUBSTRATE, V_{SS}

ADG786/ADG788

Table I. ADG786 Truth Table

A2	A1	A0	$\overline{EN}$	ON Switch
X	X	X	1	None
0	0	0	0	D1-S1A, D2-S2A, D3-S3A
0	0	1	0	D1-S1B, D2-S2A, D3-S3A
0	1	0	0	D1-S1A, D2-S2B, D3-S3A
0	1	1	0	D1-S1B, D2-S2B, D3-S3A
1	0	0	0	D1-S1A, D2-S2A, D3-S3B
1	0	1	0	D1-S1B, D2-S2A, D3-S3B
1	1	0	0	D1-S1A, D2-S2B, D3-S3B
1	1	1	0	D1-S1B, D2-S2B, D3-S3B

Table II. ADG788 Truth Table

Logic	Switch A	Switch B
0	OFF	ON
1	ON	OFF

TERMINOLOGY

V_{DD}	Most Positive Power Supply Potential
V_{SS}	Most Negative Power Supply in a Dual Supply Application. In single supply applications, this should be tied to ground close to the device.
I_{DD}	Positive Supply Current
I_{SS}	Negative Supply Current
GND	Ground (0 V) Reference
S	Source Terminal. May be an input or output
D	Drain Terminal. May be an input or output
IN	Logic Control Input
V_D (V_S)	Analog Voltage on Terminals D, S
R_{ON}	Ohmic Resistance between D and S
ΔR_{ON}	On Resistance Match between Any Two Channels, i.e., R_{ON}max – R_{ON}min.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
I_S (OFF)	Source Leakage Current with the Switch "OFF"
I_D, I_S (ON)	Channel Leakage Current with the Switch "ON"
V_{INL}	Maximum Input Voltage for Logic "0"
V_{INH}	Minimum Input Voltage for Logic "1"
$I_{INL}(I_{INH})$	Input Current of the Digital Input
C_S (OFF)	"OFF" Switch Source Capacitance. Measured with reference to ground.
C_D, C_S(ON)	"ON" Switch Capacitance. Measured with reference to ground.
C_{IN}	Digital Input Capacitance
t_{ON}	Delay time measured between the 50% and 90% points of the digital inputs and the switch "ON" condition.
t_{OFF}	Delay time measured between the 50% and 90% points of the digital input and the switch "OFF" condition.
$t_{ON}(\overline{EN})$	Delay time between the 50% and 90% points of the $\overline{EN}$ digital input and the switch "ON" condition.
$t_{OFF}(\overline{EN})$	Delay time between the 50% and 90% points of the $\overline{EN}$ digital input and the switch "OFF" condition.
t_{OPEN}	"OFF" time measured between the 80% points of both switches when switching from one address state to another.
Charge	A measure of the glitch impulse transferred Injection from the digital input to the analog output during switching.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
On Response	The Frequency Response of the "ON" Switch
Insertion Loss	The Loss Due to the ON Resistance of the Switch.
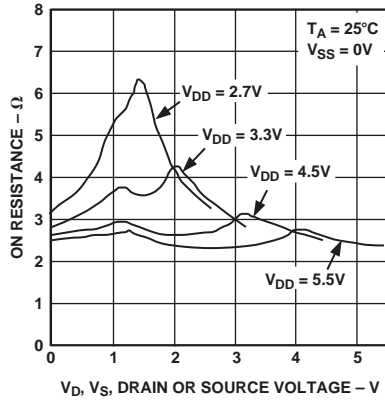
TPC 1. On Resistance as a Function of $V_D(V_S)$ for Single Supply
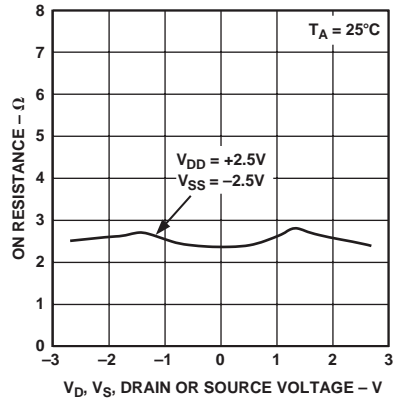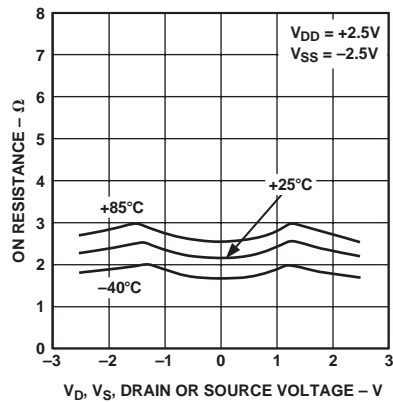
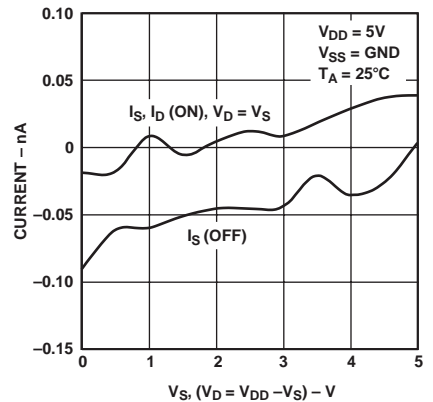TPC 2. On Resistance as a Function of $V_D(V_S)$ for Dual Supply
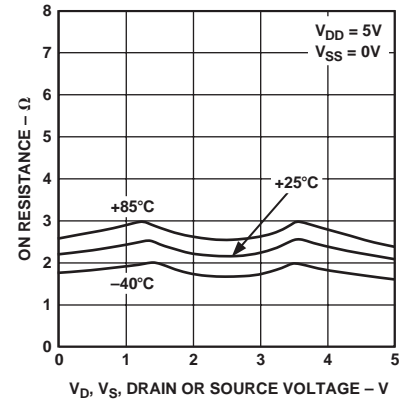
TPC 3. On Resistance as a Function of $V_D(V_S)$ for Different Temperatures, Single Supply
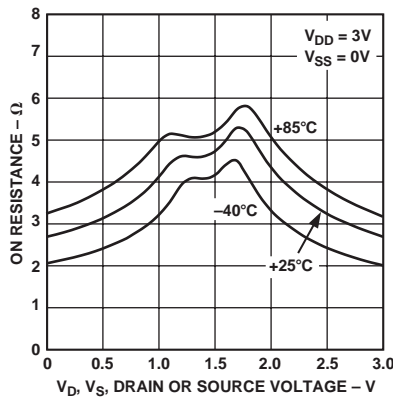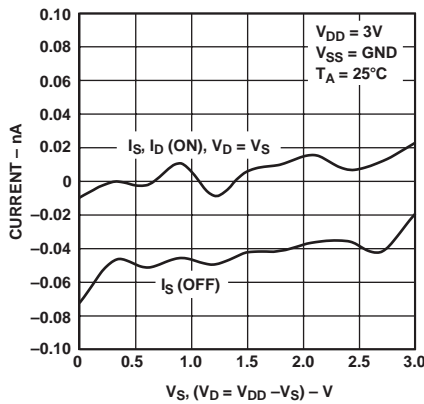
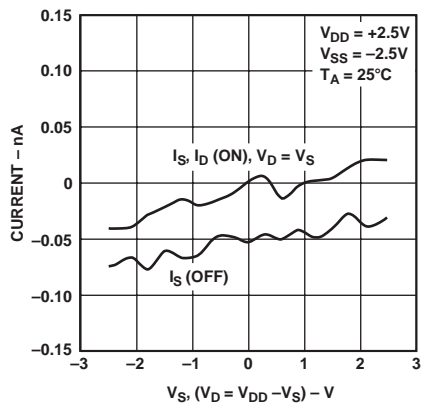TPC 4. On Resistance as a Function of $V_D(V_S)$ for Different Temperatures, Single Supply

TPC 5. On Resistance as a Function of $V_D(V_S)$ for Different Temperatures, Dual Supply
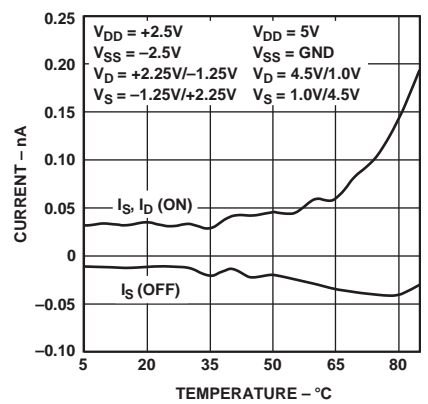
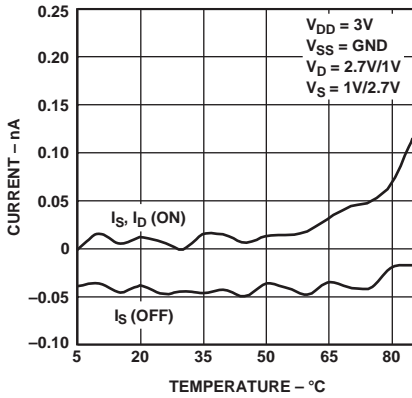TPC 6. Leakage Currents as a Function of $V_D(V_S)$

TPC 7. Leakage Currents as a Function of $V_D(V_S)$

TPC 8. Leakage Currents as a Function of $V_D(V_S)$

TPC 9. Leakage Currents as a Function of Temperature

ADG786/ADG788

TPC 10. Leakage Currents as a Function of Temperature
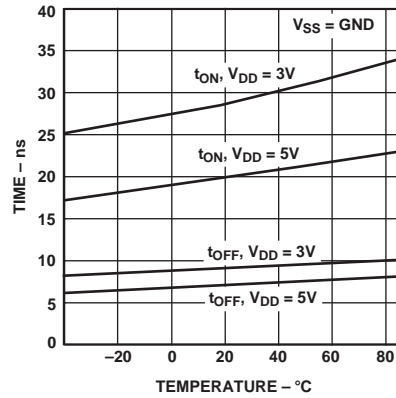
TPC 11. t_{ON}/t_{OFF} Times vs. Temperature
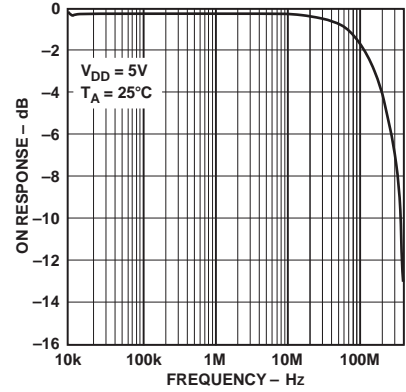
TPC 12. On Response vs. Frequency
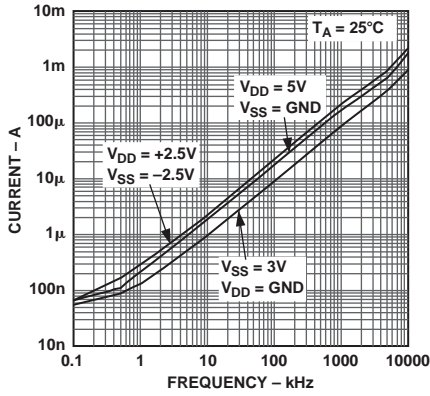
TPC 13. Input Current, I_{DD} vs. Switching Frequency
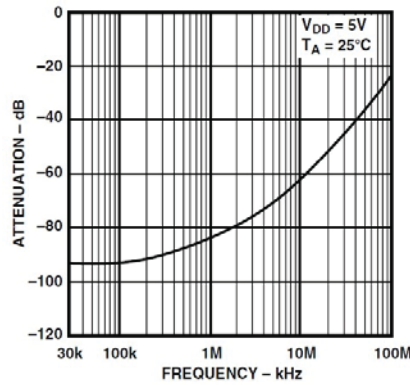
TPC 14. Off Isolation vs. Frequency
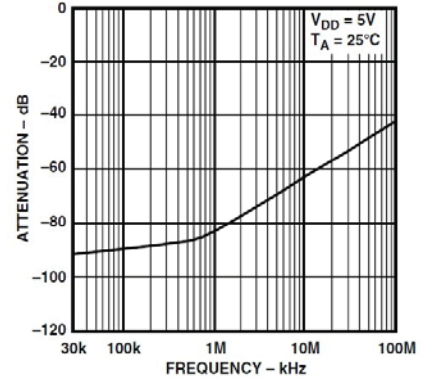
TPC 15. Crosstalk vs. Frequency
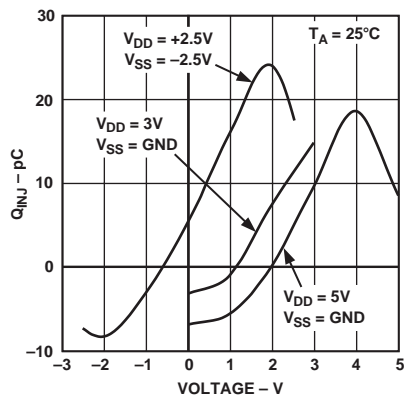
TPC 16. Charge Injection vs. Source Voltage

Test Circuits
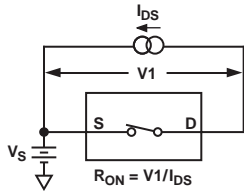
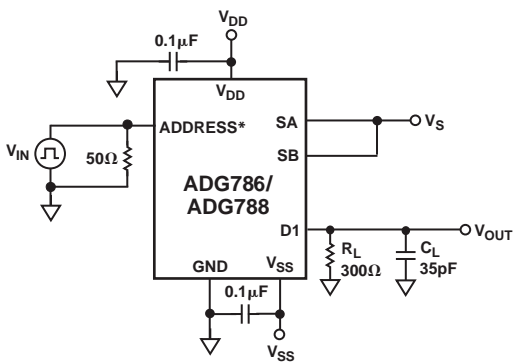Test Circuit 1. On Resistance
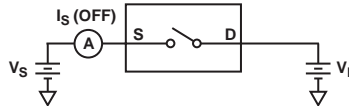
Test Circuit 2. I_S (OFF)
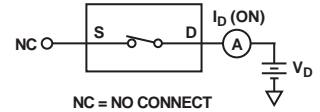
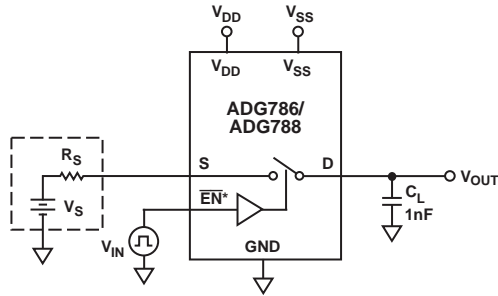Test Circuit 3. I_D (ON)
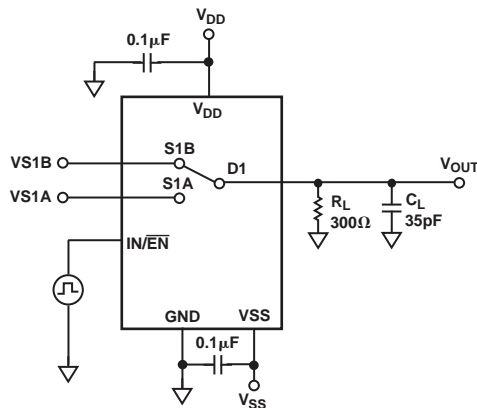
Test Circuit 4. Switching Times, t_{ON}, t_{OFF}
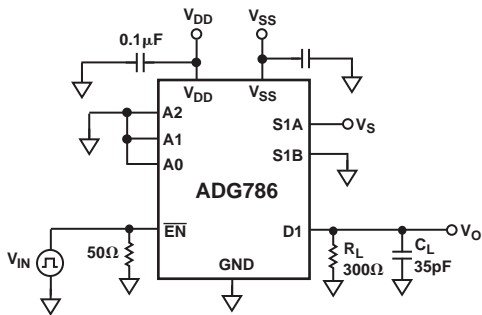
Test Circuit 5. Enable Delay, t_{ON} ($\overline{EN}$), t_{OFF} ($\overline{EN}$)
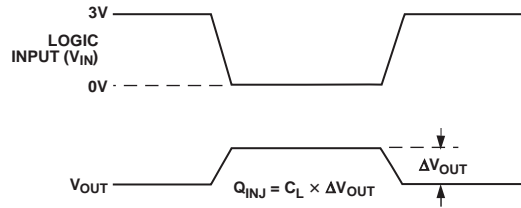

*A0, A1, A2 for ADG786, IN1-4 for ADG788
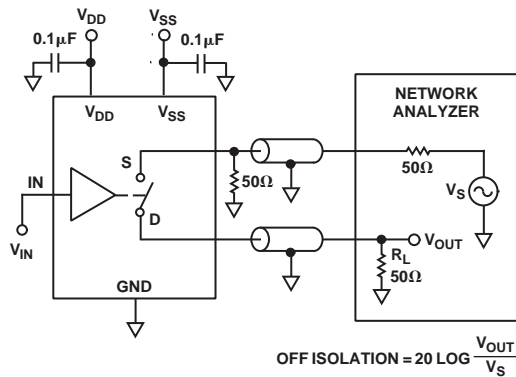
Test Circuit 6. Break-Before-Make Delay, t_{OPEN}
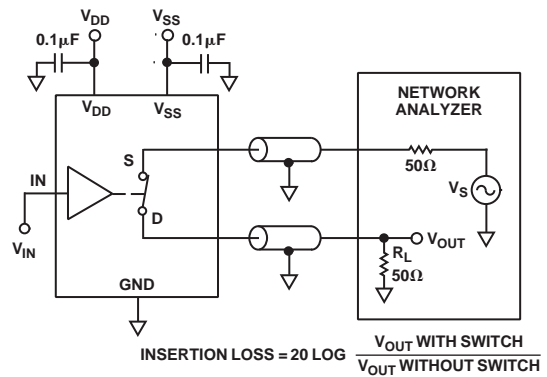
ADG786/ADG788

* IN1–4 for ADG734

Test Circuit 7. Charge Injection

$$Q_{INJ} = C_L \times \Delta V_{OUT}$$
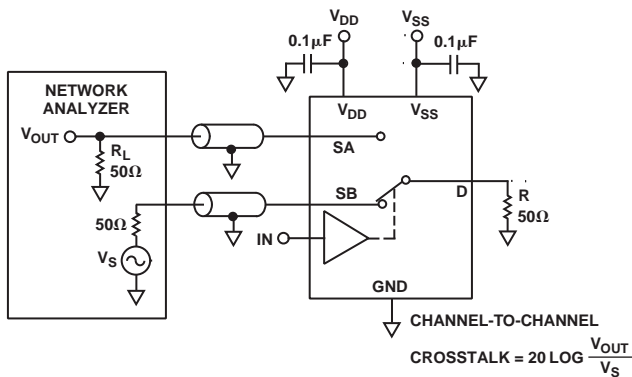

$$\text{OFF ISOLATION} = 20 \text{ LOG} \frac{V_{OUT}}{V_S}$$

Test Circuit 8. OFF Isolation

$$\text{INSERTION LOSS} = 20 \text{ LOG} \frac{V_{OUT} \text{ WITH SWITCH}}{V_{OUT} \text{ WITHOUT SWITCH}}$$

Test Circuit 10. Bandwidth

$$\text{CROSSTALK} = 20 \text{ LOG} \frac{V_{OUT}}{V_S}$$

Test Circuit 9. Channel-to-Channel Crosstalk

Power Supply Sequencing
When using CMOS devices, care must be taken to ensure correct power supply sequencing. Incorrect sequencing can result in the device being subjected to stresses beyond those maximum ratings listed in the data sheet. Digital and analog inputs should be applied to the device after supplies and ground. In dual supply applications, if digital and analog inputs may be applied prior to V_{DD} and V_{SS} supplies, the addition of a Schottky diode connected between V_{SS} and GND will ensure that the device powers on correctly. For single supply applications, V_{SS} should be tied to GND as close to the device as possible.

OUTLINE DIMENSIONS
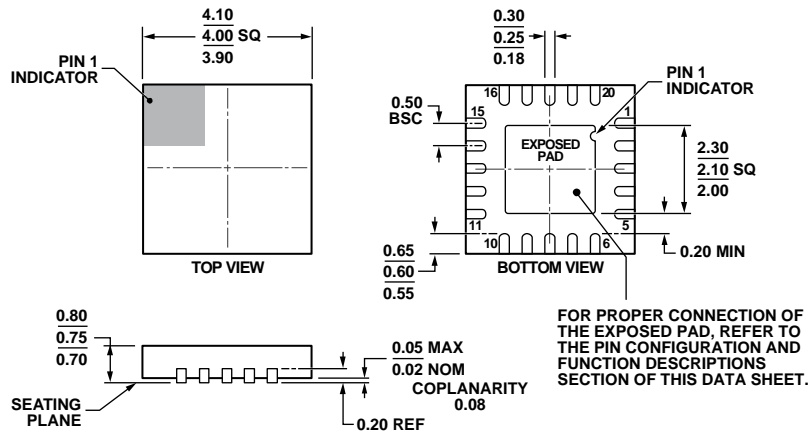
COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-1.

Figure 1. 20-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-20-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADG786BCPZ	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-6
ADG786BCPZ-REEL7	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-6
ADG786WBCPZ-REEL7	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-6
ADG788BCPZ	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-6
ADG788BCPZ-REEL	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-6
ADG788BCPZ-REEL7	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-6
EVAL-ADG788EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADG786W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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