

## FEATURES

- Extreme high temperature operation**
  - Specified temperature range
    - 55°C to +210°C (16-lead FLATPACK)
    - 55°C to +175°C (16-lead TSSOP)
- 3.0 V to 5.5 V single supply**
- ±2.5 V dual supply**
- 10 Ω on resistance, maximum**
- 2 Ω on-resistance flatness, maximum**
- 12 ns switching times**
- Single 8:1 multiplexer**
- Low power consumption**
- TTL-/CMOS-compatible inputs**

## APPLICATIONS

- Downhole drilling and instrumentation**
- Avionics**
- Heavy industrial**
- High temperature environments**

## GENERAL DESCRIPTION

The ADG798 is a low voltage, CMOS, analog multiplexer designed to operate at very high temperatures up to 210°C. The ADG798 switches one of eight inputs (S1 to S8) to a common output, D, as determined by the 3-bit binary address lines A0, A1, and A2. An EN input on the device enables or disables the device. When the device is disabled, all channels are switched off.

The ADG798 features low power consumption and a 3.3 V to 5.5 V operating supply range. All channels exhibit break-before-make switching action, preventing momentary shorting when switching channels. These switches are designed with an enhanced submicron process that provides low power dissipation, high switching speed, and very low on resistance.

The on resistance ( $R_{ON}$ ) is a maximum of 10 Ω and is closely matched between switches and very flat over the full signal range. The ADG798 operates equally well as either a multiplexer or a demultiplexer and has an input signal range that extends to the supplies.

This mux is available in a 16-lead ceramic flat package (FLATPACK) and a 16-lead ceramic flat package with reverse formed gullwing leads (FLATPACK\_RF). Both of the flat

## FUNCTIONAL BLOCK DIAGRAM

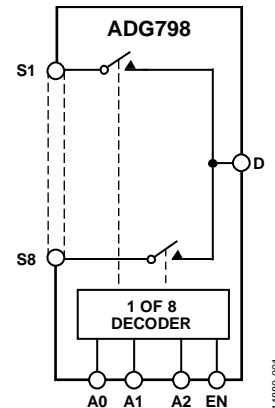


Figure 1.

packages have an operating temperature range of –55°C to +210°C. A 16-lead TSSOP package is also available that has an operating temperature range of –55°C to +175°C. All packages are designed for robustness at extreme temperatures, and are qualified for 1000 hours of continuous operation at the maximum temperature rating.

The ADG798 is a member of a growing series of high temperature qualified products offered by Analog Devices, Inc. For a complete selection table of available high temperature products, see the high temperature product list and qualification data available at <http://www.analog.com/hightemp>.

## PRODUCT HIGHLIGHTS

1. **Single-Supply/Dual-Supply Operation.**  
The ADG798 is fully specified and guaranteed with 3.3 V and 5 V single-supply rails and ±2.5 V dual-supply rails.
2. **Low  $R_{ON}$ .**  
The  $R_{ON}$  of the ADG798 is specified at 5 Ω, typical, at 210°C.
3. **Low Power Consumption.**  
The power consumption of the ADG798 is specified at <0.01 μW.
4. **Guaranteed Break-Before-Make Switching Action.**

Rev. A

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## REVISION HISTORY

### 6/2018—Rev. 0 to Rev. A

Added TSSOP Package .....	Universal
Changes to Features.....	1
Changes to General Description .....	1
Changes to Specifications, Table 1.....	3
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Added TSSOP Operating Temperature Range and Junction Temperature Range, Table 5.....	9
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### 9/2016—Revision 0: Initial Version

## SPECIFICATIONS

$V_{DD} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted. TSSOP temperature range =  $-55^{\circ}\text{C} \leq T_A \leq +175^{\circ}\text{C}$  and FLATPACK temperature range =  $-55^{\circ}\text{C} \leq T_A \leq +210^{\circ}\text{C}$ , unless otherwise noted.

**Table 1.**

Parameter	Symbol	Test Conditions/Comments <sup>1</sup>	TSSOP			FLATPACK			Unit
			Min	Typ <sup>2</sup>	Max	Min	Typ <sup>2</sup>	Max	
<b>ANALOG SWITCH</b>									
Analog Signal Range			0		$V_{DD}$	0		$V_{DD}$	V
On Resistance	$R_{ON}$	$V_S = 0\text{ V to }V_{DD}$ , $I_{DS} = 10\text{ mA}$ ; see Figure 24		4.5	9		5	10	$\Omega$
Matching Between Channels	$\Delta R_{ON}$	$V_S = 0\text{ V to }V_{DD}$ , $I_{DS} = 10\text{ mA}$		0.6	1.2		1.25	1.5	$\Omega$
Flatness	$R_{FLAT(ON)}$	$V_S = 0\text{ V to }V_{DD}$ , $I_{DS} = 10\text{ mA}$			1.5		0.75	2	$\Omega$
<b>LEAKAGE CURRENTS</b>									
Source Off Leakage	$I_S$ (Off)	$V_{DD} = 5.5\text{ V}$ $V_D = 4.5\text{ V}/1\text{ V}$ , $V_S = 1\text{ V}/4.5\text{ V}$ ; see Figure 25	-50	$\pm 0.01$	+50	-180	$\pm 0.01$	+180	nA
Drain Off Leakage	$I_D$ (Off)	$V_D = 4.5\text{ V}/1\text{ V}$ , $V_S = 1\text{ V}/4.5\text{ V}$ ; see Figure 26	-650	$\pm 0.01$	+650	-2600	$\pm 0.01$	+2600	nA
Channel On Leakage	$I_D$ (On), $I_S$ (On)	$V_D = V_S = 1\text{ V or }4.5\text{ V}$ ; see Figure 27	-650	$\pm 0.01$	+650	-2600	$\pm 0.01$	+2600	nA
<b>DIGITAL INPUTS</b>									
Input Voltage									
High	$V_{INH}$		2.4			2.4			V
Low	$V_{INL}$				0.8			0.8	V
Input Current	$I_{INL}$ or $I_{INH}$	$V_{IN} = V_{INL}$ or $V_{INH}$	-800	+0.005	+800	-800	+0.005	+800	nA
Digital Input Capacitance	$C_{IN}$			2			2		pF
<b>DYNAMIC CHARACTERISTICS<sup>3</sup></b>									
Transition Time	$t_{TRANSITION}$	$R_L = 150\ \Omega$ , $C_L = 15\text{ pF}$ ; see Figure 28 $V_{S1} = 3\text{ V}/0\text{ V}$ , $V_{S8} = 0\text{ V}/3\text{ V}$		12	21		12	23	ns
Break-Before-Make Time Delay	$t_{OPEN}$	$R_L = 150\ \Omega$ , $C_L = 15\text{ pF}$ , $V_S = 3\text{ V}$ ; see Figure 29	1	8		1	8		ns
On Time	$t_{ON(EN)}$	$T_A = \text{maximum temperature}$ $R_L = 150\ \Omega$ , $C_L = 15\text{ pF}$ $V_S = 3\text{ V}$ ; see Figure 30		9			9		ns
Off Time	$t_{OFF(EN)}$	$R_L = 150\ \Omega$ , $C_L = 15\text{ pF}$ $V_S = 3\text{ V}$ ; see Figure 30		11	17		11	20	ns
Charge Injection	$Q_{INJ}$	$V_S = 2.5\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 31		$\pm 3$			$\pm 3$		pC
Off Isolation		$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$		-60			-60		dB
		$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 32		-80			-80		dB
Channel to Channel Crosstalk		$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$		-60			-60		dB
		$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 33		-80			-80		dB
-3 dB Bandwidth		$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 34		55			55		MHz
Source Capacitance, Off	$C_S$ (Off)	$f = 1\text{ MHz}$		13			13		pF

Parameter	Symbol	Test Conditions/Comments <sup>1</sup>	TSSOP			FLATPACK			Unit
			Min	Typ <sup>2</sup>	Max	Min	Typ <sup>2</sup>	Max	
Drain Capacitance, Off	C <sub>D</sub> (Off)	f = 1 MHz		85			85		pF
Source/Drain Capacitance, On	C <sub>D</sub> (On), C <sub>S</sub> (On)	f = 1 MHz		96			96		pF
POWER REQUIREMENTS									
Supply Current	I <sub>DD</sub>	V <sub>DD</sub> = 5.5 V Digital inputs = 0 V or 5.5 V		5	35		40	70	μA

<sup>1</sup> The ADG798 is qualified for a minimum of 1000 hours of continuous operation at the maximum temperature rating.

<sup>2</sup> T<sub>A</sub> = 25°C, except for the analog switch and power requirements values where T<sub>A</sub> = 175°C (TSSOP only) or 210°C (FLATPACK only).

<sup>3</sup> Guaranteed by design, not subject to production test.

$V_{DD} = 3.3 \text{ V} \pm 10\%$ ,  $V_{SS} = 0 \text{ V}$ ,  $GND = 0 \text{ V}$ , unless otherwise noted. TSSOP temperature range =  $-55^\circ\text{C} \leq T_A \leq +175^\circ\text{C}$  and FLATPACK temperature range =  $-55^\circ\text{C} \leq T_A \leq +210^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments <sup>1</sup>	TSSOP			FLATPACK			Unit
			Min	Typ <sup>2</sup>	Max	Min	Typ <sup>2</sup>	Max	
ANALOG SWITCH									
Analog Signal Range			0		$V_{DD}$	0 V		$V_{DD}$	V
On Resistance	$R_{ON}$	$V_S = 0 \text{ V to } V_{DD}$ , $I_{DS} = 10 \text{ mA}$ ; see Figure 24		7	15		8	20	$\Omega$
Matching Between Channels	$\Delta R_{ON}$	$V_S = 0 \text{ V to } V_{DD}$ , $I_{DS} = 10 \text{ mA}$		0.4	1.2		0.5	1.5	$\Omega$
Flatness	$R_{FLAT(ON)}$	$V_S = 0 \text{ V to } V_{DD}$ , $I_{DS} = 10 \text{ mA}$		2.5	3.5		3	4.5	$\Omega$
LEAKAGE CURRENTS									
Source Off Leakage	$I_S$ (Off)	$V_{DD} = 3.63 \text{ V}$ $V_D = 2.3 \text{ V}/1 \text{ V}$ , $V_S = 1 \text{ V}/2.3 \text{ V}$ ; see Figure 25	-50	$\pm 0.01$	+50	-180	$\pm 0.01$	+180	nA
Drain Off Leakage	$I_D$ (Off)	$V_D = 2.3 \text{ V}/1 \text{ V}$ , $V_S = 1 \text{ V}/2.3 \text{ V}$ ; see Figure 26	-650	$\pm 0.01$	+650	-2600	$\pm 0.01$	+2600	nA
Channel On Leakage	$I_D$ (On), $I_S$ (On)	$V_D = V_S = 1 \text{ V or } 2.3 \text{ V}$ ; see Figure 27	-650	$\pm 0.01$	+650	-2600	$\pm 0.01$	+2600	nA
DIGITAL INPUTS									
Input Voltage High	$V_{INH}$		2.4			2.0			V
Input Voltage Low	$V_{INL}$				0.8			0.8	V
Input Current	$I_{INL}$ or $I_{INH}$	$V_{IN} = V_{INL}$ or $V_{INH}$	-800	+0.005	+800	-800	+0.005	+800	nA
Digital Input Capacitance	$C_{IN}$			2			2		pF
DYNAMIC CHARACTERISTICS <sup>3</sup>									
Transition Time	$t_{TRANSITION}$	$R_L = 150 \Omega$ , $C_L = 15 \text{ pF}$ ; see Figure 28 $V_{S1} = 2 \text{ V}/0 \text{ V}$ , $V_{S8} = 0 \text{ V}/2 \text{ V}$		18	34		18	38	ns
Break-Before-Make Time Delay	$t_{OPEN}$	$R_L = 150 \Omega$ , $C_L = 15 \text{ pF}$ , $V_S = 2 \text{ V}$ ; see Figure 29 $T_A = \text{maximum temperature}$	1	10		1	10		ns
On Time	$t_{ON(EN)}$	$R_L = 150 \Omega$ , $C_L = 15 \text{ pF}$ $V_S = 2 \text{ V}$ ; see Figure 30		15			15		ns
Off Time	$t_{OFF(EN)}$	$R_L = 150 \Omega$ , $C_L = 15 \text{ pF}$ $V_S = 2 \text{ V}$ ; see Figure 30		14	26		14	28	ns
Charge Injection	$Q_{INJ}$	$V_S = 1.5 \text{ V}$ , $R_S = 0 \Omega$ , $C_L = 1 \text{ nF}$ ; see Figure 31		$\pm 3$			$\pm 3$		pC
Off Isolation		$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 10 \text{ MHz}$		-60			-60		dB
		$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ ; see Figure 32		-80			-80		dB
Channel to Channel Crosstalk		$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 10 \text{ MHz}$		-60			-60		dB
		$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ ; see Figure 33		-80			-80		dB
-3 dB Bandwidth		$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ ; see Figure 34		55			55		MHz
Source Capacitance, Off	$C_S$ (Off)	$f = 1 \text{ MHz}$		13			13		pF
Drain Capacitance, Off	$C_D$ (Off)	$f = 1 \text{ MHz}$		85			85		pF
Source/Drain Capacitance, On	$C_D$ (On), $C_S$ (On)	$f = 1 \text{ MHz}$		96			96		pF

Parameter	Symbol	Test Conditions/Comments <sup>1</sup>	TSSOP			FLATPACK			Unit
			Min	Typ <sup>2</sup>	Max	Min	Typ <sup>2</sup>	Max	
POWER REQUIREMENTS		$V_{DD} = 3.63\text{ V}$							
Supply Current	$I_{DD}$	Digital inputs = 0 V or 3.63 V	5		35	40		70	$\mu\text{A}$

<sup>1</sup> The ADG798 is qualified for a minimum of 1000 hours of continuous operation at the maximum temperature rating.

<sup>2</sup>  $T_A = 25^\circ\text{C}$ , except for the analog switch and power requirements values where  $T_A = 175^\circ\text{C}$  (TSSOP only) or  $210^\circ\text{C}$  (FLATPACK only).

<sup>3</sup> Guaranteed by design, not subject to production test.

**DUAL SUPPLY**

$V_{DD} = 2.5 \text{ V} \pm 10\%$ ,  $V_{SS} = -2.5 \text{ V} \pm 10\%$ ,  $GND = 0 \text{ V}$ , unless otherwise noted. TSSOP temperature range =  $-55^\circ\text{C} \leq T_A \leq +175^\circ\text{C}$  and FLATPACK temperature range =  $-55^\circ\text{C} \leq T_A \leq +210^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

Parameter	Symbol	Test Conditions/Comments <sup>1</sup>	TSSOP			FLATPACK			Unit
			Min	Typ <sup>2</sup>	Max	Min	Typ <sup>2</sup>	Max	
<b>ANALOG SWITCH</b>									
Analog Signal Range			0		$V_{DD}$	$V_{SS}$		$V_{DD}$	V
On Resistance	$R_{ON}$	$V_S = V_{SS}$ to $V_{DD}$ , $I_{DS} = 10 \text{ mA}$ ; see Figure 24		4.5	9		5	10	$\Omega$
Matching Between Channels	$\Delta R_{ON}$	$V_S = V_{SS}$ to $V_{DD}$ , $I_{DS} = 10 \text{ mA}$		0.6	1.2		1.25	1.5	$\Omega$
Flatness	$R_{FLAT(ON)}$	$V_S = V_{SS}$ to $V_{DD}$ , $I_{DS} = 10 \text{ mA}$			1.5		0.6	2	$\Omega$
<b>LEAKAGE CURRENTS</b>									
Source Off Leakage	$I_S$ (Off)	$V_{DD} = +2.75 \text{ V}$ , $V_S = -2.75 \text{ V}$ $V_S = +2.25 \text{ V}/-1.25 \text{ V}$ , $V_D = -1.25 \text{ V}/+2.25 \text{ V}$ ; see Figure 25	-50	$\pm 0.01$	+50	-180	$\pm 0.01$	+180	nA
Drain Off Leakage	$I_D$ (Off)	$V_S = +2.25 \text{ V}/-1.25 \text{ V}$ , $V_D = -1.25 \text{ V}/+2.25 \text{ V}$ ; see Figure 26	-650	$\pm 0.01$	+650	-2600	$\pm 0.01$	+2600	nA
Channel On Leakage	$I_D$ (On), $I_S$ (On)	$V_D = V_S = -1.25 \text{ V}/+2.25 \text{ V}$ ; see Figure 27	-650	$\pm 0.01$	+650	-2600	$\pm 0.01$	+2600	nA
<b>DIGITAL INPUTS</b>									
Input Voltage									
High	$V_{INH}$		2.4			2.0			V
Low	$V_{INL}$				0.8			0.8	V
Input Current	$I_{INL}$ or $I_{INH}$	$V_{IN} = V_{INL}$ or $V_{INH}$	-800	+0.005	+800	-800	+0.005	+800	nA
Digital Input Capacitance	$C_{IN}$			2			2		pF
<b>DYNAMIC CHARACTERISTICS<sup>3</sup></b>									
Transition Time	$t_{TRANSITION}$	$R_L = 150 \Omega$ , $C_L = 15 \text{ pF}$ ; see Figure 28 $V_{S1} = 1.5 \text{ V}/0 \text{ V}$ , $V_{S8} = 0 \text{ V}/1.5 \text{ V}$		18	28		14	30	ns
Break-Before-Make Time Delay	$t_{OPEN}$	$R_L = 150 \Omega$ , $C_L = 15 \text{ pF}$ , $V_S = 2 \text{ V}$ ; see Figure 29 $T_A = \text{maximum temperature}$	1	10		1	10		ns
On Time	$t_{ON(EN)}$	$R_L = 150 \Omega$ , $C_L = 15 \text{ pF}$ $V_S = 2 \text{ V}$ ; see Figure 30		13	28		13	30	ns
Off Time	$t_{OFF(EN)}$	$R_L = 150 \Omega$ , $C_L = 15 \text{ pF}$ $V_S = 2 \text{ V}$ ; see Figure 30		11.5	19		11.5	20	ns
Charge Injection	$Q_{INJ}$	$V_S = 0 \text{ V}$ , $R_S = 0 \Omega$ , $C_L = 1 \text{ nF}$ ; see Figure 31		$\pm 3$			$\pm 3$		pC
Off Isolation		$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 10 \text{ MHz}$ $R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ ; see Figure 32		-60			-60		dB
Channel to Channel Crosstalk		$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 10 \text{ MHz}$		-60			-60		dB
-3 dB Bandwidth		$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ ; see Figure 33 $R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ ; see Figure 34		-80			-80		dB
Source Capacitance, Off	$C_S$ (Off)	$f = 1 \text{ MHz}$		55			55		MHz
				13			13		pF

Parameter	Symbol	Test Conditions/Comments <sup>1</sup>	TSSOP			FLATPACK			Unit
			Min	Typ <sup>2</sup>	Max	Min	Typ <sup>2</sup>	Max	
Drain Capacitance, Off	$C_D$ (Off)	$f = 1 \text{ MHz}$	85			85			pF
Source/Drain Capacitance, On	$C_D$ (On), $C_S$ (On)	$f = 1 \text{ MHz}$	96			96			pF
POWER REQUIREMENTS		$V_{DD} = 2.75 \text{ V}$							
Supply Current	$I_{DD}$	Digital inputs = 0 V or 2.75 V	5	35		40	70	$\mu\text{A}$	
	$I_{SS}$	$V_{SS} = -2.75 \text{ V}$ ; digital inputs = 0 V or 2.75 V	5	35		40	70	$\mu\text{A}$	

<sup>1</sup> The ADG798 is qualified for a minimum of 1000 hours of continuous operation at the maximum temperature rating.

<sup>2</sup>  $T_A = 25^\circ\text{C}$ , except for the analog switch and power requirements values where  $T_A = 175^\circ\text{C}$  (TSSOP) or  $210^\circ\text{C}$  (FLATPACK).

<sup>3</sup> Guaranteed by design, not subject to production test.

## CONTINUOUS CURRENT PER CHANNEL, Sx OR D

Table 4.

Parameter	175°C	210°C	Unit
CONTINUOUS CURRENT, Sx OR D			
FLATPACK $\theta_{JA} = 70^\circ\text{C}/\text{W}$			
$V_{DD} = 5 \text{ V}, V_{SS} = 0 \text{ V}$	30	30	mA maximum
$V_{DD} = 3 \text{ V}, V_{SS} = 0 \text{ V}$	30	30	mA maximum
$V_{DD} = +2.5 \text{ V}, V_{SS} = -2.5 \text{ V}$	30	30	mA maximum
TSSOP $\theta_{JA} = 109.6^\circ\text{C}/\text{W}$			
$V_{DD} = 5 \text{ V}, V_{SS} = 0 \text{ V}$	30		mA maximum
$V_{DD} = 3 \text{ V}, V_{SS} = 0 \text{ V}$	30		mA maximum
$V_{DD} = +2.5 \text{ V}, V_{SS} = -2.5 \text{ V}$	30		mA maximum



## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 5.**

Parameter	Rating
$V_{DD}$ to $V_{SS}$	7 V
$V_{DD}$ to GND	-0.3 V to +7 V
$V_{SS}$ to GND	+0.3 V to -3.5 V
Analog Inputs <sup>1</sup>	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs <sup>1</sup>	-0.3 V to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, Sx or D (Pulsed at 1 ms, 10% Duty Cycle Maximum)	94.9 mA
Continuous Current, Sx or D <sup>2</sup>	Data + 5%
Operating Temperature Range	
TSSOP	-55°C to +175°C
FLATPACK	-55°C to +210°C
Junction Temperature	
TSSOP	180°C
FLATPACK	211°C

<sup>1</sup> Overvoltages at Ax, EN, Sx, or D are clamped by internal codes. Limit the current to the maximum ratings given.

<sup>2</sup> See Table 4.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

### THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required.

**Table 6. Thermal Resistance**

Package Type <sup>1</sup>	$\theta_{JA}$	$\theta_{JC}$	Unit
F-16-1	70	22	°C/W
FR-16-1	70	10	°C/W
RU-16	109.6	36.5	°C/W

<sup>1</sup> Thermal impedance simulated values are based on a JEDEC 2s2p thermal test board. See JEDEC JESD51.

### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

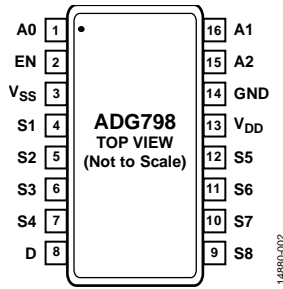


Figure 2. TSSOP and FLATPACK Pin Configuration

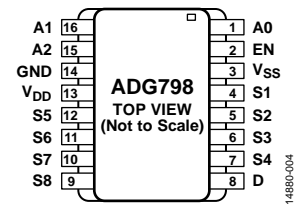


Figure 3. Reversed Formed FLATPACK Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A0	Digital Input. This pin controls the configuration of the switch, as shown in the truth table (see Table 8).
2	EN	Digital Input. This pin controls the configuration of the switch, as shown in the truth table (see Table 8).
3	V <sub>SS</sub>	Most Negative Power Supply Pin in Dual-Supply Applications. For single-supply applications, tie this pin to GND.
4	S1	Source Terminal. This pin can be an input or output.
5	S2	Source Terminal. This pin can be an input or output.
6	S3	Source Terminal. This pin can be an input or output.
7	S4	Source Terminal. This pin can be an input or output.
8	D	Drain Terminal. This pin can be an input or output.
9	S8	Source Terminal. This pin can be an input or output.
10	S7	Source Terminal. This pin can be an input or output.
11	S6	Source Terminal. This pin can be an input or output.
12	S5	Source Terminal. This pin can be an input or output.
13	V <sub>DD</sub>	Most Positive Power Supply Pin.
14	GND	Ground (0 V) Reference.
15	A2	Digital Input. This pin controls the configuration of the switch, as shown in the truth table (see Table 8).
16	A1	Digital Input. This pin controls the configuration of the switch, as shown in the truth table (see Table 8).

## TRUTH TABLE

Table 8. Truth Table

A2	A1	A0	EN	Switch Condition
X <sup>1</sup>	X <sup>1</sup>	X <sup>1</sup>	0	None
0	0	0	1	S1
0	0	1	1	S2
0	1	0	1	S3
0	1	1	1	S4
1	0	0	1	S5
1	0	1	1	S6
1	1	0	1	S7
1	1	1	1	S8

<sup>1</sup> X means don't care.

# TYPICAL PERFORMANCE CHARACTERISTICS

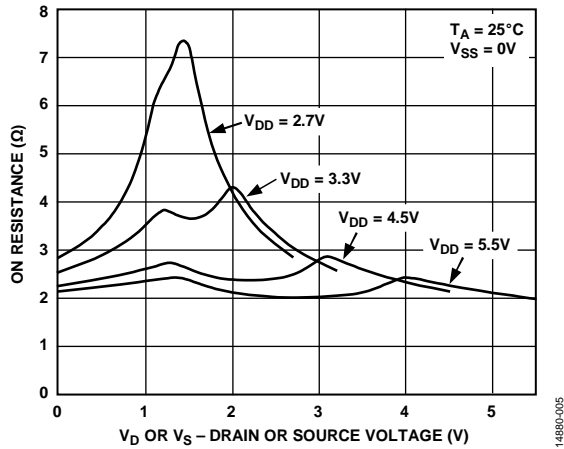


Figure 4. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Single Supply

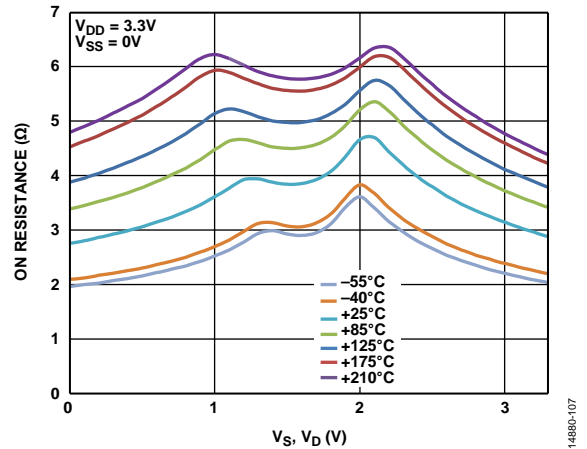


Figure 7. On Resistance as a Function of  $V_S$  ( $V_D$ ) for Different Temperatures, 3.3 V Single Supply

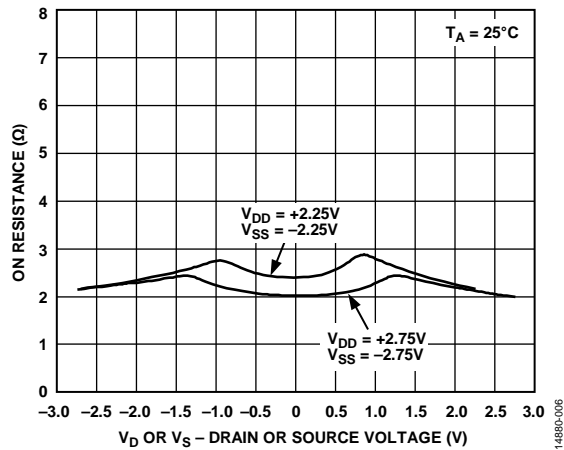


Figure 5. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Dual Supply

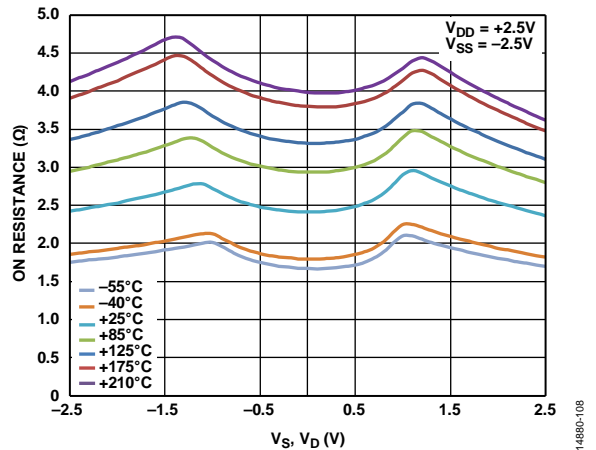


Figure 8. On Resistance as a Function of  $V_S$  ( $V_D$ ) for Different Temperatures,  $\pm 2.5$  V Dual Supply

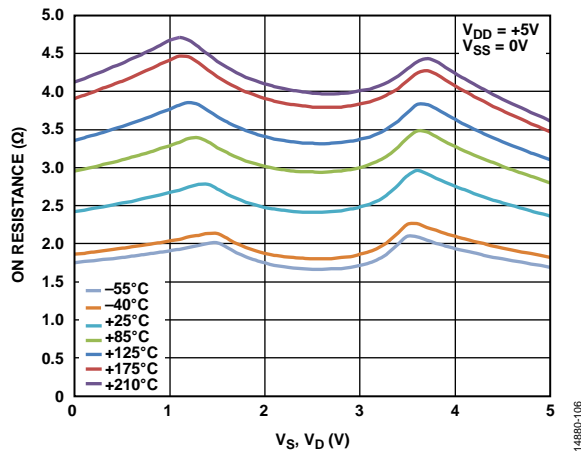


Figure 6. On Resistance as a Function of  $V_S$ ,  $V_D$  for Different Temperatures, 5 V Single Supply

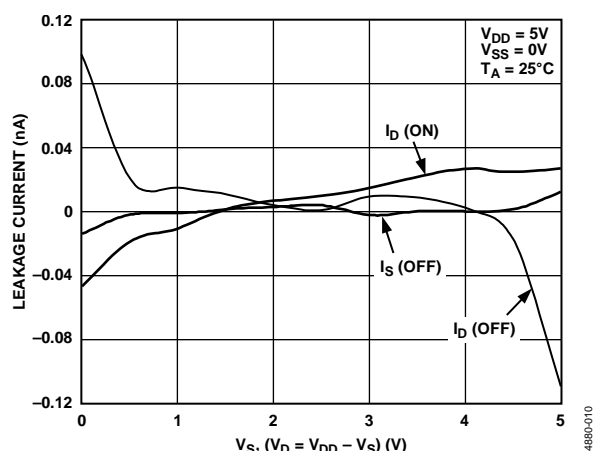


Figure 9. Leakage Current as a Function of  $V_D$  ( $V_S$ )

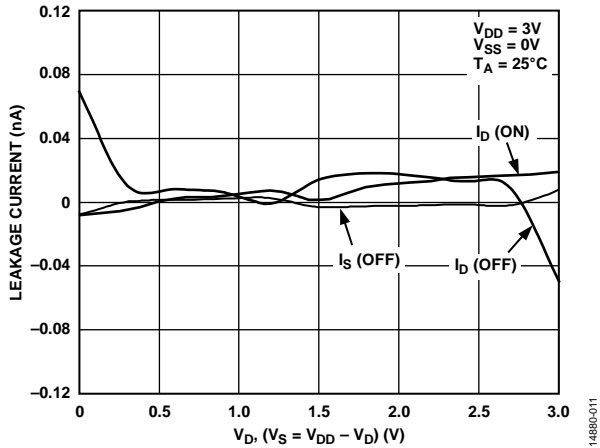


Figure 10. Leakage Current as a Function of  $V_D (V_S)$

14880-011

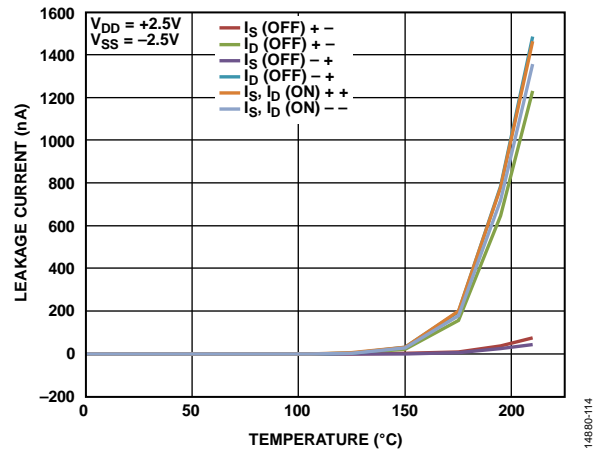


Figure 13. Leakage Current as a Function of Temperature,  $V_{DD} = +2.5V$ ,  $V_{SS} = -2.5V$

14880-114

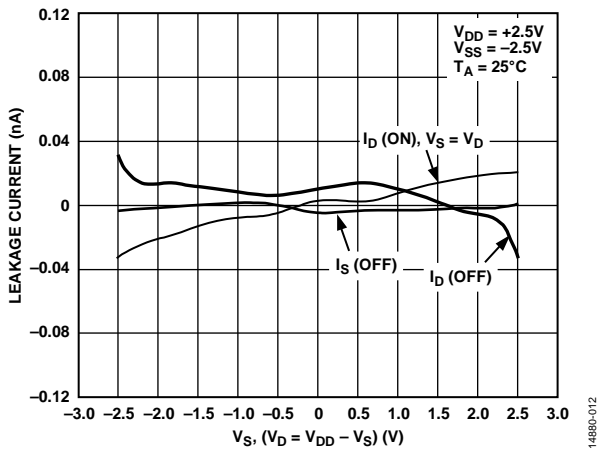


Figure 11. Leakage Current as a Function of  $V_D (V_S)$

14880-012

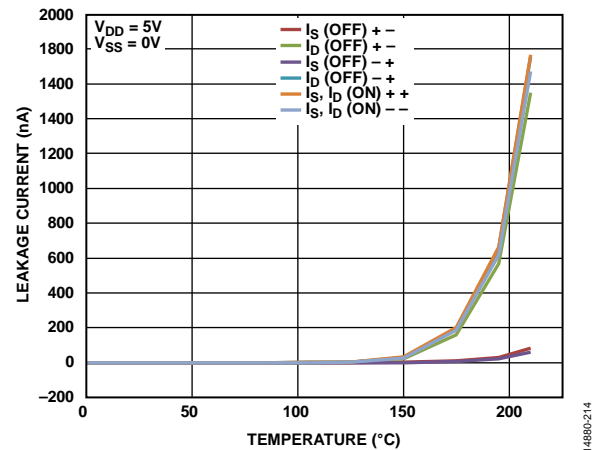


Figure 14. Leakage Current vs. Temperature,  $V_{DD} = 5V$

14880-214

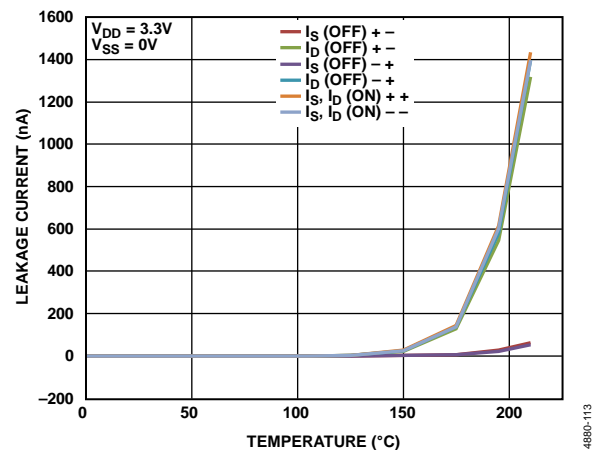


Figure 12. Leakage Current as a Function of Temperature,  $V_{DD} = 3.3V$ ,  $V_{SS} = 0V$

14880-113

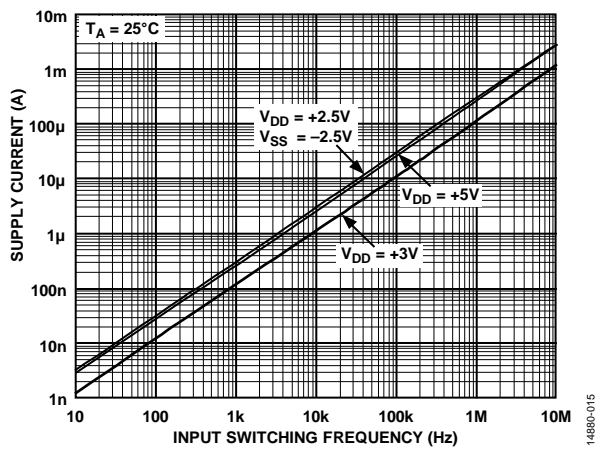


Figure 15. Supply Current vs. Input Switching Frequency

14880-015

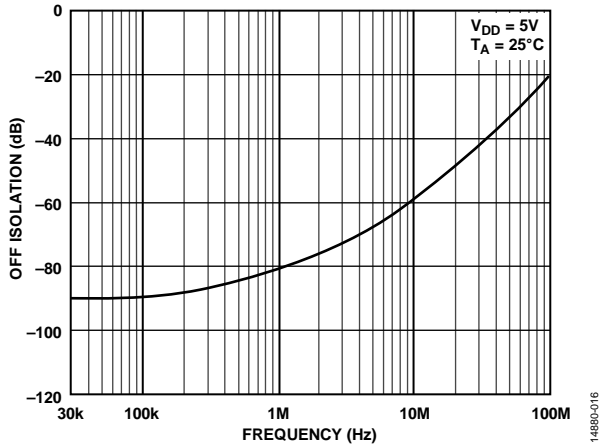


Figure 16. Off Isolation vs. Frequency

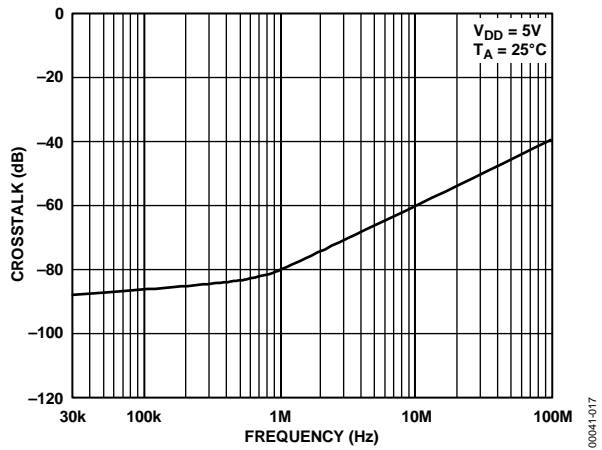


Figure 17. Crosstalk vs. Frequency

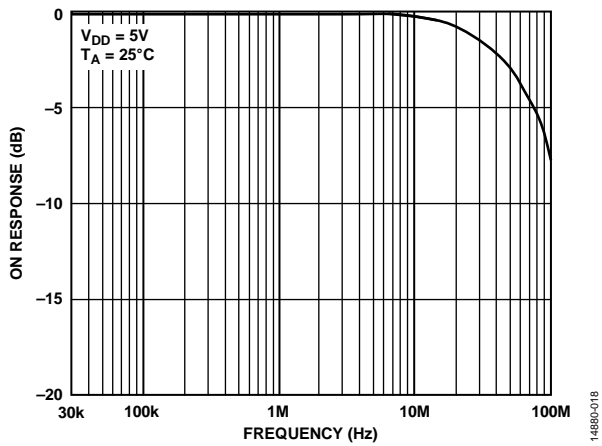


Figure 18. On Response vs. Frequency

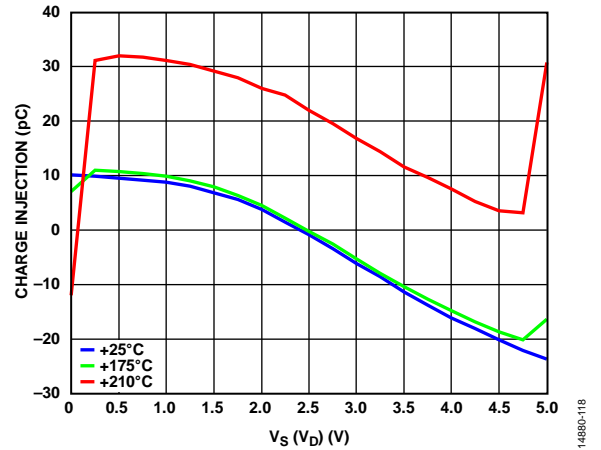


Figure 19. Charge Injection as a Function of  $V_S (V_D)$  for Various Temperatures, 5 V Single Supply

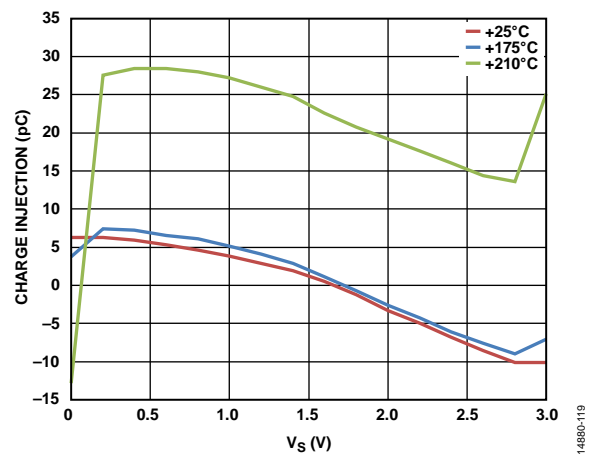


Figure 20. Charge Injection as a Function of  $V_S (V_D)$  for Various Temperatures, 3.3 V Single Supply

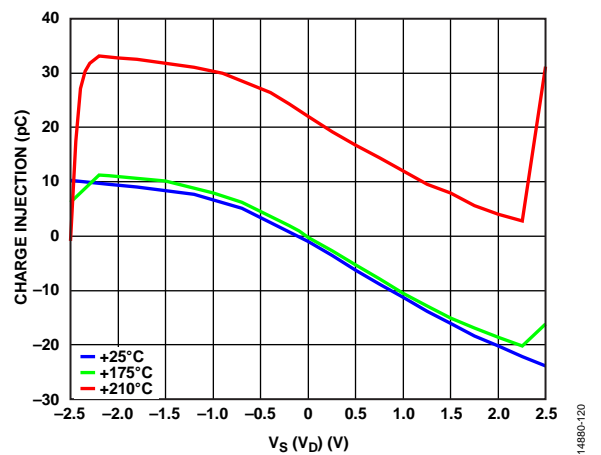


Figure 21. Charge Injection as a Function of  $V_S (V_D)$  for Various Temperatures,  $\pm 2.5$  V Dual Supply

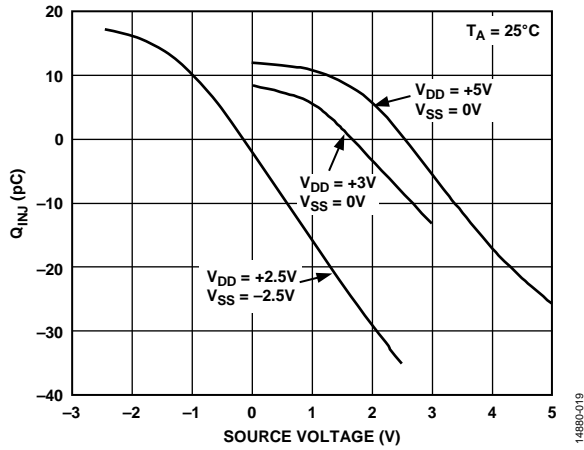


Figure 22. Charge Injection ( $Q_{INJ}$ ) vs. Source Voltage

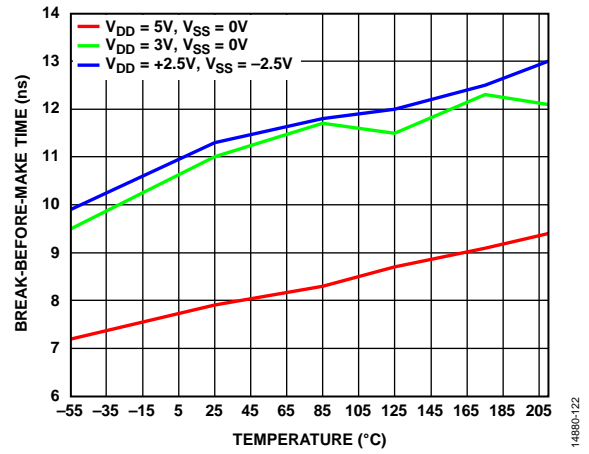


Figure 23. Break-Before-Make Time vs. Temperature

TEST CIRCUITS

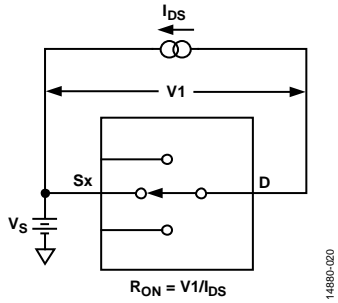


Figure 24. On Resistance

14880-020

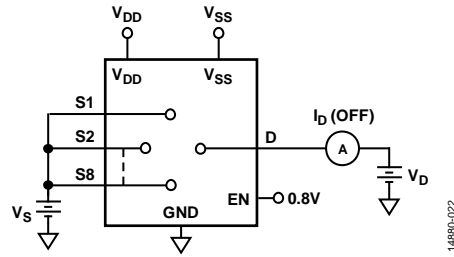


Figure 26. Id (Off)

14880-022

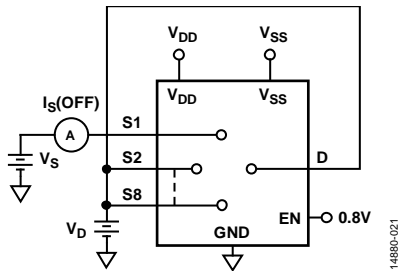


Figure 25. Is (Off)

14880-021

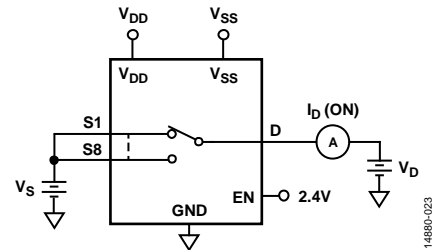


Figure 27. Id (On)

14880-023

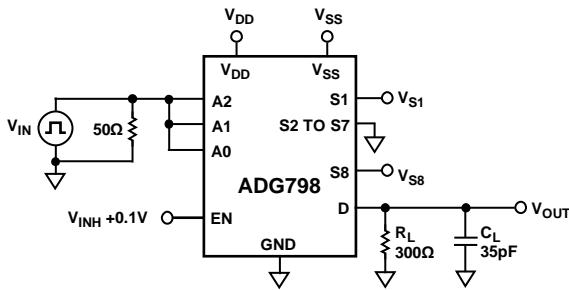
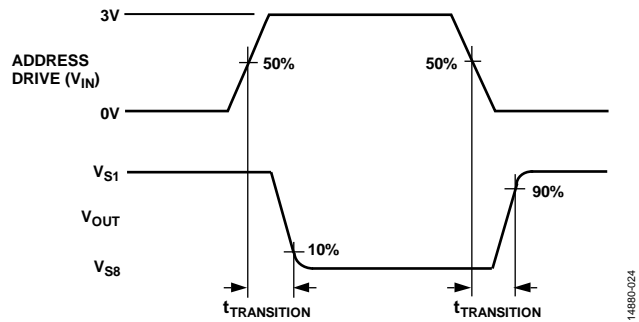


Figure 28. Switching Time of Multiplexer,  $t_{TRANSITION}$



14880-024

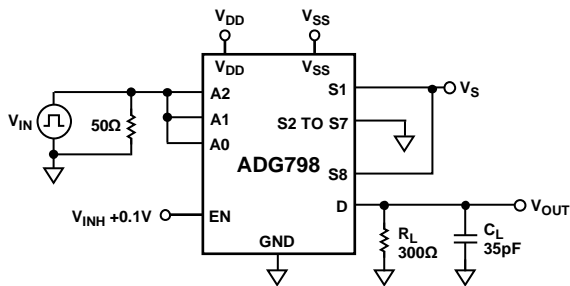
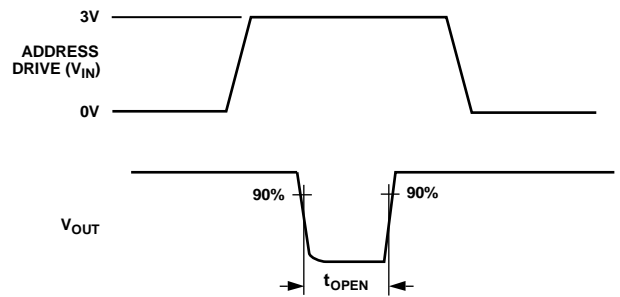


Figure 29. Break-Before-Make Delay,  $t_{OPEN}$



14880-025

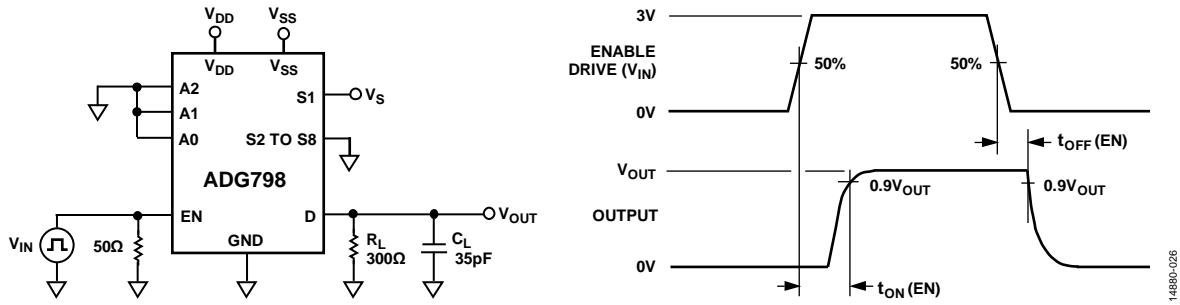


Figure 30. Enable Delay,  $t_{ON}(EN)$ ,  $t_{OFF}(EN)$

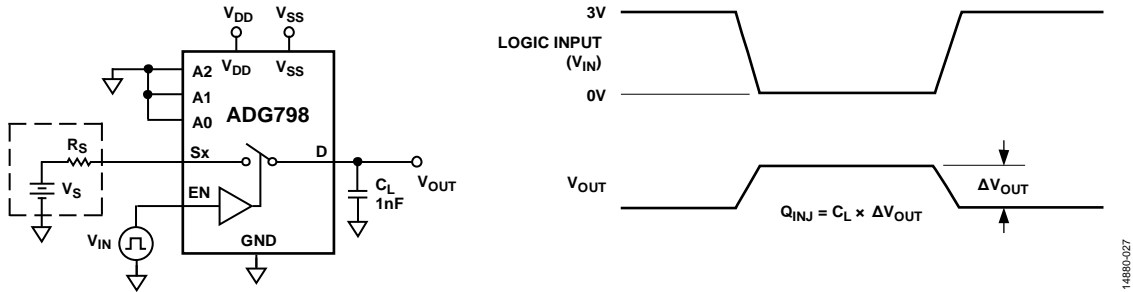
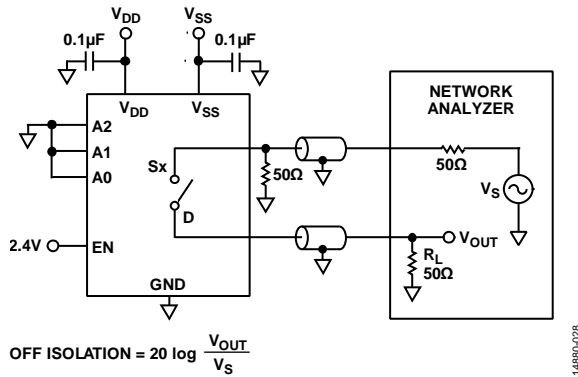
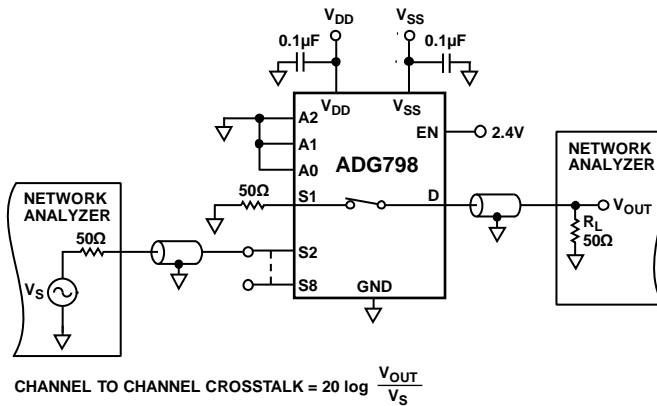


Figure 31. Charge Injection



$$\text{OFF ISOLATION} = 20 \log \frac{V_{OUT}}{V_S}$$

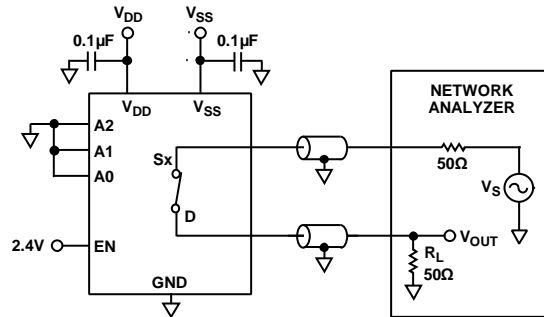
Figure 32. Off Isolation



$$\text{CHANNEL TO CHANNEL CROSSTALK} = 20 \log \frac{V_{OUT}}{V_S}$$

Figure 33. Channel to Channel Crosstalk





$$\text{INSERTION LOSS} = 20 \log \frac{V_{\text{OUT WITH SWITCH}}}{V_{\text{OUT WITHOUT SWITCH}}}$$

Figure 34. -3 dB Bandwidth

14880-030

## TERMINOLOGY

### $V_{DD}$

$V_{DD}$  is the most positive power supply potential.

### $V_{SS}$

$V_{SS}$  is the most negative power supply in a dual-supply application. In single-supply applications, tie  $V_{SS}$  to ground at the device.

### GND

GND is the ground (0 V) reference.

### Sx

Sx are the source terminals and can be inputs or outputs.

### D

D is the drain terminal and can be an input or an output.

### Ax

Ax is the logic control input.

### EN

EN is the active high enable.

### $R_{ON}$

$R_{ON}$  is the ohmic resistance between D and Sx.

### $R_{FLAT(ON)}$

$R_{FLAT(ON)}$  flatness is the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

### $I_S$ (Off)

$I_S$  (Off) is the source leakage current with the switch off.

### $I_D$ (Off)

$I_D$  (Off) is the drain leakage current with the switch off.

### $I_D, I_S$ (On)

$I_D, I_S$  (On) is the channel leakage current with the switch on.

### $V_D$ ( $V_S$ )

$V_D$  ( $V_S$ ) is the analog voltage on Terminal D and Terminal Sx.

### $C_S$ (Off)

$C_S$  (Off) is the off switch source capacitance and is measured with reference to ground.

### $C_D$ (Off)

$C_D$  (Off) is the off switch drain capacitance and is measured with reference to ground.

### $C_D, C_S$ (On)

$C_D, C_S$  (On) is the on switch capacitance and is measured with reference to ground.

### $C_{IN}$

$C_{IN}$  is the digital input capacitance.

### $t_{TRANSITION}$

$t_{TRANSITION}$  is the delay time measured between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

### $t_{ON(EN)}$

$t_{ON(EN)}$  is the delay time between the 50% and 90% points of the EN digital input and the switch on condition.

### $t_{OFF(EN)}$

$t_{OFF(EN)}$  is the delay time between the 50% and 90% points of the EN digital input and the switch off condition.

### $t_{OPEN}$

$t_{OPEN}$  is the off time measured between the 80% points of both switches when switching from one address state to another.

### Off Isolation

Off isolation is a measure of unwanted signal coupling through an off switch.

### Channel to Channel Crosstalk

Channel to channel crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

### Charge Injection

Charge injection is a measure of the glitch impulse transferred from injection of the digital input to the analog output during switching.

### -3 dB Bandwidth

-3 dB bandwidth is the frequency at which the output is attenuated by 3 dB.

### On Response

On response is the frequency response of the on switch.

### On Loss

On loss is the loss due to the on resistance of the switch.

### $V_{INL}$

$V_{INL}$  is the maximum input voltage for Logic 0.

### $V_{INH}$

$V_{INH}$  is the minimum input voltage for Logic 1.

### $I_{INL}$ ( $I_{INH}$ )

$I_{INL}$  ( $I_{INH}$ ) is the input current of the digital input.

### $I_{DD}$

$I_{DD}$  is the positive supply current.

### $I_{SS}$

$I_{SS}$  is the negative supply current.

## THEORY OF OPERATION

The ADG798 is a bidirectional, 8:1 CMOS multiplexer designed for very high temperature operation. The device is controlled by four parallel digital inputs (EN, A0, A1, and A2). The EN input allows the ADG798 to be enabled or disabled. When the ADG798 is disabled, the source pins (S1 to S8) disconnect from the drain pin (D). When the ADG798 is enabled, the address lines (A0, A1, and A2) can determine which source pin (S1 to S8) is connected to the drain pin (D).

The low on resistance and on-resistance flatness of this device means that there is minimal signal distortion across the entire signal range of the device. This minimal signal distortion, combined with the close on-resistance match between channels,

makes this device ideal for applications where the error due to on resistance is key. The ADG798 also exhibits extremely fast switching times and extremely low power consumption, making the device useful in applications where there is a tight power budget. The ADG798 is compatible with single-supply systems that have a  $V_{DD}$  range from 5.5 V to 3.3 V and dual-supply systems at  $\pm 2.5$  V.

The ADG798 operates in a wide ambient temperature range from  $-55^{\circ}\text{C}$  to  $+210^{\circ}\text{C}$  (FLATPACK) or  $-55^{\circ}\text{C}$  to  $+175^{\circ}\text{C}$  (TSSOP), making the ADG798 perfect for use in harsh environments that subject the device to extreme temperature ranges, such as downhole drilling and avionics.

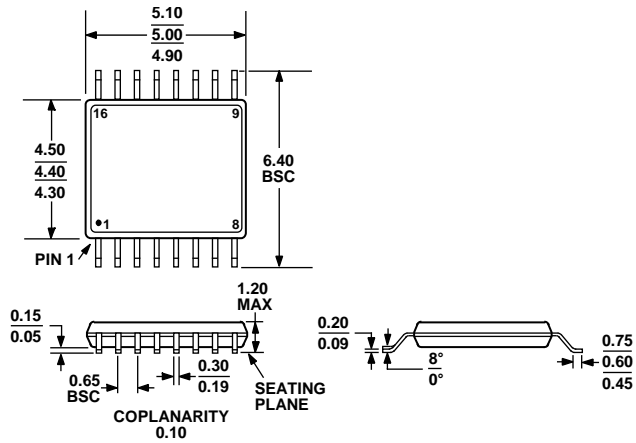
## APPLICATIONS INFORMATION

### POWER SUPPLY SEQUENCING

When using CMOS devices, take care to ensure correct power supply sequencing. Incorrect power supply sequencing may subject the device to stresses beyond the absolute maximum ratings listed in Table 5.

Always apply digital and analog inputs after power supplies and ground. For single-supply operation, tie  $V_{SS}$  to GND as close to the device as possible.

# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 35. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

Dimensions shown in millimeters

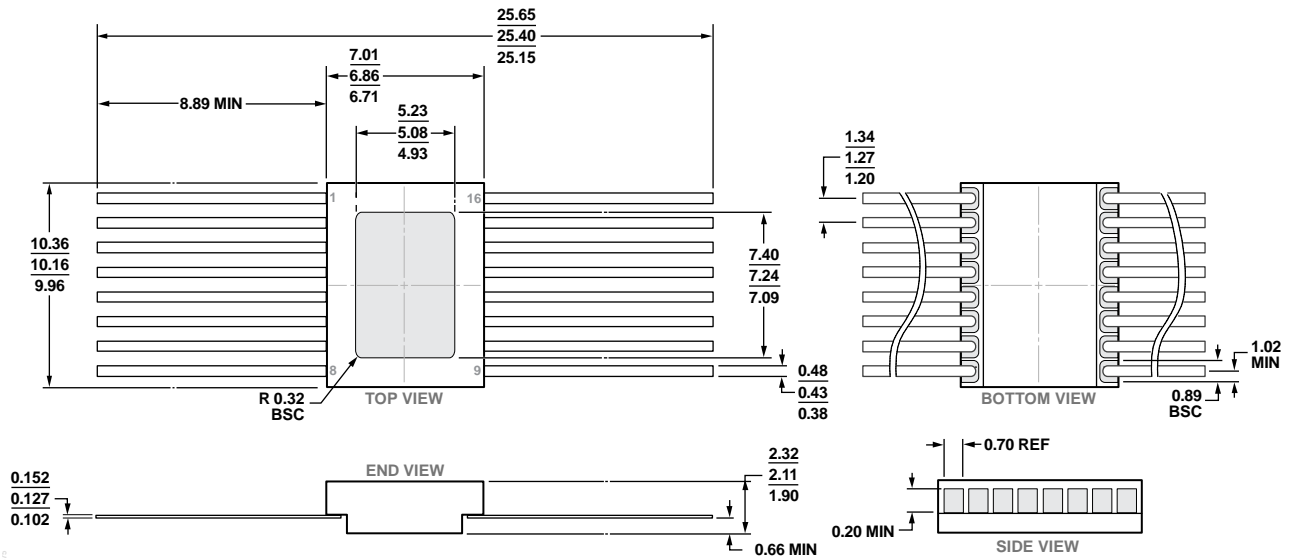


Figure 36. 16-Lead Ceramic Flat Package [FLATPACK] (F-16-1)

Dimensions shown in millimeters

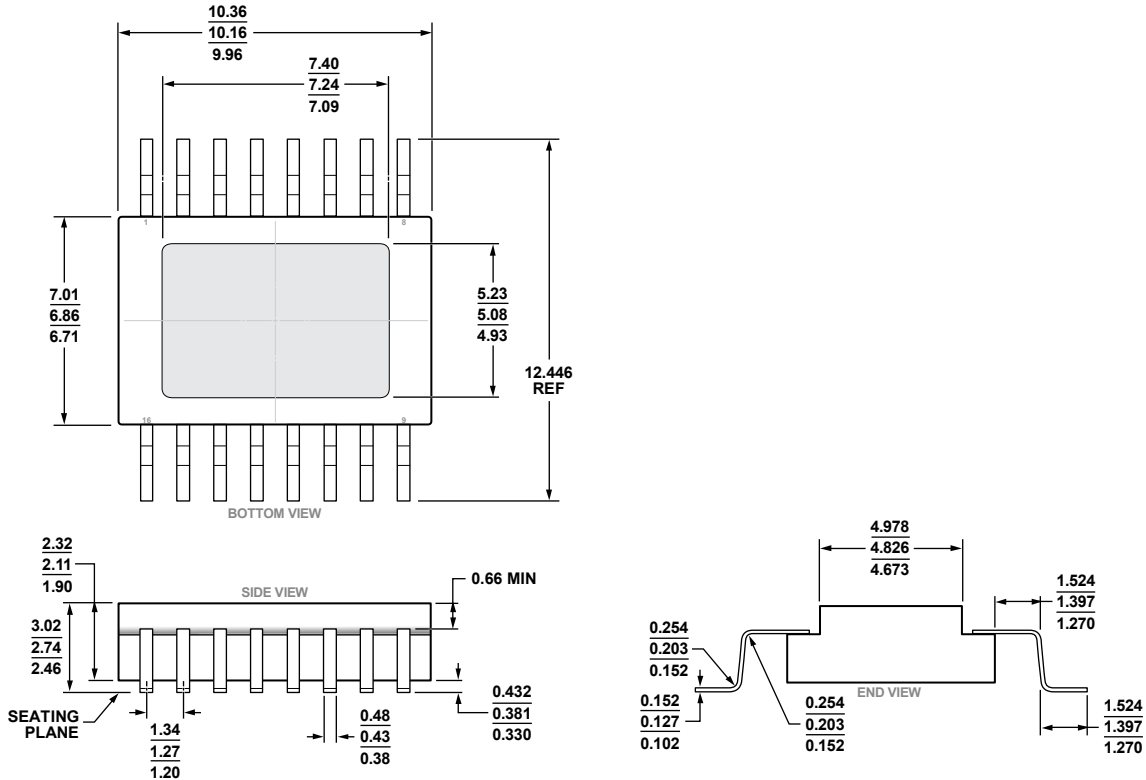


Figure 37. 16-Lead Ceramic Flat Package with Reverse Formed Gullwing Leads [FLATPACK\_RF] Cavity Down (FR-16-1)

Dimensions shown in millimeters

**ORDERING GUIDE**

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADG798HRUZ	-55°C to +175°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG798HFZ	-55°C to +210°C	16-Lead Ceramic Flat Package [FLATPACK]	F-16-1
ADG798HFRZ	-55°C to +210°C	16-Lead Ceramic Flat Package [FLATPACK_RF]	FR-16-1
EVAL-ADG798EB1Z		Evaluation Board	

<sup>1</sup> Z = RoHS Compliant Part.

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