500 kbps, 5.7 kV RMS, Signal Isolated RS-485 Transceiver with ±15 kV IEC ESD

Data Sheet **ADM2461E/ADM2463E**

FEATURES

- **5.7 kV rms, signal isolated RS-485/RS-422 transceiver**
- **Low radiated emissions, passes EN55032 Class B with margin on a 2-layer PCB**
- **Cable inversion smart feature**
  - **Correction for reversed cable connection on A, B, Y, and Z bus pins while maintaining full receiver fail-safe**
- **ESD protection on the RS-485 A, B, Y, and Z bus pins**
  - **≥±12 kV IEC61000-4-2 contact discharge**
  - **≥±15 kV IEC61000-4-2 air discharge**
- **Low speed 500 kbps data rate for EMI control**
- **Flexible power supply inputs**
  - **Primary V_{DD1} supply of 1.7 V to 5.5 V**
  - **Isolated V_{DD2} supply of 3.0 V to 5.5 V**
- **Profibus® compliant for 5 V V_{DD2}**
- **Wide −40°C to +125°C operating temperature range**
- **High common-mode transient immunity: >250 kV/µs**
- **Short-circuit, open-circuit, and floating input receiver fail-safe**
- **Supports 192 bus nodes (72 kΩ receiver input impedance)**
- **Full hot swap support (glitch free power-up and power-down)**
- **Safety and regulatory approvals (pending)**
  - **CSA Component Acceptance Notice 5A, DIN V VDE V 0884-11, UL 1577, CQC11-471543-2012, IEC 61010-1**
- **16-lead, wide body, SOIC_W package with >8.0 mm creepage and clearance in standard pinout**

APPLICATIONS

- **Heating, ventilation, and air conditioning (HVAC) networks**
- **Industrial field buses**
- **Building automation**
- **Utility networks**

FUNCTIONAL BLOCK DIAGRAMS

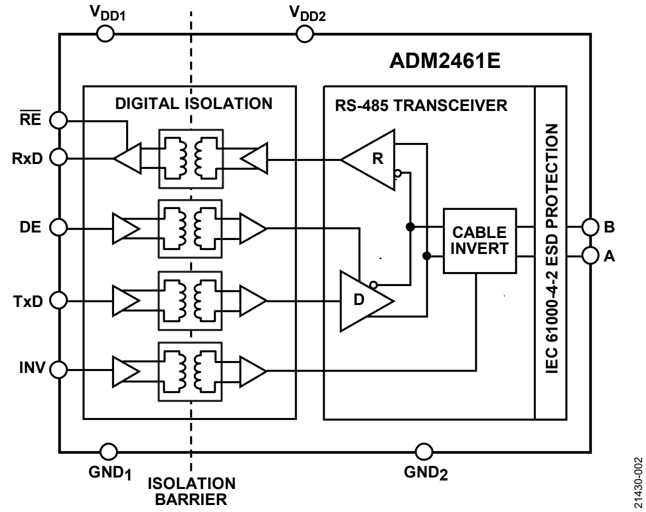

Figure 1. ADM2461E Functional Block Diagram

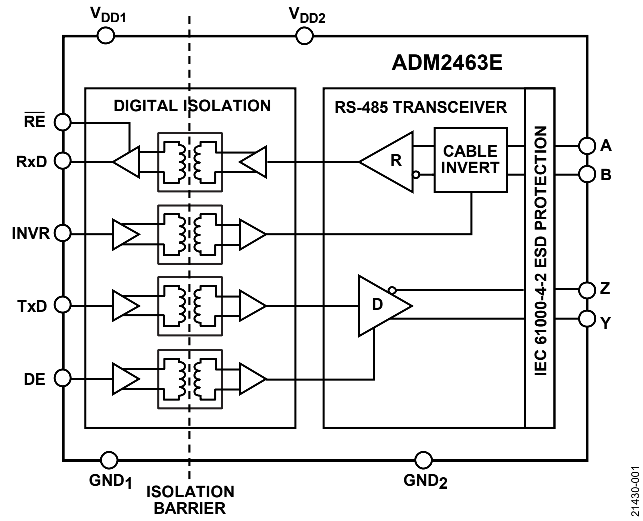

Figure 2. ADM2463E Functional Block Diagram

GENERAL DESCRIPTION

The ADM2461E/ADM2463E are 500 kbps, 5.7 kV rms, signal isolated RS-485 transceivers that pass radiated emissions testing to the EN55032 Class B standard with margin on a 2-layer printed circuit board (PCB). The ADM2461E/ADM2463E isolation barrier provides robust immunity to noise and system level EMC events. The devices are protected against ≥±12 kV contact and ≥ ±15 kV air IEC61000-4-2 electrostatic discharge (ESD) events on the RS-485 A, B, Y, and Z pins. The devices feature cable invert pins to allow quick correction of the reversed cable connection on the A, B, Y, and Z bus pins while maintaining full receiver fail-safe performance.

These devices are optimized for low speed over long cable runs and have a maximum data rate of 500 kbps. The high differential output voltage makes these devices suitable for Profibus nodes when powered with 5 V on the V_{DD2} supply. The V_{DD1} primary supply and V_{DD2} isolated supply both support a wide range of voltages (1.7 V to 5.5 V and 3 V to 5.5 V, respectively). Half-duplex and full duplex device options are available in the industry standard 16-lead, wide-body, standard SOIC_W package with >8.0 mm creepage and clearance.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support **www.analog.com**

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REVISION HISTORY

6/2020—Revision 0: Initial Version

SPECIFICATIONS

All voltages are relative to the respective ground, 1.7 V ≤ V_{DD1} ≤ 5.5 V, 3.0 V ≤ V_{DD2} ≤ 5.5 V, T_A = T_{MIN} (−40°C) to T_{MAX} (+125°C). All minimum and maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.3 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
PRIMARY SIDE SUPPLY CURRENT	$I_{DD1 (Q)}$		0.6	1	mA	DE = 0 V
	I_{DD1}		2	8	mA	DE = V_{DD1}
ISOLATED SIDE SUPPLY CURRENT	$I_{DD2 (Q)}$		5	8	mA	V_{DD2} ≤ 3.6 V, DE = 0 V
			5	8	mA	V_{DD2} ≥ 4.5 V, DE = 0 V
	I_{DD2}		6	9	mA	V_{DD2} ≤ 3.6 V, DE = V_{DD1}
			6	9	mA	V_{DD2} ≥ 4.5 V, DE = V_{DD1}
ISOLATED SIDE DYNAMIC SUPPLY CURRENT	$I_{DD2 (DYN)}$		58	78	mA	V_{DD2} ≤ 3.6 V, load resistance (R_L) = 54 Ω, DE = V_{DD1}, data rate = 500 kbps
			100	145	mA	V_{DD2} ≥ 4.5 V, R_L = 54 Ω, DE = V_{DD1}, data rate = 500 kbps
DRIVER DIFFERENTIAL OUTPUTS						
Differential Output Voltage, Loaded	$\|V_{OD2}\|$	2.0	2.5	V_{DD2}	V	V_{DD2} ≥ 3.0 V, R_L = 100 Ω, see Figure 31
		1.5	2.1	V_{DD2}	V	V_{DD2} ≥ 3.0 V, R_L = 54 Ω, see Figure 31
		2.1	3.3	V_{DD2}	V	V_{DD2} ≥ 4.5 V, R_L = 54 Ω, see Figure 31
Over Common-Mode Range	$\|V_{OD3}\|$	1.5	2.1	V_{DD2}	V	V_{DD2} ≥ 3.0 V, −7 V ≤ common-mode voltage (V_{CM}) ≤ +12 V, see Figure 32
		2.1	3.3	V_{DD2}	V	V_{DD2} ≥ 4.5 V, −7 V ≤ V_{CM} ≤ +12 V, see Figure 32
Δ$\|V_{OD2}\|$ for Complementary Output States	Δ$\|V_{OD2}\|$			0.2	V	R_L = 54 Ω or 100 Ω, see Figure 31
Common-Mode Output Voltage	V_{OC}		1.5	3.0	V	R_L = 54 Ω or 100 Ω, see Figure 31
Δ$\|V_{OC}\|$ for Complementary Output States	Δ$\|V_{OC}\|$			0.2	V	R_L = 54 Ω or 100 Ω, see Figure 31
Short-Circuit Output Current	I_{OS}	−250		+250	mA	−7 V < output voltage (V_{OUT}) < +12 V
Output Leakage Current (Y, Z)[1]	I_O		1	50	µA	DE = $\overline{RE}$ = 0 V, V_{DD2} = 0 V or 5.5 V, input voltage (V_{IN}) = 12 V
		−50	+10		µA	DE = $\overline{RE}$ = 0 V, V_{DD2} = 0 V or 5.5 V, V_{IN} = −7 V
Pin Capacitance (A, B, Y, Z)	C_{IN}		28		pF	V_{IN} = 0.4sin(10πt × 10^6)
RECEIVER DIFFERENTIAL INPUTS						
Differential Input Threshold Voltage, Noninverted	V_{TH}	−200	−125	−30	mV	−7 V < V_{CM} < +12 V, INV or INVR = 0 V
Differential Input Threshold Voltage, Inverted		30	125	200	mV	−7 V < V_{CM} < +12 V, INV or INVR = V_{DD1}
Input Voltage Hysteresis	V_{HYS}		25		mV	−7 V < V_{CM} < +12 V
Input Current (A, B)	I_I			167	µA	DE = 0 V, V_{DD2} = 0 V or 5.5 V, V_{IN} = 12 V
		−133			µA	DE = 0 V, V_{DD2} = 0 V or 5.5 V, V_{IN} = −7 V
Pin Capacitance (A, B)	C_{IN}		4		pF	V_{IN} = 0.4sin(10πt × 10^6)
DIGITAL LOGIC INPUTS						
Input Low Voltage	V_{IL}			0.3 × V_{DD1}	V	DE, $\overline{RE}$, TxD, INV, INVR
Input High Voltage	V_{IH}	0.7 × V_{DD1}			V	DE, $\overline{RE}$, TxD, INV, INVR
Input Current	I_I	−2	+0.01	+2	µA	DE, $\overline{RE}$, TxD, V_{IN} = 0 V or V_{DD1}
		−2	+10	+30	µA	INV, INVR, V_{IN} = 0 V or V_{DD1}
RxD DIGITAL OUTPUT						
Output Voltage Low	V_{OL}			0.4	V	V_{DD1} = 3.6 V, output current (I_{OUT}) = 2.0 mA, differential input voltage (V_{ID}) ≤ −0.2 V
				0.4	V	V_{DD1} = 2.7 V, I_{OUT} = 1.0 mA, V_{ID} ≤ −0.2 V
				0.2	V	V_{DD1} = 1.95 V, I_{OUT} = 500 µA, V_{ID} ≤ −0.2 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Output Voltage High	V_{OH}	2.4			V	V_{DD1} = 3.0 V, I_{OUT} = −2.0 mA, V_{ID} ≥ −0.03 V
		2.0			V	V_{DD1} = 2.3 V, I_{OUT} = −1.0 mA, V_{ID} ≥ −0.03 V
		V_{DD1} − 0.2			V	V_{DD1} = 1.7 V, I_{OUT} = −500 µA, V_{ID} ≥ −0.03 V
Short-Circuit Current				100	mA	V_{OUT} = GND_1 or V_{DD1}, $\overline{RE}$ = 0 V
Three-State Output Leakage Current	I_{OZR}	−1	+0.01	+1	µA	$\overline{RE}$ = V_{DD1}, RxD = 0 V or V_{DD1}
COMMON-MODE TRANSIENT IMMUNITY (CMTI)[2]		250			kV/µs	V_{CM} ≥ ±1 kV, transient magnitude measured between 20% and 80% of V_{CM}, see Figure 37 and Figure 38

[1] ADM2463E only.
[2] The CMTI is the maximum common-mode voltage slew rate that can be sustained while maintaining specification compliant operation. V_{CM} is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common mode is slewed. The common-mode voltage slew rates apply to rising and falling common-mode voltage edges.

TIMING SPECIFICATIONS

V_{DD1} = 1.7 V to 5.5 V, V_{DD2} = 3.0 V to 5.5 V, T_A = T_{MIN} (−40°C) to T_{MAX} (+125°C), unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.3 V, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						
Maximum Data Rate		500			kbps	
Propagation Delay	t_{DPLH}, t_{DPHL}		230	400	ns	R_L = 54 Ω, C_L = 100 pF, see Figure 33 and Figure 3.
Output Skew	t_{SKEW}		3	100	ns	R_L = 54 Ω, C_L = 100 pF, see Figure 33 and Figure 3.
Rise Time and Fall Time	t_{DR}, t_{DF}	200	400	800	ns	R_L = 54 Ω, C_L = 100 pF, see Figure 33 and Figure 3.
Enable Time	t_{ZL}, t_{ZH}		150	1000	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 34 and Figure 5.
Disable Time	t_{LZ}, t_{HZ}		1700	2200	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 34 and Figure 5.
RECEIVER						
Propagation Delay	t_{RPLH}, t_{RPHL}		30	200	ns	C_L = 15 pF, see Figure 35 and Figure 4.
Output Skew	t_{SKEW}		2.5	50	ns	C_L = 15 pF, see Figure 35 and Figure 4.
Enable Time	t_{ZL}, t_{ZH}		3	50	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 36 and Figure 6.
Disable Time	t_{LZ}, t_{HZ}		8	50	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 36 and Figure 6.
RECEIVER CABLE INVERT (INVR, INV)						
Propagation Delay	$t_{INVRPHL}$, $t_{INVRPLH}$		20	40	ns	V_{ID} ≥ −200 mV or V_{ID} ≤ +200 mV, see Figure 7.
DRIVER CABLE INVERT (INV)						
Propagation Delay	$t_{INVDPHL}$, $t_{INVDPLH}$		230	400	ns	TxD = 0 V or TxD = V_{DD1}, see Figure 8.

Timing Diagrams

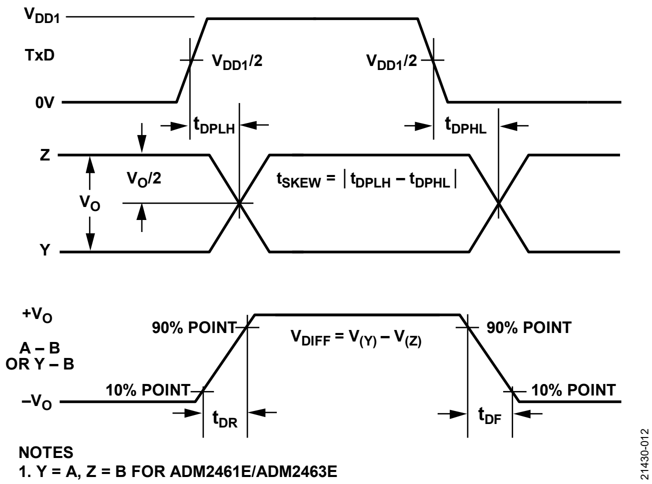

Figure 3. Driver Propagation Delay, Rise and Fall Timing

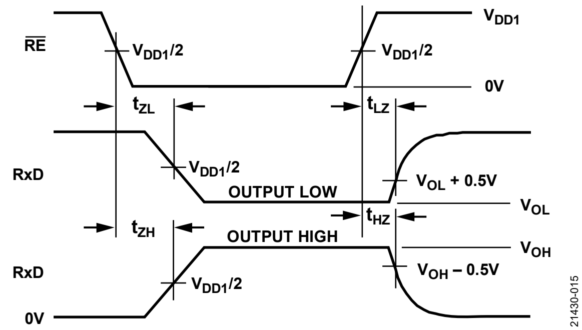

Figure 6. Receiver Enable or Disable Timing

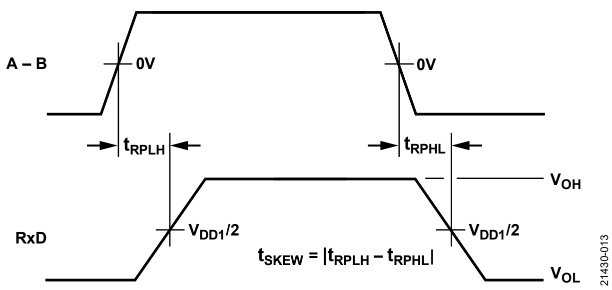

Figure 4. Receiver Propagation Delay

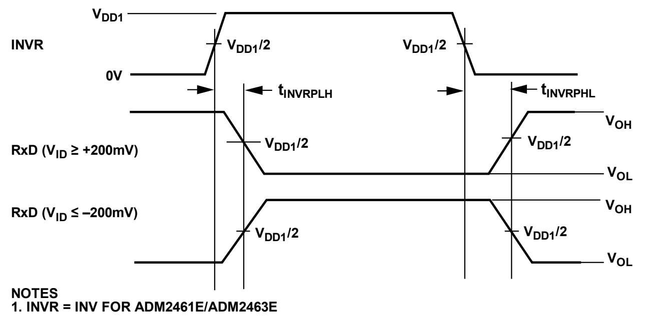

Figure 7. Receiver Cable Invert Timing Specification Measurement

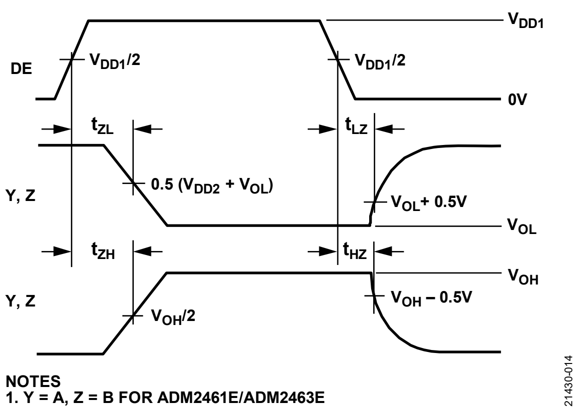

Figure 5. Driver Enable or Disable Timing

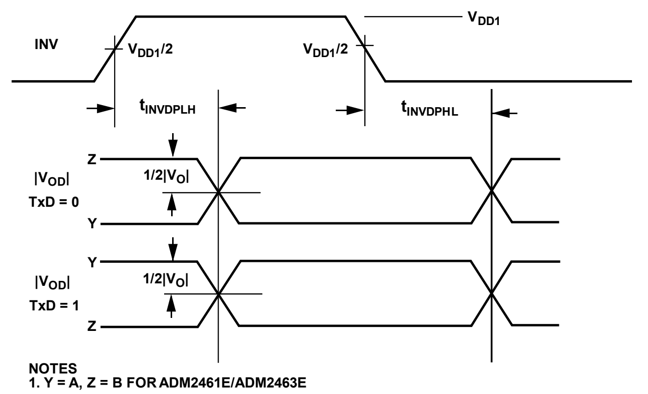

Figure 8. Driver Cable Invert Timing Specification Measurement

PACKAGE CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	Test frequency = 1 MHz
Input Capacitance[2]	C_I		3.0		pF	

[1] The device is considered a 2-terminal device. Short together Pin 1 through Pin 8 and short together Pin 9 through Pin 16 to set the device up as a 2-terminal device during testing.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

For additional information, see www.analog.com/icouplersafety.

Table 4. ADM2461E/ADM2463E Approvals

UL (Pending)	CSA (Pending)	VDE (Pending)	CQC (Pending)
Recognized Under UL 1577 Component Recognition Protection[1]	Approved under CSA Component Acceptance Notice 5A	To be certified under DIN V VDE 0884-11[2]	Certified under CQC11-471543-2012
Single Protection, 5700 V rms	CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2	Basic insulation	GB4943.1-2011
	Basic insulation at 800 V rms (1131 V peak)	Working voltage (V_{IOWM}) = 875 V rms	Basic insulation at 800 V rms (1131 V peak)
	Reinforced insulation at 400 V rms (565 V peak)	Repetitive maximum voltage (V_{IORM}) = 1237 V peak	Reinforced insulation at 400 V rms (565 V peak)
	CSA 62368-1-14, EN 62368-1:2014/A11:2017 and IEC 62368-1: 2014 second edition	Surge isolation voltage (V_{IOSM}) = 10 kV peak	
	Basic insulation at 800 V rms (1131 V peak)	Highest allowable overvoltage (V_{IOTM}) = 8000 V peak	
	Reinforced insulation at 400 V rms (565 V peak)	Reinforced insulation	
	IEC 60601-1 Edition 3.1	V_{IOWM} = 750 V rms	
	1 means of patient protection (1 MOPP), 400 V rms (565 V peak)	V_{IORM} = 1060 V peak	
	2 MOPP, 250 V rms (353 V peak)	V_{IOSM} = 6.25 kV peak	
	1 MOPP or 2 MOPP, 400 V rms (565 V peak)	V_{IOTM} = 8000 V peak	
	CSA 61010-1-12 and IEC 61010-1 third edition		
	Basic insulation at 300 V rms mains, 800 V rms (1131 V peak) from secondary circuit		
	Reinforced insulation at 300 V rms mains, 400 V rms (565 V peak) from secondary circuit		
File (pending)	File (pending)	File (pending)	File (pending)

[1] In accordance with UL 1577, each ADM2461E/ADM2463E is proof tested by applying an insulation test voltage ≥ 6840 V rms for 1 sec.
[2] In accordance with DIN V VDE 0884-11, each ADM2461E/ADM2463E is proof tested by applying an insulation test voltage ≥ 2320 V peak for 1 sec (partial discharge detection limit = 5 pC).

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 5. Critical Safety Related Dimensions and Material Properties

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5700	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8.3	mm	Measured from input terminals to output terminals, shortest distance along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	8.1	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		43	μm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN IEC 112/VDE 0303 Part 1
Material Group		I		Material Group (DIN VDE 0110: 1989-01, Table 1)

DIN V VDE 0884-11 (VDE 0884-11) INSULATION CHARACTERISTICS (PENDING)

The ADM2461E/ADM2463E are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data must be ensured by means of protective circuits.

Table 6.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
CLASSIFICATIONS				
Installation Classification per DIN VDE 0110 for Rated Mains Voltage				
≤600 V rms	Reinforced insulation		I to IV	
≤750 V rms	Reinforced insulation		I to III	
≤875 V rms	Basic insulation		I to IV	
Climatic Classification			40/125/21	
Pollution Degree	DIN VDE 0110, see Table 1		2	
VOLTAGE				
Maximum Working Insulation Voltage	Basic insulation	V_{IOWM}	875	V rms
	Reinforced insulation		750	V rms
Maximum Repetitive Peak Insulation Voltage	Basic insulation	V_{IORM}	1237	V peak
	Reinforced insulation		1060	V peak
Maximum DC Working Insulation Voltage	Basic insulation	$V_{IOWM (DC)}$	1237	V dc
	Reinforced insulation		1060	V dc
Input to Output Test Voltage		V_{PR}		
Method b1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production tested, $t_m = 1$ sec, partial discharge < 5 pC		2320	V peak
Method a				
After Environmental Tests, Subgroup 1	$V_{IORM} \times 1.5 = V_{pd}(m)$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1856	V peak
After Input and/or Safety Test, Subgroup 2/Subgroup 3	$V_{IORM} \times 1.2 = V_{pd}(m)$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1485	V peak
Highest Allowable Overvoltage	Transient overvoltage, $t_{TR} = 10$ sec	V_{IOTM}	8000	V peak
Surge Isolation Voltage, Basic	Peak voltage (V_{PEAK}) = 10 kV, 1.2 μs rise time, 50 μs, 50% fall time	V_{IOSM}	10,000	V peak
Surge Isolation Voltage, Reinforced	V_{PEAK} = 10 kV, 1.2 μs rise time, 50 μs, 50% fall time	V_{IOSM}	6250	V peak
SAFETY-LIMITING VALUES	Maximum value allowed in the event of a failure			
Case Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	1.95	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	>10^9	Ω

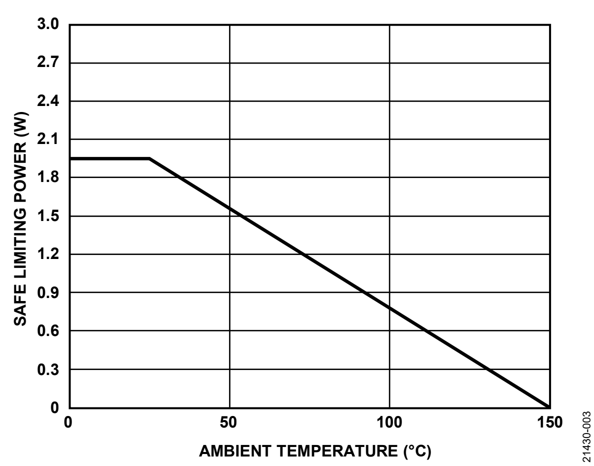

Figure 9. Thermal Derating Curve for 16-Lead, Standard, Wide Body SOIC_W, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-10

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. All voltages are relative to the respective ground.

Table 7.

Parameter	Rating
V_{DD1} to GND_1	−0.5 V to +7 V
V_{DD2} to GND_2	−0.5 V to +7 V
Digital Input Voltage (DE, $\overline{RE}$, TxD, INV, and INVR)	−0.3 V to V_{DD1} + 0.3 V
Digital Output Voltage (RxD)	−0.3 V to V_{DD1} + 0.3 V
Driver Output/Receiver Input Voltage (A, B, Y, and Z)	−9 V to +14 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature	
Soldering (10 sec)	260°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

Table 8. Thermal Resistance

Package Type	θ_{JA}	Unit
RW-16[1]	63.9	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no bias. See JEDEC JESD-51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

International Electrotechnical Commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2.

ESD Ratings for ADM2461E/ADM2463E

Table 9. ADM2461E/ADM2463E, 16-Lead SOIC_W

ESD Model	Withstand Threshold (V)	Class
HBM	±4000	3A
CDM	±1250	C5
IEC[1]	≥±12,000 (contact discharge) to GND_2	Level 4
	≥±15,000 (air discharge) to GND_2	Level 4
	≥±8,000 (contact/air discharge) to GND_1	Level 4[2]

[1] Pin A, Pin B, Pin Y, and Pin Z only.
[2] Limited by clearance across isolation barrier.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 10. Maximum Continuous Working Voltage[1, 2]

Parameter	Max	Unit	Reference Standard
AC Voltage (Bipolar)			
Basic Insulation	1237	V peak	50-year minimum lifetime
Reinforced Insulation	1060	V peak	50-year minimum lifetime
AC Voltage (Unipolar)			
Basic Insulation	2474	V peak	50-year minimum lifetime
Reinforced Insulation	1355	V peak	Lifetime limited by package creepage per IEC60664-1
DC Voltage			
Basic Insulation	1237	V dc	50-year minimum lifetime
Reinforced Insulation	830	V dc	Lifetime limited by package creepage per IEC60664-1

[1] The maximum continuous working voltage refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.
[2] Values are quoted for Material Group I, Pollution Degree II.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

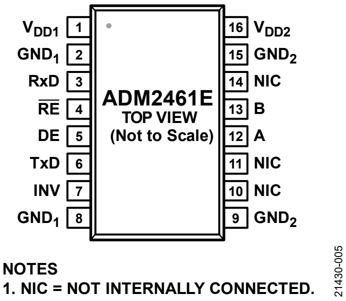

Figure 10. ADM2461E Half-Duplex Pin Configuration

Table 11. ADM2461E Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	1.7 V to 5.5 V Flexible Primary Side Power Supply. Connect a 0.1 µF decoupling capacitor between Pin 1 and Pin 2 to decouple the two supplies. An additional 10 µF decoupling capacitor can be connected between Pin 1 and Pin 2 to improve noise immunity in noisy environments.
2, 8	GND_1	Ground 1, Logic Side.
3	RxD	Receiver Output Data. When the INV pin is logic low, this output is high when A − B ≥ −30 mV and low when A − B ≤ −200 mV. When the INV pin is logic high, this output is high when A − B ≤ 30 mV and low when A − B ≥ 200 mV. When the $\overline{RE}$ pin is driven high, the receiver disables and this output is tristated.
4	$\overline{RE}$	Receiver Enable Input. This pin is an active low input. Drive this input low to enable the receiver. Drive this input high to disable the receiver.
5	DE	Driver Output Enable. A high level on this pin enables the driver differential outputs, A and B. A low level on this pin places the outputs in a high impedance state.
6	TxD	Transmit Data Input. Data to be transmitted by the driver is applied to this input. When the INV pin is logic high, the data applied to this input is inverted.
7	INV	Cable Invert Input. This pin is an active high input. Drive this pin high to invert the TxD signal applied and invert the A and B receiver inputs to correct for reversed cable installation. This pin is pulled internally to ground through a high impedance. If the cable invert function is not used, connect this pin to GND_1.
9, 15	GND_2	Isolated Ground 2 for the Integrated RS-485 Transceiver, Bus Side.
10, 11, 14	NIC	Not Internally Connected.
12	A	Driver Noninverting Output/Receiver Noninverting Input.
13	B	Driver Inverting Output/Receiver Inverting Input.
16	V_{DD2}	3.0 V to 5.5 V Isolated Side Power Supply. Connect a decoupling capacitor of 0.1 µF between Pin 16 and Pin 15 to decouple the two supplies. An additional 10 µF decoupling capacitor can be connected between Pin 16 and Pin 15 to improve noise immunity in noisy environments.

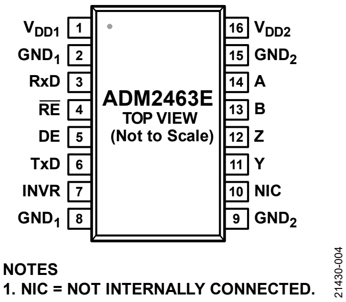

Figure 11. ADM2463E Full Duplex Pin Configuration

Table 12. ADM2463E Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	1.7 V to 5.5 V Flexible Primary Side Power Supply. Connect a 0.1 µF decoupling capacitor between Pin 1 and Pin 2 to decouple the two supplies. An additional 10 µF decoupling capacitor can be connected between Pin 1 and Pin 2 to improve noise immunity in noisy environments.
2, 8	GND_1	Ground 1, Logic Side.
3	RxD	Receiver Output Data. When the INVR pin is logic low, this output is high when the differential receiver input voltage (A – B) ≥ −30 mV and low when A – B ≤ −200 mV. When the INVR pin is logic high, this output is high when A – B ≤ 30 mV and low when A – B ≥ 200 mV. When the $\overline{RE}$ pin is driven high, the receiver disables and this output is tristated.
4	$\overline{RE}$	Receiver Enable Input. This pin is an active low input. Drive this input low to enable the receiver. Drive this input high to disable the receiver.
5	DE	Driver Output Enable. A high level on this pin enables the driver differential outputs, Y and Z. A low level on this pin places the outputs in a high impedance state.
6	TxD	Transmit Data Input. Data to be transmitted by the driver is applied to this input.
7	INVR	Receiver Cable Invert Input. This pin is an active high input. Drive this pin high to invert the A and B receiver inputs to correct for reversed cable installation. This pin is pulled internally to ground through a high impedance. If the cable invert function is not used, connect this pin to GND_1.
9, 15	GND_2	Isolated Ground 2 for the Integrated RS-485 Transceiver, Bus Side.
10	NIC	Not Internally Connected.
11	Y	Driver Noninverting Output.
12	Z	Driver Inverting Output.
13	B	Receiver Inverting Input.
14	A	Receiver Noninverting Input.
16	V_{DD2}	3.0 V to 5.5 V Isolated Side Power Supply. Connect a decoupling capacitor of 0.1 µF between Pin 16 and Pin 15 to decouple the two supplies. An additional 10 µF decoupling capacitor can be connected between Pin 16 and Pin 15 to improve noise immunity in noisy environments.

TYPICAL PERFORMANCE CHARACTERISTICS

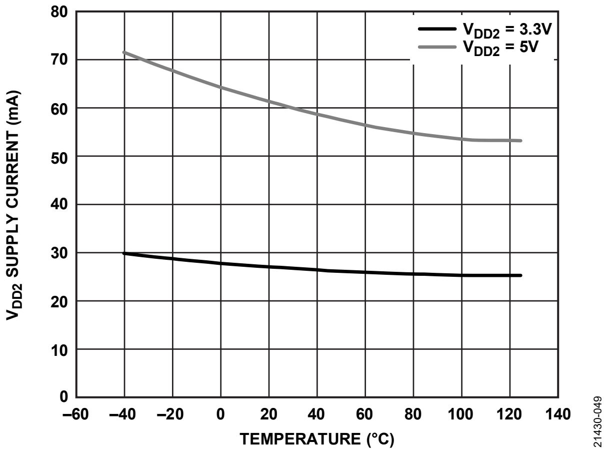

Figure 12. V_{DD2} Supply Current vs. Temperature, Data Rate = 500 kbps, No Load

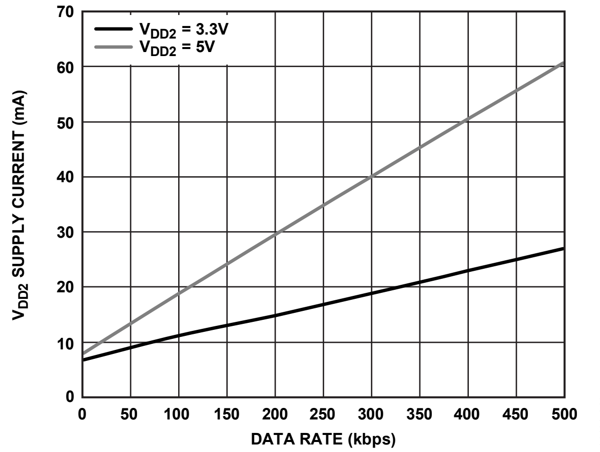

Figure 15. V_{DD2} Supply Current vs. Data Rate, T_A = 25°C, No Load

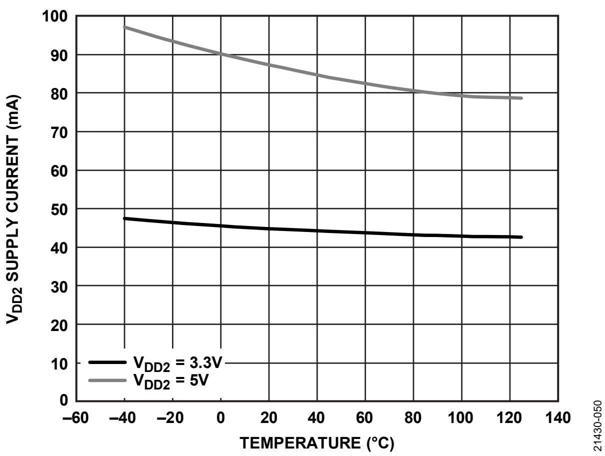

Figure 13. V_{DD2} Supply Current vs. Temperature, Data Rate = 500 kbps, R_L = 120 Ω

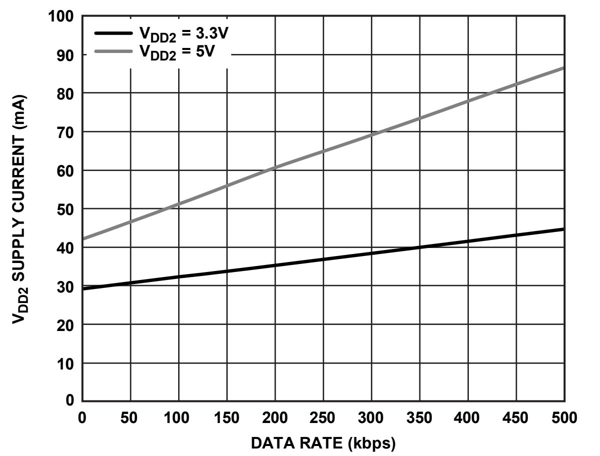

Figure 16. V_{DD2} Supply Current vs. Data Rate, T_A = 25°C, R_L = 120 Ω

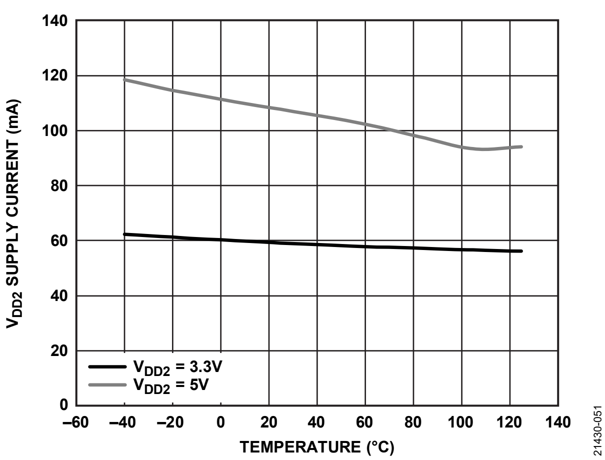

Figure 14. V_{DD2} Supply Current vs. Temperature, Data Rate = 500 kbps, R_L = 54 Ω

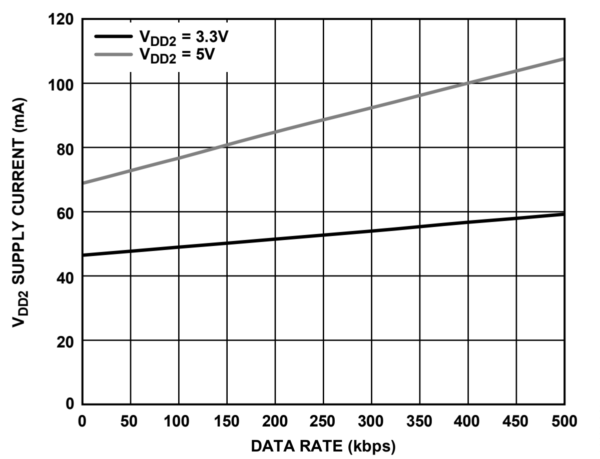

Figure 17. V_{DD2} Supply Current vs. Data Rate, T_A = 25°C, R_L = 54 Ω

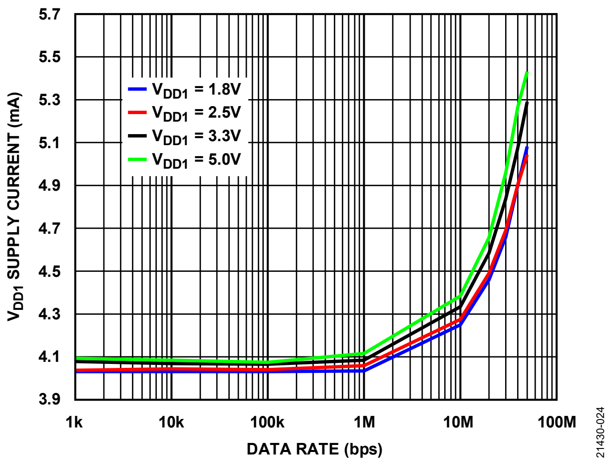

Figure 18. V_{DD1} Supply Current vs. Data Rate

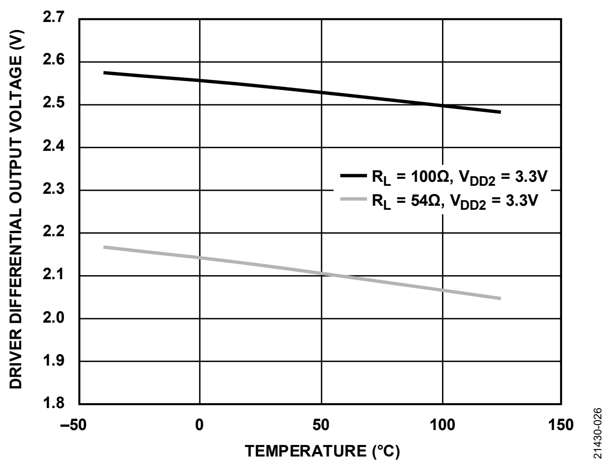

Figure 19. Driver Differential Output Voltage vs. Temperature

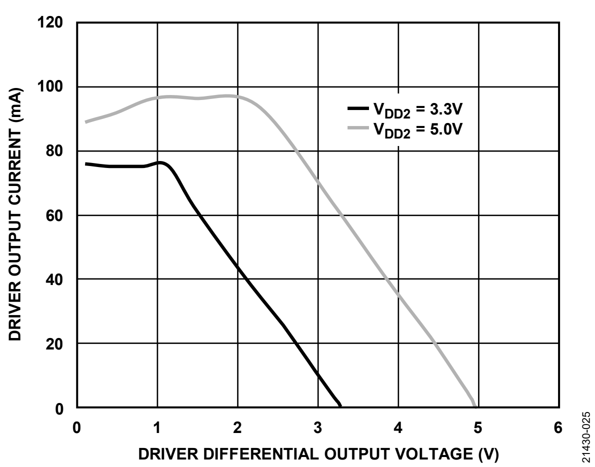

Figure 20. Driver Output Current vs. Driver Differential Output Voltage

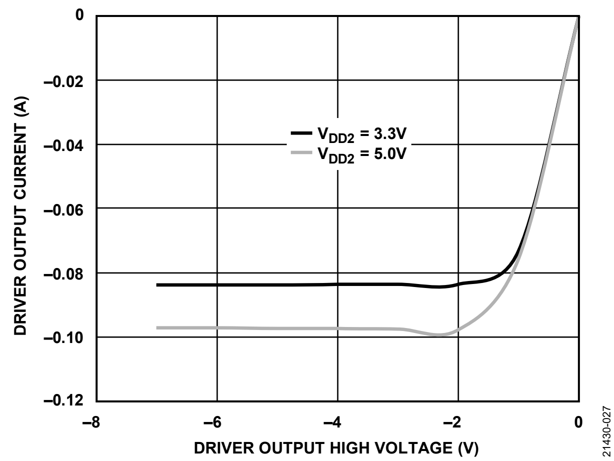

Figure 21. Driver Output Current vs. Driver Output High Voltage

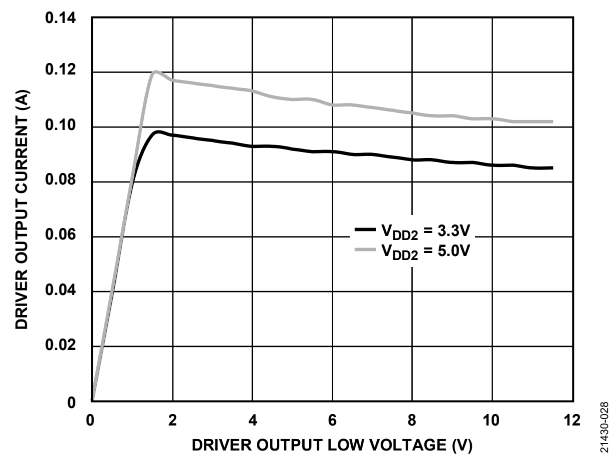

Figure 22. Driver Output Current vs. Driver Output Low Voltage

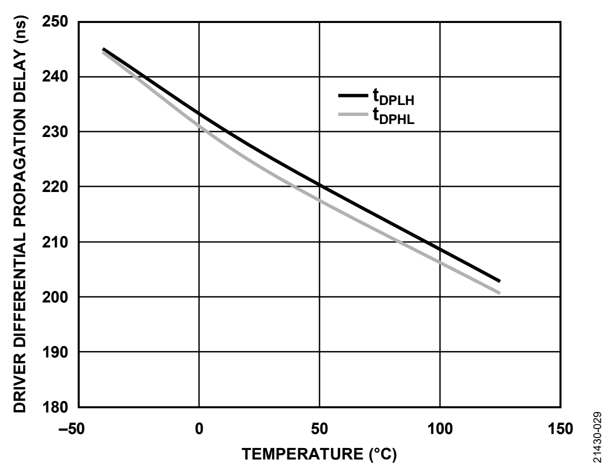

Figure 23. Driver Differential Propagation Delay vs. Temperature

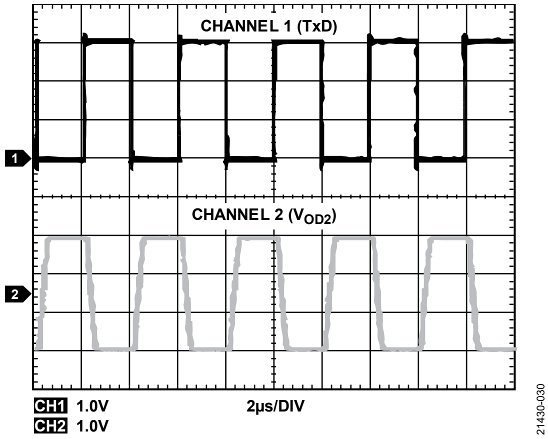

Figure 24. Driver Switching at 500 kbps

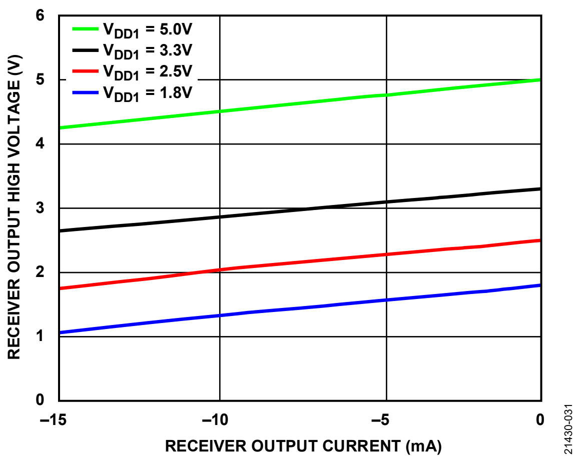

Figure 25. Receiver Output High Voltage vs. Receiver Output Current

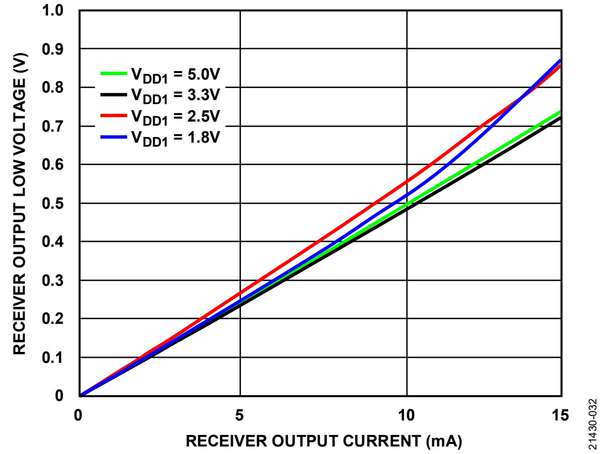

Figure 26. Receiver Output Low Voltage vs. Receiver Output Current

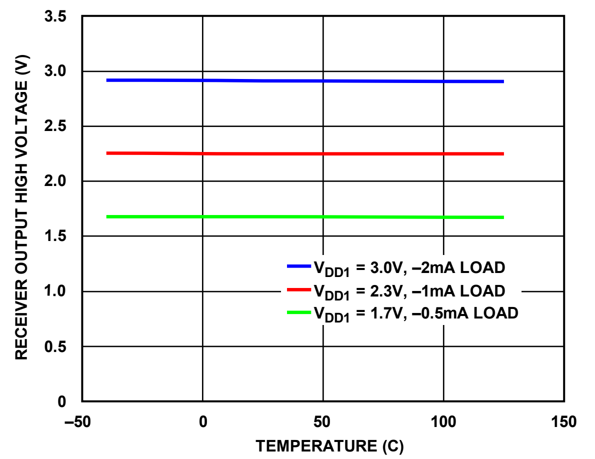

Figure 27. Receiver Output High Voltage vs. Temperature

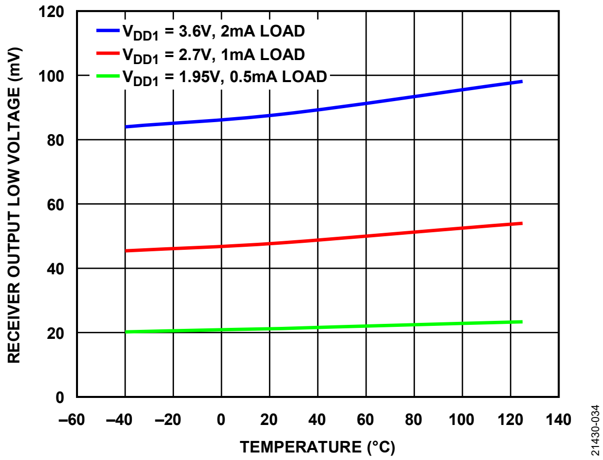

Figure 28. Receiver Output Low Voltage vs. Temperature

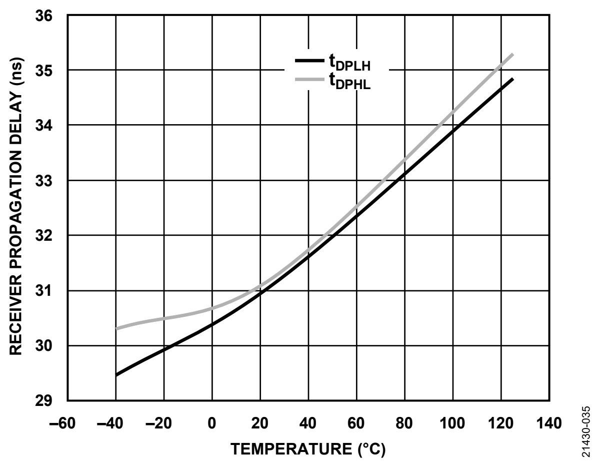

Figure 29. Receiver Propagation Delay vs. Temperature

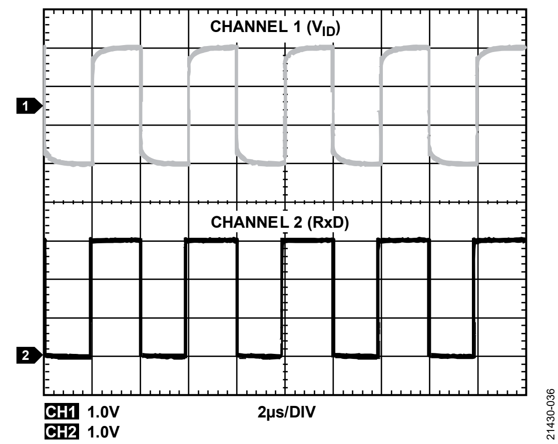

Figure 30. Receiver Switching at 500 kbps

TEST CIRCUITS AND SWITCHING CHARACTERISTICS

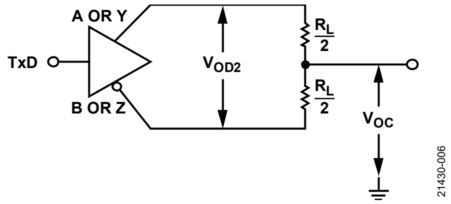

Figure 31. Driver Voltage Measurement, $|V_{OD2}|$

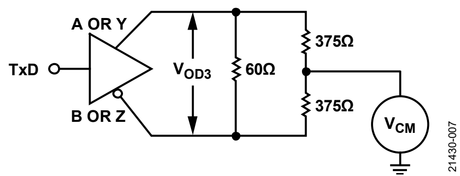

Figure 32. Driver Voltage Measurement over Common-Mode Range, $|V_{OD3}|$

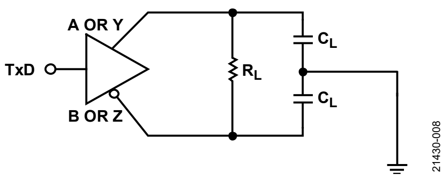

Figure 33. Driver Propagation Delay Measurement (See Figure 3 for Timing Diagram)

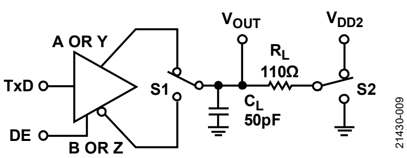

Figure 34. Driver Enable or Disable Time Measurement (See Figure 5 for Timing Diagram)

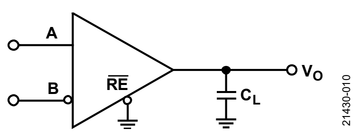

Figure 35. Receiver Propagation Delay Time Measurement (See Figure 4 for Timing Diagram)

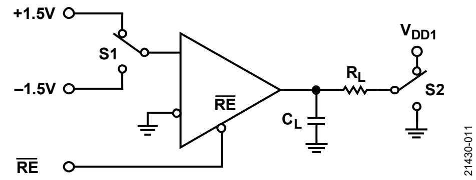

Figure 36. Receiver Enable or Disable Time Measurement (See Figure 6 for Timing Diagram)

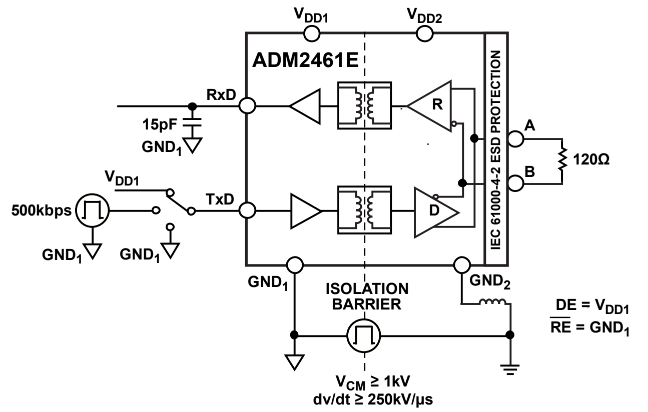

Figure 37. CMTI Test Diagram, Half-Duplex

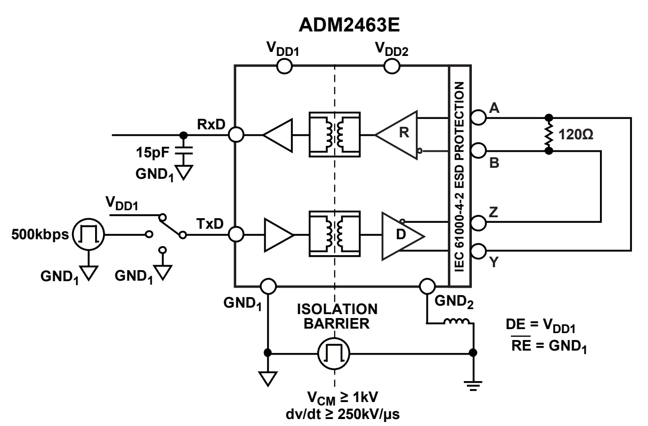

Figure 38. CMTI Test Diagram, Full Duplex

THEORY OF OPERATION

ROBUST LOW POWER DIGITAL ISOLATOR

The ADM2461E/ADM2463E feature a low power, digital isolator block to galvanically isolate the primary and secondary sides of the device. The use of coplanar transformer coils with an on or off keying modulation scheme allows high data throughput across the isolation barrier while minimizing any radiated emissions. This architecture provides a robust digital isolator with immunity to common-mode transients >250 kV/µs across the full temperature and supply range of the device. The digital isolator circuitry features a flexible V_{DD1} power supply with an input voltage range of 1.7 V to 5.5 V.

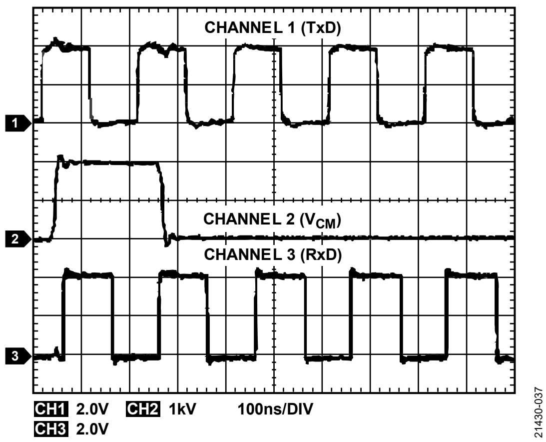

Figure 39. Switching Correctly in the Presence of >250 kV/µs Common-Mode Transients

HIGH DRIVER DIFFERENTIAL OUTPUT VOLTAGE

The ADM2461E/ADM2463E feature a proprietary transmitter architecture with a low driver output impedance that results in an increased differential output voltage. This architecture is useful when operating the device at lower data rates over long cable runs where the dc resistance of the transmission line dominates the signal attenuation. In these applications, the increased differential voltage extends the reach of the device to longer cable lengths. When operated as a 5 V transceiver (V_{DD2} > 4.5 V), the ADM2461E/ADM2463E meet or exceed the Profibus requirement of a minimum 2.1 V differential output voltage.

IEC61000-4-2 ESD PROTECTION

ESD is the sudden transfer of electrostatic charge between bodies at different potentials, which is either caused by near contact or induced by an electric field. ESD has the characteristics of a high current in a short time period. The primary purpose of the IEC61000-4-2 test is to determine system immunity to external ESD events outside the system during operation. IEC61000-4-2 describes testing using two coupling methods: contact discharge and air discharge. Contact discharge implies a direct contact between the discharge gun and the equipment under test (EUT). During air discharge testing, the charged electrode of the discharge gun is moved toward the EUT until a discharge occurs as an arc across the air gap. The discharge gun does not make direct contact with the EUT during air discharge testing. Factors including humidity, temperature, barometric pressure, distance, and rate of approach to the EUT affect the results and repeatability of the air discharge test. Air discharge testing is a more accurate representation of an actual ESD event than the contact discharge method but is not as repeatable. Therefore, contact discharge is the preferred test method. During testing, the EUT data port is subjected to at least 10 positive and 10 negative single discharges. Test voltage selection depends on the system end environment. Figure 40 shows the 8 kV contact discharge current waveform, as described in the IEC61000-4-2 specification. Waveform parameters include rise times of <1 ns and pulse widths of ~60 ns.

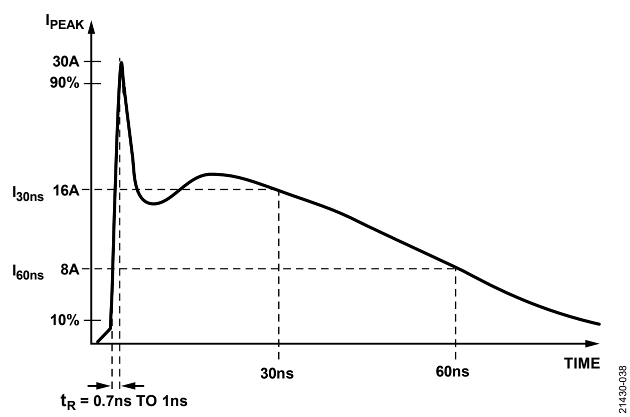

Figure 40. IEC61000-4-2 ESD Waveform (8 kV)

Figure 41 shows the 8 kV contact discharge current waveform from the IEC61000-4-2 standard compared to the HBM ESD 8 kV waveform. Figure 41 shows that the two standards specify a different waveform shape and peak current (I_{PEAK}). The I_{PEAK} associated with an IEC61000-4-2 8 kV pulse is 30 A, whereas the corresponding I_{PEAK} for HBM ESD is more than five times less at 5.33 A. The other key difference between the two standards is the rise time of the initial voltage spike. The IEC61000-4-2 ESD waveform has a faster rise time of 1 ns compared to the 10 ns associated with the HBM ESD waveform. The amount of power associated with an IEC ESD waveform is greater than that of an HBM ESD waveform. The HBM ESD standard requires the EUT to be subjected to at least three positive and three negative discharge tests, whereas the IEC ESD standard requires the EUT to be subjected to at least 10 positive and 10 negative discharge tests.

The ADM2461E/ADM2463E are rated to ≥±12 kV contact ESD protection and ≥±15 kV air ESD protection between the RS-485 bus pins (A, B, Y, and Z) and the GND_2 pin according to the IEC61000-4-2 standard. The isolation barrier provides ±8kV contact protection between the bus pins and the GND_1 pin. These devices with IEC61000-4-2 ESD ratings are better suited for operation in harsh environments when compared to other RS-485 transceivers that state varying levels of HBM ESD protection.

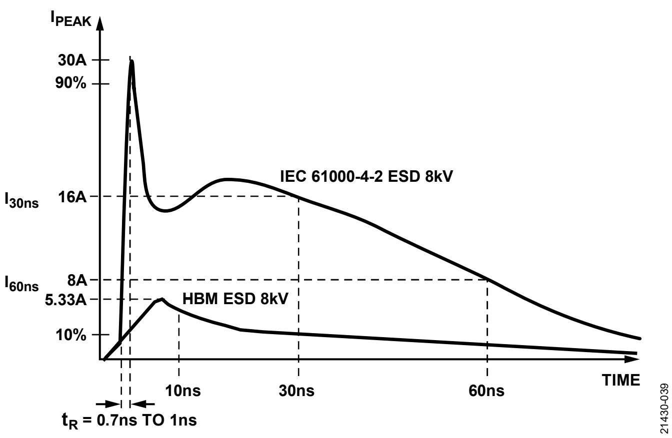

Figure 41. IEC61000-4-2 ESD 8 kV Waveform Compared to HBM ESD 8 kV Waveform

TRUTH TABLES

Table 14 and Table 15 use the abbreviations defined in Table 13. V_{DD1} supplies the DE, TxD, $\overline{RE}$, RxD, INV, and INVR pins only.

Table 13. Truth Table Abbreviations

Letter	Description
H	High level
I	Indeterminate
L	Low level
X	Any state
Z	High impedance (off)

Table 14. Transmitting Truth Table

Supply Status		Inputs			Outputs	
V_{DD1}	V_{DD2}	DE	TxD	INV	A or Y	B or Z
On	On	H	H	L	H	L
On	On	H	H	H	L	H
On	On	H	L	L	L	H
On	On	H	L	H	H	L
On	On	L	X	X	Z	Z
Off	On	X	X	X	Z	Z
X	Off	X	X	X	Z	Z

Table 15. Receiving Truth Table

Supply Status		Inputs			Outputs
V_{DD1}	V_{DD2}	A − B	INV or INVR	$\overline{RE}$	RxD
On	On	≥−0.03 V	L	L	H
On	On	≤0.03 V	H	L	H
On	On	≤−0.2 V	L	L	L
On	On	≥0.2 V	H	L	L
On	On	0.2 V < A − B < −0.03 V	L	L	I
On	On	0.03 V < A − B < 0.2 V	H	L	I
On	On	Inputs open or shorted	L	L	H
On	X	X	X	H	Z
On	Off	X	X	L	I
Off	X	X	X	X	I

RECEIVER FAIL-SAFE

The ADM2461E/ADM2463E guarantee a logic high receiver output when the receiver inputs are shorted, open, or connected to a terminated transmission line with all drivers disabled. To achieve a fail-safe logic high output when the receiver inversion feature is disabled (INV or INVR = 0 V), the receiver input threshold is set internally between −30 mV and −200 mV. If A − B ≥ −30 mV, the RxD output is logic high. If A − B ≤ −200 mV, the RxD output is logic low. To preserve the fail-safe feature when the receiver inversion feature is enabled (INV or INVR = V_{DD1}), the inverted receiver input threshold is set internally between 30 mV and 200 mV. In the case of a terminated bus with all transmitters disabled, the termination resistor pulls the receiver differential input voltage to 0 V, which results in a logic high RxD output with a 30 mV minimum noise margin. This feature eliminates the need for the external biasing components that are usually required to implement the fail-safe feature.

These features are fully compatible with external fail-safe biasing configurations and can be used in applications with legacy devices that lack fail-safe support and in applications where additional noise margin is desired. See the AN-960 Application Note, *RS-485/RS-422 Circuit Implementation Guide*, for details on external fail-safe biasing.

DRIVER AND RECEIVER CABLE INVERSION

The ADM2461E/ADM2463E feature cable inversion functionality to correct for errors during installation. This adjustment can be implemented in the software on the controller driving the RS-485 transceiver to avoid installation costs to fix wiring errors. The ADM2463E full duplex transceiver features a receiver cable invert pin, INVR, that can be used to correct receiver functionality in cases where connections to the A and B pins are made in reverse. The ADM2461E half-duplex transceiver features a single cable invert logic input pin, INV, that inverts the driver and receiver to correct for reversed connections to the A and B pins. When the receiver is inverted, the device maintains a Logic 1 receiver output with a 30 mV noise margin when inputs are shorted together or open-circuit. Figure 42 shows the receiver output in inverted and noninverted cases.

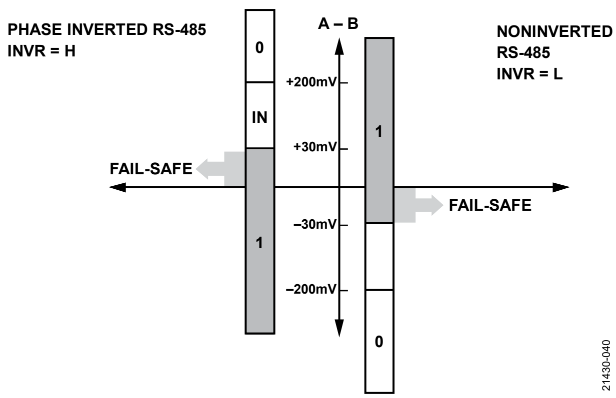

Figure 42. Noninverted RS-485 and Phase Inverted RS-485 Comparison

HOT SWAP INPUTS

When a circuit board is inserted into a powered (or hot) backplane, parasitic coupling from supply and ground rails to digital inputs can occur. The ADM2461E/ADM2463E contain circuitry to ensure that the RS-485 driver outputs remain in a high impedance state during power-up, and then default to the correct states. For example, when V_{DD1} and V_{DD2} power up at the same time and the $\overline{RE}$ pin is pulled low with the DE and TxD pins pulled high, the A and B outputs remain in high impedance until the outputs settle at an expected default high for the A pin and expected default low for the B pin.

192 TRANSCEIVERS ON THE BUS

The standard RS-485 receiver input impedance is 12 kΩ (1 unit load) and the standard driver can drive up to 32 unit loads. The ADM2461E/ADM2463E transceivers have a 1/6 unit load receiver input impedance (equivalent to 72 kΩ) that allows up to 192 transceivers to be connected in parallel on one communication line. Any combination of these devices and other RS-485 transceivers with a total of 32 unit loads or fewer can be connected to the line.

DRIVER OUTPUT PROTECTION

The ADM2461E/ADM2463E have two methods to prevent excessive output current and power dissipation caused either by faults or by bus contention. Current-limit protection on the output stage provides immediate protection against short circuits over the entire common-mode voltage range. In addition, a thermal shutdown circuit forces the driver outputs into a high impedance state if the die temperature rises excessively. This circuitry disables the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are re-enabled at a temperature of 140°C.

APPLICATIONS INFORMATION

PCB LAYOUT AND ELECTROMAGNETIC INTERFERENCE (EMI)

The ADM2461E/ADM2463E use a low power, on or off keying encoding scheme for robust communication with minimal radiated emissions. These devices can meet EN55032 and CISPR 32 Class B requirements with margin on a standard 2-layer PCB, without the need for complex and area intensive layout techniques.

MAXIMUM DATA RATE vs. AMBIENT TEMPERATURE

Under a large current load, power dissipation within the transceiver can limit the maximum ambient temperature achievable while retaining a silicon junction temperature below 150°C. This internal power dissipation is related to application conditions including supply voltage configuration, switching frequency, effective load on the RS-485 bus, and the amount of time the transceiver is in transmit mode. Thermal performance also depends on the PCB design and thermal characteristics of a system.

For high temperature applications above 85°C with a fully loaded RS-485 bus (equivalent to 54 Ω bus resistance) operating with a V_{DD2} supply of 5 V ± 10%, limiting the transmitter data rate to 300 kbps is recommended. The thermal resistance (θ_{JA}) of the package can be used in conjunction with the typical performance curves for the V_{DD2} supply current to calculate the maximum data rate for a given ambient temperature.

ISOLATED PROFIBUS SOLUTION

The ADM2461E features a transceiver that meets the requirements of an isolated Profibus node. When operating the ADM2461E as a Profibus transceiver, ensure that the V_{DD2} power supply is a minimum of 4.5 V. The ADM2461E is acceptable for use in Profibus applications as a result of the following characteristics:

- The output driver meets or exceeds the Profibus differential output requirements. To ensure that the transmitter differential output does not exceed 7 V p-p over all conditions, place 10 Ω resistors in series with the A and B transmitter outputs.
- Low bus pin capacitance of 28 pF.
- Class I (no loss of data) immunity to IEC61000-4-4 electrical fast transients (EFTs) up to ±1 kV with respect to the GND_2 pin can be achieved using a Profibus shielded cable. IEC 61000-4-4 Class I up to ±3 kV can be achieved with the addition of a 470 pF capacitor connected between the GND_1 pin and the RxD output pin.

EMC, EFT, AND SURGE PROTECTION

In applications where additional levels of protection against IEC61000-4-5 EFT or IEC61000-4-4 surge events are required, external protection circuits can be added to enhance the EMC robustness of the device. See Figure 43 for a recommended EMC protection circuit that uses a series of SM712 transient voltage suppressors (TVS) and 10 Ω pulse proof resistors to achieve Level 2 IEC61000-4-5 surge protection and an excess of Level 4 IEC61000-4-2 ESD and IEC61000-4-4 EFT protection. Table 16 and Table 17 list the recommended protection components and protection levels for this circuit.

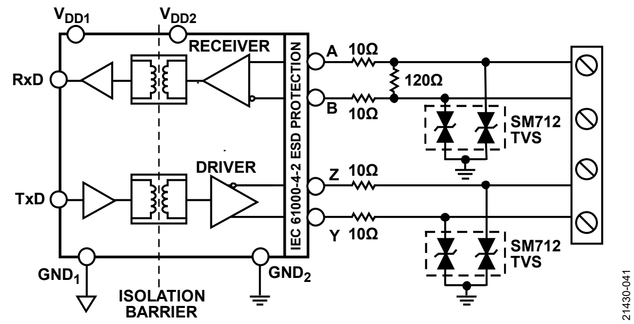

Figure 43. Isolated RS-485 Solution with ESD, EFT, and Surge Protection

Table 16. Recommended Components for ESD, EFT, and Surge Protection Solution

Recommended Components	Part Number
TVS	CDSOT23-SM712
10 Ω Pulse Proof Resistors	CRCW060310R0FKEAHP

Table 17. Protection Levels with Recommend Circuit

EMC Standard	Protection Level (kV)
ESD—Contact (IEC 61000-4-2)	≥ ±30 (exceeds Level 4)
ESD—Air (IEC 61000-4-2)	≥ ±30 (exceeds Level 4)
EFT (IEC 61000-4-4)	≥ ±4 (exceeds Level 4)
Surge (IEC 61000-4-5)	≥ ±1 (Level 2)

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period of time. The rate of insulation degradation depends on the characteristics of the voltage waveform applied across the insulation and on the materials and material interfaces.

The two types of insulation degradation of primary interest are breakdown along surfaces exposed to the air and insulation wear out. Surface breakdown is the phenomenon of surface tracking and is the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components to allow the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and can provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total rms voltage across the isolation, pollution degree, and material group. See Table 5 for the material group and creepage information for the ADM2461E/ADM2463E isolated RS-485 transceivers.

Insulation Wear Out

The lifetime of insulation caused by wear out is determined by the insulation thickness, the material properties, and the voltage stress applied across the insulation. Ensure that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. The working voltage applicable to tracking is specified in most standards.

Testing and modeling show that the primary driver of long-term degradation is displacement current in the polyimide insulation, which causes incremental damage. The stress on the insulation can be divided into broad categories such as dc stress and ac component, time varying voltage stress. DC stress causes little wear out because there is no displacement current. AC component, time varying voltage stress causes wear out.

The ratings in certification documents are typically based on 60 Hz sinusoidal stress to reflect isolation from the line voltage. However, many practical applications have combinations of 60 Hz ac and dc across the barrier, as shown in Equation 1. Because only the ac portion of the stress causes wear out, the equation can be rearranged to solve for the ac rms voltage, as shown in Equation 2. For insulation wear out with the polyimide materials used in these products, the ac rms voltage determines the product lifetime.

$$V_{RMS} = \sqrt{V_{AC\,RMS}^2 + V_{DC}^2} \quad (1)$$

or

$$V_{AC\,RMS} = \sqrt{V_{RMS}^2 - V_{DC}^2} \quad (2)$$

where:
V_{RMS} is the total rms working voltage.
$V_{AC\,RMS}$ is the time varying portion of the working voltage.
V_{DC} is the dc offset of the working voltage.

Calculation and Use of Parameters Example

The following example frequently arises in power conversion applications. Assume that the line voltage on one side of the isolation barrier is 240 V ac rms and that a 400 V dc bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages in determining the creepage, clearance, and lifetime of a device, see Figure 44, Equation 3, and Equation 4, where V_{PEAK} is the peak voltage.

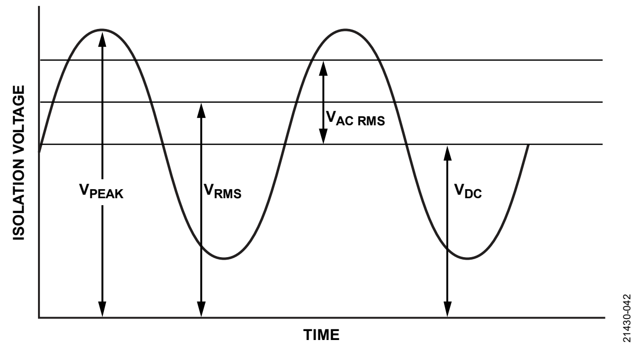

Figure 44. Critical Voltage Example

For this example, the V_{RMS} from Equation 1 is calculated as follows:

$$V_{RMS} = \sqrt{240^2 + 400^2} = 466\text{ V} \quad (3)$$

This V_{RMS} value is the working voltage used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain $V_{AC\,RMS}$. To calculate $V_{AC\,RMS}$ for this example, use Equation 2 as follows:

$$V_{AC\,RMS} = \sqrt{466^2 - 400^2} = 240\text{ V rms} \quad (4)$$

In this case, $V_{AC\,RMS}$ is the line voltage of 240 V rms. This calculation is more relevant when the waveform is not sinusoidal. The $V_{AC\,RMS}$ value is compared to the limits for the working ac voltage in Table 10 for the expected lifetime (which is less than a 60 Hz sine wave) and is well within the limit for a 50-year service life.

Note that the dc working voltage limit is set by the creepage of the package, as specified in IEC60664-1. This dc value can differ for specific system level standards.

OUTLINE DIMENSIONS

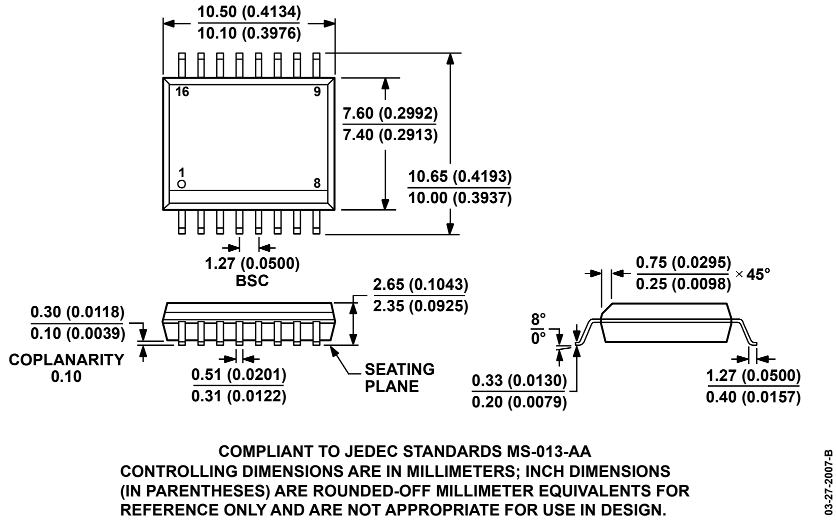

Figure 45. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Data Rate (Mbps)	Duplex	Temperature Range	Package Description	Package Option
ADM2461EBRWZ	0.5	Half	−40°C to +125°C	16-Lead SOIC_W	RW-16
ADM2461EBRWZ-R7	0.5	Half	−40°C to +125°C	16-Lead SOIC_W	RW-16
ADM2463EBRWZ	0.5	Full	−40°C to +125°C	16-Lead SOIC_W	RW-16
ADM2463EBRWZ-RL7	0.5	Full	−40°C to +125°C	16-Lead SOIC_W	RW-16
EVAL-ADM2461EEBZ				Half-Duplex Evaluation Board	
EVAL-ADM2463EEBZ				Full Duplex Evaluation Board	

[1] Z = RoHS Compliant Part.