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Evaluating the 5.7 kV RMS ADM2867E Signal and Power Isolated RS-485 Transceiver with ±15 kV IEC ESD

FEATURES

- Simplified evaluation of the 25 Mbps ADM2867E RS-485 transceiver
- 2-layer PCB compliant to EN 55032 Class B radiated emissions
- Footprint for 10.15 mm × 10.05 mm, 28-lead SOIC_W_FP package with >8.0 mm creepage and clearance
- On-board ADP7104 LDO regulator with jumper options for simplified evaluation in 5 V or 3.3 V configuration
- Flexible, low voltage V_{IO} supply rail to interface with I/O nodes as low as 1.7 V
- Selectable 3.3 V or 5 V isolated supply voltage options available
- IEC 61000-4-2 ESD protection on the A, B, Y, and Z pins
- ±12 kV contact discharge and ±15 kV air discharge
- SMA connector for high speed 25 Mbps TxD input signal
- Optional on-board LTC6900 oscillator to provide TxD input signal
- Screw terminal blocks for power connections, digital signals, and RS-485 signals
- Jumper-selectable enable and disable for digital input signals
- Resistors and footprints for termination and loopback test
- Test points to measure all signals

EVALUATION KIT CONTENTS

EVAL-ADM2867EEBZ

EQUIPMENT NEEDED

- Oscilloscope
- Signal generator
- 3.0 V to 5.5 V supply
- 1.62 V to 5.5 V supply

DOCUMENTS NEEDED

ADM2867E data sheet

GENERAL DESCRIPTION

The EVAL-ADM2867EEBZ allows the simplified, efficient evaluation of the 5.7 kV rms ADM2867E signal and power isolated RS-485 transceiver.

The ADM2867E features an integrated, isolated, dc-to-dc converter that provides power to the isolated side of the device with no additional ICs required.

An on-board ADP7104 low dropout (LDO) regulator accepts an input voltage of 3.3 V to 20 V and regulates the voltage to a selectable 3.3 V or 5 V supply for the V_{CC} pin of the ADM2867E. The LDO regulator can be bypassed to power the V_{CC} pin of the ADM2867E directly.

A flexible logic V_{IO} supply allows the device to operate with a digital input/output (I/O) voltage from 1.7 V to 5.5 V, which enables communication with modern nodes using either a 1.8 V or 2.5 V power supply. The V_{IO} pin can also be supplied from the ADP7104 regulated supply.

The EVAL-ADM2867EEBZ comes with options to evaluate the ADM2867E in an individual system. Digital and RS-485 bus signals are accessible via the screw terminal blocks on the EVAL-ADM2867EEBZ. Each digital input can be configured via the on-board jumper options.

Alternative methods can provide the transmit data input (TxD) signal to the device. An optional LTC6900 oscillator is included on the EVAL-ADM2867EEBZ and can be configured to provide a clock signal as the TxD digital input within a 1 kHz to 20 MHz range. For optimal signal integrity, use the on-board Subminiature Version A (SMA) connector to connect an external TxD signal at high data rates up to 25 Mbps.

The EVAL-ADM2867EEBZ has a footprint for the full duplex, isolated, RS-485 transceiver in a 10.15 mm × 10.05 mm, 28-lead, small outline, wide body with fine pitch (SOIC_W_FP) package. The EVAL-ADM2867EEBZ is populated with the ADM2867E 5.7 kV rms, isolated RS-485 transceiver.

For full details on the ADM2867E, see the ADM2867E data sheet, which must be used in conjunction with this user guide when using the EVAL-ADM2867EEBZ.

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REVISION HISTORY

5/2020—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPH

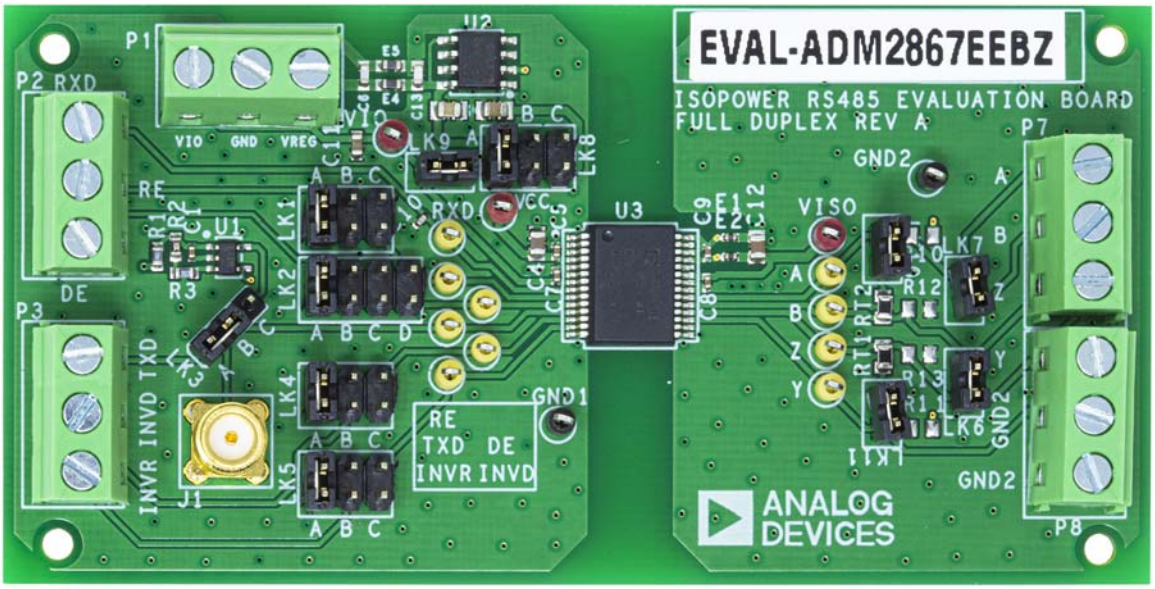

Figure 1.

EVALUATION BOARD HARDWARE

SETTING UP THE EVALUATION BOARD

The EVAL-ADM2867EEBZ is powered via the VREG_IN connection on the P1 screw terminal connector. The voltage connected to VREG_IN on the P1 screw connector can either be regulated or connected directly to the V_{CC} pin of the ADM2867E. Insert the LK8 jumper into Position A to power the ADM2867E directly from the VREG_IN terminal.

The on-board ADP7104 voltage regulator accepts a voltage from 3 V to 20 V on the VREG_IN terminal and can supply either a 3.3 V or a 5 V regulated supply to the V_{CC} pin of the ADM2867E. Select the regulated voltage via the LK8 jumper. Insert the LK8 jumper into Position B to operate the device with a regulated V_{CC} supply of 3.3 V. Insert the LK8 jumper into Position C to operate the device with a regulated V_{CC} supply of 5.5 V. The V_{CC} pin is fitted with a 10 µF decoupling capacitor (C4) and a 0.1 µF decoupling capacitor (C5).

To power the V_{IO} supply pin of the ADM2867E from the VCC terminal block and operate the V_{IO} and V_{CC} supply pins at the same voltage, insert Jumper LK9. To power the V_{IO} supply pin from a separate VIO terminal block, remove Jumper LK9. In this configuration, the VIO input of the P1 terminal block can be connected to a separate, low voltage logic supply between 1.7 V and 5.5 V. A 0.1 µF decoupling capacitor (C7) is fitted at the connector between the V_{IO} pin and GND_1 pins of the ADM2867E. A footprint for a second 10 µF capacitor (C11) can provide additional decoupling capacitance to the V_{IO} pin.

Use the V_{SEL} pin of the ADM2867E to select the isolated supply voltage for the RS-485 transceiver. To configure the device to output a 3.3 V isolated supply voltage, connect the V_{SEL} pin of the ADM2867E to the GND_{ISO} pins. To configure the device to output a 5 V isolated supply voltage, connect the V_{SEL} pin of the ADM2867E to the V_{ISOOUT} pin. The R6 and R7 resistors can be inserted or removed as needed to make these connections. Avoid inserting the R6 and R7 resistors together because this connection shorts the power and ground pins together.

See Table 2 and Table 3 for more details on the jumper and power supply connections. The corresponding labeled test points allow power supply monitoring on the EVAL-ADM2867EEBZ with the probe referenced to ground.

INPUT AND OUTPUT CONNECTIONS

Digital input and output signals are connected via the P2 and P3 screw terminal blocks to allow wire connections from the EVAL-ADM2867EEBZ to a signal generator. The EVAL-ADM2867EEBZ includes screw terminals for the TxD signal, receiver data output (RxD) signal, receiver enable ($\overline{RE}$), and driver enable (DE) test points. Screw terminals for the driver inversion function (INVD) and receiver inversion function (INVR) are also available on P3. Alternatively, jumper connections can connect these signals to the V_{IO} pin or GND_1 pins of the ADM2867E (see Table 2).

Connections to the RS-485 bus are made via the P7 and P8 screw terminal blocks. The EVAL-ADM2867EEBZ has four bus input and output signals: Signal A for noninverting input signals, Signal B for inverting input signals, Signal Y for noninverting output signals, and Signal Z for inverting output signals. The bus cables also include a common ground connection and can be connected to the P8 screw terminal block of the EVAL-ADM2867EEBZ. Test points are available on the EVAL-ADM2867EEBZ and are appropriately labeled for all digital and bus input and output signals.

RADIATED EMISSIONS

The EVAL-ADM2867EEBZ is a 2-layer printed circuit board (PCB) that meets the EN 55032 Class B radiated emissions requirements under full load while operating at the maximum data rate. Advances in the isolated dc-to-dc converter eliminate the need for complex mitigation techniques, such as edge guarding and embedded stitching capacitance. Two 0402, surface-mount ferrite beads are used to suppress high frequency noise and minimize the amount of noise radiated by the ADM2867E. The recommended ferrite beads have a high impedance in the 100 MHz to 1 GHz frequency range (see Table 1). The EVAL-ADM2867EEBZ is populated with the BLM15HD182SN1 ferrite beads on E1 and E2.

Table 1. Recommended Surface-Mount Ferrite Beads

Manufacturer	Part Number
Murata Electronics	BLM15HD182SN1
Taiyo Yuden	BKH1005LM182-T

To maximize the margin to the EN 55032 Class B specification, adhere to the following guidelines:

- Ensure that the decoupling capacitors are placed as close to the corresponding ADM2867E pins as possible.
- Place a 10 µF capacitor (C4) and a 0.1 µF capacitor (C5) between the V_{CC} pin and GND_1 pins of the ADM2867E.
- Place a 0.1 µF capacitor (C7) between the V_{IO} pin and GND_1 pins of the ADM2867E.
- Connect Pin 24, Pin 26, and Pin 28 of the ADM2867E together to form a single GND_{ISO} net. Connect this net to the GND_2 pins through the E1 ferrite bead.
- Place a 0.1 µF capacitor (C9) between the V_{ISOOUT} supply pin and the GND_{ISO} net of the ADM2867E.
- Connect the V_{ISOOUT} pin to the V_{ISOIN} pin of the ADM2867E through the E2 ferrite bead.
- Place a 10 µF capacitor (C12) and a 0.1 µF capacitor (C8) between the V_{ISOIN} supply pin (Pin 23) and the GND_2 pins (Pin 22) of the ADM2867E.
- Remove any metal planes or floods from the area around or under the GND_{ISO} net and V_{ISOOUT} net.

The EVAL-ADM2867EEBZ designed according to these guidelines meets the EN 55032 Class B requirements with margin. See Figure 2, Figure 7, and Figure 8 for further details on the recommended PCB layout.

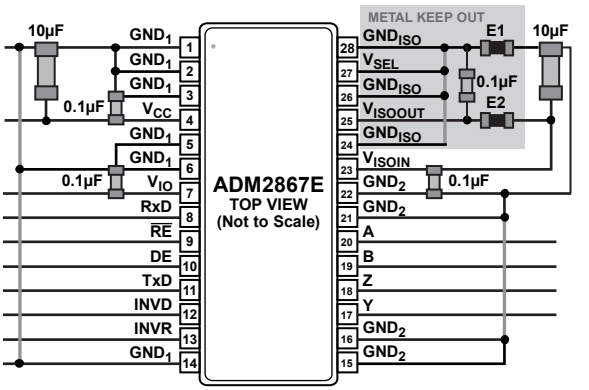

Figure 2. Layout Guidelines to Achieve EN 55032 Class B

EN 55032 RADIATED EMISSIONS TEST RESULTS

The EVAL-ADM2867EEBZ meets the EN 55032 and CISPR32 Class B requirements for radiated emissions with margin. The testing was performed in worst case conditions under a full 54 Ω load with both the transceiver and receiver transmitting at 25 Mbps. Figure 3 shows the results obtained in a 10 meter, semianechoic chamber, which are below the Class B limit.

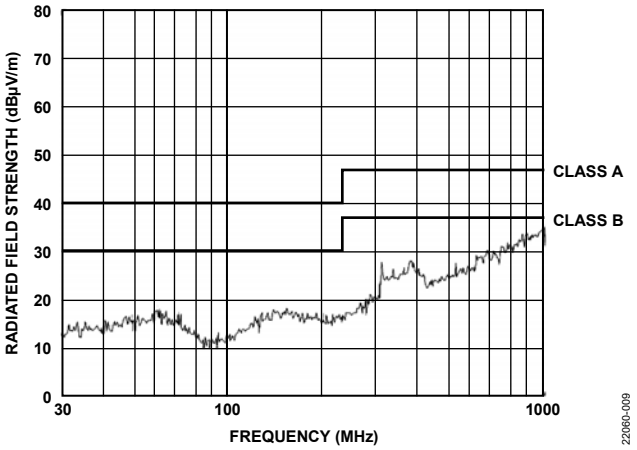

Figure 3. CISPR32/EN 55032 Radiated Emissions Test

Table 2. Jumper Configurations

Link	Jumper Connection	Description
LK1	A	Connects the $\overline{RE}$ input of the ADM2867E to the V_{IO} pin. This setting disables the receiver.
	B	Connects the $\overline{RE}$ input of the ADM2867E to the $\overline{RE}$ terminal on the P2 connector.
	C	Connects the $\overline{RE}$ input of the ADM2867E to the GND_1 pins. This setting enables the receiver.
LK2	A	Connects the DE input of the ADM2867E to the V_{IO} pin. This setting enables the driver.
	B	Connects the DE input of the ADM2867E to the DE terminal on the P2 connector.
	C	Connects the DE input of the ADM2867E to the GND_1 pins. This setting disables the driver.
	D	Connects the DE input of the ADM2867E to the $\overline{RE}$ input signal. Therefore, the input for both $\overline{RE}$ and DE is set by the LK1 jumper. This setting ensures that when the driver is enabled, the receiver is disabled, or when the driver is disabled, the receiver is enabled.
LK3	AB	Connects the TxD input of the ADM2867E and J1 SMA connector to the TxD terminal on the P3 connector.
	BC	Connects the TxD input of the ADM2867E and J1 SMA connector to the LTC6900 oscillator output. To configure the oscillator frequency to be between 1 kHz and 12.5 MHz, set the R2 and R3 resistors. Only use this option when the V_{IO} supply input is between 3 V to 5.5 V.
	Not inserted	Connects the TxD input of the ADM2867E to the J1 SMA connector.
LK4	A	Connects the INVD input of the ADM2867E to the V_{IO} pin. This setting enables the driver inversion feature.
	B	Connects the INVD input of the ADM2867E to the INVD terminal on the P3 connector.
	C	Connects the INVD input of the ADM2867E to the GND_1 pins. This setting is used for normal driver operation.

Link	Jumper Connection	Description
LK5	A	Connects the INVR input of the ADM2867E to the V_{IO} pin. This setting enables the receiver inversion feature.
	B	Connects the INVR input of the ADM2867E to the INVR terminal on the P3 connector.
	C	Connects the INVR input of the ADM2867E to the GND_1 pins. This setting is used for normal receiver operation.
LK6	Inserted	Connects the Pin B of the ADM2867E to Pin Z.
	Not inserted	Disconnects the Pin B of the ADM2867E from Pin Z.
LK7	Inserted	Connects the Pin A of the ADM2867E to Pin Y.
	Not inserted	Disconnects the Pin A of the ADM2867E from Pin Y.
LK8	A	Connects the V_{CC} pin of the ADM2867E to the VREG_IN terminal on the P1 connector. This option bypasses the ADP7104 regulator and allows an external power supply to connect directly to the V_{CC} pin of the ADM2867E.
	B	Powers the V_{CC} pin of the ADM2867E with a regulated 3.3 V power supply from the ADP7104. The ADP7104 must be supplied with at least 4 V through the VREG_IN terminal on the P1 connector.
	C	Powers the V_{CC} pin of the ADM2867E with a regulated 5 V power supply from the ADP7104. The ADP7104 must be supplied with at least 6 V through the VREG_IN terminal on the P1 connector.
LK9	Inserted	Connects the V_{CC} pin of the ADM2867E to the V_{IO} pin.
	Not inserted	Disconnects the V_{CC} pin of the ADM2867E from the V_{IO} pin. The V_{IO} pin is powered from the VIO terminal on the P1 connector.
LK10	Inserted	Connects the 120 Ω RT2 termination resistor across the Pin A and Pin B of the ADM2867E.
	Not inserted	Disconnects the 120 Ω RT2 termination resistor across the Pin A and Pin B of the ADM2867E.
LK11	Inserted	Connects the 120 Ω RT1 termination resistor across the Pin Y and Pin Z of the ADM2867E.
	Not inserted	Disconnects the 120 Ω RT1 termination resistor across the Pin Y and Pin Z of the ADM2867E.

OTHER BOARD COMPONENTS

The EVAL-ADM2867EEBZ has footprints for the RT1 and RT2 termination resistors. Two 120 Ω termination resistors are fitted to the EVAL-ADM2867EEBZ, but these resistors can be removed or replaced with a resistor of a different value as needed. Insert the LK11 jumper to add a 120 Ω load to the RS-485 driver. When LK6, LK7, and LK10 are inserted, an additional 120 Ω termination resistor is connected, resulting in a 60 Ω load on the RS-485 driver.

Biasing Resistors for Bus Idle Fail-Safe

The ADM2867E has a built in receiver fail-safe for the bus idle condition, but there are footprints on the EVAL-ADM2867EEBZ for fitting the R10 and R11 pull-up resistors to the V_{ISO} supply on Pin A and Pin Y of the ADM2867E, as well as the R12 and R13 pull-down resistors to the GND_2 supply pins on Pin B and Pin Z. These resistors can be fitted if the user is connecting to other devices that require external biasing resistors on the bus. The exact value required for a 200 mV minimum differential voltage in bus idle condition depends on the minimum supply voltage and the termination scheme. For 5 V transceiver operation, 1140 Ω is recommended. For 3.3 V transceiver operation, 900 Ω is recommended.

See the AN-960 Application Note, *RS-485/RS-422 Circuit Implementation Guide* for more information about the bus idle fail-safe.

On-Board LTC6900 Oscillator

An LTC6900 clock oscillator is provided on the EVAL-ADM2867EEBZ to allow efficient evaluation of the device without the need for an external signal source.

To use the LTC6900 oscillator for evaluation, insert the LK3 jumper into Position BC. This setting connects the clock oscillator output to the TxD input pin of the ADM2867E.

The R2 and R3 resistors can be used to configure the switching frequency of the clock oscillator within the 100 kHz to 12.5 MHz range. Calculate the frequency using the following equation:

$$f_{OSC} = 10\ \text{MHz}\left(\frac{20\ \text{k}\Omega}{(\text{R2} + \text{R3})}\right)\ 16\ \text{k}\Omega \le (\text{R2} + \text{R3}) \le 2\ \text{M}\Omega$$

where f_{OSC} is the output frequency of the LTC6900 oscillator.

The LTC6900 oscillator is powered from the V_{IO} supply, and must only be used when the V_{IO} supply voltage is between 2.7 V and 5.5 V.

ADP7104 LDO Regulator

The EVAL-ADM2867EEBZ features an on-board ADP7104 LDO regulator that allows flexible power supply configurations during evaluation.

To use the on-board regulator, insert the LK8 jumper into Position B or Position C. This setting connects the regulator output to the V_{CC} pin of the ADM2867E. In this configuration, power must be supplied to the VREG_IN input on the P1 connector.

The ADP7104 LDO regulator can be configured to provide regulated 3.3 V or 5 V power to the V_{CC} pin of the ADM2867E via the LK8 jumper. When using the ADP7104 regulator, insert the LK8 jumper at Position C to provide a regulated 5 V power supply to the V_{CC} pin of the ADM2867E. Insert the LK8 jumper at Position B to provide a 3.3 V power supply to the V_{CC} pin of the ADM2867E. Note that when LK8 is inserted at Position B, 5 V transceiver operation is not supported.

Insert the LK8 jumper into Position A to bypass the regulator and power of the ADM2867E directly from the VREG_IN input on the P1 connector. In this configuration, the VREG_IN input on the P1 connector supports a voltage range of 3 V to 5.5 V.

Table 3 lists the supported power supply configurations and the associated jumper configurations.

FULL DUPLEX RS-485 TRANSCEIVERS LOOPBACK TEST

To set up a loopback test with the EVAL-ADM2867EEBZ, close the LK6 and LK7 jumpers. The test details are shown in Table 3 and in Figure 5. A signal generator is connected to the TxD pin, which allows verification of the bus signals and the receiver output. Note that the jumper position for LK1 is Position C, LK2 is Position A, LK4 is Position C, and LK5 is Position C on the EVAL-ADM2867EEBZ. See Table 3 for the jumper configurations required for different power supply configurations. The LK11 and LK12 jumpers can be inserted to terminate the transmitter and the receiver with 120 Ω resistors. Connect both these jumpers while the EVAL-ADM2867EEBZ is configured for the loopback test to ensure that the driver is terminated with a standard RS-485 load of 60 Ω (bus terminated at both ends by 120 Ω).

IEC 61000-4-2 ELECTROSTATIC DISCHARGE (ESD) PROTECTION

The EVAL-ADM2867EEBZ is tested to achieve protection against IEC 61000-4-2 ESD to ±12 kV (contact) and ±15 kV (air) on Pin A, Pin B, Pin Y, and Pin Z of the ADM2867E.

The IEC 61000-4-2 ESD standard describes testing using two coupling methods known as contact discharge and air discharge. Contact discharge implies direct contact between the discharge gun and the equipment under test (EUT).

During air discharge testing, the charged electrode of the discharge gun is moved toward the EUT until a discharge occurs as an arc across the air gap. The discharge gun does not make direct contact with the EUT.

During testing, Pin A, Pin B, Pin Y, and Pin Z of the ADM2867E are subjected to at least 10 positive and 10 negative single discharges with a 1 sec interval between each pulse. The highest specified IEC 61000-4-2 ESD test is Level 4, which defines a contact discharge voltage of ±8 kV and an air discharge voltage of ±15 kV.

Figure 4 shows the 8 kV contact discharge current waveform, as described in the ADM2867E data sheet, which has a peak current (I_{PEAK}) of 30 A. The IEC 61000-4-2 waveform parameters include rise times (t_R) of <1 ns and pulse widths of ~60 ns.

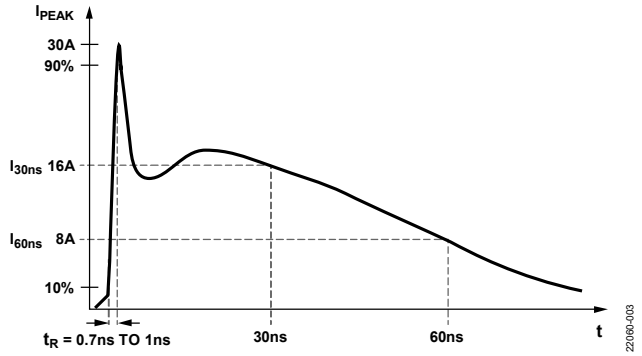

Figure 4. IEC 61000-4-2 ESD Waveform (8 kV)

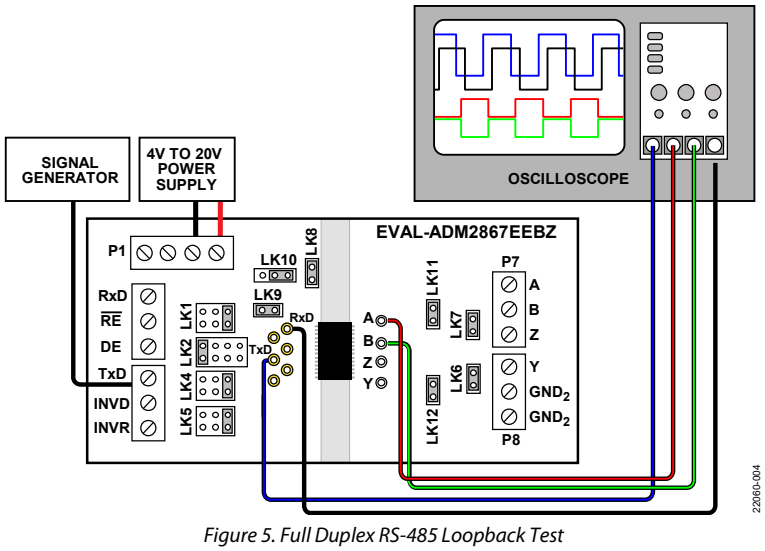

Figure 5. Full Duplex RS-485 Loopback Test

Table 3. Input Supply Configurations

Jumper LK8	V_{SEL} Pin	VREG_IN Input Voltage Range	V_{CC} Supply	V_{ISO} Supply
A	Low	Not used	Power V_{CC} directly on connector P1 with a supply voltage between 3 V and 5.5 V	3.3 V isolated output
	High	Not used	Power V_{CC} directly on connector P1 with a supply voltage between 4.5 V and 5.5 V	5 V isolated output
B	Low	6 V to 20 V	Regulator provides 5 V supply to V_{CC}	3.3 V isolated output
	High	Invalid condition, 5 V isolated output is not supported with V_{CC} < 4.5 V	B	High
C	Low	4 V to 20 V	Regulator provides 3.3 V supply to V_{CC}	3.3 V isolated output
	High	6 V to 20 V	Regulator provides 5 V supply to V_{CC}	5 V isolated output

EVALUATION BOARD SCHEMATIC AND ARTWORK

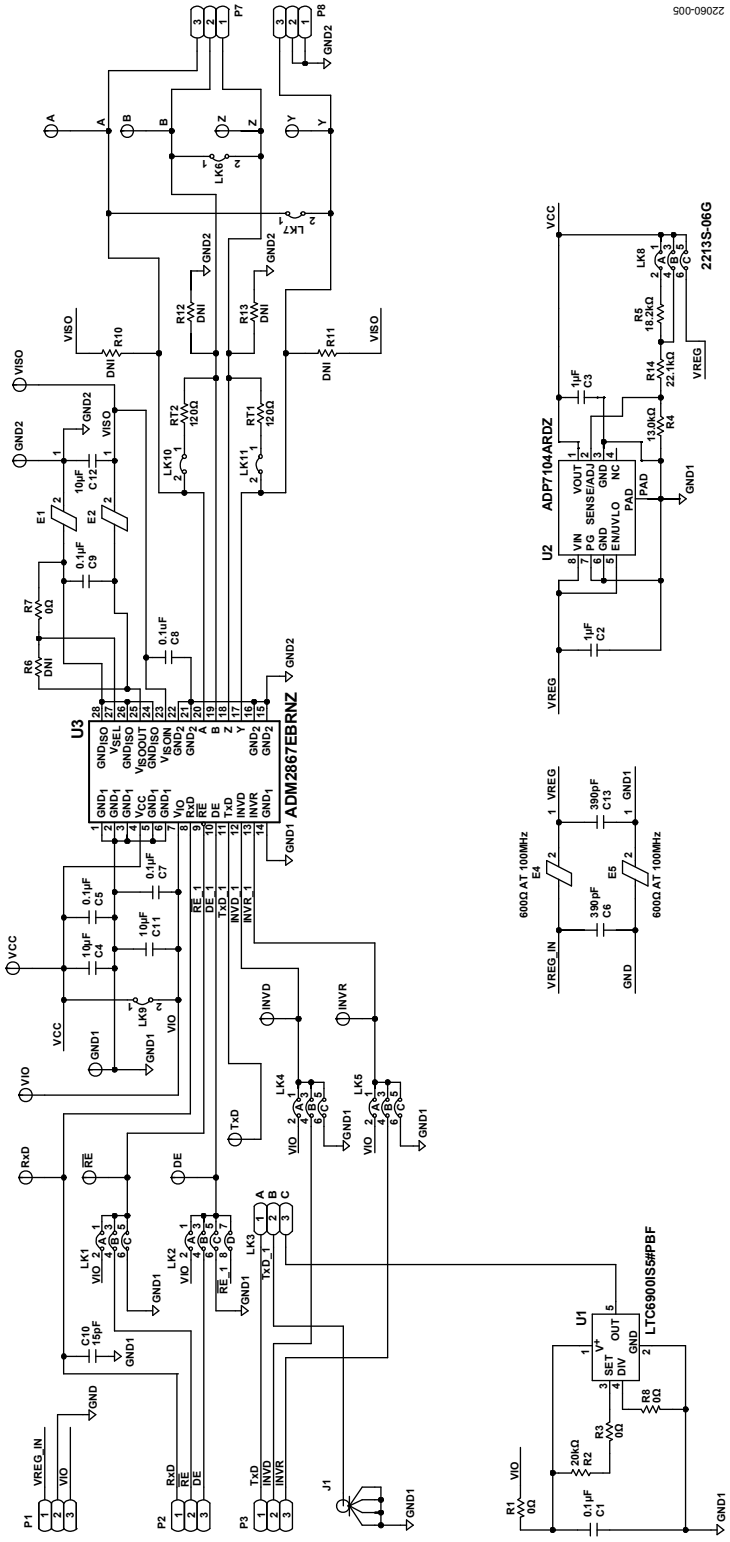

Figure 6. EVAL-ADM2867EEBZ Schematic

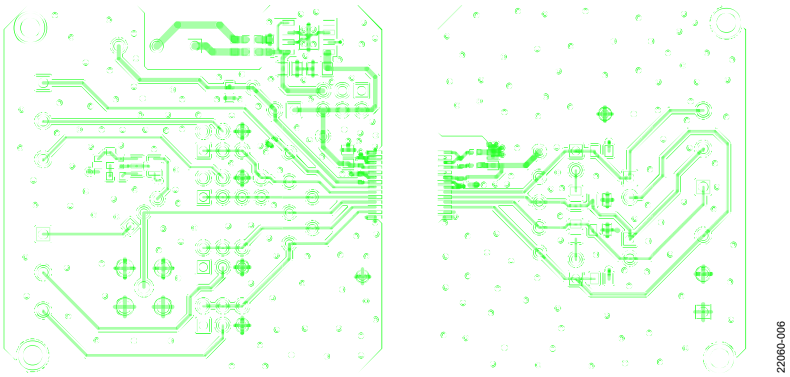

Figure 7. EVAL-ADM2867EEBZ Component Side, Layer 1

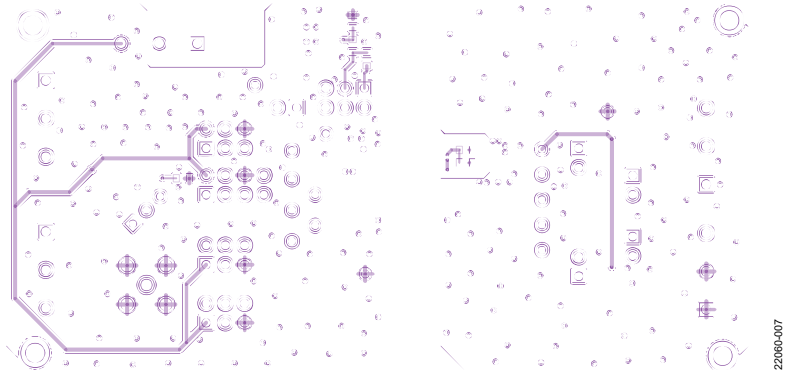

Figure 8. EVAL-ADM2867EEBZ, Layer 2

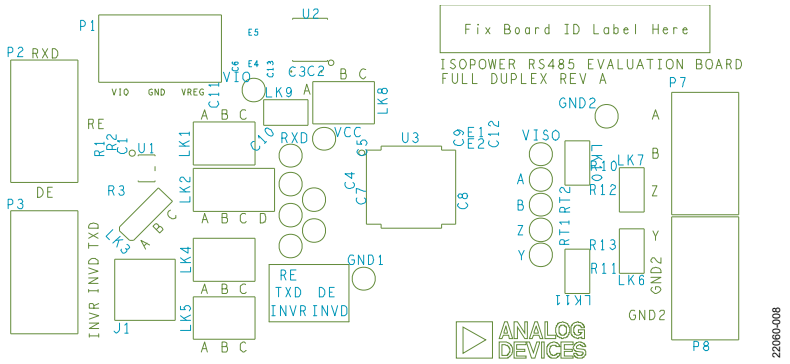

Figure 9. EVAL-ADM2867EEBZ, Silkscreen

ORDERING INFORMATION

BILL OF MATERIALS

Table 4. EVAL-ADM2867EEBZ Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Part Number
10	A, B, DE, INVD, INVR, $\overline{RE}$, RxD, TxD, Y, Z	Test points, yellow	Keystone Electronics	36-5004-ND
5	C1, C5, C7 to C9	Capacitors, 0.1 µF, 0402	Kemet	C0402C104K4RACTU
2	C2, C3	Capacitors, 1 µF, 0805	Murata	GCM21BR71E105KA56L
2	C4, C12	Capacitors, 10 µF, 0805	TDK	C2012X5R1E106K085AC
2	C6, C13	Capacitors, 390 pF, 0603	AVX Corporation	0603YC391KAT2A
1	C10	Capacitor, 15 pF, 0402	Murata	GCM1555C1H150FA16D
1	C11	Capacitor, 10 µF, 0603	TDK	C1608X5R1A106M080AC
2	E1, E2	Ferrite beads, 0402	Murata	BLM15HD182SN1D
2	E4, E5	Ferrite beads, 0603, 600 Ω at 100 MHz	Murata	BLM18HE601SN1D
2	GND1, GND2	Test points, black	Components Corporation	TP-105-01-00
1	J1	Coaxial, straight SMA connector	TE Connectivity	5-1814832-1
4	LK1, LK4, LK5, LK8	6-pin (3 × 2), 0.1 inch headers and shorting block	Multicomp	2213S-06G
1	LK2	8-pin (4 × 2), 0.1 inch header and shorting block	Multicomp	2213S-08G
1	LK3	3-pin (3 × 1), 0.1 inch header and shorting block	Molex	22-28-4033
5	LK6, LK7, LK9 to LK11	2-pin (1 × 2), 0.1 inch headers and shorting block	Harwin	M20-9990246
5	P1 to P3, P7, P8	Three-way terminal blocks	Wurth Elektronik	691131710003
3	R1, R3, R7, R8	Resistors, 0 Ω, 0603	Vishay	CRCW0603000ZRT1
1	R2	Resistor, 20 kΩ, 0603	Panasonic	ERJ-3EKF2002V
1	R4	Resistor, 13 kΩ, 0603	Panasonic	ERJ-3EKF1302V
1	R5	Resistor, 18.2 kΩ, 0603	Panasonic	ERJ-3EKF1822V
1	R6	Resistor, do not install, 0603	Not applicable	Not applicable
1	R14	Resistor, 22.1 kΩ, 0603	Panasonic	ERJ-3EKF2212V
4	R10 to R13	Resistors, do not install, 0805	Not applicable	Not applicable
2	RT1, RT2	Resistors, 120 Ω, 0805	Panasonic	ERJ-P6WF1200V
1	U1	Low power, 1 kHz to 20 MHz oscillator	Analog Devices	LTC6900IS5#PBF
1	U2	Low noise CMOS LDO	Analog Devices	ADP7104ARDZ-R7
1	U3	25 Mbps, 5.7 kV signal and power isolated RS-485 transceiver	Analog Devices	ADM2867EBRNZ
3	VCC, VIO, VISO	Test points, red	Components Corporation	TP-105-01-02

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG22060-5/20(0)

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