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Evaluating the ADM2463E and ADM2763E 500 kbps, 5.7 kV RMS, Signal Isolated, Full Duplex RS-485 Transceivers with ±15 kV IEC ESD

FEATURES

- Simplified evaluation of the ADM2463E and ADM2763E signal isolated, 500 kbps, full duplex RS-485 transceiver
- 2-layer PCB compliant to EN 55032 Class B radiated emissions
- Footprint for standard full duplex, 16-lead, SOIC_W package with >8 mm creepage and clearance
- On-board ADP7104 LDO regulators with jumper options for simplified evaluation in multiple supply configurations
- Flexible, low voltage V_{DD1} supply rail for interfacing with I/O nodes as low as 1.7 V
- Wide bus voltage V_{DD2} supply rail from 3 V to 5.5 V
- IEC 61000-4-2 ESD protection on the A pin, B pin, Y pin, and Z pin
  - ≥±12 kV contact discharge and ≥±15 kV air discharge
- SMA connector for TxD input signal
- Optional on-board LTC1799 oscillator for providing TxD signal
- Screw terminal blocks for connecting power, digital, and RS-485 signals
- Jumper-selectable enable and disable for digital input signals
- Resistors and footprints for termination and loopback test
- Test points for measuring all signals

EVALUATION KIT CONTENTS

EVAL-ADM2463EEBZ/EVAL-ADM2763EEBZ

EQUIPMENT NEEDED

- Oscilloscope
- Signal generator
- 3 V to 5.5 V secondary side supply
- 1.7 V to 5.5 V primary side supply

DOCUMENTS NEEDED

- ADM2463E data sheet
- ADM2763E data sheet

GENERAL DESCRIPTION

The EVAL-ADM2463EEBZ/EVAL-ADM2763EEBZ allow simplified, efficient evaluation of the ADM2463E and ADM2763E 5.7 kV rms, 500 kbps signal isolated RS-485 transceivers. The functionality of the EVAL-ADM2463EEBZ and the EVAL-ADM2763EEBZ are the same. Figure 1 shows the EVAL-ADM2463EEBZ and represents both evaluation boards.

The EVAL-ADM2463EEBZ/EVAL-ADM2763EEBZ come with options for the evaluation of the ADM2463E and ADM2763E devices in an individual system. Digital and RS-485 bus signals are easily accessible via the screw terminal blocks on the evaluation boards. Each digital input can be configured via the on-board jumper options.

Two on-board ADP7104 low dropout (LDO) regulators accept an input voltage of up to 20 V and output a range of selectable supply voltages to the V_{DD1} pin and V_{DD2} pin, configurable via jumper options. The LDO regulators can be bypassed to power the ADM2463E and ADM2763E V_{DD1} supply pins and V_{DD2} supply pins directly from an external power supply.

The flexible V_{DD1} pin primary side logic supply allows the device to operate with a digital input/output (I/O) voltage from 1.7 V to 5.5 V, which enables communication with modern nodes using either a 1.8 V or 2.5 V power supply. The V_{DD1} pin can also be supplied from the ADP7104 regulated supply.

Alternative methods can be used to provide the transmit data input (TxD) signal to the device. An optional LTC1799 oscillator is included on the evaluation boards and can be configured to provide a clock signal as the TxD digital input within a 10 kHz to 250 kHz range. A terminal block allows an easy wired connection to a microcontroller or processor. For optimal signal integrity, use the on-board Subminiature Version A (SMA) connector to connect an external data signal.

The evaluation boards have footprints for the ADM2463E and ADM2763E full duplex, signal isolated, RS-485 transceivers in a 10.10 mm × 10 mm, 16-lead, standard small outline, wide body (SOIC_W) package.

For full details on the ADM2463E and ADM2763E, see the ADM2463E and ADM2763E data sheets, which must be used in conjunction with this user guide when using the EVAL-ADM2463EEBZ/EVAL-ADM2763EEBZ.

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REVISION HISTORY

6/2020—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPH

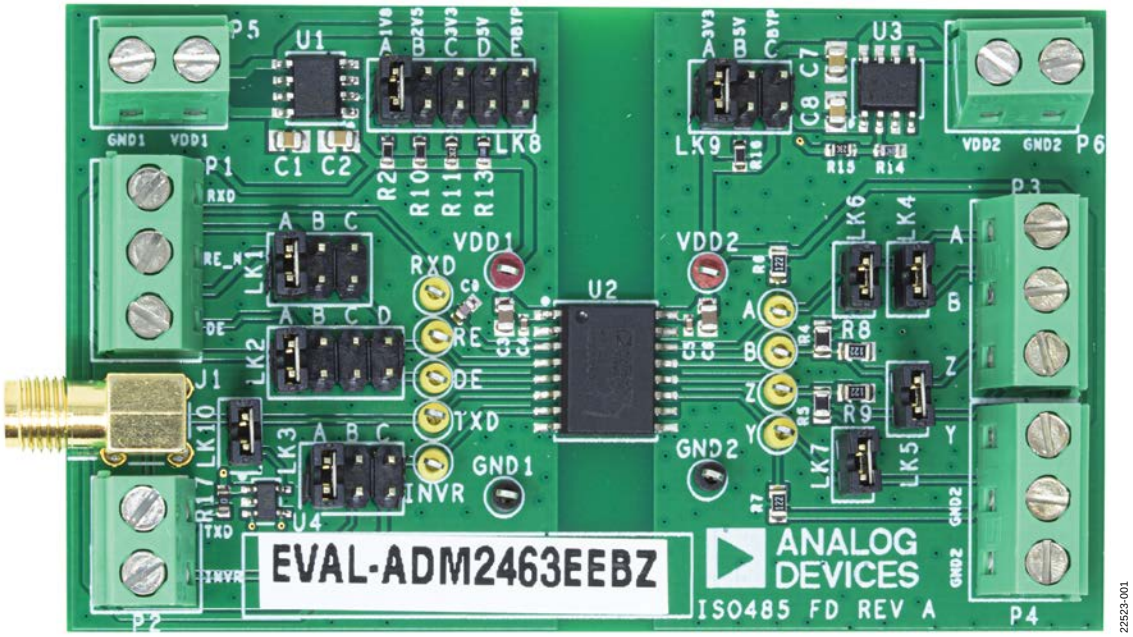

Figure 1. EVAL-ADM2463EEBZ

EVALUATION BOARD HARDWARE

SETTING UP THE EVALUATION BOARD

The EVAL-ADM2463EEBZ/EVAL-ADM2763EEBZ are used to evaluate the ADM2463E and ADM2763E isolated RS-485 transceivers, which require a power supply on both sides of the device. The evaluation boards are powered via the VDD1 and VDD2 connections on the P5 and P6 screw terminal connectors. The supply voltages connected to these terminals can either be regulated or connected directly to the V_{DD1} pin and V_{DD2} pin of the ADM2463E or ADM2763E. Insert the LK8 jumper into Position E to power the V_{DD1} pin directly from the VDD1 connector. Insert the LK9 jumper into Position C to power the V_{DD2} pin directly from the VDD2 terminal on P6.

The two on-board ADP7104 voltage regulators can be configured to provide a range of regulated supply voltages to the V_{DD1} pin and V_{DD2} pin of the ADM2463E or ADM2763E. Various voltage options can be selected using the LK8 and LK9 jumpers. The V_{DD1} pin is fitted with a 10 µF decoupling capacitor (C3) and a 0.1 µF decoupling capacitor (C4). The V_{DD2} pin is fitted with a 10 µF decoupling capacitor (C6) and a 0.1 µF decoupling capacitor (C5).

See Table 1, Table 2, and Table 3 for more details on the jumper and power supply connections. The corresponding labeled test points allow monitoring of the EVAL-ADM2463EEBZ/EVAL-ADM2763EEBZ V_{DD1} and V_{DD2} supply voltages.

Table 1. Jumper Configurations

Link	Jumper Connection	Description
LK1	A	Connects the ADM2463E or ADM2763E $\overline{RE}$ input to the V_{DD1} pin. This setting disables the receiver.
	B	Connects the ADM2463E or ADM2763E $\overline{RE}$ input to the $\overline{RE}$ terminal on the P1 connector.
	C	Connects the ADM2463E or ADM2763E $\overline{RE}$ input to the GND_1 pin. This setting enables the receiver.
LK2	A	Connects the ADM2463E or ADM2763E DE input to the V_{DD1} pin. This setting enables the driver.
	B	Connects the ADM2463E or ADM2763E DE input to the DE terminal on the P1 connector.
	C	Connects the ADM2463E or ADM2763E DE input to the GND_1 pin. This setting disables the driver.
	D	Connects the ADM2463E or ADM2763E DE input to the $\overline{RE}$ input signal. Therefore, the input for both $\overline{RE}$ and DE is set by the LK1 jumper. This setting ensures that when the driver is enabled, the receiver is disabled, or when the driver is disabled, the receiver is enabled.
LK3	A	Connects the ADM2463E or ADM2763E INVR input to the V_{DD1} pin. This setting enables the receiver inversion feature.
	B	Connects the ADM2463E or ADM2763E INVR input to the INVR terminal on the P2 connector.
	C	Connects the ADM2463E or ADM2763E INVR input to the GND_1 pin. This setting is used for normal receiver operation.
LK4	Inserted	Connects the ADM2463E or ADM2763E Pin A to Pin Y.
	Not inserted	Disconnects the ADM2463E or ADM2763E Pin A from Pin Y.
LK5	Inserted	Connects the ADM2463E or ADM2763E Pin B to Pin Z.
	Not inserted	Disconnects the ADM2463E or ADM2763E Pin B from Pin Z.
LK6	Inserted	Connects the 120 Ω R4 termination resistor across the ADM2463E or ADM2763E Pin A and Pin B.
	Not inserted	Disconnects the 120 Ω R4 termination resistor across the ADM2463E or ADM2763E Pin A and Pin B.
LK7	Inserted	Connects the 120 Ω R5 termination resistor across the ADM2463E or ADM2763E Pin Y and Pin Z.
	Not inserted	Disconnects the 120 Ω R5 termination resistor across the ADM2463E or ADM2763E Pin Y and Pin Z.
LK8	A	Configures the ADP7104 voltage regulator, U1, to supply a regulated 1.8 V to the ADM2463E or ADM2763E V_{DD1} pin.
	B	Configures the ADP7104 voltage regulator, U1, to supply a regulated 2.5 V to the ADM2463E or ADM2763E V_{DD1} pin.
	C	Configures the ADP7104 voltage regulator, U1, to supply a regulated 3.3 V to the ADM2463E or ADM2763E V_{DD1} pin.
	D	Configures the ADP7104 voltage regulator, U1, to supply a regulated 5 V to the ADM2463E or ADM2763E V_{DD1} pin.
	E	Bypasses the ADP7104 voltage regulator, U1, and powers the ADM2463E or ADM2763E V_{DD1} supply pin directly from the VDD1 terminal on the P5 connector.
LK9	A	Configures the ADP7104 voltage regulator, U3, to supply a regulated 3.3 V to the ADM2463E or ADM2763E V_{DD2} pin.
	B	Configures the ADP7104 voltage regulator, U3, to supply a regulated 5 V to the ADM2463E or ADM2763E V_{DD2} pin.
	C	Bypasses the ADP7104 voltage regulator, U3, and powers the ADM2463E or ADM2763E V_{DD2} supply pin directly from the VDD2 terminal on the P6 connector.
LK10	Inserted	Connects the output of the LTC1799 oscillator to the ADM2463E or ADM2763E TxD pin.
	Not inserted	Disconnects the output of the LTC1799 oscillator from the ADM2463E or ADM2763E TxD pin.

INPUT AND OUTPUT CONNECTIONS

Digital input and output signals are connected via the P1 and P2 screw terminal blocks to allow wire connections from the EVAL-ADM2463EEBZ/EVAL-ADM2763EEBZ to a signal generator or microcontroller. The evaluation boards include screw terminals for receiver data output (RxD), receiver enable ($\overline{RE}$), and driver enable (DE) on P1. Screw terminals for the TxD and receiver invert (INVR) functions are also available on P2. Alternatively, jumper connections can connect these signals to the V_{DD1} pin or GND_1 pins of the ADM2463E or ADM2763E (see Table 1).

Connections to the RS-485 bus are made via the P3 and P4 screw terminal blocks. The EVAL-ADM2463EEBZ/EVAL-ADM2763EEBZ have four bus input and output signals: Signal A for the noninverting input signal, Signal B for the inverting input signal, Signal Y for the noninverting output signal, and Signal Z for the inverting output signal. The bus cables also include a common ground connection and can be connected to the P4 screw terminal block of the evaluation boards. Test points are available on the evaluation boards and are appropriately labeled for all digital and bus input and output signals.

RADIATED EMISSIONS

The ADM2463E or ADM2763E encodes data across the isolation barrier using an amplitude shift keying (ASK) modulation scheme, which is optimized for both high noise immunity and minimal radiated emissions. The EVAL-ADM2463EEBZ/EVAL-ADM2763EEBZ are 2-layer printed circuit boards (PCB) that meet the EN 55032 Class B radiated emissions requirements under full load while operating at a maximum data rate of 500 kbps. To maximize the margin to the EN 55032 Class B specification, adhere to the following guidelines:

- Place a 0.1 µF capacitor (C4) between the V_{DD1} pin and GND_1 pin.
- Place a 0.1 µF capacitor (C5) between the V_{DD2} pin and GND_1 pin.
- Ensure that the decoupling capacitors are placed as close as possible to the corresponding ADM2463E or ADM2763E pins.

The EVAL-ADM2463EEBZ/EVAL-ADM2763EEBZ, designed according to these guidelines, meet EN 55032 Class B requirements with margin.

OTHER BOARD COMPONENTS

The EVAL-ADM2463EEBZ/EVAL-ADM2763EEBZ have footprints for the R4 and R5 termination resistors. The 120 Ω termination resistors are fitted to the evaluation boards, but these resistors can be removed or replaced with a resistor of a different value as needed. Insert the LK6 jumper to connect the R4 resistor and add a 120 Ω load to the RS-485 receiver. Insert the LK7 jumper to connect the R5 resistor and add a 120 Ω load to the RS-485 driver. The LK6 and LK7 jumpers can be inserted to connect the RS-485 driver outputs to the RS-485 receiver inputs. When LK4, LK5, LK6, and LK7 are inserted, the two 120 Ω termination resistors are connected in parallel, resulting in a 60 Ω load on the RS-485 driver.

Biasing Resistors for Bus Idle Fail-Safe

The ADM2463E or ADM2763E has a built in receiver fail-safe for the bus idle condition, but there are footprints on the EVAL-ADM2463EEBZ/EVAL-ADM2763EEBZ for fitting the R6 and R7 pull-up resistors to the V_{DD2} supply on the ADM2463E or ADM2763E Pin A and Pin Y, as well as the R8 and R9 pull-down resistors to the GND_2 supply on Pin B and Pin Z. These resistors can be fitted if the user is connecting to other devices that require external biasing resistors on the bus. The exact value required for a 200 mV minimum differential voltage in the bus idle condition depends on the minimum supply voltage and the termination scheme. For 5 V transceiver operation, 1140 Ω is recommended. For 3.3 V transceiver operation, 900 Ω is recommended.

See the AN-960 Application Note, *RS-485/RS-422 Circuit Implementation Guide*, for more information about the bus idle fail-safe.

On-Board LTC1799 Oscillator

An LTC1799 clock oscillator is provided on the EVAL-ADM2463EEBZ/EVAL-ADM2763EEBZ to allow convenient evaluation of the ADM2463E or ADM2763E without the need for an external signal source.

To use the LTC1799 oscillator for evaluation, insert the LK10 jumper. This setting connects the clock oscillator output to the ADM2463E or ADM2763E TxD input pin.

The sum of the R3 and R12 resistors can be used to configure the switching frequency of the clock oscillator (f_{OSC}) within the 100 kHz to 250 kHz range. The frequency is calculated using the following equation:

$$f_{OSC} = 10\ \text{MHz}\left(\frac{10\ \text{k}}{N\left(R3 + R12\right)}\right)$$

where:
$4\ \text{k}\Omega \le (R3 + R12) \le 1\ \text{M}\Omega$.
$N = 1$ or 10

The value of N is controlled with the R18 resistor. When R18 is not inserted, N = 10. Insert a 0 Ω resistor at R18 to set N = 1 for higher frequency operation. The EVAL-ADM2463EEBZ/EVAL-ADM2763EEBZ ship with N = 10 and R3 + R12 = 40 kΩ, setting the oscillator output frequency to 250 kHz.

The LTC1799 oscillator is powered from the V_{DD1} supply, and can only be used when the V_{DD1} supply voltage is between 2.7 V and 5.5 V. By removing the 0 Ω R17 resistor, the LTC1799 can be disconnected from the V_{DD1} supply.

ADP7104 LDO Regulator

The EVAL-ADM2463EEBZ/EVAL-ADM2763EEBZ feature two on-board ADP7104 LDO regulators that allow flexible power supply configurations during evaluation.

The V_{DD1} regulator, U1, is powered from the VDD1 terminal on Connector P5, and is configured using the LK8 jumper. This jumper position selects the regulator output to the V_{DD1} pin. Options of 1.8 V, 2.5 V, 3.3 V, and 5 V are available. To bypass the V_{DD1} ADP7104 regulator, U1, and power the V_{DD1} pin directly from the VDD1 terminal, insert the LK8 jumper into Position E.

The V_{DD2} regulator, U3, is powered from the VDD2 terminal on Connector P6, and is configured using the LK9 jumper. This jumper position selects the regulator output to the ADM2463E or ADM2763E V_{DD2} pin. Options of 3.3 V and 5 V are available. To bypass the V_{DD2} regulator, U3, and power the V_{DD2} pin directly from the VDD2 terminal, insert the LK9 jumper into Position C.

Table 2 and Table 3 lists the supported power supply configurations and the associated jumper configurations.

FULL DUPLEX RS-485 TRANSCEIVERS LOOPBACK TEST

A loopback test can be set up with the EVAL-ADM2463EEBZ/EVAL-ADM2763EEBZ by closing the LK4 and LK5 jumpers. The details of this test are shown in Table 1 and in Figure 2. A signal generator is connected to the TxD pin, which allows verification of the bus signals and the receiver output. Note that during the test, the jumper position for LK1 is Position C, LK2 is Position A, and LK3 is Position C. See Table 2 for the jumper configurations for different power supply configurations. The LK6 and LK7 jumpers can be inserted to terminate the transmitter and receiver with 120 Ω resistors. Connect both jumpers when the board is configured in parallel by the loopback to ensure that the test is conducted with a standard RS-485 load of 60 Ω (bus terminated at both ends by 120 Ω).

Table 2. Primary Side Input Supply Configurations

Jumper LK8	VDD1 Input Voltage Range	V_{DD1} Supply
A	2.2 V to 20 V	Regulator provides 1.8 V
B	2.9 V to 20 V	Regulator provides 2.5 V
C	3.7 V to 20 V	Regulator provides 3.3 V
D	5.4 V to 20 V	Regulator provides 5 V
E	1.7 V to 5.5 V	Supplied directly from the VDD1 terminal on P5

Table 3. Secondary Side Input Supply Configurations

Jumper LK9	VDD2 Input Voltage Range	V_{DD2} Supply
A	3.7 V to 20 V	Regulator provides 3.3 V
B	5.4 V to 20 V	Regulator provides 5 V
C	3 V to 5.5 V	Supplied directly from the VDD2 terminal on P6

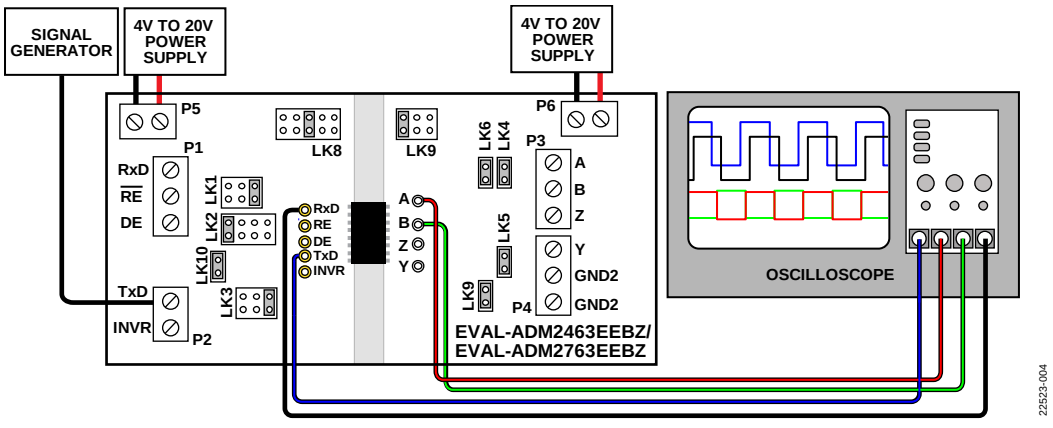

Figure 2. Full Duplex RS-485 Loopback Test

IEC 61000-4-2 ELECTROSTATIC DISCHARGE (ESD) PROTECTION

The EVAL-ADM2463EEBZ/EVAL-ADM2763EEBZ are tested and verified to achieve protection against IEC 61000-4-2 ESD to ≥±12 kV (contact discharge) and ≥±15 kV (air discharge) on the ADM2463E or ADM2763E Pin A, Pin B, Pin Y, and Pin Z.

The IEC 61000-4-2 ESD standard describes testing using two coupling methods known as contact discharge and air discharge. Contact discharge implies a direct contact between the discharge gun and the equipment under test (EUT). The ADM2463E or ADM2763E is tested using both of these methods.

During testing, the ADM2463E or ADM2763E Pin A, Pin B, Pin Y, and Pin Z are subjected to at least 10 positive and 10 negative single discharges with a 1 sec interval between each pulse. The highest specified IEC 61000-4-2 ESD test is Level 4, which defines a contact discharge voltage of ±8 kV and an air discharge voltage of ±15 kV.

EVALUATION BOARD SCHEMATIC AND ARTWORK

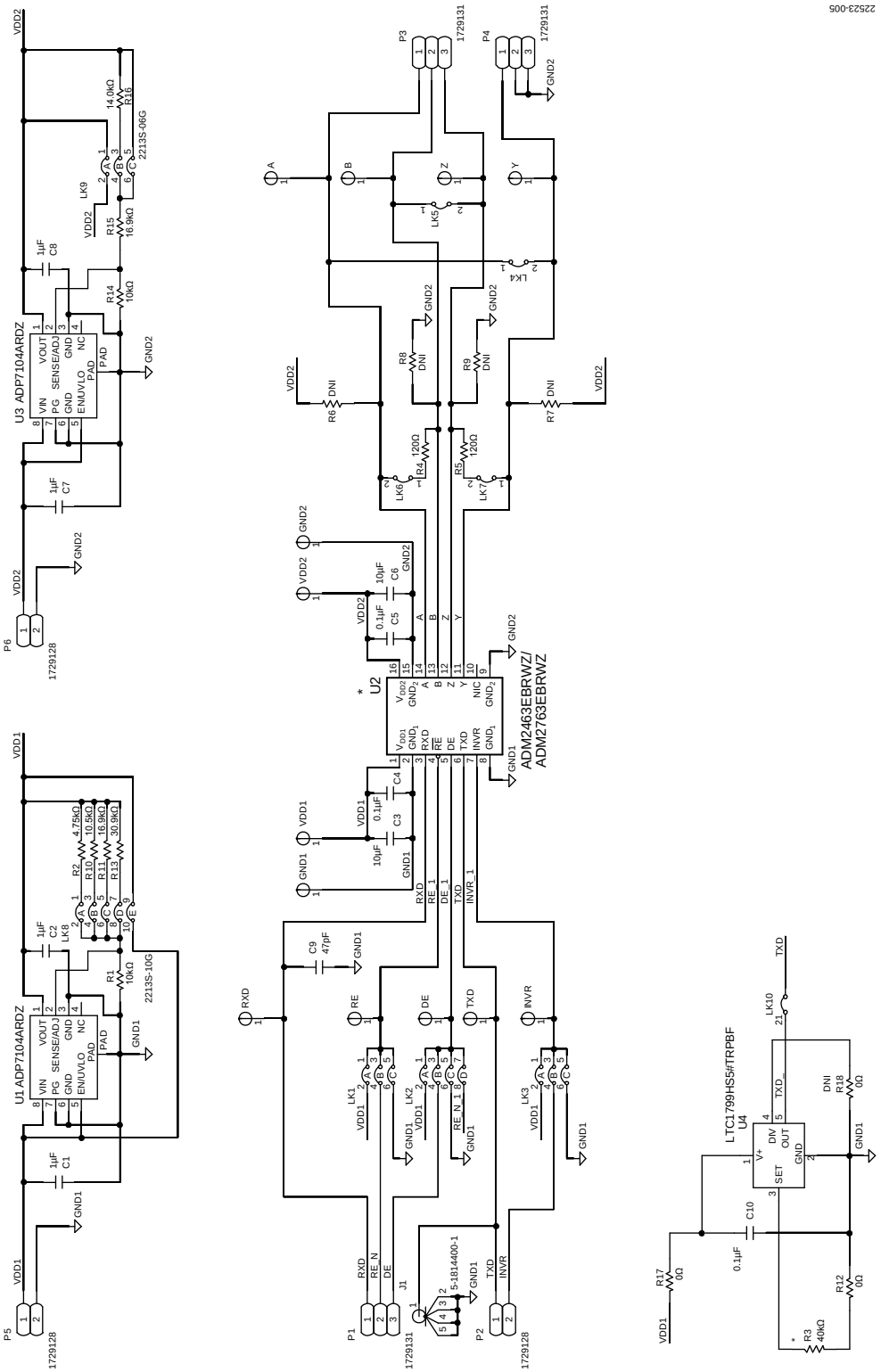

Figure 3. EVAL-ADM2463EEBZ/EVAL-ADM2763EEBZ Schematic

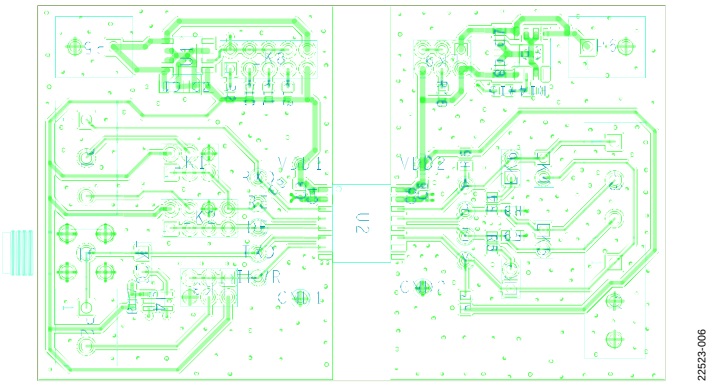

Figure 4. EVAL-ADM2463EEBZ/EVAL-ADM2763EEBZ Component Side, Layer 1

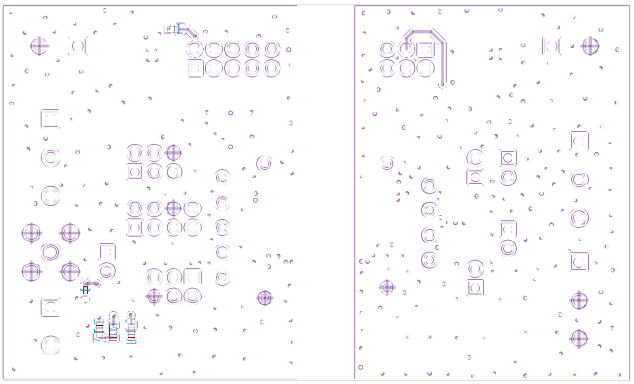

Figure 5. EVAL-ADM2463EEBZ/EVAL-ADM2763EEBZ, Layer 2

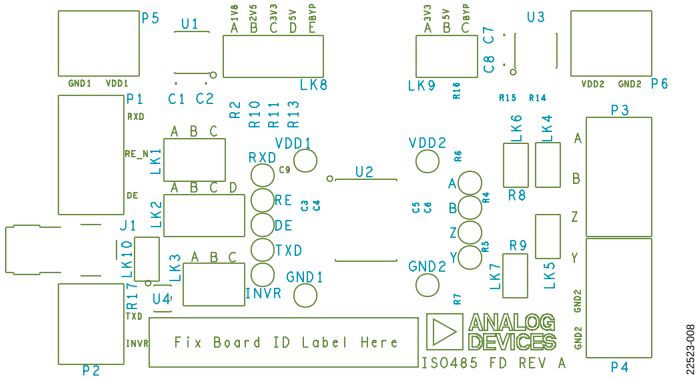

Figure 6. EVAL-ADM2463EEBZ/EVAL-ADM2763EEBZ, Silkscreen

ORDERING INFORMATION

BILL OF MATERIALS

Table 4. EVAL-ADM2463EEBZ/EVAL-ADM2763EEBZ Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Part Number
9	A, B, DE, INVR, $\overline{RE}$, RxD, TxD, Y, Z	Test points, yellow	Keystone Electronics	36-5004-ND
3	C4, C5, C10	Capacitors, 0.1 µF, 0402	Murata	GRM155R61E104KA87D
4	C1, C2, C7, C8	Capacitors, 1 µF, 0805	Murata	GCM21BR71E105KA56L
2	C3, C6	Capacitors, 10 µF, 0805	TDK	C2012X5R1E106K085AC
1	C9	Capacitor, 47 pF, 0603	AVX Corporation	06035A470JAT2A
2	GND1, GND2	Test points, black	Components Corporation	TP-105-01-00
1	J1	Coaxial, right angle SMA connector	TE Connectivity	5-1814400-1
3	LK1, LK3, LK9	6-pin (3 × 2), 0.1 inch headers and shorting blocks	Multicomp	2213S-06G
1	LK2	8-pin (4 × 2), 0.1 inch header and shorting block	Multicomp	2213S-08G
1	LK8	10-pin (5 × 2), 0.1 inch header and shorting block	Multicomp	2213S-10G
5	LK4 to LK7, LK10	2-pin (1 × 2), 0.1 inch headers and shorting blocks	Harwin	M20-9990246
3	P1, P3, P4	Three-position terminal blocks	Phoenix Contact	1729131
3	P2, P5, P6	Two-position terminal blocks	Phoenix Contact	1729128
2	R12, R17	Resistors, 0 Ω, 0603	Multicomp	MC0603WG00000T5E-TC
1	R18	Resistor, do not install (DNI), 0603	Not applicable	Not applicable
2	R1, R14	Resistors, 10 kΩ, 0603	Panasonic	ERJ-3EKF1002V
1	R10	Resistor, 10.5 kΩ, 0603	Panasonic	ERA-3AEB1052V
2	R11, R15	Resistors, 16.9 kΩ, 0603	Panasonic	ERJ-3EKF1692V
1	R13	Resistor, 30.9 kΩ, 0603	Panasonic	ERJ-3EKF3092V
1	R16	Resistor, 14 kΩ, 0603	Panasonic	ERJ-3EKF1402V
1	R2	Resistor, 4.75 kΩ, 0603	Panasonic	ERJ-3EKF4751V
1	R3	Resistor, 40 kΩ, 0603	Vishay	CRCW060340K0FKEA
4	R6 to R9	Resistors, DNI, 0805	Not applicable	Not applicable
2	R4, R5	Resistors, 120 Ω, 0805	Panasonic	ERJ-P6WF1200V
2	U1, U3	Low noise CMOS LDO regulators	Analog Devices	ADP7104ARDZ-R7
1	U2	500 kbps, 5.7 kV, signal isolated RS-485 transceiver, and 500 kbps, high working voltage isolated RS-485 transceiver	Analog Devices	ADM2463EBRWZ, ADM2763EBRWZ
1	U4	1 kHz to 33 MHz oscillator	Analog Devices	LTC1799HS5#TRPBF
2	VDD1, VDD2	Test points, red	Components Corporation	TP-105-01-02

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG22523-6/20(0)

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