5.7 kV rms, Signal Isolated, Basic CAN FD Transceiver

Enhanced Product

ADM3050E-EP

FEATURES

- 5.7 kV rms signal isolated CAN FD transceiver
- 1.7 V to 5.5 V supply and logic side levels
- 4.5 V to 5.5 V supply on bus side
- ISO 11898-2:2016-compliant CAN FD
- Data rates up to 12 Mbps for CAN FD
- Low maximum loop propagation delay: 145 ns
- Extended common-mode range (V_{CANx}): ±25 V
- Bus fault protection (CANH, CANL): ±40 V
- Passes EN 55022, Class B by 6 dB
- Safety and regulatory approvals
  - VDE certificate of conformity, VDE V 0884-10 (pending)
  - UL: 5700 V rms for 1-minute duration per UL 1577 (pending)
  - CSA component acceptance 5A at 5.7 kV rms
    - IEC 60950, IEC 61010 (pending)
- High CMTI: >75 kV/µs

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range (−55°C to +125°C)
- Controlled manufacturing baseline
- 1 assembly/test site
- 1 fabrication site
- Product change notification
- Qualification data available on request

APPLICATIONS

- CANOpen, DeviceNet, and other CAN bus implementations
- Industrial automation
- Military and aerospace (MILA) avionics for sensors, actuators, and engine control

FUNCTIONAL BLOCK DIAGRAM

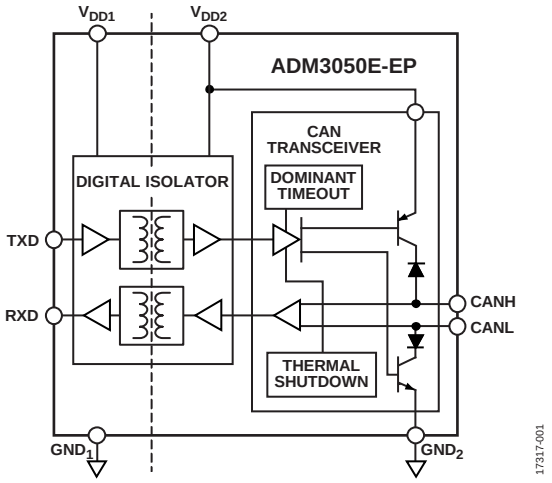

Figure 1.

GENERAL DESCRIPTION

The ADM3050E-EP is a 5.7 kV rms isolated controller area network (CAN) physical layer transceiver with a high performance, basic feature set. The ADM3050E-EP fully meets the CAN flexible data rate (CAN FD) ISO 11898-2:2016 requirements and is further capable of supporting data rates as high as 12 Mbps.

The device employs Analog Devices, Inc., *i*Coupler® technology to combine a 2-channel isolator and a CAN transceiver into a single small outline integrated circuit (SOIC) surface-mount package. The ADM3050E-EP is a fully isolated solution for CAN and CAN FD applications. The ADM3050E-EP provides isolation between the CAN controller and physical layer bus. Safety and regulatory approvals (pending) for a 5.7 kV rms withstand voltage, an 849 V_{PEAK} working voltage, and a 12.8 kV surge test, ensure that the ADM3050E-EP meets application isolation requirements.

Low loop propagation delays and the extended common-mode range of ±25 V support robust communication on longer bus cables. Dominant timeout functionality protects against bus lock up in a fault condition, and current limiting and thermal shutdown features protect against output short circuits. The CAN bus input and output pins are protected to ±40 V against accidental connection to a +24 V bus supply. The device is fully specified over the −55°C to +125°C industrial temperature range.

Additional application and technical information can be found in the ADM3050E data sheet.

Rev. 0 Document Feedback

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REVISION HISTORY

2/2019—Revision 0: Initial Version

SPECIFICATIONS

All voltages are relative to their respective ground, 1.7 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −55°C ≤ T_A ≤ +125°C, unless otherwise noted. Typical specifications are at V_{DD1} = V_{DD2} = 5 V and T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						
Bus Side	I_{DD2}					
Recessive State			5.3	7	mA	TXD high, load resistance (R_L) = 60 Ω
Dominant State			63	75	mA	Limited by transmit dominant timeout (t_{DT}), R_L = 60 Ω
				73	mA	Limited by t_{DT}, R_L = 60 Ω, 4.75 V ≤ V_{DD2} ≤ 5.25 V
70% Dominant/30% Recessive						Worst case, R_L = 60 Ω
1 Mbps			45	58	mA	
5 Mbps			49	60	mA	
12 Mbps			58	65	mA	
Logic Side *i*Coupler Current	I_{DD1}			5.5	mA	TXD high, low, or switching
DRIVER						
Differential Outputs						See Figure 18
Recessive State Voltage						TXD high, R_L, and common-mode filter capacitor (C_F) open
CANH, CANL	V_{CANL}, V_{CANH}	2.0		3.0	V	
Differential Output	V_{OD}	−500		+50	mV	
Dominant State Voltage						TXD low, C_F open
CANH	V_{CANH}	2.75		4.5	V	50 Ω ≤ R_L ≤ 65 Ω
CANL	V_{CANL}	0.5		2.0	V	50 Ω ≤ R_L ≤ 65 Ω
Differential Output	V_{OD}	1.5		3.0	V	50 Ω ≤ R_L ≤ 65 Ω
		1.4		3.3	V	45 Ω ≤ R_L ≤ 70
		1.5		5.0	V	R_L = 2240 Ω
Output Symmetry (V_{DD2} − V_{CANH} to V_{CANL})	V_{SYM}	−0.55		+0.55	V	R_L = 60 Ω, C_F = 4.7 nF
Short-Circuit Current	$\|I_{SC}\|$					R_L open
Absolute						
CANH				115	mA	V_{CANH} = −3 V
CANL				115	mA	V_{CANL} = 18 V
Steady State						
CANH				115	mA	V_{CANH} = −24 V
CANL				115	mA	V_{CANL} = 24 V
Logic Input TXD						
Input Voltage						
High	V_{IH}	0.65 × V_{DD1}			V	
Low	V_{IL}			0.35 × V_{DD1}	V	
Complementary Metal-Oxide Semiconductor (CMOS) Logic Input Currents	$\|I_{IH}\|$, $\|I_{IL}\|$			10	μA	Input high or low
RECEIVER						
Differential Inputs						
Differential Input Voltage Range	V_{ID}					See Figure 19, RXD capacitance (C_{RXD}) open, −25 V < V_{CANL}, V_{CANH} < +25 V
Recessive		−1.0		+0.5	V	
Dominant		0.9		5.0	V	
Input Voltage Hysteresis	V_{HYS}		150		mV	
Unpowered Input Leakage Current	$\|I_{IN\ (OFF)}\|$			10	μA	V_{CANH}, V_{CANL} = 5 V, V_{DD2} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Input Resistance						
CANH, CANL	R_{INH}, R_{INL}	6		25	kΩ	
Differential	R_{DIFF}	20		100	kΩ	
Input Resistance Matching	m_R	−0.03		+0.03		$m_R = 2 \times (R_{INH} - R_{INL})/(R_{INH} + R_{INL})$
CANH, CANL Input Capacitance	C_{INH}, C_{INL}		35		pF	
Differential Input Capacitance	C_{DIFF}		12		pF	
Logic Output (RXD)						
Output Voltage						
Low	V_{OL}		0.2	0.4	V	Output impedance (I_{OUT}) = 2 mA
High	V_{OH}	V_{DD1} − 0.2			V	I_{OUT} = −2 mA
Short-Circuit Current	I_{OS}	7		85	mA	Output voltage (V_{OUT}) = GND_1 or V_{DD1}
COMMON-MODE TRANSIENT IMMUNITY (CMTI)[1]						Common-mode voltage (V_{CM}) ≥ 1 kV, transient magnitude ≥ 800 V
Input High, Recessive	$\|CM_H\|$	75	100		kV/µs	Input voltage (V_{IN}) = V_{DD1} (TXD) or CANH/CANL recessive
Input Low, Dominant	$\|CM_L\|$	75	100		kV/µs	V_{IN} = 0 V (TXD) or CANH/CANL dominant

[1] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining CANH/CANL recessive or RXD ≥ V_{DD1} − 0.2 V. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining CANH/CANL dominant or RXD ≤ 0.4 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

TIMING SPECIFICATIONS

All voltages are relative to their respective ground, 1.7 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −55°C ≤ T_A ≤ +125°C, unless otherwise noted. Typical specifications are at V_{DD1} = V_{DD2} = 5 V and T_A = 25°C, unless otherwise noted. See the ADM3050E data sheet for information about t_{BIT_BUS}.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						See Figure 2 and Figure 18, t_{BIT_TXD} = 200 ns, R_L = 60 Ω, C_L = 100 pF
Maximum Data Rate		12			Mbps	
Propagation Delay from TXD to Bus (Recessive to Dominant)	t_{TXD_DOM}		35	60	ns	
Propagation Delay from TXD to Bus (Dominant to Recessive)	t_{TXD_REC}		45	70	ns	
Transmit Dominant Timeout	t_{DT}	1175		4000	µs	TXD low, see Figure 3
RECEIVER						See Figure 2 and Figure 20, t_{BIT_TXD} = 200 ns, R_L = 60 Ω, C_L = 100 pF, C_{RXD} = 15 pF
Falling Edge Loop Propagation Delay (TXD to RXD)	t_{LOOP_FALL}			145	ns	
Rising Edge Loop Propagation Delay (TXD to RXD)	t_{LOOP_RISE}			145	ns	
Loop Delay Symmetry (Minimum Recessive Bit Width)	t_{BIT_RXD}					
2 Mbps		450		550	ns	t_{BIT_TXD} = 500 ns
5 Mbps		160		220	ns	t_{BIT_TXD} = 200 ns
8 Mbps		85		140	ns	t_{BIT_TXD} = 125 ns
12 Mbps		50		91.6	ns	t_{BIT_TXD} = 83.3 ns

Timing Diagrams

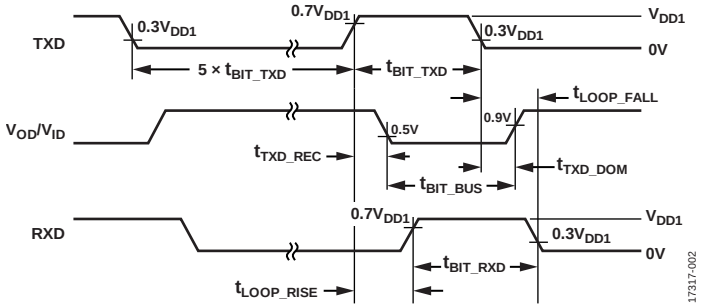


Figure 2. Transceiver Timing Diagram

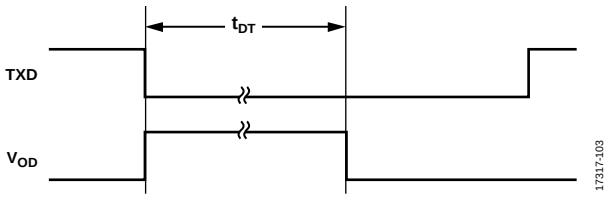


Figure 3. Dominant Timeout, t_{DT}

INSULATION AND SAFETY RELATED SPECIFICATIONS

For additional information, see www.analog.com/icouplersafety.

Table 3.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5700	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (I01)	7.8	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	7.8	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB) Clearance	L (PCB)	8.3	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		25.5	µm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN IEC 112/VDE 0303 Part 1
Material Group		I		Material group (DIN VDE 0110, 1/89, Table 1)

PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		1.1		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	

[1] The device is considered a two-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

See Table 9 and the ADM3050E data sheet for the recommended maximum working voltages for specific cross isolation waveforms and insulation levels. The ADM3050E-EP is pending approval or approved by the organizations listed in Table 5.

Table 5.

UL (Pending)	CSA (Pending)	VDE (Pending)	CQC (Pending)
UL1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]	Certified under CQC11-471543-2012
Single Protection, 5700 V rms Isolation Voltage	CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2:	Reinforced insulation, 849 V_{PEAK}, V_{IOTM} = 8 kV_{PEAK}	GB4943.1-2011
	Basic insulation at 780 V rms (1103 V_{PEAK})		Basic insulation at 780 V rms (1103 V_{PEAK})
	Reinforced insulation at 390 V rms (552 V_{PEAK})		Reinforced insulation at 390 V rms (552 V_{PEAK})
	IEC 60601-1 Edition 3.1:		
	Basic insulation (1 MOPP), 490 V rms (686 V_{PEAK})		
	Reinforced insulation (2 MOPP), 238 V rms (325 V_{PEAK})		
	CSA 61010-1-12 and IEC 61010-1 third edition:		
	Basic insulation at: 300 V rms mains, 780 V secondary (1103 V_{PEAK})		
	Reinforced insulation at: 300 V rms mains, 390 V secondary (552 V_{PEAK})		
File E214100	File 205078	File 2471900-4880-0001	File (pending)

[1] In accordance with UL 1577, each ADM3050E-EP is proof tested by applying an insulation test voltage ≥ 6840 V rms for 1 sec.
[2] In accordance with DIN V VDE V 0884-10, each ADM3050E-EP is proof tested by applying an insulation test voltage ≥ 1592 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS (PENDING)

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data.

Table 6.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 600 V rms			I to IV	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage				
Reinforced		V_{IORM}	849	V_{PEAK}
Basic, DC Working Voltage	See the Absolute Maximum Ratings section and Table 9 for the maximum continuous working voltage for ac bipolar, ac unipolar, and dc voltages, basic and reinforced insulation, and 50 year lifetime to 1% failure	$V_{IORM(DC)}$	1500	V_{DC}
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1592	V_{PEAK}
Input to Output Test Voltage, Method A		$V_{pd(m)}$		
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1274	V_{PEAK}
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1019	V_{PEAK}
Highest Allowable Overvoltage		V_{IOTM}	8000	V_{PEAK}
Impulse	1.2 µs rise time, 50 µs, 50% fall time in air to the preferred sequence	$V_{IMPULSE}$	8000	V_{PEAK}
Surge Isolation Voltage				V_{PEAK}
Basic	V_{PEAK} = 12.8 kV, 1.2 µs rise time, 50 µs, and 50% fall time	V_{IOSM}	12000	V_{PEAK}
Reinforced	V_{PEAK} = 12.8 kV, 1.2 µs rise time, 50 µs, and 50% fall time	V_{IOSM}	8000	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 4)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	2.08	W
Insulation Resistance at T_S	Test voltage = 500 V	R_S	$>10^9$	Ω

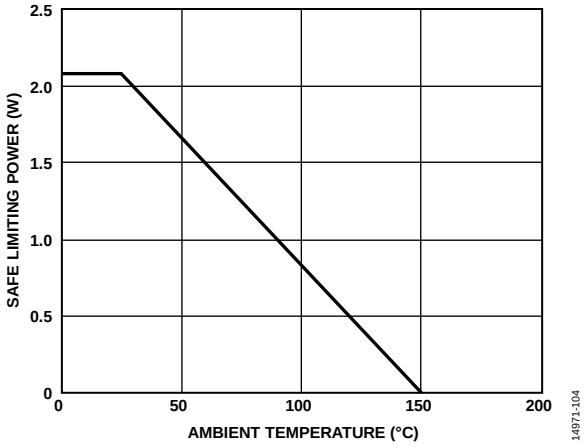


Figure 4. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-10 (See the Thermal Resistance Section for Additional Information)

ABSOLUTE MAXIMUM RATINGS

Pin voltages with respect to GND_1/GND_2 are on same side, unless otherwise noted.

Table 7.

Parameter	Rating
V_{DD1}/V_{DD2}	−0.5 V to +6 V
Logic Side Input and Output: TXD, RXD	−0.5 V to V_{DD1} + 0.5 V
CANH, CANL	−40 V to +40 V
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature (T_J)	150°C
Electrostatic Discharge (ESD), IEC 61000-4-2, CANH/CANL	
Across Isolation Barrier with Respect to GND_1	±8 kV
Contact Discharge with Respect to GND_2	±8 kV typical
Air Discharge with Respect to GND_2	±15 kV
Human Body Model (HBM), All Pins, 1.5 kΩ, 100 pF	±4 kV
Moisture Sensitivity Level (MSL)	MSL3

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

The thermal resistance value specified in Table 8 is simulated based on JEDEC specifications (unless specified otherwise) and must be used in compliance with JESD51-12.

Table 8. Thermal Resistance

Package Type	θ_{JA}	Unit
RW-16[1]	60	°C/W

[1] The θ_{JA} value is based on simulations of a devices mounted on a JEDEC standard, 4-layer board with fine width traces and still air. See the ADM3050E data sheet for the thermal model definitions.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 9. Maximum Continuous Working Voltage[1]

Parameter	Insulation Rating (20-Year Lifetime)[2]	VDE 0884-11 Lifetime Conditions Fulfilled
AC Voltage		
Bipolar Waveform		
Basic Insulation	849 V_{PEAK}	Lifetime limited by insulation lifetime per VDE-0884-11
Reinforced Insulation	707 V_{PEAK}	Lifetime limited by insulation lifetime per VDE-0884-11
Unipolar Waveform		
Basic Insulation	1697 V_{PEAK}	Lifetime limited by insulation lifetime per VDE-0884-11
Reinforced Insulation	1275 V_{PEAK}	Lifetime limited by package creepage per IEC 60664-1
DC Voltage		
Basic Insulation	1560 V_{PEAK}	Lifetime limited by package creepage per IEC 60664-1
Reinforced Insulation	780 V_{PEAK}	Lifetime limited by package creepage per IEC 60664-1

[1] The maximum continuous working voltage refers to the continuous voltage magnitude imposed across the isolation barrier. See the ADM3050E data sheet for more details.

[2] Insulation capability without regard to creepage limitations. Working voltage may be limited by the PCB creepage when considering rms voltages for components soldered to a PCB (assumes Material Group I up to 1250 V rms), or by the SOIC_W package creepage of 7.8 mm, when considering rms voltages for Material Group II.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

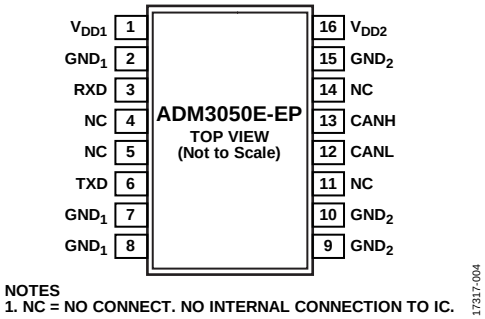


Figure 5. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Power Supply, Logic Side, 1.7 V to 5.5 V. This pin requires a 0.1 µF decoupling capacitor.
2, 7, 8	GND_1	Ground, Logic Side.
3	RXD	Receiver Output Data.
4, 5, 11, 14	NC	No Connect. No internal connection to IC.
6	TXD	Driver Input Data.
9, 10, 15	GND_2	Ground, Bus Side.
12	CANL	CAN Low Input and Output.
13	CANH	CAN High Input and Output.
16	V_{DD2}	Power Supply, Bus Side, 4.5 V to 5.5 V. This pin requires a 0.1 µF decoupling capacitor.

OPERATIONAL TRUTH TABLE

Table 11. Truth Table

V_{DD1}	V_{DD2}	TXD	Mode	RXD	CANH/CANL
On	On	Low	Normal	Low	Dominant (limited by t_{DT})
On	On	High	Normal	High per bus	Recessive and set by bus
Off	On	Don't care	Normal	Indeterminate	Recessive and set by bus
On	Off	Don't care	Transceiver off	High	High-Z

TYPICAL PERFORMANCE CHARACTERISTICS

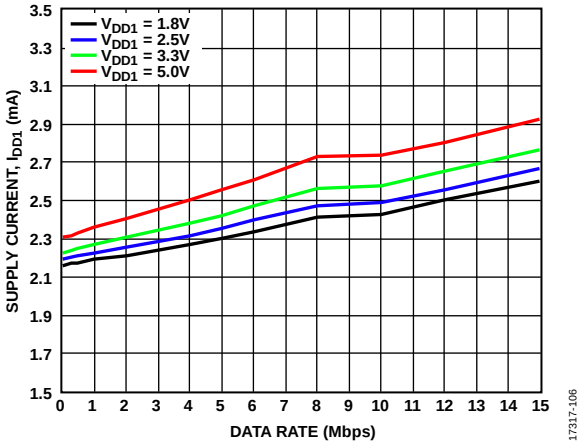


Figure 6. Supply Current (I_{DD1}) vs. Data Rate

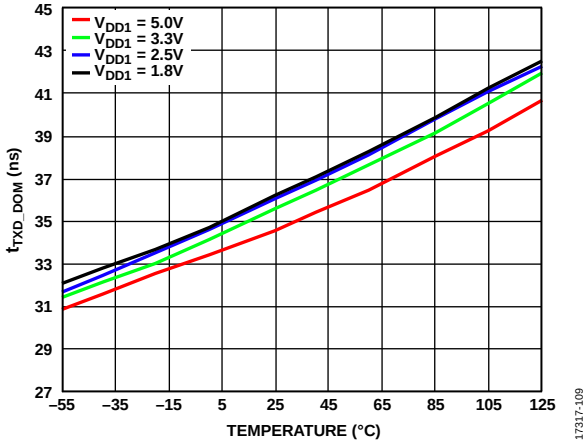


Figure 9. t_{TXD_DOM} vs. Temperature

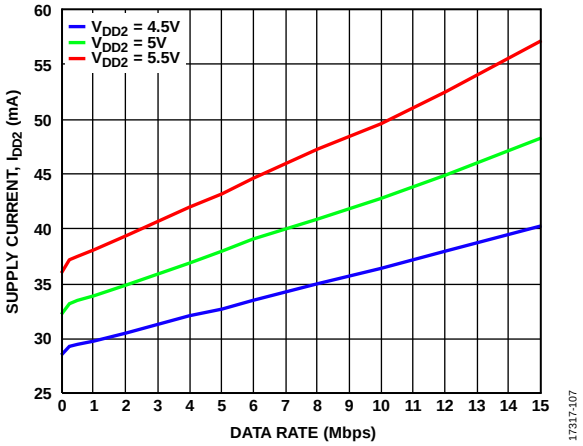


Figure 7. Supply Current (I_{DD2}) vs. Data Rate

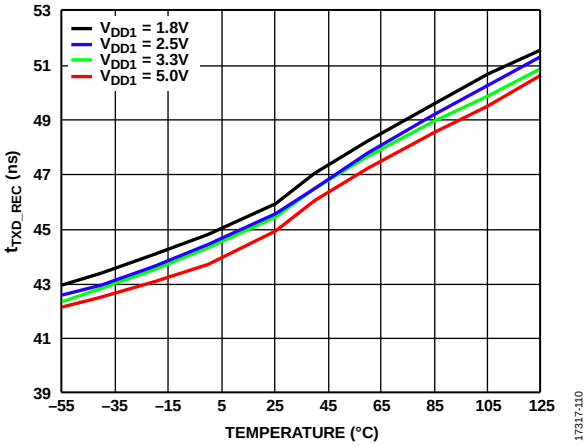


Figure 10. t_{TXD_REC} vs. Temperature

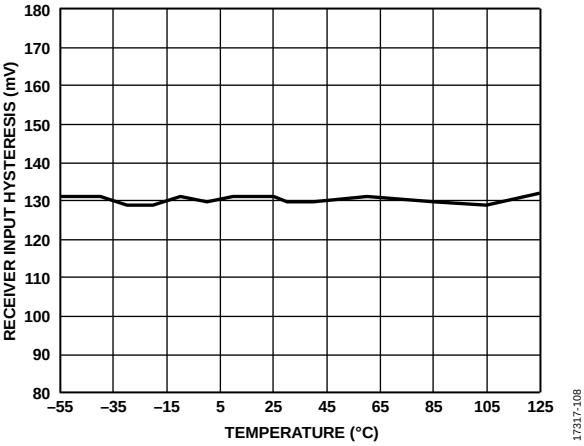


Figure 8. Receiver Input Hysteresis vs. Temperature

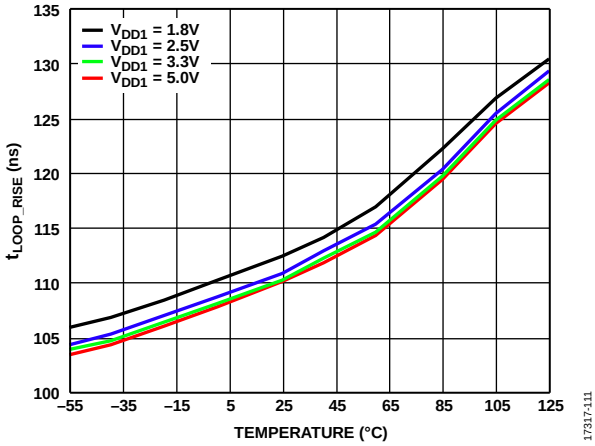


Figure 11. t_{LOOP_RISE} vs. Temperature

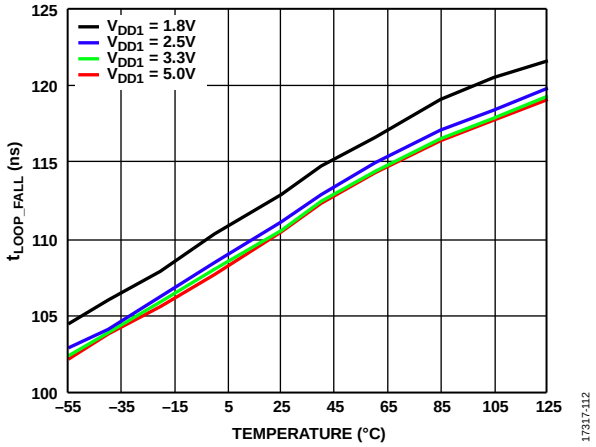


Figure 12. t_{LOOP_FALL} vs. Temperature

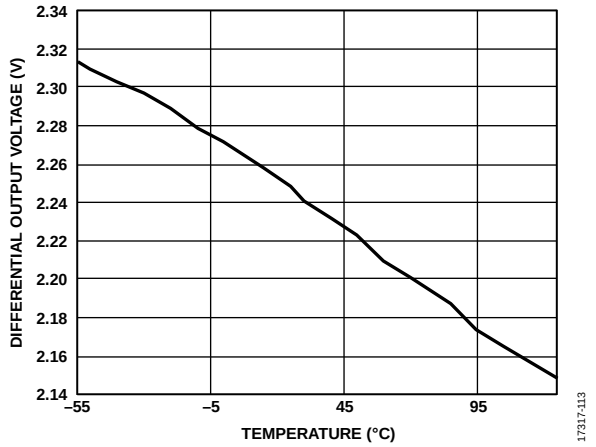


Figure 13. Differential Output Voltage vs. Temperature, R_L = 60 Ω

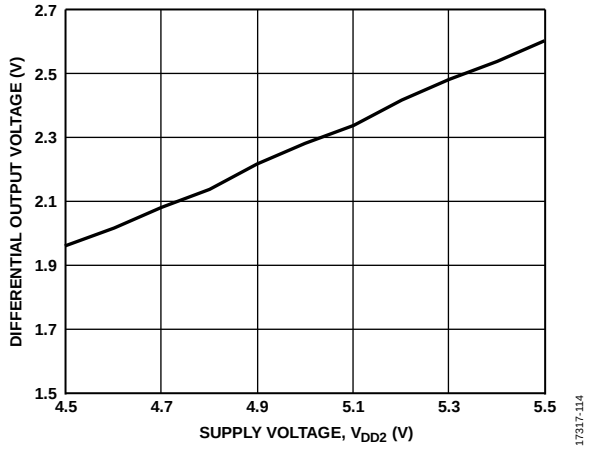


Figure 14. Differential Output Voltage vs. Supply Voltage (V_{DD2}), R_L = 60 Ω

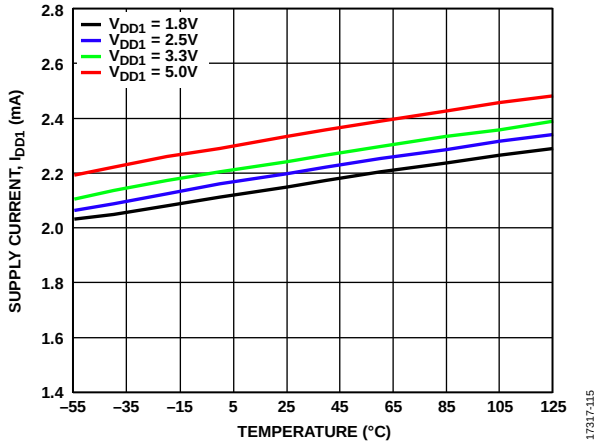


Figure 15. Supply Current (I_{DD1}) vs. Temperature

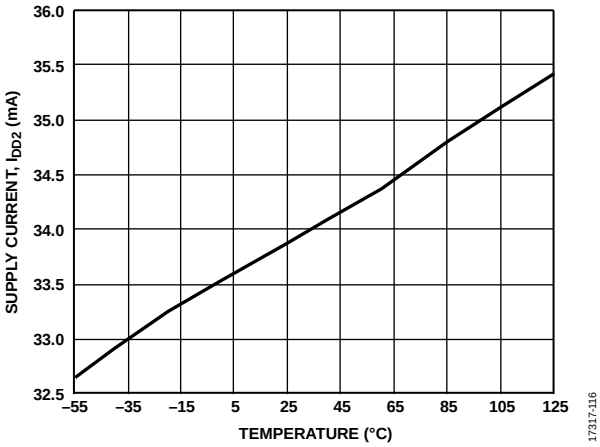


Figure 16. Supply Current (I_{DD2}) vs. Temperature

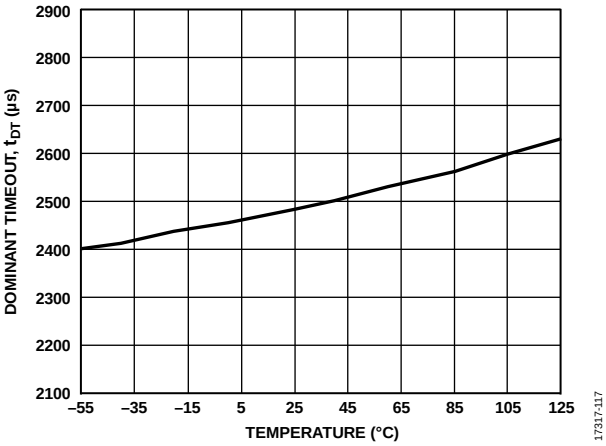


Figure 17. Dominant Timeout (t_{DT}) vs. Temperature

TEST CIRCUITS

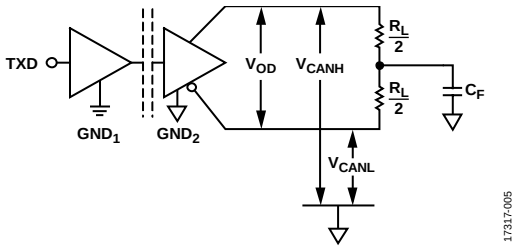


Figure 18. Driver Voltage Measurement

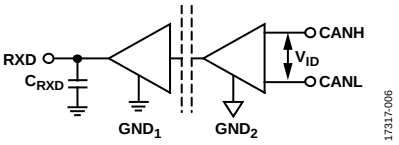
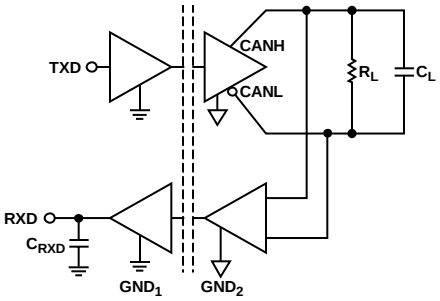


Figure 19. Receiver Voltage Measurement



NOTES
1. 1% TOLERANCE FOR ALL RESISTORS AND CAPACITORS.

Figure 20. Switching Characteristics Measurements

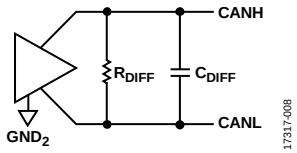


Figure 21. R_{DIFF} and C_{DIFF} Measured in Recessive State, Bus Disconnected

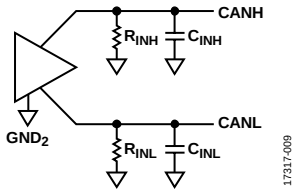


Figure 22. Input Resistance (R_{INx}) and Input Capacitance (C_{INx}) Measured in Recessive State, Bus Disconnected

OUTLINE DIMENSIONS

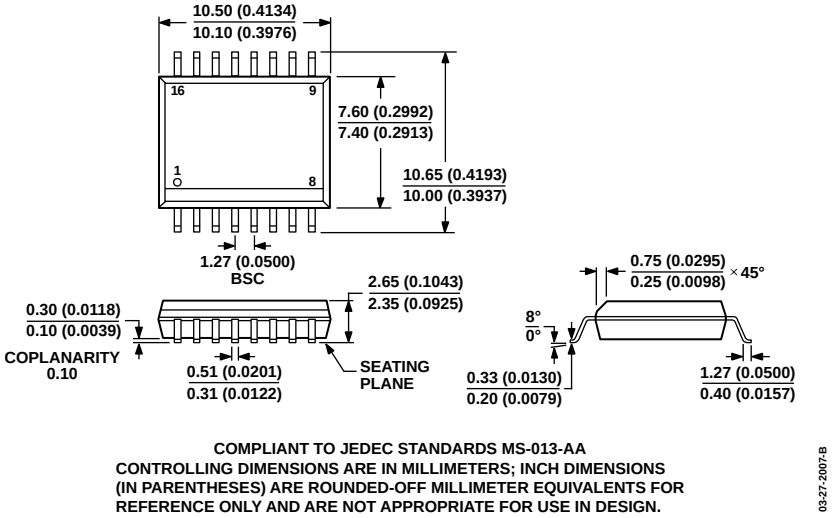


Figure 23. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADM3050ETRWZ-EP	−55°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADM3050ETRWZ-EP-RL	−55°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
EVAL-ADM3050EEBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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