Isolated CAN Transceiver with Integrated High Voltage, Bus-Side, Linear Regulator

Data Sheet **ADM3052**

FEATURES

- **5 kV rms isolated CAN transceiver**
- **Integrated V_+ linear regulator**
- **Bus side powered by V_+ and V_-**
- **11 V to 25 V operation on V_+**
- **5 V or 3.3 V operation on V_{DD1}**
- **Complies with ISO 11898 standard**
- **High speed data rates up to 1 Mbps**
- **Short-circuit protection on bus pins**
- **Integrated bus miswire protection**
- **Unpowered nodes do not disturb the bus**
- **110 or more nodes on the bus**
- **Thermal shutdown protection**
- **High common-mode transient immunity: >25 kV/μs**
- **Safety and regulatory approvals**
  - **UL recognition**
    - **5000 V_{RMS} for 1 minute per UL 1577**
  - **VDE Certificates of Conformity**
    - **DIN V VDE V 0884-10 (VDE V 0884-10):2006-12**
    - **V_{IORM} = 846 V peak**
- **Industrial operating temperature range: −40°C to +85°C**
- **Wide body, 16-lead SOIC package**

APPLICATIONS

- **CAN data buses**
- **Industrial field networks**
- **DeviceNet applications**

GENERAL DESCRIPTION

The ADM3052 is an isolated controller area network (CAN) physical layer transceiver with a V_+ integrated linear regulator. The ADM3052 complies with the ISO 11898 standard.

The device employs Analog Devices, Inc., *i*Coupler® technology to combine a 3-channel isolator, a CAN transceiver, and a linear regulator into a single package. The power is isolated between a single 3.3 V or 5 V supply on V_{DD1}, the logic side, and a single 24 V supply provided on V_+, the bus side.

The ADM3052 creates an isolated interface between the CAN protocol controller and the physical layer bus. It is capable of running at data rates up to 1 Mbps.

The device has integrated miswire protection on the bus pins, V_+, V_-, CANH, and CANL.

The device has current-limiting and thermal shutdown features to protect against output short circuits and situations where the bus may be shorted to ground or power terminals. The device is fully specified over the industrial temperature range and is available in a 16-lead, wide-body SOIC package.

FUNCTIONAL BLOCK DIAGRAM

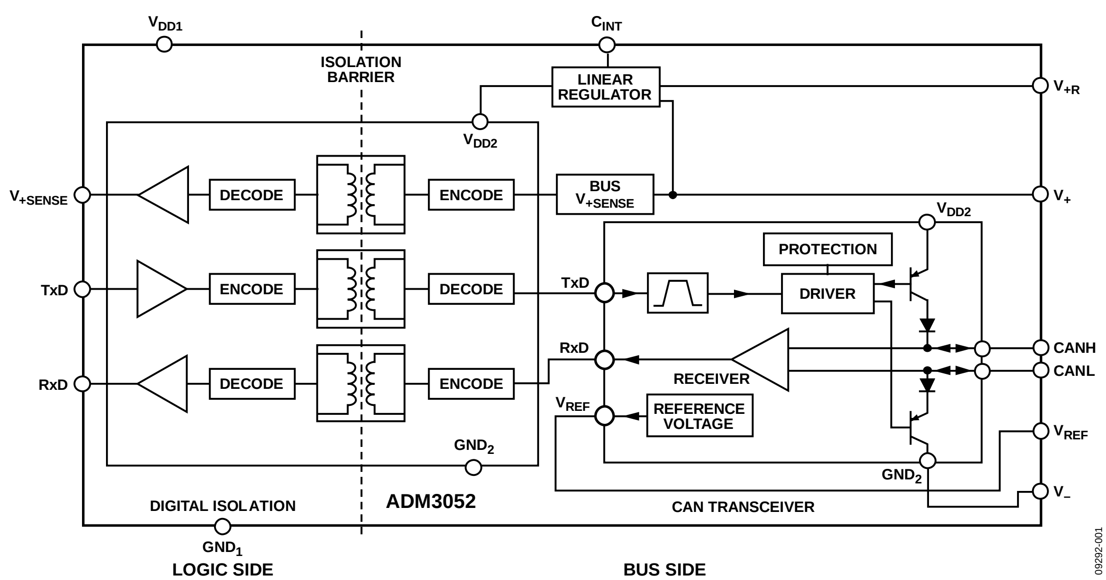

Figure 1.

Rev. B Document Feedback

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REVISION HISTORY

6/2016—Rev. A to Rev. B

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12/2012—Rev. 0 to Rev. A

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Changed VDE 0884 Insulation Characteristics (Pending) Section to VDE 0884 Insulation Characteristics Section ... 5
Changes to Table Summary Text Prior to Table 5 ... 5
Added DeviceNet™ and the ADM3052 CAN Transceiver Section ... 17

6/2011—Revision 0: Initial Version

SPECIFICATIONS

All voltages are relative to their respective ground; 3.0 V ≤ V_{DD1} ≤ 5.5 V, T_A = −40°C to +85°C, V_+ = 11 V to 25 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SUPPLY CURRENT						
Power Supply Current Logic Side						
TxD/RxD Data Rate 1 Mbps	I_{DD1}		0.7	2	mA	
Power Supply Current Bus Side						
Recessive State	I_+			10	mA	R_L = 60 Ω, see Figure 26
Dominant State	I_+		64	75	mA	R_L = 60 Ω, see Figure 26
TxD/RxD Data Rate 1 Mbps	I_+		48	55	mA	R_L = 60 Ω, see Figure 26
EXTERNAL RESISTOR						
Resistance	R_P	297	300	303	Ω	
Power Rating		0.75			W	
DRIVER						
Logic Inputs						
Input Voltage High	V_{IH}	0.7 V_{DD1}			V	TxD
Input Voltage Low	V_{IL}			0.25 V_{DD1}	V	TxD
CMOS Logic Input Currents	I_{IH}, I_{IL}			500	µA	TxD
Differential Outputs						
Recessive Bus Voltage	V_{CANL}, V_{CANH}	2.0		3.0	V	V_{TxD} = high, R_L = ∞, see Figure 23
CANH Output Voltage	V_{CANH}	2.75		4.5	V	V_{TxD} = low, see Figure 23
CANL Output Voltage	V_{CANL}	0.5		2.0	V	V_{TxD} = low, see Figure 23
Differential Output Voltage	V_{OD}	1.5		3.0	V	V_{TxD} = low, R_L = 45 Ω, see Figure 23
	V_{OD}	−500		+50	mV	V_{TxD} = high, R_L = ∞, see Figure 23
Short-Circuit Current, CANH	I_{SCCANH}			−200	mA	V_{CANH} = −5 V
			−100		mA	V_{CANH} = −36 V
Short-Circuit Current, CANL	I_{SCCANL}			200	mA	V_{CANL} = 36 V
RECEIVER						
Differential Inputs						
Voltage Recessive	V_{IDR}	−1.0		+0.5	V	−7 V < V_{CANL}, V_{CANH} < 12 V, see Figure 24, C_L = 15 pF
Voltage Dominant	V_{IDD}	0.9		5.0	V	−7 V < V_{CANL}, V_{CANH} < 12 V, see Figure 24, C_L = 15 pF
Input Voltage Hysteresis	V_{HYS}		150		mV	See Figure 24
CANH, CANL Input Resistance	R_{IN}	5		25	kΩ	
Differential Input Resistance	R_{DIFF}	20		100	kΩ	
Logic Outputs						
Output Low Voltage	V_{OL}		0.2	0.4	V	I_{OUT} = 1.5 mA
Output High Voltage	V_{OH}	V_{DD1} − 0.3	V_{DD1} − 0.2		V	I_{OUT} = −1.5 mA
Short-Circuit Current	I_{OS}	7		85	mA	V_{OUT} = GND_1 or V_{DD1}
VOLTAGE REFERENCE						
Reference Output Voltage	V_{REF}	2.025		3.025	V	$\|I_{REF}$ = 50 µA$\|$
BUS VOLTAGE SENSE						
V_{+SENSE} Output Voltage Low	V_{OL}		0.2	0.4	V	$I_{O+SENSE}$ = 1.5 mA
V_{+SENSE} Output Voltage High	V_{OH}	V_{DD1} − 0.3	V_{DD1} − 0.2		V	$I_{O+SENSE}$ = −1.5 mA
Threshold Voltage	$V_{+SENSETH}$	7.0		10	V	
COMMON-MODE TRANSIENT IMMUNITY[1]		25			kV/µs	V_{CM} = 1 kV, transient magnitude = 800 V

[1] CM is the maximum common-mode voltage slew rate that can be sustained while maintaining specification-compliant operation. V_{CM} is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

TIMING SPECIFICATIONS

All voltages are relative to their respective ground; 3.0 V ≤ V_{DD1} ≤ 5.5 V, T_A = −40°C to +85°C, V_+ = 11 V to 25 V, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DRIVER						
Maximum Data Rate		1			Mbps	
Propagation Delay from TxD On to Bus Active	t_{onTxD}			90	ns	See Figure 25 and Figure 27, R_L = 60 Ω, C_L = 100 pF
Propagation Delay from TxD Off to Bus Inactive	t_{offTxD}			120	ns	See Figure 25 and Figure 27, R_L = 60 Ω, C_L = 100 pF
RECEIVER						
Propagation Delay from TxD On to Receiver Active	t_{onRxD}			200	ns	See Figure 25 and Figure 27, R_L = 60 Ω, C_L = 100 pF
Propagation Delay from TxD Off to Receiver Inactive	t_{offRxD}			250	ns	See Figure 25 and Figure 27, R_L = 60 Ω, C_L = 100 pF
POWER-UP						
Enable Time, V_+ High to V_{+SENSE} Low	t_{SE}			300	µs	See Figure 29
Disable Time, V_+ Low to V_{+SENSE} High	t_{SD}			10	ms	See Figure 29

REGULATORY INFORMATION

Table 3. ADM3052 Approvals

Organization	Approval Type	Notes
UL	Recognized under the component recognition program of Underwriters Laboratories, Inc.	In accordance with UL 1577, each ADM3052 is proof tested by applying an insulation test voltage ≥6000 V rms for 1 second (current leakage detection limit = 10 µA)
VDE	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12	In accordance with DIN V VDE V 0884-10, each ADM3052 is proof tested by applying an insulation test voltage ≥1590 V peak for 1 second (partial discharge detection limit = 5 pC)

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	7.7	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	7.6	mm	Measured from input terminals to output terminals, shortest distance along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303-1
Isolation Group		II		Material group (DIN VDE 0110)

VDE 0884 INSULATION CHARACTERISTICS

This isolator is suitable for reinforced electrical isolation within the safety limit data. Maintenance of the safety data must be ensured by means of protective circuits. An asterisk (*) on packages denotes DIN V VDE V 0884-10 approval.

Table 5.

Description	Test Conditions	Symbol	Characteristic	Unit
CLASSIFICATIONS				
Installation Classification per DIN VDE 0110 for Rated Mains Voltage				
≤150 V rms			I to IV	
≤300 V rms			I to III	
≤400 V rms			I to II	
Climatic Classification			40/85/21	
Pollution Degree	DIN VDE 0110		2	
VOLTAGE				
Maximum Working Insulation Voltage		V_{IORM}	846	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production tested, $t_m = 1$ sec, partial discharge < 5 pC	V_{PR}	1590	V peak
Input-to-Output Test Voltage, Method A		V_{PR}	1357	V peak
After Environmental Tests, Subgroup 1	$V_{IORM} \times 1.6 = V_{PR}$, $t_m = 60$ sec, partial discharge < 5 pC			
After Input and/or Safety Test, Subgroup 2/Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, $t_m = 60$ sec, partial discharge < 5 pC		1018	V peak
Highest Allowable Overvoltage		V_{TR}	6000	V peak
SAFETY-LIMITING VALUES				
Case Temperature		T_S	150	°C
Input Current		$I_{S, INPUT}$	265	mA
Output Current		$I_{S, OUTPUT}$	335	mA
Insulation Resistance at T_S		R_S	$>10^9$	Ω

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. All voltages are relative to their respective ground.

Table 6.

Parameter	Rating
V_{DD1}	−0.5 V to +6 V
V_+	−36 V to +36 V
V_{+R}	−36 V to +36 V
Digital Input Voltage	
TxD	−0.5 V to V_{DD1} + 0.5 V
Digital Output Voltage	
RxD	−0.5 V to V_{DD1} + 0.5 V
V_{+SENSE}	−0.5 V to V_{DD1} + 0.5 V
CANH, CANL	−36 V to +36 V
V_{REF}	−0.5 V to +6 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +150°C
ESD (Human Body Model)	3 kV
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
$θ_{JA}$, Thermal Impedance	53°C/W
T_J, Junction Temperature	130°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 7. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Reference Standard
AC Voltage			
Bipolar Waveform			
Basic Insulation	565	V peak	50-year minimum lifetime
Reinforced Insulation	565	V peak	50-year minimum lifetime
Unipolar Waveform			
Basic Insulation	1131	V peak	50-year minimum lifetime
Reinforced Insulation	864	V peak	Lifetime limited by package creepage
DC Voltage			
Basic Insulation	1066	V peak	Lifetime limited by package creepage
Reinforced Insulation	529	V peak	Lifetime limited by package creepage

[1] Refers to continuous voltage magnitude imposed across the isolation barrier.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

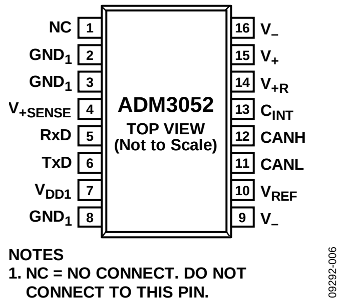

Figure 2. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	No Connect. Do not connect to this pin.
2	GND_1	Ground (Logic Side).
3	GND_1	Ground (Logic Side).
4	V_{+SENSE}	Bus Voltage Sense. A low level on V_{+SENSE} indicates that there is power connected on the bus on V_+ and V_-. A high level on V_{+SENSE} indicates that power is not connected on the bus on V_+ and V_-.
5	RxD	Receiver Output Data.
6	TxD	Driver Input Data.
7	V_{DD1}	Power Supply (Logic Side). Decoupling capacitor to GND_1 required; capacitor value should be between 0.01 μF and 0.1 μF.
8	GND_1	Ground (Logic Side).
9	V_-	Ground (Bus Side).
10	V_{REF}	Reference Voltage Output.
11	CANL	Low Level CAN Voltage Input/Output.
12	CANH	High Level CAN Voltage Input/Output.
13	C_{INT}	A capacitor of 1 μF, 10 V is required on this pin.
14	V_{+R}	Connect a 300 Ω, 750 mW resistor between V_{+R} and V_+. It is recommended that a 10 μF capacitor be fitted between V_{+R} and GND_2.
15	V_+	Bus Power Connection. Connect a 300 Ω, 750 mW resistor between V_{+R} and V_+.
16	V_-	Ground (Bus Side).

TYPICAL PERFORMANCE CHARACTERISTICS

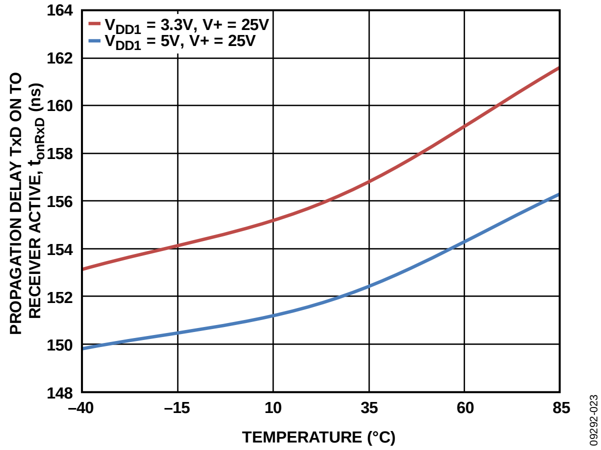

Figure 3. Propagation Delay from TxD On to Receiver Active vs. Temperature

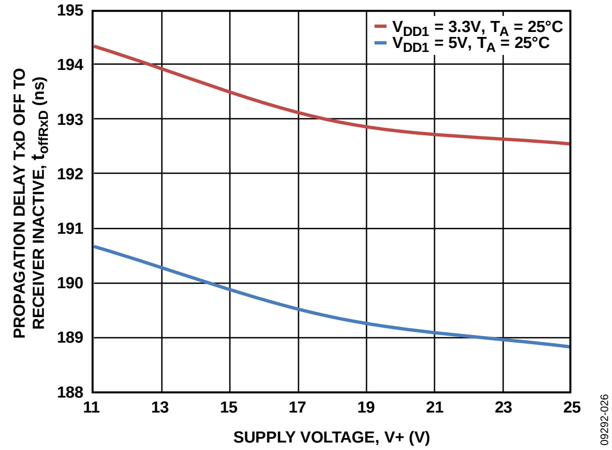

Figure 6. Propagation Delay from TxD Off to Receiver Inactive vs. Supply Voltage, V_+

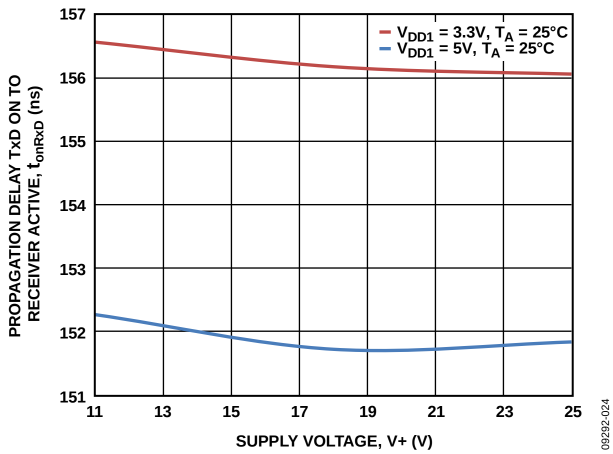

Figure 4. Propagation Delay from TxD On to Receiver Active vs. Supply Voltage, V_+

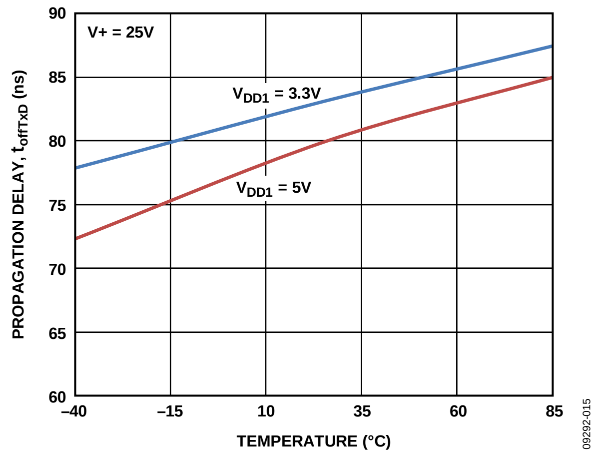

Figure 7. Propagation Delay from TxD Off to Bus Inactive vs. Temperature

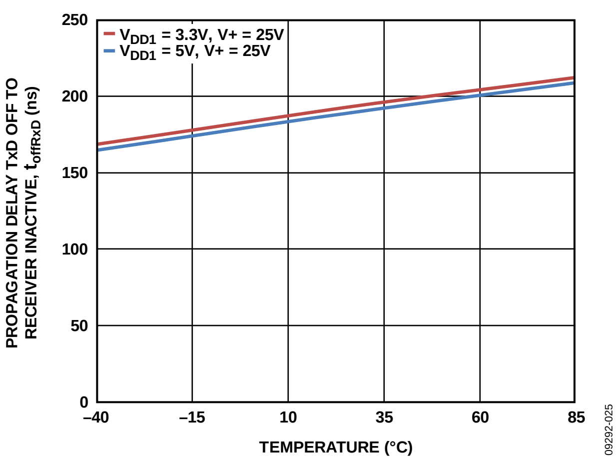

Figure 5. Propagation Delay from TxD Off to Receiver Inactive vs. Temperature

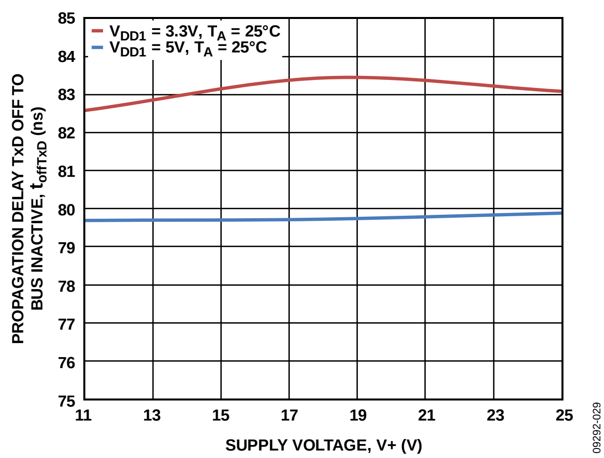

Figure 8. Propagation Delay from TxD Off to Bus Inactive vs. Supply Voltage, V_+

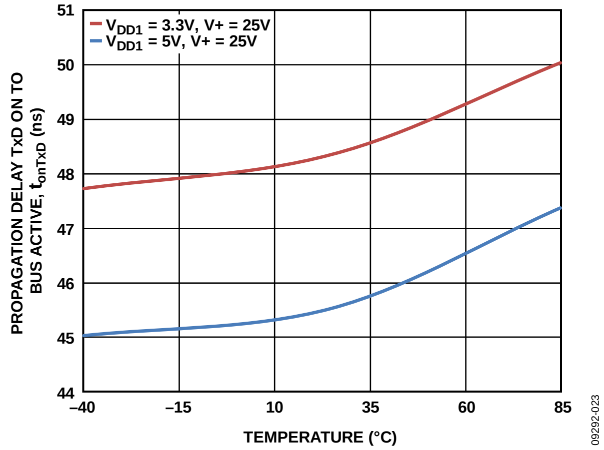

Figure 9. Propagation Delay from TxD On to Bus Active vs. Temperature

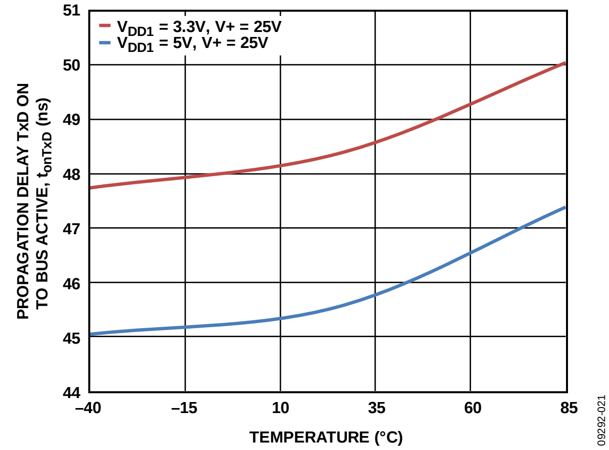

Figure 12. Propagation Delay from TxD On to Bus Active vs. Temperature

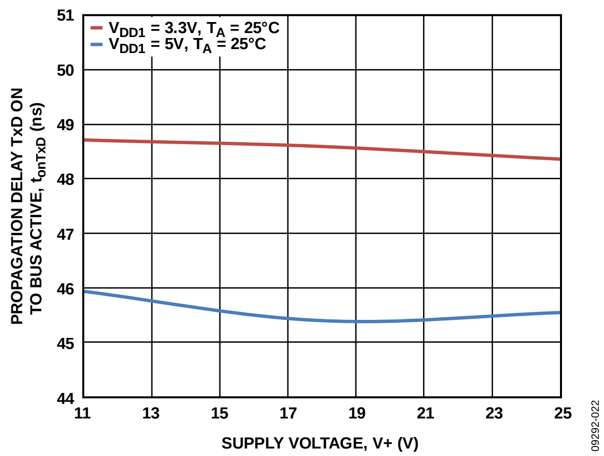

Figure 10. Propagation Delay from TxD On to Bus Active vs. Supply Voltage, V_+

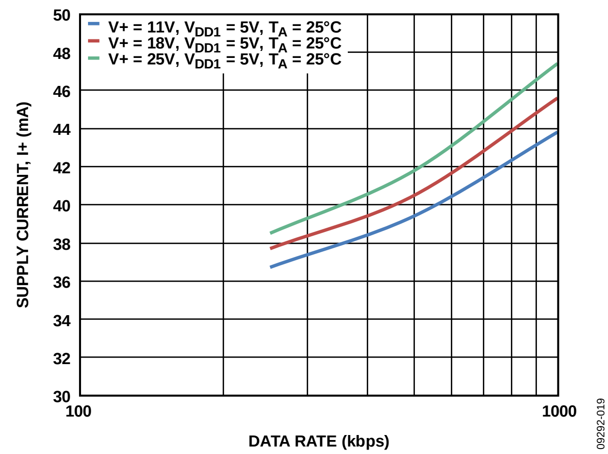

Figure 13. Supply Current (I_+) vs. Data Rate (Across V_+, V_{DD1} = 5 V)

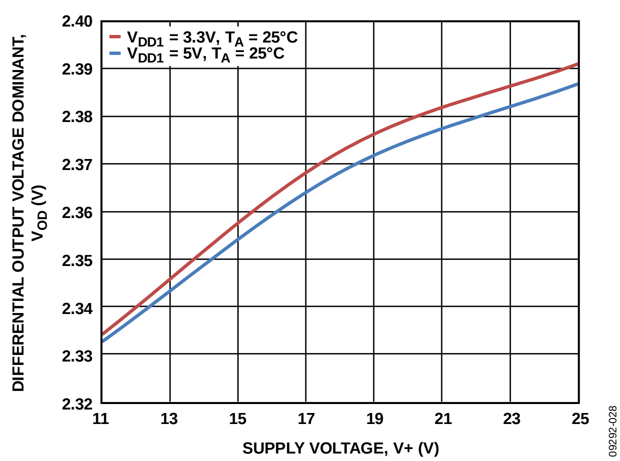

Figure 11. Differential Output Voltage Dominant vs. Supply Voltage, V_+

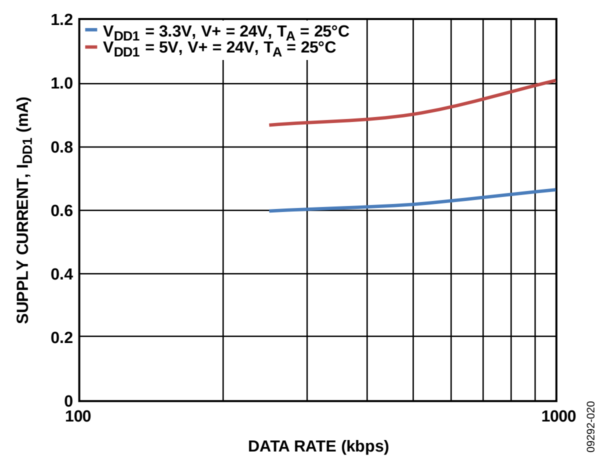

Figure 14. Supply Current (I_{DD1}) vs. Data Rate (V_{DD1} = 3.3 V, 5 V; V_+ = 24 V)

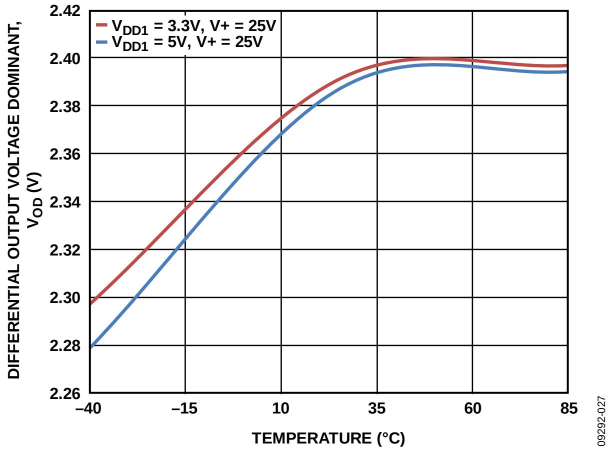

Figure 15. Driver Differential Output Voltage Dominant vs. Temperature

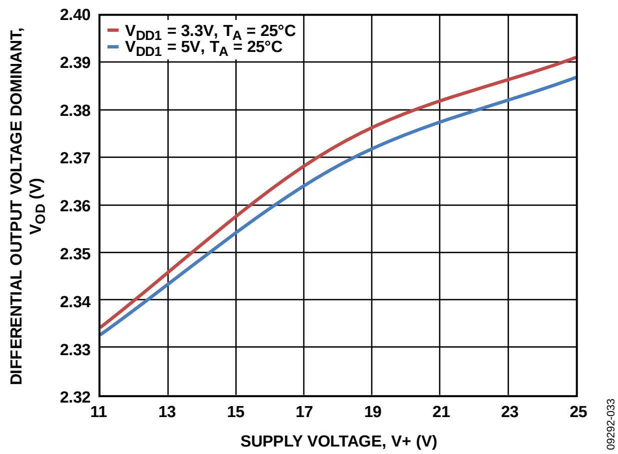

Figure 16. Driver Differential Output Voltage Dominant vs. Supply Voltage, V_+

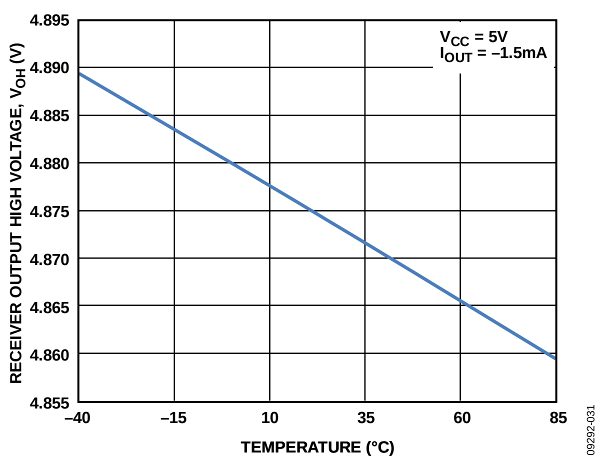

Figure 17. Receiver Output High Voltage vs. Temperature

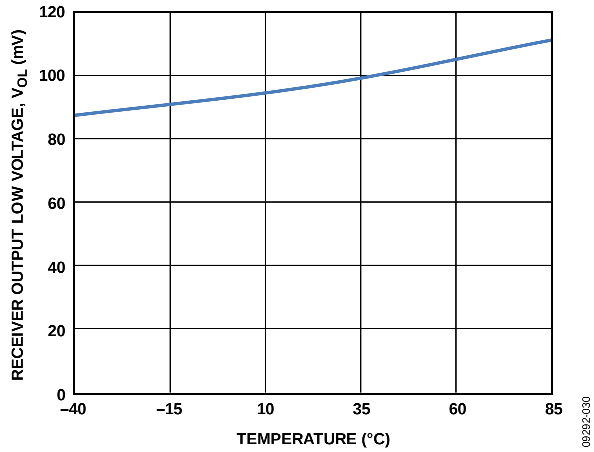

Figure 18. Receiver Output Low Voltage vs. Temperature

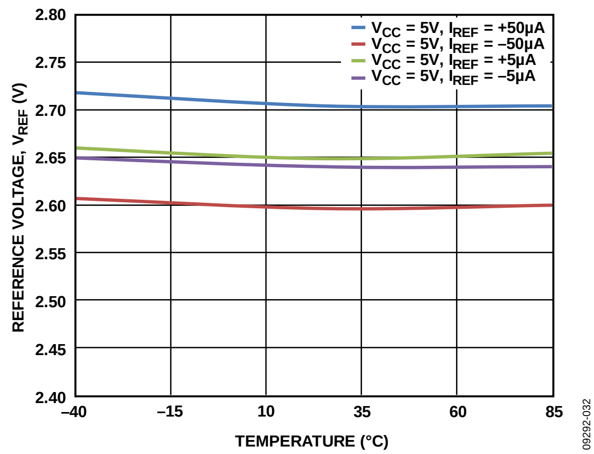

Figure 19. V_{REF} vs. Temperature

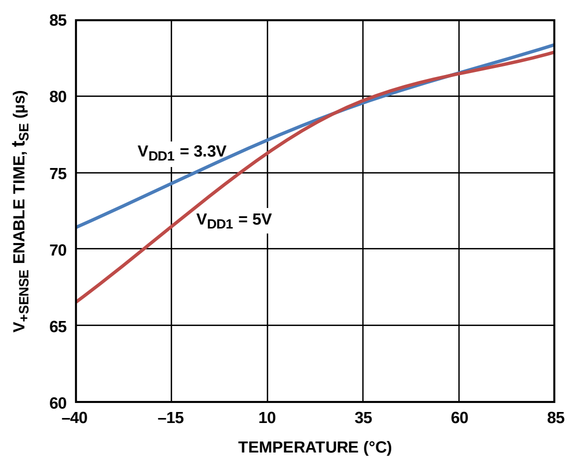

Figure 20. Enable Time, V_+ High to V_{+SENSE} Low vs. Temperature

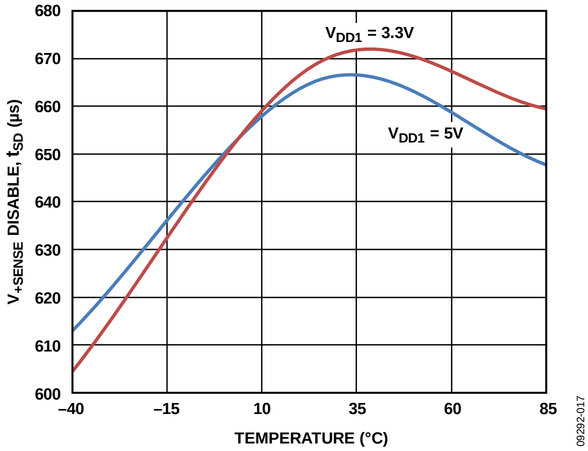

Figure 21. Disable Time, V_+ Low to V_{+SENSE} High vs. Temperature

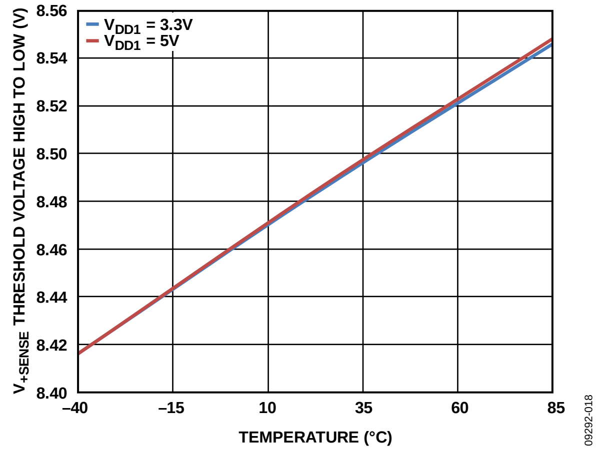

Figure 22. Bus Voltage Sense Threshold Voltage High to Low vs. Temperature

TEST CIRCUITS

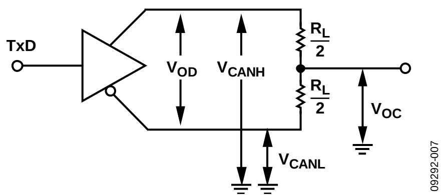

Figure 23. Driver Voltage Measurements

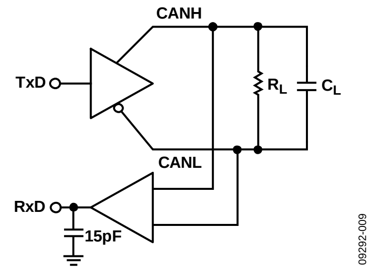

Figure 25. Switching Characteristics Measurements

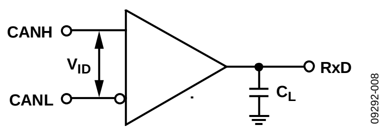

Figure 24. Receiver Voltage Measurements

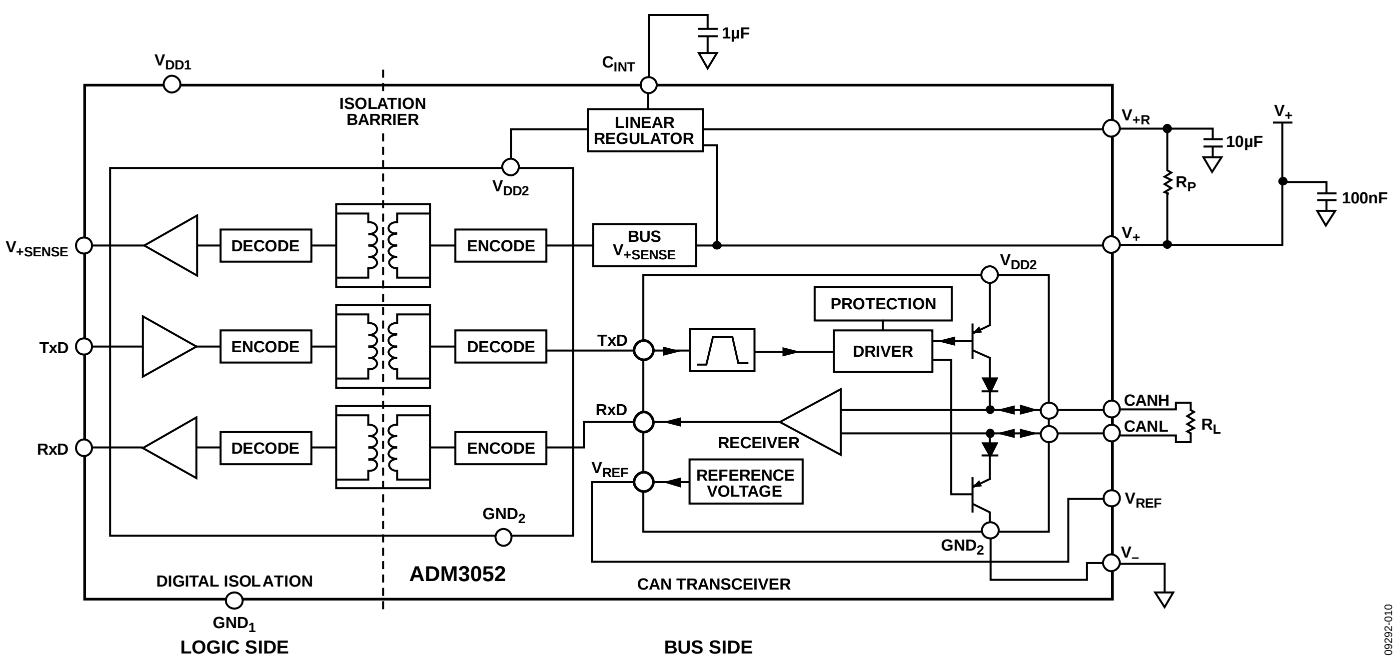

Figure 26. Supply Current Measurement Test Circuit

SWITCHING CHARACTERISTICS

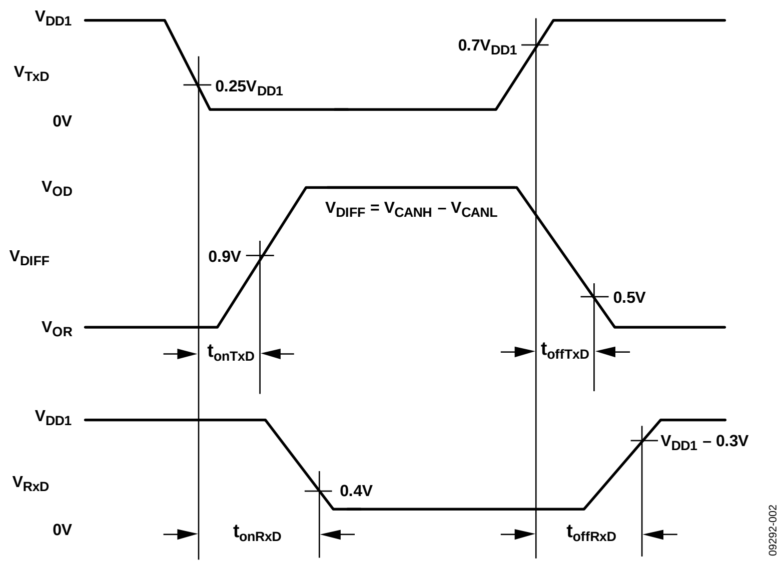

Figure 27. Driver and Receiver Propagation Delay

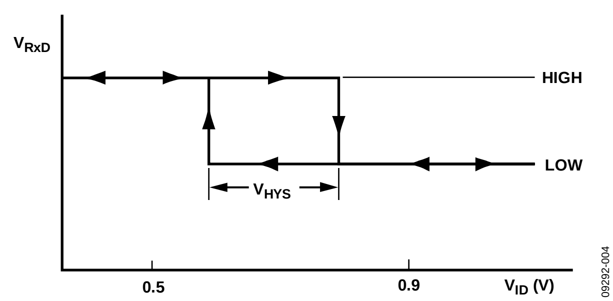

Figure 28. Receiver Input Hysteresis

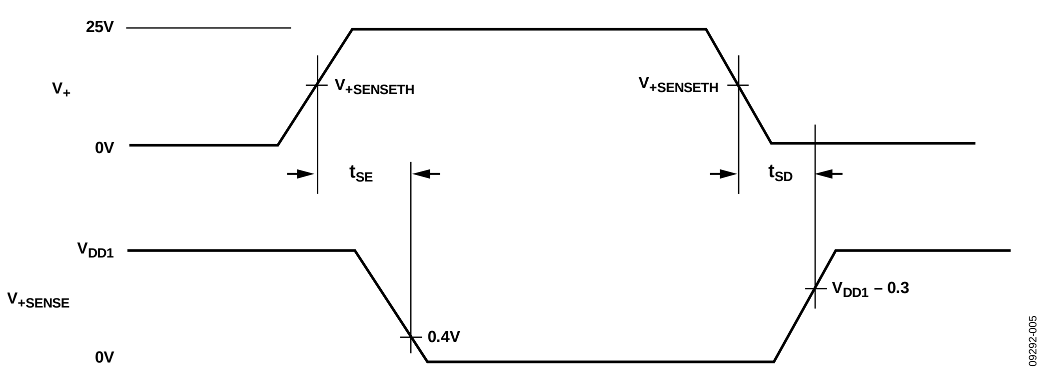

Figure 29. V_{+SENSE} Enable/Disable Time

CIRCUIT DESCRIPTION

CAN TRANSCEIVER OPERATION

A CAN bus has two states: dominant and recessive. A dominant state is present on the bus when the differential voltage between CANH and CANL is greater than 0.9 V. A recessive state is present on the bus when the differential voltage between CANH and CANL is less than 0.5 V. During a dominant bus state, the CANH pin is high and the CANL pin is low. During a recessive bus state, both the CANH and CANL pins are in the high impedance state.

ELECTRICAL ISOLATION

In the ADM3052, electrical isolation is implemented on the logic side of the interface. Therefore, the device has two main sections: a digital isolation section and a transceiver section (see Figure 30). The driver input signal, which is applied to the TxD pin and referenced to the logic ground (GND_1), is coupled across an isolation barrier to appear at the transceiver section referenced to the isolated ground (V_-). Similarly, the receiver input and V_+, which are referenced to the isolated ground in the transceiver section, are coupled across the isolation barrier to appear at the RxD pin and V_{+SENSE} referenced to the logic ground, respectively.

*i*Coupler *Technology*

The digital signals transmit across the isolation barrier using *i*Coupler technology. This technique uses chip scale transformer windings to couple the digital signals magnetically from one side of the barrier to the other. Digital inputs are encoded into waveforms that are capable of exciting the primary transformer winding. At the secondary winding, the induced waveforms are decoded into the binary value that was originally transmitted.

Positive and negative logic transitions at the input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than ~1 µs, a periodic set of refresh pulses, indicative of the correct input state, is sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than about 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case the output is forced to a default state (see Table 10 and Table 11).

TRUTH TABLES

The truth tables in this section use the abbreviations shown in Table 9.

Table 9. Truth Table Abbreviations

Letter	Description
H	High level
L	Low level
I	Indeterminate
X	Don't care
Z	High impedance (off)
NC	Disconnected

Table 10. Transmitting

Supply Status		Input	Outputs			
V_{DD1}	V_+	TxD	Bus State	CANH	CANL	V_{+SENSE}
On	On	L	Dominant	H	L	L
On	On	H	Recessive	Z	Z	L
On	On	Floating	Recessive	Z	Z	L
Off	On	X	Recessive	Z	Z	I
On	Off	L	I	I	I	H

Table 11. Receiving

Supply Status		Inputs		Outputs	
V_{DD1}	V_+	V_{ID} = CANH − CANL	Bus State	RxD	V_{+SENSE}
On	On	≥ 0.9 V	Dominant	L	L
On	On	≤ 0.5 V	Recessive	H	L
On	On	0.5 V < V_{ID} < 0.9 V	I	I	L
On	On	Inputs open	Recessive	H	L
Off	On	X	X	I	I
On	Off	X	X	H	H

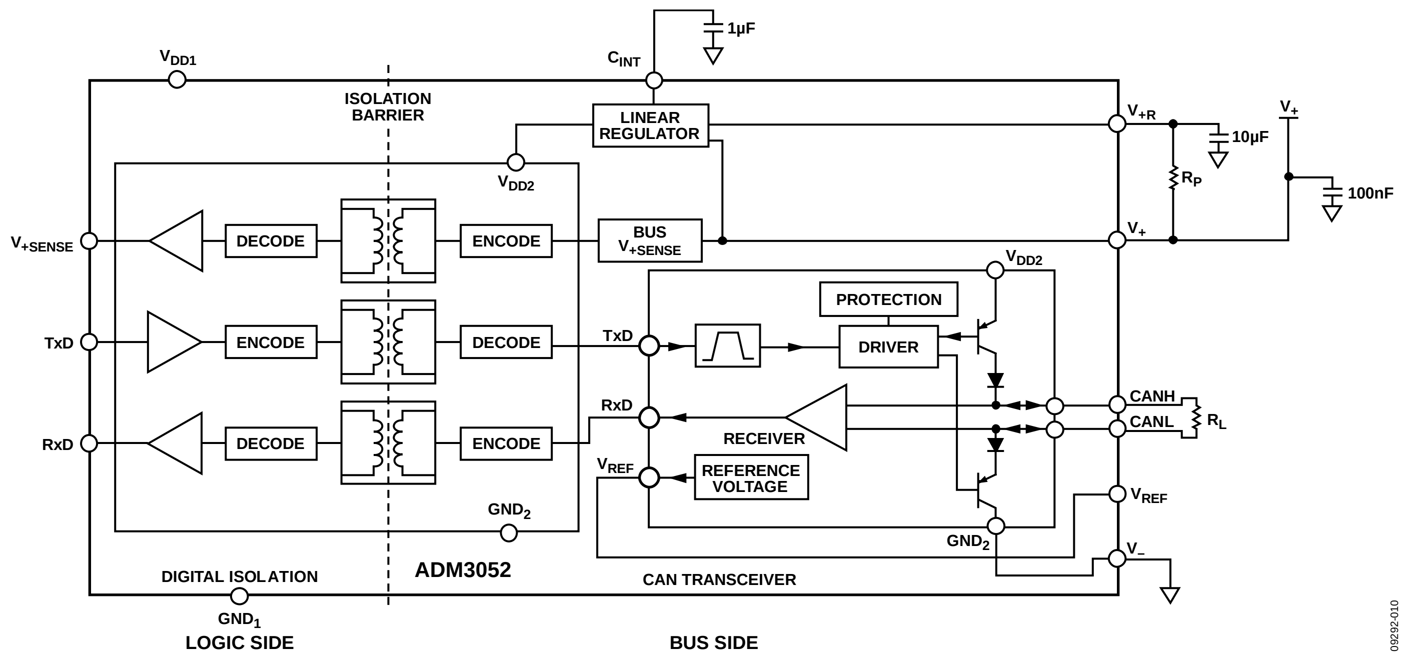

Figure 30. Digital Isolation and Transceiver Sections

THERMAL SHUTDOWN

The ADM3052 contains thermal shutdown circuitry that protects the device from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. This circuitry is designed to disable the driver outputs when a junction temperature of 150°C is reached. As the device cools, the drivers reenable at a temperature of 140°C.

LINEAR REGULATOR

The linear regulator takes the V_+ bus power (ranging between 11 V to 25 V) and regulates this voltage to 5 V to provide power to the internal bus-side circuitry (*i*Coupler isolation, V_{+SENSE}, and transceiver circuits). The linear regulator uses two regulation loops to share the power dissipation between the internal die and an external resistor. This reduces the internal heat dissipation in the package. The 300 Ω external resistor should be capable of dissipating 750 mW of power and have a tolerance of 1%.

MAGNETIC FIELD IMMUNITY

The limitation on the magnetic field immunity of the *i*Coupler is set by the condition in which an induced voltage in the receiving coil of the transformer is large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this may occur. The 3 V operating condition of the ADM3052 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1 V. The decoder has a sensing threshold of about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated.

The voltage induced across the receiving coil is given by

$$V = \left(\frac{-d\beta}{dt}\right)\sum \pi r_n^2 \; ; \; n = 1, 2, \ldots, N$$

where:
β is the magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the n^{th} turn in the receiving coil (cm).

Given the geometry of the receiving coil and an imposed requirement that the induced voltage is, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field can be determined using Figure 31.

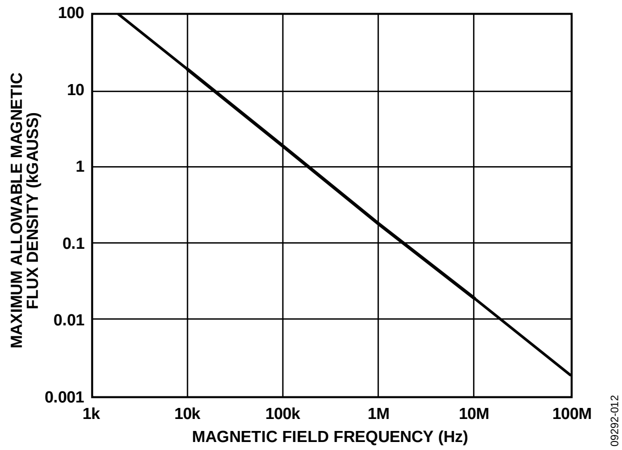

Figure 31. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse and is the worst-case polarity, it reduces the received pulse from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

Figure 32 shows the magnetic flux density values in terms of more familiar quantities, such as maximum allowable current flow at given distances away from the ADM3052 transformers.

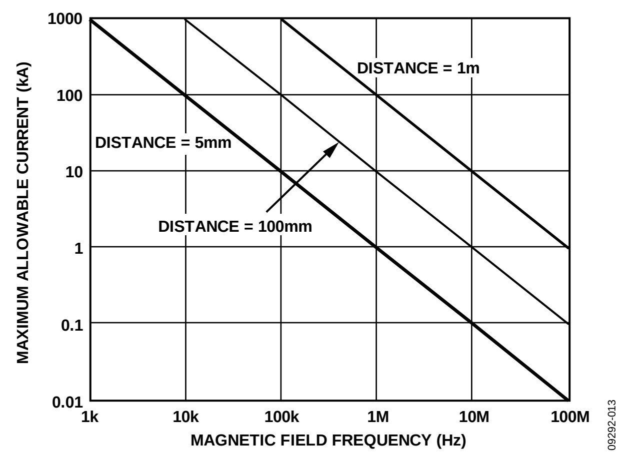

Figure 32. Maximum Allowable Current for Various Current-to-ADM3052 Spacings

With combinations of strong magnetic field and high frequency, any loops formed by PCB traces can induce error voltages large enough to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

APPLICATIONS INFORMATION

TYPICAL APPLICATIONS

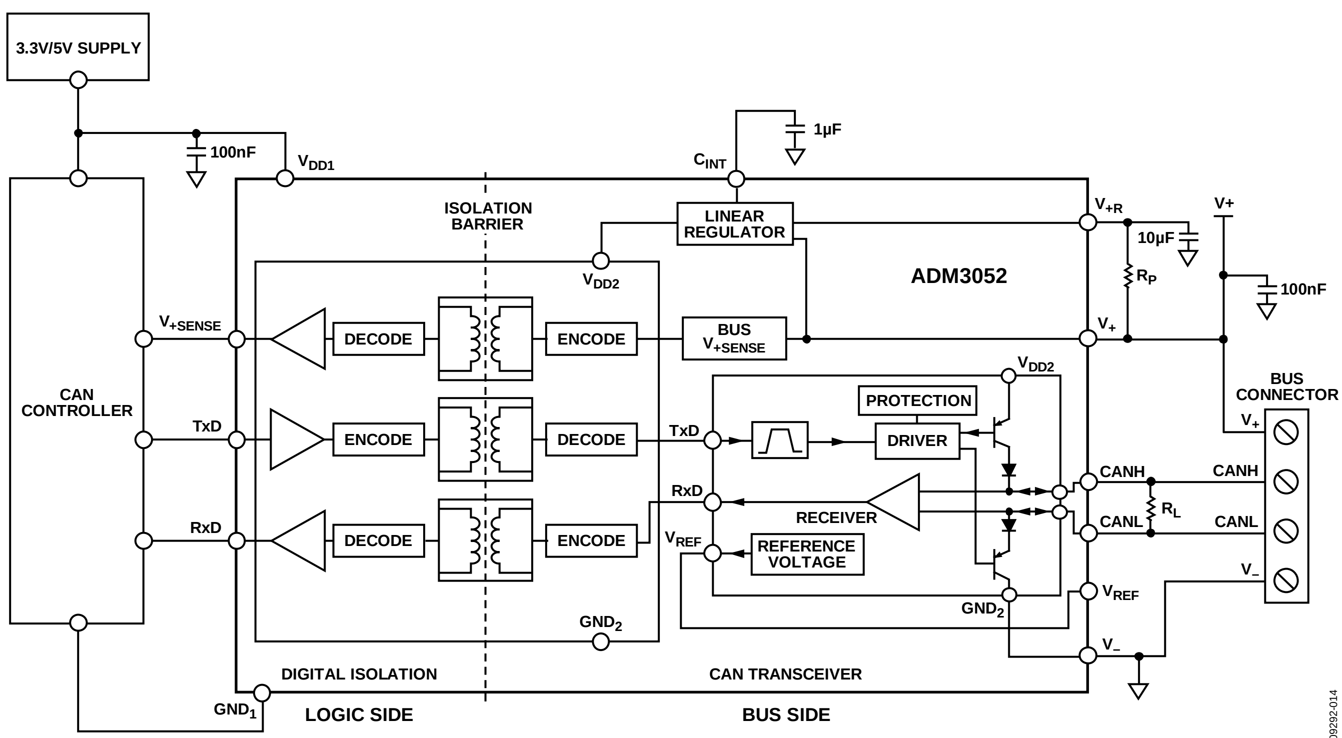

Figure 33. Typical Isolated CAN Node Using the ADM3052

DEVICENET™ AND THE ADM3052 CAN TRANSCEIVER

DeviceNet is a digital multidrop network that connects actuators, sensors, and a broad range of industrial automation systems. DeviceNet is managed by the Open DeviceNet Vendor Association (ODVA) and is accepted by international standards bodies around the world, with a large number of companies offering DeviceNet products.

The Communications and Information Protocol (CIP™) is a communications protocol for transferring automation data between two devices. DeviceNet is a combination of CIP™ (for upper layers of the network) and the CAN physical layer for the data link layer. DeviceNet allows up to 64 nodes on a single network, with node addresses ranging from 0 to 63. DeviceNet supports 125 kbps, 250 kbps, and 500 kbps data rates and supports master and slave as well as peer-to-peer communication. The ADM3052 can be used as the CAN physical layer transceiver for a DeviceNet implementation. Refer to the AN-1123 Application Note for a CAN implementation guide.

DeviceNet supports both isolated and nonisolated physical layer design of devices. An isolated design option allows externally powered devices (for example, ac drive starters and solenoid valves) to share the same bus cable. DeviceNet requires the support of the standard industrial voltage range from 11 V dc to 25 V dc. The ADM3052 employs Analog Devices iCoupler technology, combines a 3-channel isolator, a CAN transceiver, and a linear regulator into a single package. Isolated power is supplied to the bus side of the ADM3052 by an isolated 24 V supply across the bus.

The internal regulator provides the 5 V supply required internally by the CAN transceiver. The logic side of the ADM3052 requires a single 3.3 V or 5 V supply.

OUTLINE DIMENSIONS

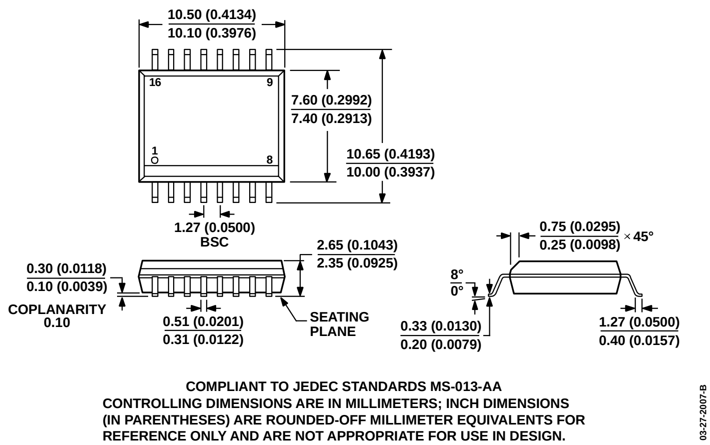

Figure 34. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADM3052BRWZ	−40°C to +85°C	16-Lead SOIC_W	RW-16
ADM3052BRWZ-REEL7	−40°C to +85°C	16-Lead SOIC_W	RW-16
EVAL-ADM3052EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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