Data Sheet

ADPD4200

Multimodal Sensor Front End

FEATURES

- Multimodal analog front end
- 4 input channels with multiple operation modes to accommodate the following measurements: PPG, ECG, EDA, impedance, and temperature
- Dual-channel processing with simultaneous sampling
- 12 programmable time slots for synchronized sensor measurements
- Flexible input multiplexing to support differential and single-ended sensor measurements
- 4 LED drivers, which can be driven simultaneously
- Flexible sampling rate from 0.004 Hz to 9 kHz using internal oscillators
- On-chip digital filtering
- SNR: 105 dB (100 kΩ TIA gain, 100 Hz ODR, 80 pulses, C_{PD} = 70 pF, 0.5 Hz to 10 Hz bandwidth)
- AC ambient light rejection: 60 dB up to 1 kHz
- 400 mA total LED peak drive current
- Total system power dissipation: 30 µW (combined LED and AFE power), continuous PPG measurement at 75 dB SNR, 25 Hz ODR, 100 nA/mA CTR
- SPI communications supported
- 512-byte FIFO size

APPLICATIONS

- Wearable health and fitness monitors: heart rate monitors (HRMs), heart rate variability (HRV), stress, blood pressure estimation, SpO_2, hydration, and body composition
- Industrial monitoring: CO, CO_2, smoke, and aerosol detection
- Home patient monitoring

GENERAL DESCRIPTION

The ADPD4200 operates as a complete multimodal sensor front end, stimulating up to four light emitting diodes (LEDs) and measuring the return signal on up to four separate current inputs. Twelve time slots are available, enabling 12 separate measurements per sampling period.

The data output and functional configuration utilize a serial port interface (SPI) on the ADPD4200. The control circuitry includes flexible LED signaling and synchronous detection. The device uses a 1.8 V analog core and 1.8 V or 3.3 V compatible digital input/output (I/O).

The analog front end (AFE) rejects signal offsets and corruption from asynchronous modulated interference, typically from ambient light, eliminating the need for optical filters or externally controlled dc cancellation circuitry. Multiple operating modes are provided, enabling the ADPD4200 to be a sensor hub for synchronous measurements of photodiodes, biopotential electrodes, resistance, capacitance, and temperature sensors.

The ADPD4200 is available in a 2.619 mm × 1.804 mm, 0.40 mm pitch, 24-ball WLCSP.

Analog Devices is in the process of updating documentation to provide terminology and language that is culturally appropriate. This is a process with a wide scope and will be phased in as quickly as possible. Thank you for your patience.

Rev. 0

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REVISION HISTORY

3/2022—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

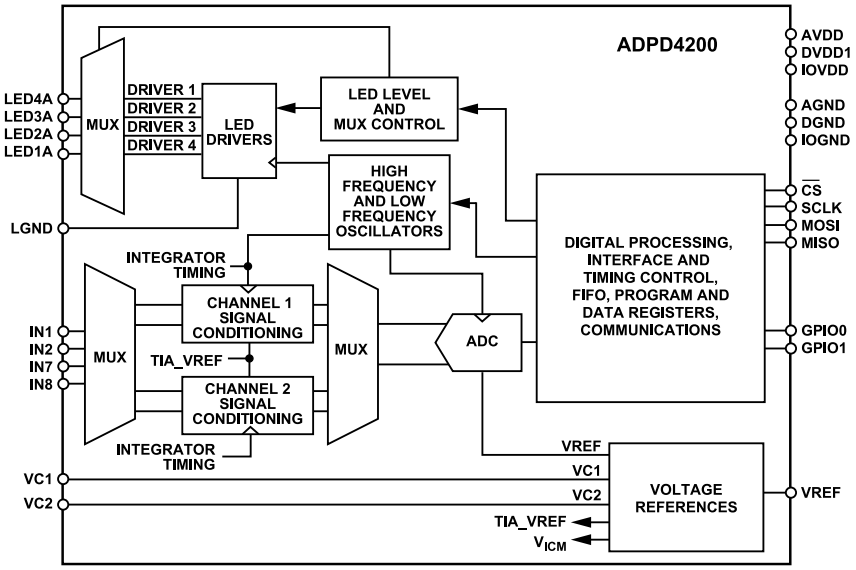

Figure 1.

SPECIFICATIONS

TEMPERATURE AND POWER SPECIFICATIONS

Table 1. Operating Conditions

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
TEMPERATURE RANGE					
Operating Range		−40		+85	°C
Storage Range		−65		+150	°C
POWER SUPPLY VOLTAGE					
Supply Voltage, V_{DD}	Applied at the AVDD and DVDD1 pins	1.7	1.8	1.9	V
Input and Output Driver Supply, IOV_{DD}	Applied at the IOVDD pin	1.7	1.8	3.6	V

AVDD = DVDD1 = IOVDD = 1.8 V and T_A = 25°C, unless otherwise noted.

Table 2. Current Consumption

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY (V_{DD}) CURRENT						
V_{DD} Supply Current[1]		Signal-to-noise ratio (SNR) = 75 dB, 25 Hz output data rate (ODR), single time slot		10		µA
Total System Power Dissipation		Combined LED and AFE power, continuous photoplethysmography (PPG) measurement at 75 dB SNR, 25 Hz ODR, 100 nA/mA current transfer ratio (CTR)		30		µW
Peak V_{DD} Supply Current (1.8 V)						
1-Channel Operation	I_{VDD_PEAK}	Peak V_{DD} current during time slot sampling		4.5		mA
Standby Mode Current	$I_{VDD\_STANDBY}$			0.250		µA

[1] V_{DD} is the voltage applied at the AVDD and DVDD1 pins.

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PERFORMANCE SPECIFICATIONS

AVDD = DVDD1 = IOVDD = 1.8 V, and T_A = full operating temperature range, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DATA ACQUISITION					
Datapath Width				32	Bits
FIRST IN, FIRST OUT (FIFO) SIZE				512	Bytes
LED DRIVER					
LED Peak Current per Driver	LED pulse enabled	2		200	mA
LED Peak Current, Total	Using multiple LED drivers simultaneously			400	mA
Driver Compliance Voltage	For any LED driver output at ILED = 40 mA			200	mV
LED PERIOD	AFE width = 4 µs[1]	10			µs
	AFE width = 3 µs	8			µs
SAMPLING RATE[2]	Single time slot, four data bytes to FIFO, 2 µs LED pulse	0.004		9000	Hz
OSCILLATOR DRIFT					
32 kHz Oscillator	Percent variation from 25°C to 85°C		3.00	5.00	%
	Percent variation from +25°C to –40°C		–3.00	–7.00	%
1 MHz Oscillator	Percent variation from 25°C to 85°C		1.00	2.00	%
	Percent variation from +25°C to –40°C		–1.00	–3.00	%
32 MHz Oscillator	Percent variation from 25°C to 85°C		1.00	2.00	%
	Percent variation from +25°C to –40°C		–2.00	–4.00	%

[1] Minimum LED period = (2 × AFE width) + 2 µs.

[2] The maximum value in this specification is the internal analog-to-digital converter (ADC) sampling rate using the internal 1 MHz state machine clock. The communication interface like SPI read rates in some configurations may limit the ODR.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
TRANSIMPEDANCE AMPLIFIER (TIA) GAIN		12.5		200	kΩ
PULSED SIGNAL CONVERSIONS, 3 µs LED PULSE	4 µs integration width, signal integration mode				
ADC Resolution[1]	TIA feedback resistor				
	12.5 kΩ		6.2		nA/LSB
	25 kΩ		3.1		nA/LSB
	50 kΩ		1.5		nA/LSB
	100 kΩ		0.77		nA/LSB
	200 kΩ		0.38		nA/LSB
ADC Saturation Level[2]	TIA feedback resistor				
	12.5 kΩ		50		µA
	25 kΩ		25		µA
	50 kΩ		12.5		µA
	100 kΩ		6.22		µA
	200 kΩ		3.11		µA
PULSED SIGNAL CONVERSIONS, 2 µs LED PULSE	3 µs integration width, single integration mode				
ADC Resolution[1]	TIA feedback resistor				
	12.5 kΩ		8.2		nA/LSB
	25 kΩ		4.1		nA/LSB
	50 kΩ		2.04		nA/LSB
	100 kΩ		1.02		nA/LSB
	200 kΩ		0.51		nA/LSB

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Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC Saturation Level[2]	TIA feedback resistor				
	12.5 kΩ		67		µA
	25 kΩ		33		µA
	50 kΩ		16.7		µA
	100 kΩ		8.37		µA
	200 kΩ		4.19		µA
FULL SIGNAL CONVERSIONS					
TIA Linear Dynamic Range (per Channel)	Total input current, 1% compression point, TIA_VREF = 1.265 V				
	12.5 kΩ		72		µA
	25 kΩ		38		µA
	50 kΩ		18.7		µA
	100 kΩ		9.3		µA
	200 kΩ		4.6		µA
SYSTEM PERFORMANCE					
Referred to Input Noise	Single integration mode, single pulse, single channel, floating input, TIA_VREF = 1.265 V, 3 µs integration time				
	12.5 kΩ TIA gain		8.2		nA rms
	25 kΩ TIA gain		4.1		nA rms
	50 kΩ TIA gain		2.2		nA rms
	100 kΩ TIA gain		1.2		nA rms
	200 kΩ TIA gain		0.61		nA rms
Referred to Input Noise	Single integration mode, single pulse, single channel, 90% full-scale input signal, no ambient light, TIA_VREF = 1.265 V, VCx = TIA_VREF + 250 mV, 2 µs LED pulse, photodiode capacitance (C_{PD}) = 70 pF, input resistor = 500 Ω				
	12.5 kΩ TIA gain		10.3		nA rms
	25 kΩ TIA gain		5.3		nA rms
	50 kΩ TIA gain		2.7		nA rms
	100 kΩ TIA gain		1.5		nA rms
	200 kΩ TIA gain		0.97		nA rms
SNR	12.5 kΩ TIA gain, single pulse		76		dB
	25 kΩ TIA gain, single pulse		76		dB
	50 kΩ TIA gain, single pulse		75		dB
	100 kΩ TIA gain, single pulse		74		dB
	200 kΩ TIA gain, single pulse		72		dB
	100 kΩ TIA gain, 100 Hz ODR, 80 pulses, C_{PD} = 70 pF, 0.5 Hz to 10 Hz bandwidth		105		dB
AC Ambient Light Rejection	DC to 1 kHz, linear range of TIA		60		dB
DC Power Supply Rejection Ratio (DC PSRR)	At 75% full-scale input		50		dB

[1] ADC resolution is listed per pulse. If using multiple pulses, divide by the number of pulses.

[2] ADC saturation level applies to pulsed signal only, because ambient signal is rejected prior to ADC conversion.

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DIGITAL SPECIFICATIONS

IOVDD = 1.7 V to 3.6 V, unless otherwise noted.

Table 5. Digital Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS						
Input Voltage Level						
GPIOx, MISO, MOSI, SCLK, $\overline{CS}$						
High	V_{IH}		0.7 × IOVDD		IOVDD + 0.3	V
Low	V_{IL}		−0.3		+0.3 × IOVDD	V
Input Current Level		All logic inputs				
High	I_{IH}				10	µA
Low	I_{IL}		−10			µA
Input Capacitance	C_{IN}			2		pF
LOGIC OUTPUTS						
Output Voltage Level						
GPIOx, MISO						
High	V_{OH}	2 mA high level output current	IOVDD – 0.5			V
Low	V_{OL}	2 mA low level output current			0.5	V
Output Current Level		SDA				
Low	I_{OL}	V_{OL1} = 0.4 V	20			mA

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TIMING SPECIFICATIONS

Table 6. SPI Timing Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SPI PORT						
SCLK						
Frequency	f_{SCLK}				24	MHz
Minimum Pulse Width						
High	$t_{SCLKPWH}$		15			ns
Low	$t_{SCLKPWL}$		15			ns
$\overline{CS}$						
Setup Time	$t_{\overline{CSS}}$	$\overline{CS}$ setup to SCLK rising edge	11			ns
Hold Time	$t_{\overline{CSH}}$	$\overline{CS}$ hold from SCLK rising edge	5			ns
Pulse Width High	$t_{\overline{CSPWH}}$	$\overline{CS}$ pulse width high	15			ns
MOSI						
Setup Time	t_{MOSIS}	MOSI setup to SCLK rising edge	5			ns
Hold Time	t_{MOSIH}	MOSI hold from SCLK rising edge	5			ns
MISO Output Delay	t_{MISOD}	MISO valid output delay from SCLK falling edge				
		Register 0x00B4 = 0x0050 (default)			28.1	ns
		Register 0x00B4 = 0x005F (maximum slew rate, maximum drive strength for SPI)			21.2	ns

Table 7. Timing Specifications for Provision of External Low Frequency Oscillator

Parameter	Min	Typ	Max	Unit
FREQUENCY				
1 MHz Low Frequency Oscillator	500		2000	kHz
32 kHz Low Frequency Oscillator	10		100	kHz
DUTY CYCLE				
1 MHz Low Frequency Oscillator	10		90	%
32 kHz Low Frequency Oscillator	10		90	%

Timing Diagram

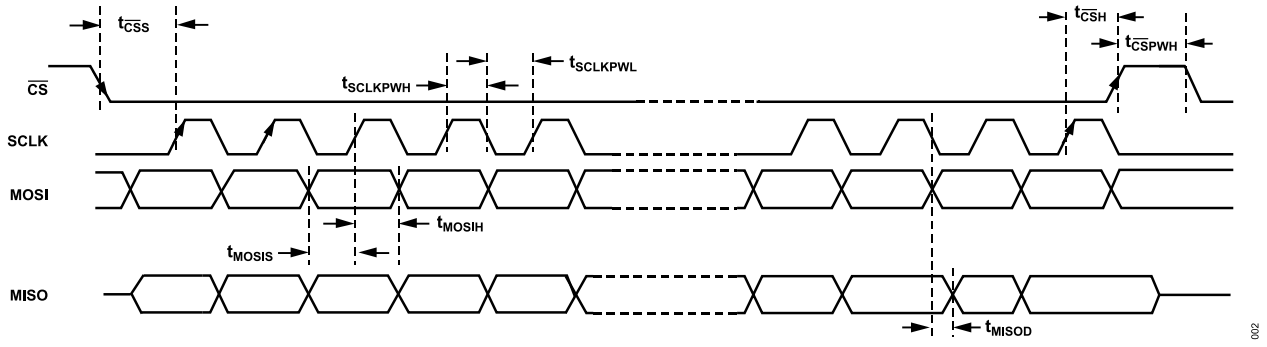

Figure 2. SPI Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
AVDD to AGND	−0.3 V to +2.2 V
DVDD1 to DGND	−0.3 V to +2.2 V
IOVDD to DGND	−0.3 V to +3.9 V
GPIOx, MOSI, MISO, SCLK, $\overline{CS}$	−0.3 V to +3.9 V
LEDxx to LGND	−0.3 V to +3.9 V
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 9. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC}	Unit
CB-24-5	46	1.154	°C/W

[1] The thermal resistance values are defined as per the JESD51-12 standard.

RECOMMENDED SOLDERING PROFILE

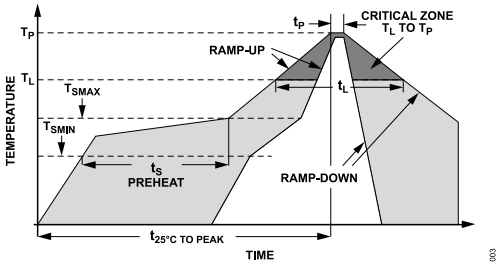

Figure 3. Recommended Soldering Profile

Table 10.

Profile Feature	Condition (Pb-Free)
Average Ramp Rate (T_L to T_P)	3°C/sec maximum
Preheat	
Minimum Temperature (T_{SMIN})	150°C
Maximum Temperature (T_{SMAX})	200°C
Time (T_{SMIN} to T_{SMAX}) (t_S)	60 sec to 180 sec
T_{SMAX} to T_L Ramp-Up Rate	3°C/sec maximum
Time Maintained Above Liquidous Temperature	
Liquidous Temperature (T_L)	217°C
Time (t_L)	60 sec to 150 sec
Peak Temperature (T_P)	+260 (+0/−5)°C
Time Within 5°C of Actual Peak Temperature (t_P)	<30 sec
Ramp-Down Rate	6°C/sec maximum
Time from 25°C to Peak Temperature	8 minutes maximum

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001 and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADPD4200

Table 11. ADPD4200, 24-Ball WLCSP

ESD Model	Withstand Threshold (V)	Class
HBM	2500	2
CDM	1250	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

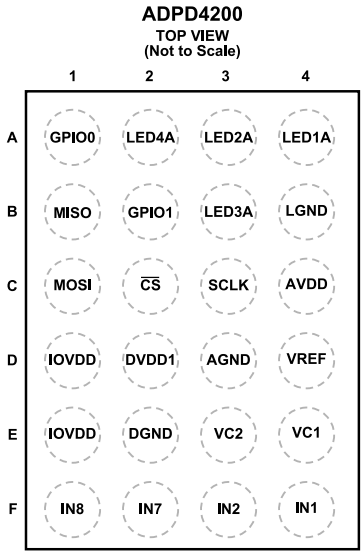

Figure 4. Pin Configuration

Table 12. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1	GPIO0	DIO	General-Purpose Input and Output 0. The GPIO0 pin is used for interrupts and various clocking options.
A2	LED4A	AO	LED Driver 4A Current Sink. If not in use, leave the LED4A pin floating.
A3	LED2A	AO	LED Driver 2A Current Sink. If not in use, leave the LED2A pin floating.
A4	LED1A	AO	LED Driver 1A Current Sink. If not in use, leave the LED1A pin floating.
B1	MISO	DO	SPI Master Input/Slave Output.
B2	GPIO1	DIO	General-Purpose Input and Output 1. The GPIO1 pin is used for interrupts and various clocking options.
B3	LED3A	AO	LED Driver 3A Current Sink. If not in use, leave the LED3A pin floating.
B4	LGND	AO	LED Driver Ground.
C1	MOSI	DIO	SPI Master Output/Slave Input.
C2	$\overline{CS}$	DIO	SPI Chip Select Input.
C3	SCLK	DIO	SPI Clock Input.
C4	AVDD	S	1.8 V Analog Supply.
D1	IOVDD	S	Input and Output Driver Ground.
D2	DVDD1	S	1.8 V Digital Supply.
D3	AGND	S	Analog Ground.
D4	VREF	REF	Internally Generated ADC Voltage Reference. Buffer the VREF pin with a 1 µF capacitor to AGND.
E1	IOVDD	S	1.8 V or 3.3 V Input and Output Driver Supply.
E2	DGND	S	Digital Ground.
E3	VC2	AO	Output Voltage Source 2 for Photodiode Common Cathode Bias or Other Sensor Stimulus.
E4	VC1	AO	Output Voltage Source 1 for Photodiode Common Cathode Bias or Other Sensor Stimulus.
F1	IN8	AI	Current Input 8. If not in use, leave the IN8 pin floating.
F2	IN7	AI	Current Input 7. If not in use, leave the IN7 pin floating.
F3	IN2	AI	Current Input 2. If not in use, leave the IN2 pin floating.
F4	IN1	AI	Current Input 1. If not in use, leave the IN1 pin floating.

[1] DIO means digital input and output, AO means analog output, DO means digital output, S means supply, REF means voltage reference, and AI means analog input.

TYPICAL PERFORMANCE CHARACTERISTICS

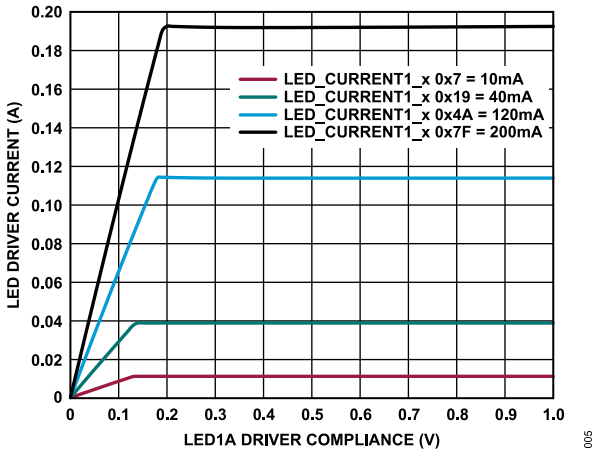

Figure 5. LED Driver Current vs. LED1A Driver Compliance at 10 mA, 40mA, 120 mA, and 200 mA

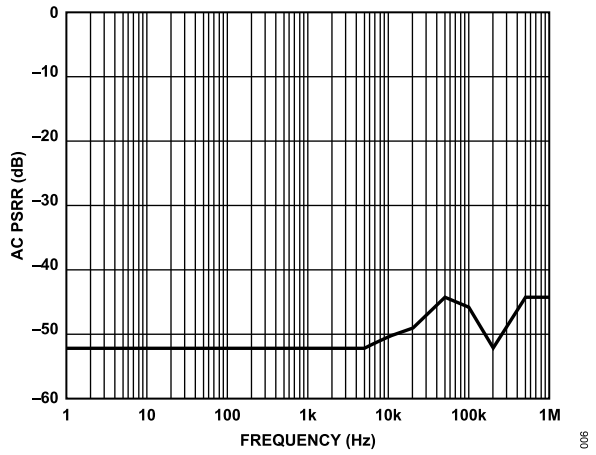

Figure 6. AC PSRR vs. Frequency

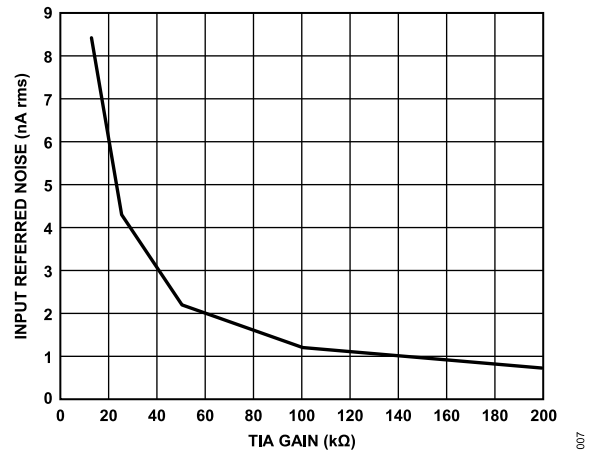

Figure 7. Input Referred Noise vs. TIA Gain

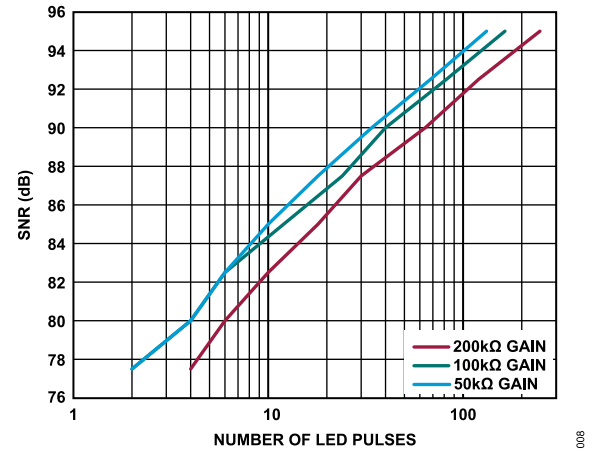

Figure 8. SNR vs. Number of Pulses, C_{PD} = 70 pF

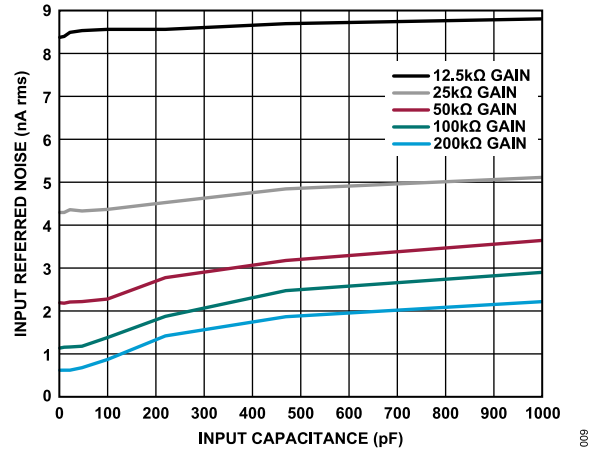

Figure 9. Referred to Input Noise vs. Input Capacitance

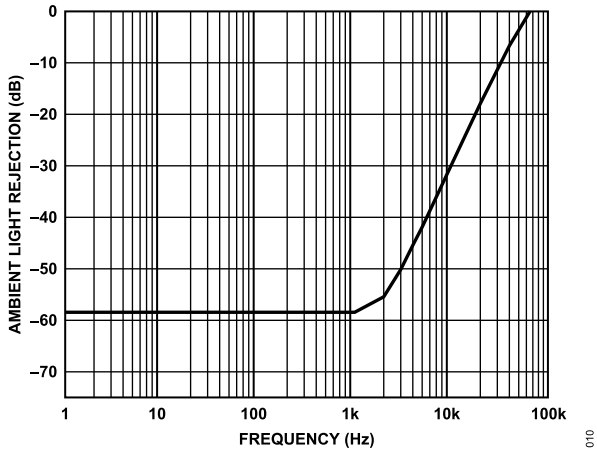

Figure 10. Ambient Light Rejection vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

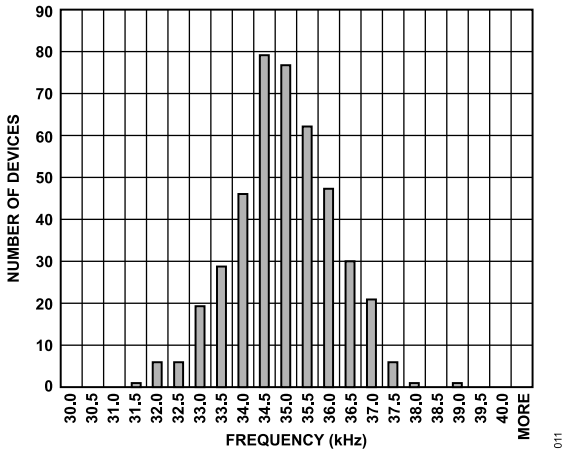

Figure 11. 32 kHz Clock Frequency Distribution, Untrimmed

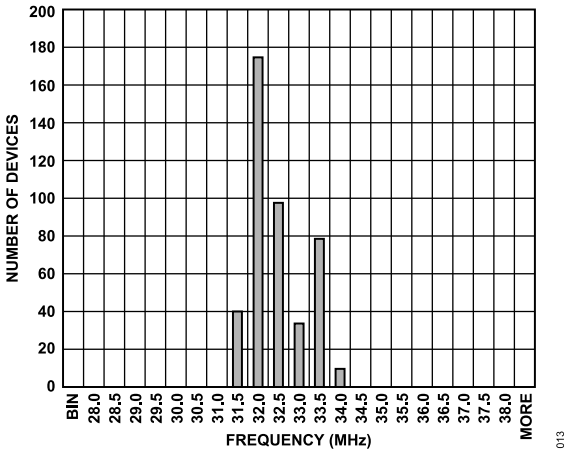

Figure 13. 32 MHz Clock Frequency Distribution, Untrimmed

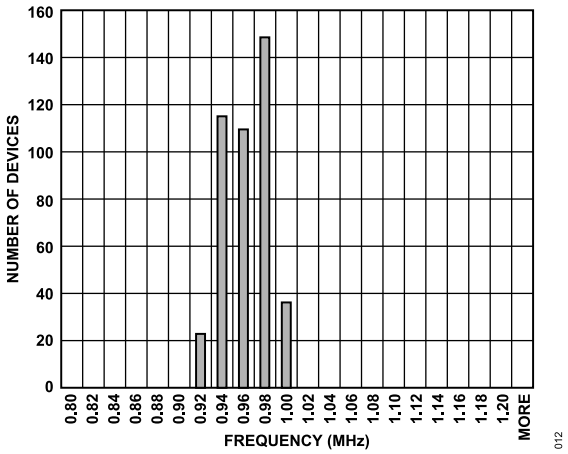

Figure 12. 1 MHz Clock Frequency Distribution, Untrimmed

THEORY OF OPERATION

INTRODUCTION

The ADPD4200 operates as a complete multimodal sensor front end, stimulating up to four LEDs and measuring the return signal on up to four separate current inputs. Twelve time slots are available, enabling 12 separate measurements per sampling period. The analog inputs can be driven single-ended or in differential pairs. The four analog inputs are multiplexed into a single channel or two independent channels, enabling simultaneous sampling of two sensors.

The analog front end (AFE) consists of a TIA, band-pass filter (BPF), integrator, and ADC. The digital block provides multiple operating modes, programmable timing, two GPIOx pins, block averaging, and a selectable second-order through fourth-order cascaded integrator comb (CIC) filter. Four independent LED drivers are provided that can each drive up to 200 mA. Four LED drivers can be enabled in any time slot and can be programmed from 2 mA to 200 mA monotonically, with a 7-bit register setting. The LED drivers enabled in any time slot can provide a total combined maximum of 400 mA of LED current.

The core circuitry provides stimulus to the sensors connected to the inputs of the device and measures the response, storing the results in discrete data locations. The four inputs can drive two simultaneous input channels, either in a single-ended or differential configuration. Data is read directly by a register or through a FIFO method. This highly integrated system includes an analog signal processing block, digital signal processing block, an SPI communication interface, programmable pulsed LED current sources, and pulsed voltage sources for sensors that require voltage excitation.

When making optical measurements, the ADPD4200 provides 60 dB of ambient light rejection using a synchronous modulation scheme with pulses as short as 1 µs combined with a BPF. Ambient light rejection is automatic without the need of external control loops, dc current subtraction, or digital algorithms.

The LED driver is a current sink and is independent from the LED supply voltage and the LED type. The inputs can be connected to any sensor that provides currents up to 200 µA. The ADPD4200 can also interface with voltage output sensors with a series resistor placed between the sensor output and the ADPD4200 inputs to convert the voltage to a current. The ADPD4200 produces a high SNR for relatively low LED power while greatly reducing the effect of ambient light on the measured signal.

ANALOG SIGNAL PATH

The ADPD4200 analog signal path consists of four current inputs that can be configured as single-ended or differential pairs into one of two independent channels. The two channels can be sampled simultaneously for applications that require instantaneous sampling of two sensors. Each channel contains a TIA with programmable gain, a BPF with a high-pass corner at 100 kHz and a low-pass cut-off frequency of 390 kHz, and an integrator capable of integrating ±7.5 pC per sample. Each channel is time multiplexed into a 14-bit ADC. In Figure 14, R_F is the TIA feedback resistor, and R_{INT} is the series resistor to the input of the integrator.

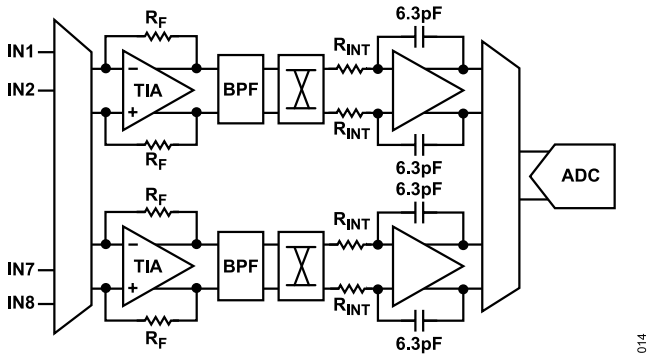

Figure 14. Analog Signal Path Block Diagram

THEORY OF OPERATION

Analog Input Multiplexer

The ADPD4200 supports four analog input pins. Each input can be used as a single-ended input or as part of a differential pair. Figure 15 shows a single representation of the input switch matrix, which allows programmable connection to the two AFE channels. Each pair of inputs has an exact duplicate of this multiplexer: IN1 and IN2, and IN7 and IN8. The connections are programmable per time slot.

The PAIR12 and PAIR78 bits select whether the matching input pair is used as two single-ended inputs or as a differential pair. This selection is valid for all active time slots. The INP12_x and INP78_x bits specify whether the input pair is enabled during the corresponding time slot and, if enabled, which input is connected to which AFE channel.

The sleep conditions are used for any inputs that are not enabled. Sleep conditions are determined by the INP_SLEEP_12 and INP_SLEEP_78 bits, which specify the state for the input pairs during sleep and when the inputs are not active. Inputs are only considered active during the precondition and pulse regions for time slots where they are enabled.

Preconditioning of the sensor connected to the input is provided to set the operating point at the input just before sampling. There are several different options for preconditioning determined by the PRECON_x bits. The PRECON_x bits are provided for each time slot to specify the precondition for enabled inputs or input pairs during the corresponding time slot. Preconditioning options include: float the input(s), VC1, VC2, input common-mode voltage (V_{ICM}), TIA_VREF, TIA input, and short the input pair. The preconditioning time at the start of each time slot is programmable using the PRE_WIDTH_x bits. The default preconditioning period is 8 µs.

The block diagram in Figure 15 shows all the bias levels that can be switched into the input connections during sleep and preconditioning. These connections are not available during the sampling phase of a time slot in which the input is selected.

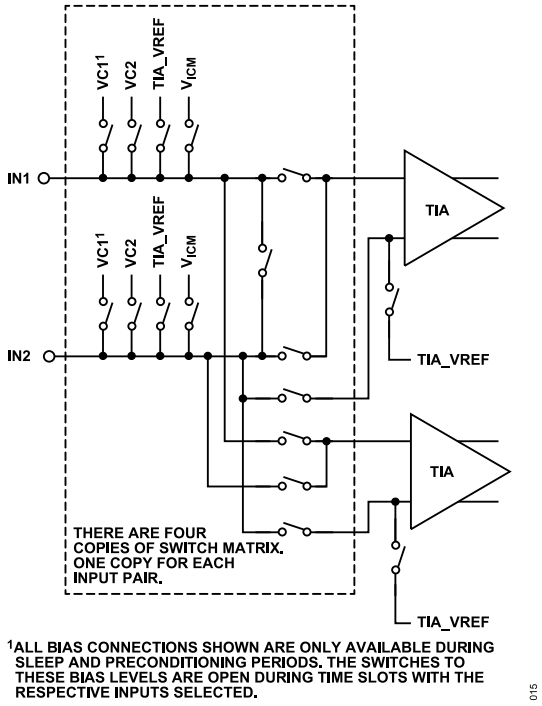

Figure 15. Analog Input Multiplexer

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Second AFE Channel

The second AFE channel is disabled by default. When disabled, the three amplifiers (TIA, BPF, and integrator) are automatically powered down, and no ADC cycles occur for the second channel. Digital integration and impulse response mode do not use the second channel.

The second AFE channel can be enabled with the CH2_EN_x bits on a per time slot basis. When the second channel is enabled, ADC conversions and the datapath bits of the second channel operate. When data is being written to the FIFO, the Channel 2 data is written after the Channel 1 data.

The Channel 2 TIA gain, integrator resistor, and buffer gain (when in digital integrate or TIA ADC mode) are set separately from Channel 1.

LED DRIVERS

The ADPD4200 has four LED drivers, which can drive up to four LEDs simultaneously. The LED output driver is a current sink. Figure 16 shows an example of a single LED driver output pair. The ADPD4200 supports only one side of each LED driver, unlike the ADPD4100/ADPD4101 devices. Therefore, there is no LEDxB pin in the ADPD4200 device, but there is still a register to configure the relative LED.

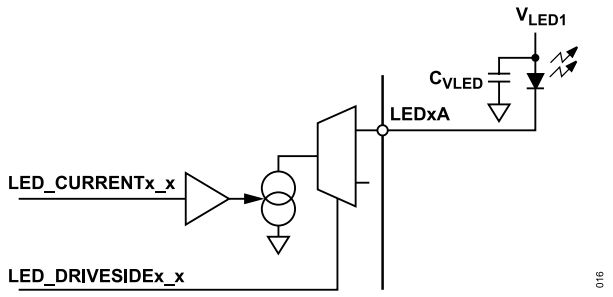

Figure 16. Block Diagram of LED Driver Output Pair

The LED driver output pins, LED1A, LED2A, LED3A, and LED4A, have an absolute maximum voltage rating of 3.9 V. Any voltage exposure over this rating affects the reliability of the device operation and, in certain circumstances, causes the device to cease proper operation. The voltage of the LED driver output pins must not be confused with the supply voltages for the LED themselves. V_{LEDx} is the voltage applied to the anode of the external LED, whereas the LED output driver pin is connected to the cathode of the external LED. The compliance voltage is the amount of headroom voltage at the LED driver pin, measured with respect to ground, required to maintain the programmed LED current level and is a function of the current required. Figure 5 shows the typical compliance voltages required at various LED current settings.

Either side of each LED driver output pair, but not both, can be driven in any of the 12 available time slots. Up to four LED driver outputs can be enabled in any time slot using the LED_DRIVESIDE1_x, LED_DRIVESIDE2_x, LED_DRIVESIDE3_x, and LED_DRIVESIDE4_x bit fields. The current is set on a per driver, per time slot basis using the LED_CURRENT1_x, LED_ CURRENT2_x, LED_CURRENT3_x, and LED_CURRENT4_x bit fields. Each driver can be programmed from 1.5 mA to 200 mA with a monotonic 7-bit setting, as shown in Figure 17. Each setting from 1 to 127 increases the LED drive current by ~1.6 mA. Setting LED_CURRENTx_x = 0 disables that particular driver.

Although each driver can be programmed to 200 mA and up to four LED drivers can be enabled in any time slot, there is a 400 mA limit of combined LED driver current that can be provided in any time slot. It is up to the user to program the LED drivers such that this 400 mA limit is not exceeded. If the 400 mA limit is exceeded by the user settings, priority is given, in the following order, to LED1x, LED2x, LED3x, and LED4x. For example, if the user settings have LED1A set to 150 mA, LED2A set to 150 mA, and LED3A set to 150 mA in a single time slot, LED1A and LED2A both provide 150 mA. However, LED3A is limited to 100 mA to maintain the 400 mA total LED drive current limit for the device.

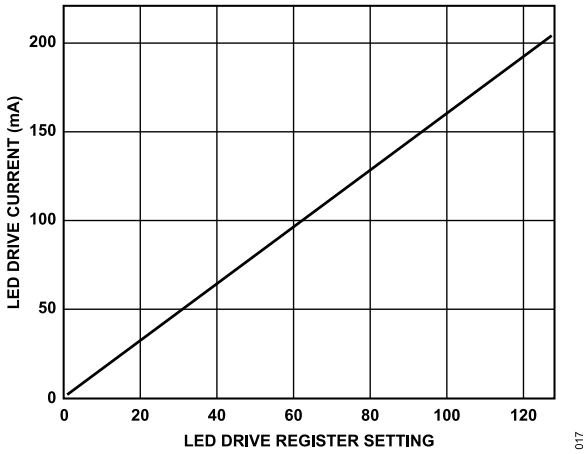

Figure 17. LED Driver Current vs. LED Drive Register Setting

DETERMINING C_{VLED}

To determine the bypass capacitor (C_{VLED}) value, determine the maximum forward-biased voltage, $V_{FB\_LED\_MAX}$, of the LED in operation. The maximum LED current, I_{LED_MAX}, converts to $V_{FB\_LED\_MAX}$ as shown in Figure 18. In this example, 125 mA of current through two green LEDs in parallel yields $V_{FB\_LED\_MAX}$ = 3.5 V. Any series resistance in the LED path must also be included in this voltage. When designing the LED path, keep in mind that small resistances can add up to large voltage drops due to the LED peak current being large. In addition, these resistances can be unnecessary constraints on the V_{LEDx} supply.

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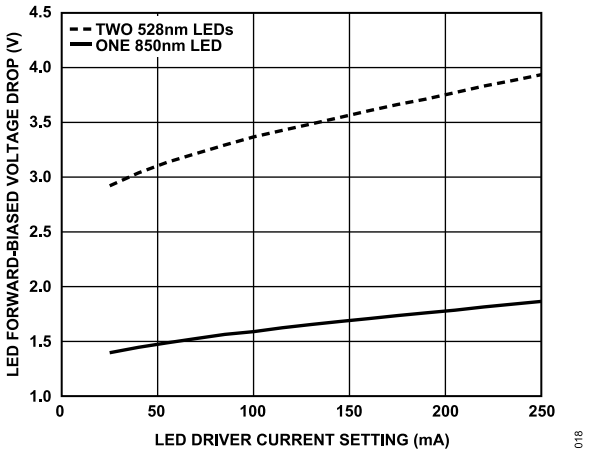

Figure 18. Example of the Average LED Forward-Biased Voltage Drop as a Function of the LED Driver Current Setting

To correctly size the C_{VLED} capacitor, do not deplete it during the pulse of the LED to the point where the voltage on the capacitor is less than the forward bias on the LED. Calculate the minimum value for C_{VLED} as follows:

$$C_{VLED} = \left(t_{LED\_PW} \times I_{LED\_MAX}\right) / \left(V_{LED\_MIN} - \left(V_{FB\_LED\_MAX} + V_{COMP}\right)\right) \quad (1)$$

where:
t_{LED_PW} is the LED pulse width.
I_{LED_MAX} is the maximum forward-biased current on the LED used in operating the devices.
V_{LED_MIN} is the lowest voltage from the V_{LEDx} supply with no load.
$V_{FB\_LED\_MAX}$ is the maximum forward-biased voltage required on the LED to achieve I_{LED_MAX}.
V_{COMP} is the compliance voltage of the LED driver at the programmed LED drive level.

The numerator of Equation 1 sets up the total discharge amount in coulombs from the bypass capacitor to satisfy a single programmed LED pulse of the maximum current. The denominator represents the difference between the lowest voltage from the V_{LEDx} supply and the LED required voltage. The LED required voltage is the voltage of the anode of the LED such that the compliance of the LED driver and the forward-biased voltage of the LED operating at the maximum current is satisfied. At a 125 mA drive current, the compliance voltage of the driver is ~0.4 V. For a typical ADPD4200 example, assume that the lowest value for the V_{LEDx} supply is 4.5 V, and that the peak current is 125 mA for two 528 nm LEDs in parallel. The minimum value for C_{VLED} is then equal to 1 µF.

$$C_{VLED} = \left(3 \times 10^{-6} \times 0.125\right) / (4.5 - (3.5 + 0.4)) = 0.625 \quad \mu F \quad (2)$$

As shown in Equation 2, as the minimum supply voltage drops close to the maximum anode voltage, the demands on C_{VLED} become more stringent, forcing the capacitor value higher. It is important to insert the correct values into Equation 2. For example, using an average value for V_{LED_MIN} instead of the worst case value for V_{LED_MIN} can cause a serious design deficiency, resulting in a C_{VLED} value that is too small, causing insufficient optical power in the application.

Additionally, multiple pulses can cause further droop on the V_{LEDx} supply if the C_{VLED} capacitor is not fully recharged between pulses. Therefore, adding a sufficient margin on C_{VLED} is strongly recommended. Add additional margin to C_{VLED} to account for multiple pulses and derating of the capacitor value over voltage, bias, temperature, and other factors over the life of the component.

DATAPATH, DECIMATION, SUBSAMPLING, AND FIFO

ADC samples are gathered for each pulse in each time slot and combine to create a running positive and negative sum for each time slot. These sums are each kept as a 32-bit unsigned value register and saturate if the values overflow 32 bits. Each ADC sample is added to either the positive or negative sum based on the SUBTRACT_x bits for the current pulse in standard sampling mode, or in the lit or dark acquisition regions for digital integration mode. In impulse mode, the positive sum is used to add two values and the result is written directly to the FIFO. Figure 19 shows the datapath structure.

At the end of the pulse operations in each time slot, the signal value is calculated by subtracting the negative accumulator from the positive accumulator. The signal and dark values are then clipped to positive numbers and are processed by the decimation unit. If the decimated value is ready, the data registers update, and the selected values are written to the FIFO. The data interrupt for that time slot is also set at this time.

THEORY OF OPERATION

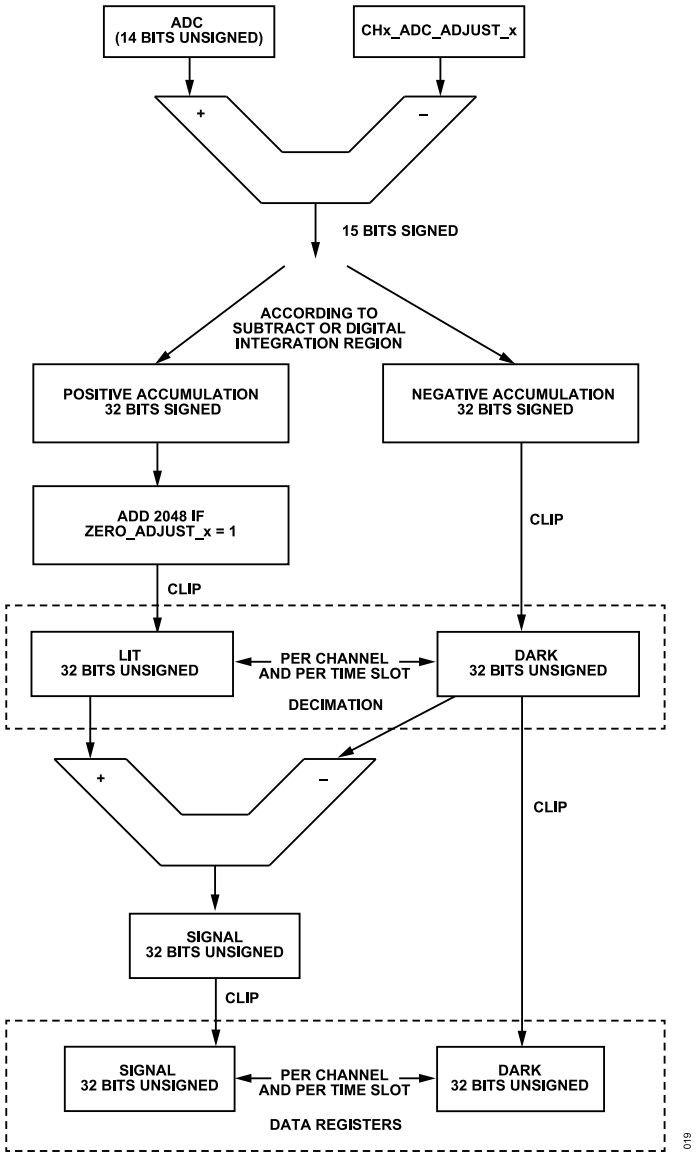

Figure 19. Datapath Block Diagram

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Decimation

The DECIMATE_FACTOR_x bits determine the number of time slot values used to create a 32-bit final sample value at a rate of

$$Sample\ \ Rate = (1/TIMESLOT\_PERIOD\_x)/(DECIMATE\_FACTOR\_x + 1)$$

If DECIMATE_FACTOR_x is 0, the output sample rate equals the time slot rate. The final value is the sum of the decimated samples. There is no divide by (DECIMATE_FACTOR_x + 1) operation performed on the decimated data, but final data values can be bit shifted to the right before being written to the FIFO, creating a direct average when the number of samples is a power of 2. DECIMATE_TYPE_x selects the method of decimation used. A setting of 0 selects a simple block sum with other settings allowing higher order CIC filters up to fourth order. If using higher order CIC filters for the signal data, the dark data still uses the simple block sum at the same decimation rate. Each time slot maintains its own block sum or CIC filter state. The entire decimation path uses a 32-bit datapath. When using the CIC filter, the number of bits required for the result is dependent on the number of pulses, the decimation rate, and the order of the CIC filter according to the following equation:

$$N_{BITS} = 14 + \log_2(Number\ \ of\ \ Pulses) + (\log_2(Decimation\ \ Rate))(CIC\ \ Order)$$

It is up to the user to ensure that there is no undesired overflow.

Final data results can be read from data registers or a 512-byte data FIFO. Data written to the FIFO is configurable to allow the different data registers, formats, and data sizes as required. Each time slot can use its own decimation rate. Data from each time slot is written to the FIFO at its respective ODR.

Subsampling

The ADPD4200 supports a subsampling mode that allows selected time slots to run at slower sampling rates than the programmed sampling rate. For example, in a multiparameter application where most of the measurements must be taken at a sampling rate of 300 Hz but one of the measurements must only be taken at 25 Hz, the subsampling mode can be used on the time slot that only needs to operate at 25 Hz. To enable subsampling mode for a specific time slot, set the SUBSAMPLE_x bit to 1 and set the DECIMATE_FACTOR_x bits to the desired subsampling rate. The subsampled time slot then samples only once every (DECIMATE_FACTOR_x + 1) cycle, instead of operating every time slot sequence. If other time slots are decimating at the same rate, the subsampled cycles occur at the same time the decimated data is presented to the FIFO. For example, if Time Slot A is operating at 300 Hz but decimating to 25 Hz, and Time Slot B is set to subsample by 12, both time slots write the FIFO during the same time slot sequence and at the same rate.

More complicated patterns can be made if the decimate and subsample rates for the enabled time slots are different. The user must manage the varying packet sizes by reading the data in multiples of the repeating packet size. For example, if Time Slot A is not decimating or subsampling, Time Slot B is subsampling every second cycle, and Time Slot C is subsampling every fourth cycle, the data pattern written to the FIFO is A, AB, A, ABC, and so on, as the repeating packet.

Decimation and subsampling have the same effect on the output data rate. The only difference is that the decimated time slots operate every input cycle but produce data at the slower rate using the on-chip decimating filter. The subsampling time slots only occur at the slower rate.

Status bytes are written to the FIFO every wake-up period, regardless of which time slots execute. Using the same example as the different decimate and subsample rates scenario, but with a status byte enabled, the pattern is AS, ABS, AS, ABCS, and so on, where S is a status byte.

FIFO

Data is written to the FIFO at the end of each sampling period. This packet can include 0, 8-, 16-, 24-, or 32-bit data for each of the dark data and signal data values. The bit alignment of the data written to the FIFO is selectable with a shift of 0 bits to 31 bits, with saturation provided. Lower bits are ignored. The DARK_SHIFT_x and SIGNAL_SHIFT_x bit fields select the number of bits to shift the output data to the right before writing to the FIFO. The DARK_SIZE_x and SIGNAL_SIZE_x bit fields select the number of bytes of each field to be written from 0 bytes to 4 bytes. When set to 0, no data is written for that data type. If there are any nonzero bits at more significant bit positions than those selected, the data written to the FIFO is saturated. If both channels are enabled, all selected Channel 1 data values are written to the FIFO first, followed by the Channel 2 data.

For example, in modes that utilize dark data, the eight upper bits of the dark data can be stored with 24 appropriately selected bits from the signal data for each time slot to allow detection of whether the ambient light is becoming large, while limiting the size of the amount of data transferred.

Data is written to the FIFO at the end of the sampling period only if there is enough FIFO space left to write data for each active timeslot. For example, if one active timeslot is running at an ODR of 100 Hz and a second timeslot is decimating by 4 or subsampling at 1/4th the rate of the first timeslot for an ODR of 25 Hz, data is only going to be written to the FIFO at the end of the sampling period if there is enough room for both active timeslots to write data, regardless of whether or not the timeslot that is decimating or subsampling is supposed to write data during that sampling period. It is up to the user to manage the data appropriately at the microprocessor end when using timeslots with different decimation and/or subsampling rates.

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The FIFO is never written with partial packets of data. If there is not enough room for all of the data to be written to the FIFO for all enabled time slots and any selected status bytes, no data is written from any of the time slots during that period, and the INT_FIFO_OFLOW status bit is set.

The order of samples written to the FIFO (if selected) is dark data followed by signal data. The byte order for multibyte words is shown in Table 13.

Table 13. Byte Order for FIFO Writes

Size	Byte Order (After Shift)
8	[7:0]
16	[15:8], [7:0]
24	[15:8], [7:0], [23:16]
32	[15:8], [7:0], [31:24], [23:16]

The FIFO size is 512 bytes. When the FIFO is empty, a read operation returns 0xFF, and the INT_FIFO_UFLOW status bit is set.

In addition to the FIFO, the signal and dark 32-bit registers can be directly read. These registers are effectively two-stage registers where there is an internal data register that updates with every sample and a latched output data register that is accessed by the host. The data interrupts can be used to align the access of these registers to just after the registers are written. If using the interrupt timing is troublesome, use the HOLD_REGS_x bit field to prevent update of the output registers during access not aligned to the interrupt. Setting the HOLD_REGS_x bit field blocks the update of the latched output data register and ensures that the dark and signal values read by the host are from the same sample point. If additional samples occur while the HOLD_REGS_x bit field is set, the samples are written to the internal data register but not latched into the output data register that is accessed by the host. Setting the HOLD_REGS_x bit field to 0 reenables the pass through of new data.

After all time slots have completed, the optional status bytes are written to the FIFO. See the Optional Status Bytes section for more information.

CLOCKING

Low Frequency Oscillator

A low frequency oscillator clocks the low speed state machine, which sets the time base used to control the sample timing, wake-up states, and overall operation. There are three options for low frequency oscillator generation. The first option is an internal, selectable 32 kHz or 1 MHz oscillator. The second option is for the host to provide a low frequency oscillator externally. Finally, the low frequency oscillator can be generated by a divide by 32 or divide by 1000 of an external high frequency clock source at 32 MHz. When powering up the device, it is expected that the low frequency oscillator is enabled and left running continuously.

To operate with the on-chip low frequency oscillator, use the following writes. Set the LFOSC_SEL bit to 0 to select the 32 kHz clock or 1 if the 1 MHz clock is desired. Then, set either the OSC_1M_EN or OSC_32K_EN bit to 1 to turn on the desired internal oscillator. The internal 32 kHz clock frequency is set using the 6-bit OSC_32K_ADJUST bit field. The internal 1 MHz clock frequency is set using the 10-bit OSC_1M_FREQ_ ADJ bit field.

If higher timing precision is required than can be provided by the on-chip low frequency oscillator, this oscillator can be driven directly from an external source provided on a GPIOx input. To enable an external low frequency clock, use the following writes. Enable one of the GPIOx inputs using the GPIO_PIN_CFGx bit fields. Next, use the ALT_CLK_GPIO bit field to choose the enabled GPIOx input to be used for the external low frequency oscillator. Set the ALT_CLOCKS bit field to 0x1 to select an external low frequency oscillator. Finally, use the LFOSC_SEL bit to match whether a 32 kHz or 1 MHz clock is being provided.

In a third method, an external 32 MHz clock is used for both the high frequency clock and to be divided down to generate the low frequency clock. To use this method, follow the previous instructions for an external low frequency clock but set the ALT_CLOCKS bit field to 0x3, and use the LFOSC_SEL bit to determine if a divide by 32 or 1000 is used to generate the low frequency clock so that either a 32 kHz or 1 MHz clock is generated from the external 32 MHz clock.

High Frequency Oscillator

A 32 MHz high frequency oscillator is generated internally or can be provided externally. This high frequency clock clocks the high speed state machine, which controls the AFE operations during the time slots, such as LED timing and integration times.

The high frequency oscillator can be internally generated by setting the ALT_CLOCKS bits to 0x0 or 0x1. When selected, the internal 32 MHz oscillator is enabled automatically by the low speed state machine during the appropriate wake-up time or during the 32 MHz oscillator calibration routine.

The high frequency oscillator can also be driven from an external source. To provide an external 32 MHz high frequency oscillator, enable one of the GPIOx inputs using the GPIO_PIN_CFGx bits. Then, use the ALT_CLK_GPIO bits to choose the enabled GPIOx input for the external high frequency oscillator. Finally, write 0x2 or 0x3 to the ALT_CLOCKS bits to select an external high frequency oscillator. Writing 0x2 provides only the high frequency oscillator from the external source, whereas writing 0x3 generates both the low frequency oscillator and high frequency oscillator from the external 32 MHz source. When using an external 32 MHz oscillator, it must be kept running continuously for proper device operation.

TIME STAMP OPERATION

The time stamp feature is useful for calibration of the low frequency oscillator as well as providing the host with timing information

THEORY OF OPERATION

during time slot operation. Time stamping is supported by the use of any GPIOx as a time stamp request input, the CAPTURE_TIMESTAMP bit to enable capture of the time stamp trigger, a time counter running in the low frequency oscillator domain, and two output registers. The output bits include TIMESTAMP_COUNT_x, which holds the number of low frequency oscillator cycles between time stamp triggers, and TIMESTAMP_SLOT_DELTA, which holds the number of low frequency oscillator cycles remaining to the next time slot start.

The setup for using the time stamp operation is as follows:

1. Set CLK_CAL_ENA = 1 to enable the oscillator calibration circuitry.
2. Configure a GPIOx to support the time stamp input using the appropriate GPIO_PIN_CFGx bits. Select the matching GPIOx to provide the time stamp using the TIMESTAMP_GPIOx bits.
3. Configure the ADPD4200 for operation and enable the low frequency oscillator.
4. If the TIMESTAMP_SLOT_DELTA function is desired, start the time slot operation by placing the device in go mode using the OP_MODE bit (see Table 14). For low frequency oscillator calibration, it is only required that the low frequency oscillator be enabled. The device does not have to be in go mode for low frequency oscillator calibration.

Use the following procedure to capture the time stamp:

1. Set the CAPTURE_TIMESTAMP bit to 1 to enable the capture of the time stamp on the next rising edge of the selected GPIOx input.
2. The host provides the initial time stamp trigger on the selected GPIOx at an appropriate time.
3. The CAPTURE_TIMESTAMP bit is cleared when the time stamp signal is captured unless the TIMESTAMP_ALWAYS_EN bit is set, in which case, the capture of the time stamp is always enabled. Reenable the capture if necessary.
4. The host provides a subsequent time stamp trigger on the selected GPIOx at an appropriate time.
5. The number of low frequency oscillator cycles that occurred between time stamp triggers can be read from the TIMESTAMP_COUNT_x bits.

The host must continue to handle the FIFO and/or data register data normally during time stamp processing.

If using a dedicated pin for a time stamp that does not have transitions other than the time stamp, set the TIMESTAMP_ALWAYS_EN bit to avoid automatic clearing of the CAPTURE_TIMESTAMP bit. This setting removes the need to enable the time stamp capture each time.

The time stamp can calibrate the low frequency oscillator as described in the Low Frequency Oscillator Calibration section. The host can also use TIMESTAMP_SLOT_DELTA to determine when the next time slot occurs. TIMESTAMP_SLOT_DELTA can determine the arrival time of the samples currently in the FIFO. TIMESTAMP_SLOT_DELTA does not account for the decimation factor.

The time stamp trigger is edge sensitive and can be set to either trigger on the rising edge (default) or falling edge using TIMESTAMP_INV.

LOW FREQUENCY OSCILLATOR CALIBRATION

The time stamp circuitry can be used to calibrate either the 32 kHz or 1 MHz low frequency oscillator circuit by adjusting the frequency to match the timing of the time stamp triggers. Simply compare the TIMESTAMP_COUNT_x value in low frequency oscillator cycles to the actual time stamp trigger period and adjust the OSC_32K_ADJUST or OSC_1M_FREQ_ ADJ value accordingly.

HIGH FREQUENCY OSCILLATOR CALIBRATION

The high frequency oscillator is calibrated by comparing multiples of its cycles with multiple cycles of the low frequency oscillator, which is calibrated to the system time. Calibration of the low frequency oscillator precedes calibration of the high frequency oscillator. The method for calibrating the high frequency oscillator is as follows:

1. Write 1 to the OSC_32M_CAL_START bit.
2. The ADPD4200 automatically powers up the high frequency oscillator.
3. The device automatically waits for the high frequency oscillator to be stable.
4. An internal counter automatically counts the number of 32 MHz high frequency oscillations that occur during 128 cycles of the 1 MHz low frequency oscillator or 4 cycles of the 32 kHz low frequency oscillator, depending on which low frequency oscillator is enabled based on the setting of the LFOSC_SEL bit.
5. The OSC_32M_CAL_COUNT bits are updated with the final count.
6. The 32 MHz oscillator automatically powers down following calibration unless time slots are active.
7. The device resets the OSC_32M_CAL_START bit indicating the count has been updated.

The OSC_32M_FREQ_ADJ bits adjust the frequency of the 32 MHz oscillator to the desired frequency. When using an external low frequency oscillator, the 32 MHz oscillator calibration is performed with respect to the externally provided low frequency oscillator.

When low frequency oscillator and high frequency oscillator calibrations are complete, set the CLK_CAL_ENA bit = 0 to disable the clocking of the oscillator calibration circuitry to reduce power. The CLK_CAL_ENA bit defaults to 0 so that the calibration circuitry is disabled by default.

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TIME SLOT OPERATION

Operation of the ADPD4200 is controlled by an internal configurable controller that generates all the timing needed to generate sampling regions and sleep periods. Measurements of multiple sensors and control of synchronous stimulus sources are handled by multiple time slots. The device provides up to 12 time slots for multisensor applications. The enabled time slots are repeated at the sampling rate, which is configured by the 23-bit TIMESLOT_PERIOD_x bit field in the TS_FREQ register. The sampling rate is determined by the following formula:

Sampling Rate = *Low Frequency Oscillator Frequency* (Hz) ÷ *TIMESLOT_PERIOD_x*

Each time slot allows the creation of one or more LED and/or modulation pulses, and the acquisition of the photodiode or other sensor current based on that stimulus. The operating parameters for each time slot are highly configurable.

Figure 20 shows the basic time slot operation sequence. Each time slot is repeated at the sampling rate, followed by an ultra low power sleep period. By default, subsequent time slots are initiated immediately following the end of the previous time slot. In addition, there is an option to add an offset to the start of the subsequent time slots using the TIMESLOT_OFFSET_x bit field as shown in Figure 21, which shows the TIMESLOT_ OFFSET_B bit field being used to offset the start of Time Slot B. In this case, each time slot still operates at the sampling rate, but there is a sleep period between Time Slot A and Time Slot B. The wake period shown in Figure 20 and Figure 21 is used to power up and stabilize the analog circuitry before data acquisition begins. If the TIMESLOT_OFFSET_B bit field is set to 0, the time slot starts as soon as the previous time slot finishes.

The time slot offset is always applied to the Time Slot A start time. For example, TIMESLOT_OFFSET_D is an offset added to the beginning of Time Slot A, not Time Slot C, which immediately precedes Time Slot D.

The amount of offset applied is dependent on the low frequency oscillator used. If using the 1 MHz low frequency oscillator,

Offset = 64 × (Number of 1 MHz Low Frequency Oscillator Cycles) × TIMESLOT_OFFSET_x

If using the 32 kHz low frequency oscillator,

Offset = 2 × (Number of 32 kHz Low Frequency Oscillator Cycles) × *TIMESLOT_OFFSET_x*

For example, if TIMESLOT_OFFSET_C is set to 0x040 and the 1 MHz low frequency oscillator is being used, the offset from the start of Time Slot A to the start of Time Slot C is

Offset = (64 × 1 µs × 64) = 4.096 ms

The sampling rate is controlled by the low frequency oscillator. The low frequency oscillator is driven by one of three sources as described in the Clocking section.

If the sampling period is set too short to allow the enabled time slots to complete, a full cycle of enabled time slot samples is skipped, effectively reducing the overall sample rate. For example, if the sampling rate is set to 100 Hz (10 ms period) and the total amount of time required to complete all enabled time slots is 11 ms, the next cycle of time slots does not begin until t = 20 ms, effectively reducing the sampling rate to 50 Hz.

If TIMESLOT_OFFSET_x is set too short to allow the previous time slot to finish, the time slot occurs immediately after the previous time slot. Time slots always occur in A through L order.

Using External Synchronization for Sampling

An external signal driven to a configured GPIOx pin can be used to wake the device from sleep instead of the TIMESLOT_PERIOD_x counter, which allows external control of the sample rate and time. This mode of operation is enabled using the EXT_SYNC_EN bit and uses the GPIOx pin selected by the EXT_SYNC_GPIO bits. If using this feature, be sure to enable the selected GPIOx pin as an input using the appropriate GPIO_PIN_CFGx bits.

When operating with external synchronization and set in go mode, the device enters sleep first and waits for the next external synchronization signal before waking up. This external synchronization signal is then synchronized to the low frequency oscillator and then starts the wake-up sequence. If an additional external synchronization is provided prior to completing time slot operations, it is ignored.

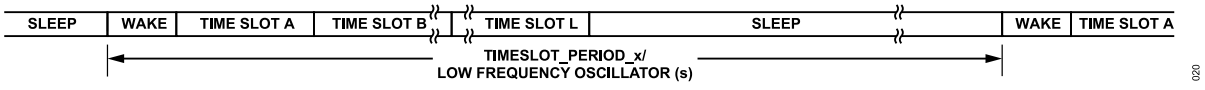

Figure 20. Basic Time Slot Operation Sequence

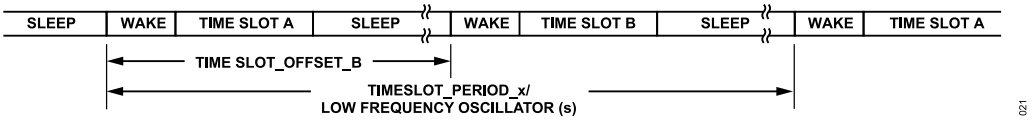

Figure 21. Time Slot Operation with Offset Using TIMESLOT_OFFSET_B

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EXECUTION MODES

A state machine in the low frequency oscillator clock domain controls sleep times, wake-up cycles, and the start of time slot operations. The low frequency oscillator serves as the time base for all time slot operations, controls the sample rates, and clocks the low frequency state machine. This state machine controls all operations and is controlled by the OP_MODE bit.

Table 14. OP_MODE Bit Setting Descriptions

OP_MODE Setting	Mode	Description
0	Standby	All operations stopped. Time slot actions reset. Low power standby state.
1	Go	Transitioning to this state from standby mode starts time slot operation.

At power-up and following any subsequent reset operations, the ADPD4200 is in standby mode. The user can write 0 to the OP_MODE bit to immediately stop operations and return to standby mode.

Register writes that affect operating modes cannot occur during go mode. The user must enter standby mode before changing the control registers. Standby mode resets the digital portion of the ADC, all of the pulse generators, and the state machine.

When OP_MODE is set to 1, the device immediately starts the first wake-up sequence and time slot operations unless using an external synchronization trigger. If using an external synchronization trigger, the device enters the sleep state before the first wake-up and time slot regions begin.

HOST INTERFACE

The ADPD4200 provides a SPI to communicate with the host. The device also provides numerous FIFO, data register, error, and threshold status bits, each of which can be provided by an interrupt function from a GPIOx, read from status registers, or appended as optional status bytes at the end of a FIFO packet.

Interrupt Status Bits

Data Register Interrupts

The data interrupt status bits, INT_DATA_x for each time slot, are set every time that the data registers for each time slot are updated. The state of the HOLD_REGS_x bit has no effect on the interrupt logic.

FIFO Threshold Interrupt

The FIFO threshold interrupt status bit, INT_FIFO_TH, is set when the number of bytes in the FIFO exceeds the value stored in the FIFO_TH register. The INT_FIFO_TH bit is cleared automatically when a FIFO read reduces the number of bytes below the value in the FIFO_TH register, which allows the user to set an appropriate data size for their host needs.

Level Interrupts

Two level interrupt status bits, INT_LEV0_x and INT_LEV1_x, provide an interrupt when the dark data or signal data values cross greater than or less than a programmed threshold level.

Two comparison circuits are available per time slot. The INT_LEV0_x or INT_LEV1_x status bits are set when the data register update meets the criteria set by the associated THRESH0_TYPE_x, THRESH0_DIR_x, THRESH0_CHAN_x settings, or by the associated THRESH1_TYPE_x, THRESH1_DIR_x, and THRESH1_CHAN_x settings.

The Level 0 interrupt operates as follows. The user sets an 8-bit threshold value in the THRESH0_VALUE_x bit field for the corresponding time slot. This value is then shifted to the left by anywhere from 0 bits to 24 bits, specified by the setting of the THRESH0_SHIFT_x bit field. A comparison is then made between the shifted threshold value and the register chosen by the THRESH0_TYPE_x bit field and the THRESH0_CHAN_x bit. The INT_LEV0_x status bit is set if the selected data register meets the criteria set in the THRESH0_DIR_x bit field. The Level 1 interrupt operates in the same fashion.

Clearing Interrupt Status Bits

All status bits are set regardless of whether the status bit is routed to one of the interrupt outputs, Interrupt X or Interrupt Y. The status bits are independent of the interrupt enable bits. The status bits are always set by the corresponding event. The interrupt bits stay set until they are either manually or automatically cleared.

The user can manually clear a given interrupt by writing a 1 to the matching interrupt status bit. In addition, the data interrupt status bits can be configured to clear automatically. When the INT_ACLEAR_DATA_x or INT_ACLEAR_FIFO bit is set, the appropriate interrupt status bit is automatically cleared when any matching data register or FIFO register is read. Automatic clearing of the interrupt status bits removes the need to manually clear these interrupts.

Optional Status Bytes

There is an option to append each data packet with status bits. This option is useful for hosts that cannot spare an interrupt channel to service. The status bytes can each be individually selected in the FIFO_STATUS_BYTES register. Each bit in the FIFO_ STATUS_BYTES register enables a status byte that is appended to the data packet in the FIFO. If any bit in the FIFO_STATUS_ BYTES register is set to 1, the byte that is appended to the data packet contains the status bits, as shown in Table 15. Table 15 shows the order, enable bit, and contents of each status byte.

The 4-bit sequence number cycles from 0 to 15 and is incremented with a wraparound every time the time slot sequence completes. This sequence number can also be made available bitwise on the GPIOx pins.

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Table 15. FIFO Status Byte Order and Contents

		Contents[1]							
Byte Order	Enable Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	ENA_STAT_SUM	0	0	Any LEV1_x	Any LEV0_x	4-bit sequence			
1	ENA_STAT_D1	DATA_H	DATA_G	DATA_F	DATA_E	DATA_D	DATA_C	DATA_B	DATA_A
2	ENA_STAT_D2	0	0	0	0	DATA_L	DATA_K	DATA_J	DATA_I
3	ENA_STAT_L0	LEV0_H	LEV0_G	LEV0_F	LEV0_E	LEV0_D	LEV0_C	LEV0_B	LEV0_A
4	ENA_STAT_L1	LEV1_H	LEV1_G	LEV1_F	LEV1_E	LEV1_D	LEV1_C	LEV1_B	LEV1_A
5	ENA_STAT_LX	LEV1_L	LEV1_K	LEV1_J	LEV1_I	LEV0_L	LEV0_K	LEV0_J	LEV0_I

[1] DATA_x refers to the data register interrupts for the corresponding time slot. LEV0_x and LEV1_x refer to Level 0 and Level 1 time slot interrupts, respectively, for Time Slot A through Time Slot L.

Interrupt Outputs, Interrupt X and Interrupt Y

The ADPD4200 supports two separate interrupt outputs, Interrupt X and Interrupt Y. Each interrupt has the option to be driven to any of the two GPIOx pins. The two different interrupt outputs can be generated for a host processor if desired. For example, the FIFO threshold interrupt, INT_FIFO_TH, can be routed to Interrupt X and used to drive the direct memory access (DMA) channel of the host, while the INT_FIFO_ OFLOW and INT_FIFO_UFLOW interrupts can be routed to Interrupt Y and used to drive an additional host interrupt pin. Another example case includes routing the data interrupt from a single time slot to Interrupt X and the FIFO threshold interrupt to Interrupt Y. The host receives one interrupt when the interrupt of that particular channel occurs and the host can then read that register directly. Interrupt Y, in this case, is handled by the host with the DMA or with an interrupt. Each of the different interrupt status bits can be routed to Interrupt X or Interrupt Y, or both.

For each interrupt, there is an associated Interrupt X and Interrupt Y enable bit. The logic for the Interrupt X and Interrupt Y function is a logic AND of the status bit with its matching enable bit. All enabled status bits are then logically OR'ed to create the interrupt function. The enable bits do not affect the status bits.

General-Purpose Inputs and Outputs

The ADPD4200 provides two general-purpose input and output pins: GPIO0 and GPIO1. These GPIOx pins can be used as previously described in the Interrupt Outputs, Interrupt X and Interrupt Y section for interrupt outputs or for providing external clock signals to the device. The GPIOx pins can also be used for many different control signals, as synchronization controls to external devices, as well as test signals that are useful during system debugging. All of the available signals that can be brought out on a GPIOx pin.

SPI

The ADPD4200 contains a SPI port, which operates synchronously with its respective input clocks and requires no internal clocks to operate.

The ADPD4200 has an internal power-on reset circuit that sets the device into a known idle state during the initial power-up. After the power-on reset is released, approximately 2 µs to 6 µs after the DVDD supply is active, the device can be read and written through the SPI.

The registers are accessed using addresses within a 15-bit address space. Each address references a 15-bit register with one address reserved for the FIFO read accesses. Reads and writes auto-increment to the next register if additional words are accessed as part of the same access sequence. This automatic address increment occurs for all addresses except the FIFO address, one less than the FIFO address and the last used address, which is 0x277. Reads from the FIFO address continue to access the next byte from the FIFO.

SPI Operations

The SPI single register write operation is shown in Figure 22. The first two bytes contain the 15-bit register address and specify that a write is requested. The remaining two bytes are the 16 data bits to write to the register. The register write occurs only when all 16 bits are shifted in prior to deassertion of the $\overline{CS}$ signal.

In addition, multiple registers can be written if an additional 16-bit data is shifted in before deassertion of the $\overline{CS}$ signal. The register address automatically increments to the next register after each 16 bits of data.

The SPI single register read operation is shown in Figure 23. The first two bytes contain the 15-bit register address and specify that a read is requested. Register bits are shifted out starting with the MSB. In addition, multiple registers can be read if an additional 16-bit data is shifted out prior to deassertion of the $\overline{CS}$ signal.

It is recommended that reading from the FIFO is performed byte wise. There is no requirement to read multiples of 16 bits.

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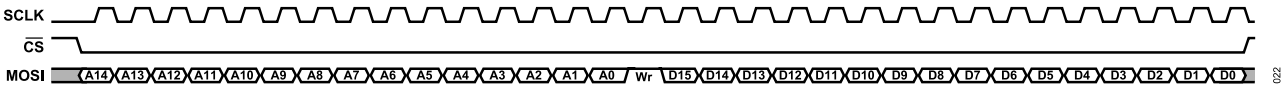

Figure 22. SPI Write Operation

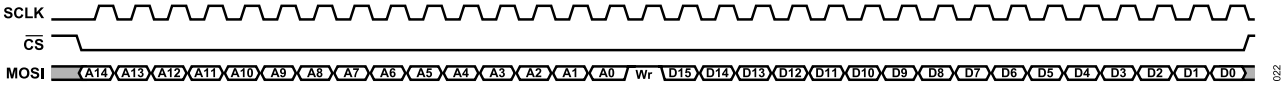

Figure 23. SPI Read Operation

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OPERATING MODE OVERVIEW

The ADPD4200 is effectively a charge measuring device that can interface with many different sensors enabling synchronous measurements of PPG, electrocardiography (ECG), electrodermal activity (EDA), impedance, capacitance, and temperature measurements. A selection of operating modes are built into the device to optimize each of the different sensor measurements supported.

SINGLE INTEGRATION MODE

Single integration mode is used for a single integration of incoming charge per ADC conversion and is the most common operating mode for the ADPD4200. In single integration mode, most of the dynamic range of the integrator is used when integrating the charge from the sensor response to a single stimuli event, for example, an LED pulse. There is also a multiple integration mode available for situations with very small sensor responses (see the Multiple Integration Mode section for more information).

Using LED as Stimulus

Single integration mode is the typical operating mode used for a PPG measurement, where an LED is pulsed into human tissue and the resultant charge from the photodiode response is integrated and subsequently converted by the ADC. Figure 24 shows an example of a typical PPG measurement circuit.

The MOD_TYPE_x value is left at the default value of 0 so that the TIA is continuously connected to the input of the TIA. Set the PRECON_x bit field to 0x5 to set the anode of the photodiode to the TIA_VREF potential during the preconditioning period. The VCx pin is connected to the cathode of the photodiode and is set to TIA_VREF + 250 mV to apply a 250 mV reverse bias across the photodiode, which reduces the photodiode capacitance and reduces the noise of the signal path. Set TIA_VREF to 1.27 V using the AFE_TRIM_VREF_x bit field for maximum dynamic range.

The LED pulse is controlled with the LED_OFFSET_x and LED_WIDTH_x bit field. The default LED offset (LED_OFFSET_x = 0x10) is 16 µs from the end of the preconditioning period and is suitable for most use cases. Recommended LED pulse widths are either 2 µs or 3 µs when using the BPF. Shorter LED pulse widths provide the greatest amount of ambient light rejection and the lowest power dissipation. The period is automatically calculated by the ADPD4200. The automatic calculation is based on the integration width selected and the number of ADC conversions. To use the automatic calculation, leave the MIN_PERIOD_x bit field at its default value of 0. If a longer period is desired, for example, if a specific pulse frequency is desired, use the MIN_PERIOD_x bit field to enable a longer period. In single integration mode for PPG measurements using 2 µs or 3 µs, the automatic period calculation is

$$Period = (2 + 2 \times INTEG\_WIDTH + (Number\ \ of\ \ Channels\ \ Enabled \times (ADC\_COUNT + 1)))$$

The integration pulses are controlled with the INTEG_OFFSET_x and INTEG_WIDTH_x bit fields. It is recommended that an integration width of 1 µs greater than the LED width be used because the signal spreads due to the response of the BPF. By setting the integration width 1 µs wider than the LED width, a maximum amount of charge from the incoming signal is integrated.

The number of ADC conversions defaults to a single ADC conversion. However, oversampling is available for increased SNR. The ADC conversions can be set to 1, 2, 3, or 4 based on the ADC_COUNT_x bit field. If two channels are enabled, Channel 1 occurs first, followed by Channel 2. The total number of pulses is equal to NUM_INT_x × NUM_REPEAT_x. In single integration mode, NUM_INT_x = 1 for a single integration sequence per ADC conversion. Therefore, the total number of pulses is controlled by NUM_REPEAT_x. Increasing the number of pulses reduces the noise floor of the measurement by a factor of √n, where n is the total number of pulses.

Figure 25 shows the timing operation where a single integration cycle is used per ADC conversion. Table 16 details the relevant registers using single integration mode for a PPG measurement.

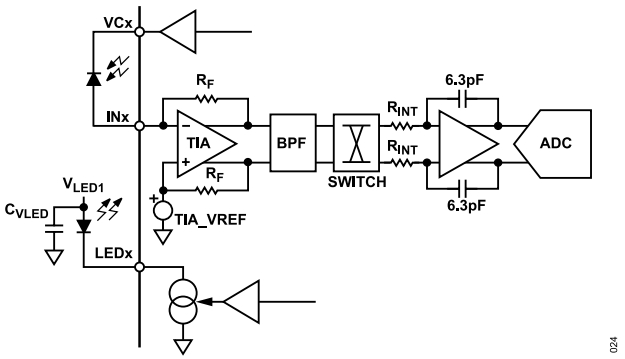

Figure 24. Typical PPG Measurement Circuit

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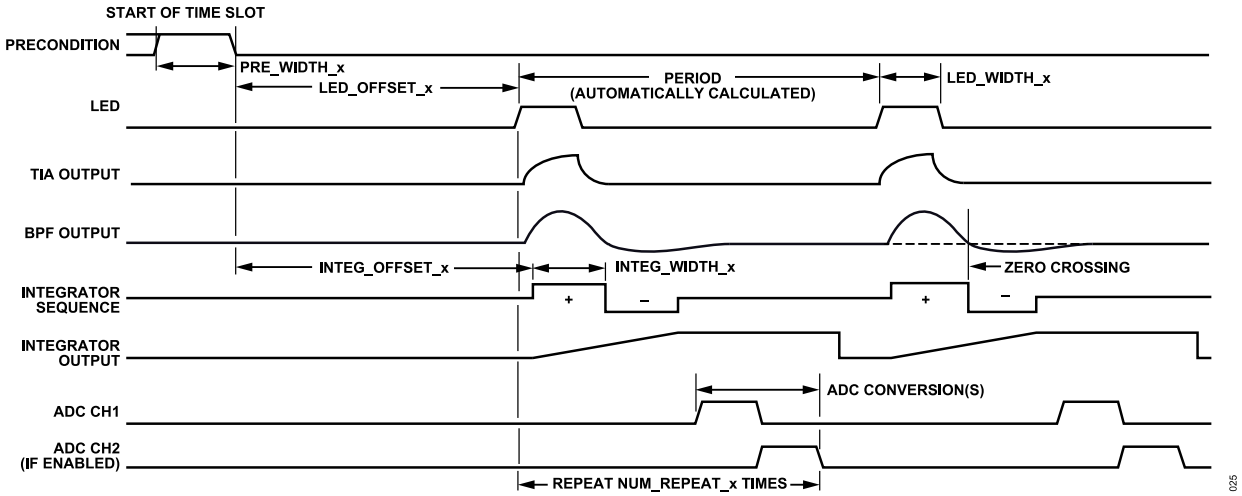

Figure 25. Single Integration per ADC Conversion with LED as Stimulus

Table 16. Single Integration Mode Settings

Group	Time Slot A Register Address[1]	Bit Field Name	Description
Signal Path Setup	0x0100, Bits[13:12]	SAMPLE_TYPE_x	Leave at the default setting (0) for default sampling mode.
	0x0101, Bits[8:0]	AFE_PATH_CFG_x	Set to 0x0DA for TIA, BPF, integrator, and ADC.
	0x0102, Bits[15:12], 0x102, Bits[3:0]	INPxx_x	Enable desired inputs.
	0x0103[14:12]	PRECON_x	Set to 0x5 to precondition anode of the photodiode to TIA_VREF.
	0x0103, Bits[7:6], 0x0103, Bits[1:0]	VCx_SEL_x	Set to 0x2 to set ~250 mV reverse bias across the photodiode.
	0x0104, Bits[5:0]	TIA_GAIN_CHx_x	Select TIA gain.
	0x0104, Bits[9:8]	AFE_TRIM_VREF_x	Set to 0x3 to set TIA_VREF = 1.27 V for maximum dynamic range.
	0x0108, Bits[13:12]	MOD_TYPE_x	Set to 0 for continuous TIA connection to inputs following preconditioning.
Timing	0x0109, Bits[7:0]	LED_OFFSET_x	Sets start time of first LED pulse in 1 µs increments, and 0x10 is the default (16 µs).
	0x0109, Bits[15:8]	LED_WIDTH_x	Sets width of LED pulse in 1 µs increments, and 2 µs or 3 µs recommended.
	0x010A, Bits[4:0]	INTEG_WIDTH_x	Integration time in µs. Set to LED_WIDTH_x + 1.
	0x010B, Bits[12:0]	INTEG_OFFSET_x	Integration sequence start time = INTEG_OFFSET_x. Optimize as described in the Optimizing Position of Integration Sequence section.
	0x0107, Bits[15:8]	NUM_INT_x	Set to 1 for a single integration per group of ADC conversions.
	0x0107, Bits[7:0]	NUM_REPEAT_x	With NUM_INT_x = 1, NUM_REPEAT_x sets the total number of pulses.
LED Settings	0x0105, Bit 15, 0x0105, Bit 7, 0x0106, Bit 15, 0x0106, Bit 7	LED_DRIVESIDEx_x	Select LED for time slot used.

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Table 16. Single Integration Mode Settings

Group	Time Slot A Register Address[1]	Bit Field Name	Description
	0x0105, Bits[14:8], 0x0105, Bits[6:0], 0x0106, Bits[14:8], 0x0106, Bits[6:0]	LED_CURRENTx_x	Set LED current for selected LED.

[1] This is the Time Slot A register address. Add 0x020 for the identical register address for each subsequent time slot. For example, Register 0x0100 is the location for SAMPLE_TYPE_A. For Time Slot B, this register is at Address 0x0120. For Time Slot C, this register is at Address 0x0140. For Time Slot D, this register is at Address 0x0160, and so on.

Optimizing Position of Integration Sequence

It is critical that the zero crossing of the output response of the BPF be aligned with the integration sequence such that the positive integration is aligned with the positive portion of the BPF output response and the negative integration is aligned with the negative portion of the BPF output response (see Figure 25).

A simple test to find the zero crossing is to setup the circuit so that the LED is reflecting off a reflector at a fixed distance from the photodiode such that a steady dc level of photodiode current is provided to the ADPD4200. Monitor the output while sweeping the integrator offset, INTEG_OFFSET_x[12:5], from a low value to a high value in 1 µs steps. The zero crossing is located when a relative maxima is seen at the output. The zero crossing can then be identified with much finer precision by sweeping the INTEG_OFFSET_x[4:0] bit field in 31.25 ns increments.

The optimal timing point is a function of TIA bandwidth that varies with TIA gain. To achieve the maximum SNR at each TIA gain setting, it is recommended that the user find the optimal timing point at each TIA gain setting for a given use case. Because there is minimal part to part variation in this optimal timing point, that same integrator offset timing for each gain setting can be used for all parts. If the user must use the same integrator timing for all TIA gain settings without re-optimizing for each TIA gain setting, the 200 kΩ TIA gain optimal timing must be used for the other TIA gain settings.

Improving SNR Using Multiple Pulses

The ADPD4200 use short LED pulses, on the order of 2 µs or 3 µs. The SNR of a single pulse is approximately 68 dB to 74 dB, depending on the TIA gain. The SNR can be extended to ~100 dB by increasing the number of pulses per sample and filtering to a relevant signal bandwidth, for example, 0.5 Hz to 20 Hz for a heart rate signal. The SNR increases as the square root of the number of pulses. Thus, for every doubling of pulses, 3 dB of SNR increase is achieved. The number of pulses is increased with the NUM_REPEAT_x bit field.

Improving SNR Using Integrator Chopping

The last stage in the ADPD4200 datapath is a charge integrator. The integrator uses an on and off integration sequence, synchronized to the emitted light pulse, which acts as an additional high-pass filter to remove offsets, drifts, and low frequency noise from the previous stages. However, the integrating amplifier can itself introduce low frequency signal content at a low level. The ADPD4200 has a mode that enables additional chopping in the digital domain to remove this signal. Chopping is achieved by using an even number of pulses per sample and inverting the integration sequence for half of those sequences. When the math is done to combine the digitized result of each of the pulses of the sample, the sequences with an inverted integrator sequence are subtracted, and the sequences with a normal integrator sequence are added. An example diagram of the integrator chopping sequence is shown in Figure 26.

The result of chopping is that any low frequency signal contribution from the integrator is eliminated, leaving only the integrated signal and resulting in higher SNR, especially at higher numbers of pulses and at lower TIA gains where the noise contribution of the integrator becomes more pronounced.

Digital chopping is enabled using the registers and bits detailed in Table 17. The bit fields define the chopping operation for the first four pulses. This 4-bit sequence is then repeated for all subsequent sequence of four pulses. In Figure 26, a sequence is shown where the second and fourth pulses are inverted while the first and third pulses remain in the default polarity (noninverted). This configuration is achieved by setting the REVERSE_INTEG_x bit field = 0xA to reverse the integration sequence for the second and fourth pulses. To complete the operation, the math must be adjusted by setting the SUBTRACT_x bit field = 0xA. An even number of pulses must be used with integrator chop mode.

When using integrator chop mode, the ADC offset bit fields, CH1_ADC_ADJUST_x and CH2_ADC_ADJUST_x, must be set to 0 because, when the math is adjusted to subtract the inverted integration sequences while the default integration sequences are added, any digital offsets at the output of the ADC are automatically eliminated. Integrator chop mode also eliminates the need to manually null the ADC offsets at startup in a typical application. Note that the elimination of the offset using chop mode can clip at least half of the noise signal when no input signal is present, which makes it difficult to measure the noise floor during characterization of the system. Three options for performing noise floor characterization of the system include the following:

- Chop mode disabled.
- Chop mode enabled but with a minimal signal present at the input, which increases the noise floor enough such that it is no longer clipped.

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- Setting the ZERO_ADJUST_x bit = 1, which adds 2048 codes to the end result.

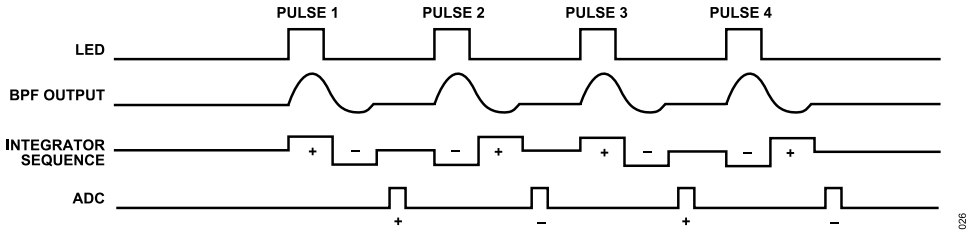

Figure 26. Diagram of Integrator Chopping Sequence

Table 17. Register Settings for Integrator Chop Mode

Group	Time Slot A Register Address[1]	Bit Field Name	Description
Integrator Chop Mode	0x010D, Bits[7:4]	SUBTRACT_x	Four-pulse subtract pattern. Set to 1 to negate the math operation in the matching position in a group of four pulses. The LSB maps to the first pulse.
	0x010D, Bits[3:0]	REVERSE_INTEG_x	Four-pulse integration reverse pattern. Set to 1 to reverse the integrator positive and negative pulse order in the matching position in a group of four pulses. The LSB maps to the first pulse.

[1] This is the Time Slot A register address. Add 0x020 for the identical register address for each subsequent time slot. For example, Register 0x010D is the location for SUBTRACT_A. For Time Slot B, this register is at Address 0x012D. For Time Slot C, this register is at Address 0x014D. For Time Slot D, this register is at Address 0x016D, and so on.

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Connection Modulation

The ADPD4200 uses three different types of modulation connections to a sensor, controlled by the MOD_TYPE_x bits. Table 18 shows the different functions controlled by this register. The default mode of operation is MOD_TYPE_x = 0, which is the mode where there is no modulation of the input connection, and is the mode used as described in the Using LED as Stimulus section.

Table 18. Modulation Connections Based on MOD_TYPE_x

MOD_TYPE_x	Connect Function
0	TIA is continuously connected to INx after the precondition period. There is no modulation of the input connection.
1	Float mode operation. The TIA is connected to INx only during the modulation pulse and disconnected (floated) between pulses.
2	Nonfloat mode connection modulation. The TIA is connected to INx during the modulation pulse and connected to the precondition value between pulses.

Float Mode Operation

The ADPD4200 has a unique operating mode, float mode, that allows high SNR at low power in low light situations. In float mode, the photodiode is first preconditioned to a known state. Then, the photodiode anode is disconnected from the receive path of the device for a preset amount of float time. During the float time, light falls on the photodiode, either from ambient light, pulsed LED light, or a combination of the two depending on the operating mode. Charge from the sensor is stored directly on the capacitance of the sensor, C_{PD}. At the end of the float time, the photodiode is switched into the receive path of the ADPD4200 and an inrush of the accumulated charge occurs, which is then integrated, allowing the maximum amount of charge to be processed per pulse with the minimum amount of noise added by the signal path. The charge is integrated externally on the capacitance of the photodiode for as long as it takes to acquire maximum charge, independent of the amplifiers of the signal path, effectively integrating noise free charge. Float mode allows the user the flexibility to increase the amount of charge per measurement by either increasing the LED drive current or by increasing the float time.

In float mode, the signal path bypasses the BPF and uses only the TIA and integrator. The BPF is bypassed because the shape of the signal produced when transferring the charge from the photodiode by modulating the connection to the TIA can differ across devices and conditions. A filtered signal from the BPF is not able to be reliably aligned with the integration sequence. Therefore, the BPF cannot be used. In float mode, the entire charge transfer is integrated in the negative cycle of the integrator, and the positive cycle cancels any offsets.

Float LED Mode for Synchronous LED Measurements

Float LED mode is desirable in low signal conditions where the CTR is below 5 nA/mA. In addition, float mode is an ideal option when limiting the LED drive current of the green LEDs in a heart rate measurement to keep the forward voltage drop of the green LED to a level that allows the elimination of a boost converter for the LED supply. For example, the LED current can be limited to 10 mA to ensure that the LED voltage drop is ~3 V so that it can operate directly from the battery without the need of a boost converter. Float mode accumulates the received charge during longer LED pulses without adding noise from the signal path, effectively yielding the highest SNR per photon attainable.

In float LED mode, multiple pulses are used to cancel electrical offsets, drifts, and ambient light. To achieve this ambient light rejection, an even number of equal length pulses is used. For every pair of pulses, the LED flashes in one of the pulses and does not flash in the other. The return from the combination of the LED, ambient light, and offset is present in one of the pulses. In the other, only the ambient light and offset are present. A subtraction of the two pulses is made that eliminates ambient light as well as any offset and drift. It is recommended to use groups of four pulses for measurement where the LED is flashed on Pulse 2 and Pulse 3. The accumulator adds Pulse 2 and Pulse 3 and then subtracts Pulse 1 and Pulse 4. To gain additional SNR, use multiple groups of four pulses.

For each group of four pulses, the settings of LED_DISABLE_x determine if the LED flashes in a specific pulse position. Which pulse positions are added or subtracted is configured in the SUBTRACT_x bits. These sequences are repeated in groups of four pulses. The value written to the FIFO or data registers is dependent on the total number of pulses per sample period. With NUM_INT_x set to 1, NUM_REPEAT_x determines the total number of pulses. For example, if the device is set up for 32 pulses, the four pulse sequence, as defined in LED_DISABLE_x and SUBTRACT_x, repeats eight times and a single register or FIFO write of the final value based on 32 pulses executes.

In float mode, the MIN_PERIOD_x bits must be set to control the pulse period. The automatic period calculation is not designed to work with float mode. Set the MIN_PERIOD_x bits, in 1 µs increments, to accommodate the amount of float time and connect time required.

Placement of the integration sequence is such that the negative phase of the integration is centered on the charge transfer phase. The TIA is an inverting stage. Therefore, placing the negative phase of the integration during the transferring of the charge from the photodiode causes the integrator to increase with the negative going output signal from the TIA.

In the example shown in Figure 27, the LED flashes in the second and third pulses of the four pulse sequence. SUBTRACT_x is set up to add the second and third pulses while subtracting the first and

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fourth pulses, effectively cancelling out the ambient light, electrical offsets, and drift.

Additionally, set the INPUT_R_SELECT_x bit field equal to 1 to place a 6.5 kΩ resistor in series between the photodiode and the TIA input to slow the inrush of current from the photodiode when the input switch is closed.

Table 19 details the relevant registers for float LED mode.

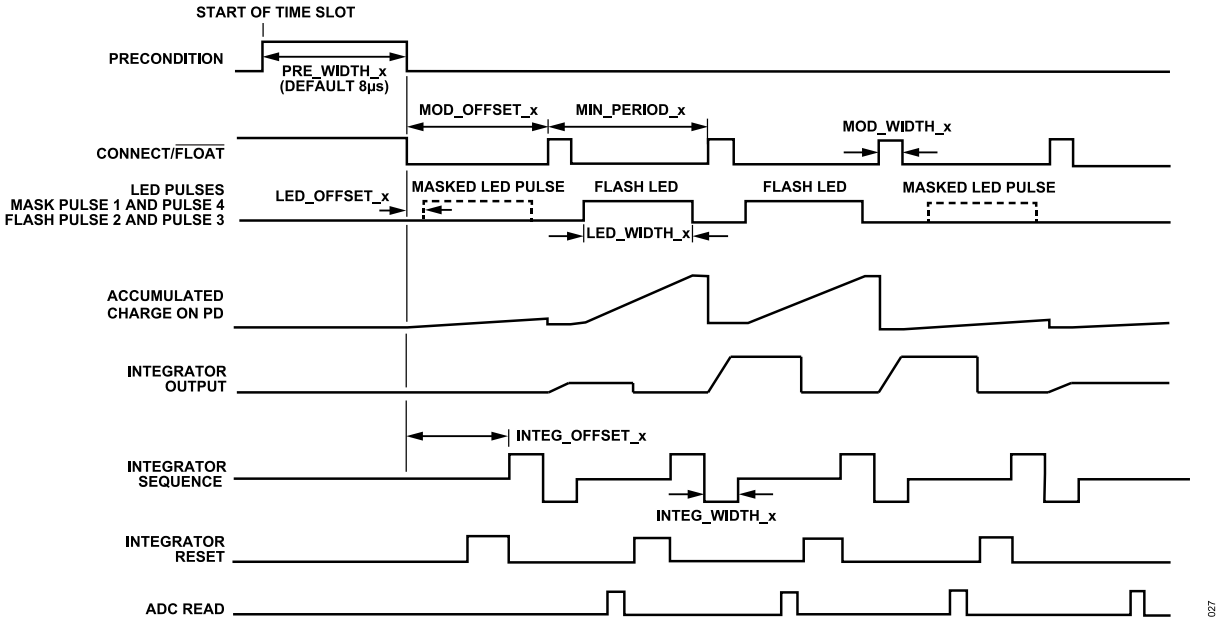

Figure 27. Four Pulse Float Mode Operation

Table 19. Float LED Mode Settings

Group	Time Slot A Register Address[1]	Bit Field Name	Description
Signal Path Setup	0x0100, Bits[13:12]	SAMPLE_TYPE_x	Leave at the default setting (0) for default sampling mode.
	0x0100, Bits[11:10]	INPUT_R_SELECT_x	Set to 0x1 for 6.25 kΩ series input resistor.
	0x0101, Bits[8:0]	AFE_PATH_CFG_x	Set to 0x0E6 for TIA, integrator, and ADC. Bypass BPF.
	0x0102, Bits[15:12], 0x0102, Bits[3:0]	INPxx_x	Enable desired inputs.
	0x0103, Bits[14:12]	PRECON_x	Set to 0x4 to precondition anode of photodiode to the input of the TIA.
	0x0103, Bits[7:6], 0x0103, Bits[1:0]	VCx_SEL_x	Set to 0x2 to set ~250 mV reverse bias across photodiode.
	0x0104, Bits[5:0]	TIA_GAIN_CHx_x	Select TIA gain (100 kΩ or 200 kΩ for float mode).
	0x0104, Bits[9:8]	AFE_TRIM_VREF_x	Set to 0x2 to set TIA_VREF = 0.9 V.
Float Mode Configuration	0x0107, Bits[15:8]	NUM_INT_x	Set to 1 for a single integration per group of ADC conversions.
	0x0107, Bits[7:0]	NUM_REPEAT_x	Number of sequence repeats. Must be set to a multiple of 2 for float mode.
	0x0108, Bits[13:12]	MOD_TYPE_x	Set to 0x1 for float mode operation.
	0x0108, Bits[9:0]	MIN_PERIOD_x	Set the period to accommodate float time plus connect time, in 1 µs increments.
	0x010A, Bits[4:0]	INTEG_WIDTH_x	Integration time in µs. Set to MOD_WIDTH_x + 1.
	0x010A, Bits[10:8], 0x010A, Bits[14:12]	CHx_AMP_DISABLE_x	Set 0x010A, Bit 9 to 1 to power down the BPF for Channel 1, and Bit 13 to 1 to power down the BPF for Channel 2 if Channel 2 is enabled.
	0x010B, Bits[12:0]	INTEG_OFFSET_x	Integration sequence start time. Set to (MOD_OFFSET_x − INTEG_WIDTH_x – 250 ns).
	0x010C, Bits[15:8]	MOD_WIDTH_x	Sets width of connect pulse in 1 µs increments. Typical values of 2 µs or 3 µs.
	0x010C, Bits[7:0]	MOD_OFFSET_x	Sets start time of first connect pulse in 1 µs increments.

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Table 19. Float LED Mode Settings

Group	Time Slot A Register Address[1]	Bit Field Name	Description
	0x010D, Bits[7:4]	SUBTRACT_x	In any given sequence of four pulses, negate the math operation in the selected position. Selections are active high (that is, subtract if 1) and the LSB of this register maps to the first pulse. For a float mode sequence, add pulses when the LED flashes and subtract pulses when the LED is disabled, according to LED_DISABLE_x.
LED Settings	0x0105, Bit 15 and 0x0105, Bit 7, 0x0106, Bit 15 and 0x0106, Bit 7	LED_DRIVESIDEx_x	Select LED for time slot used.
	0x0105, Bits[14:8], 0x0105, Bits[6:0], 0x0106, Bits[14:8], 0x0106, Bits[6:0]	LED_CURRENTx_x	Set LED current for selected LED.
	0x0109, Bits[7:0]	LED_OFFSET_x	Sets start time of first LED pulse in 1 µs increments.
	0x0109, Bits[15:8]	LED_WIDTH_x	Sets width of LED pulse in 1 µs increments.
	0x010D, Bits[15:12]	LED_DISABLE_x	In any given sequence of four pulses, disable the LED pulse in the selected position. Selections are active high (that is, disable LED if 1) and the LSB of this register maps to the first pulse. For a sequence of four pulses, it is recommended to turn on the LED in the second and third pulses by writing 0x9 to this register.

[1] This is the Time Slot A register address. Add 0x020 for the identical register address for each subsequent time slot. For example, Register 0x0100 is the location for SAMPLE_TYPE_A. For Time Slot B, this register is at Address 0x0120. For Time Slot C, this register is at Address 0x0140. For Time Slot D, this register is at Address 0x0160, and so on.

Float Mode Limitations

When using float mode, the limitations of the mode must be well understood. For example, a finite amount of charge can accumulate on the capacitance of the photodiode, and there is a maximum amount of charge that can be integrated by the integrator. Based on an initial reverse bias of 250 mV on the photodiode and assuming that the photodiode begins to become nonlinear at ~200 mV of forward bias, there is ~450 mV of headroom for the anode voltage to increase from its starting point at the beginning of the float time before the charge ceases to accumulate in a linear fashion. It is desirable to operate only in the linear region of the photodiode (see Figure 28). To verify that float mode is operating in the linear region of the diode, the user can perform a simple check. Record data at a desired float time and then record data at half the float time. The recommended ratio of the two received signals is 2:1. If this ratio does not hold true, the diode is likely beginning to forward bias at the longer float time and becomes nonlinear.

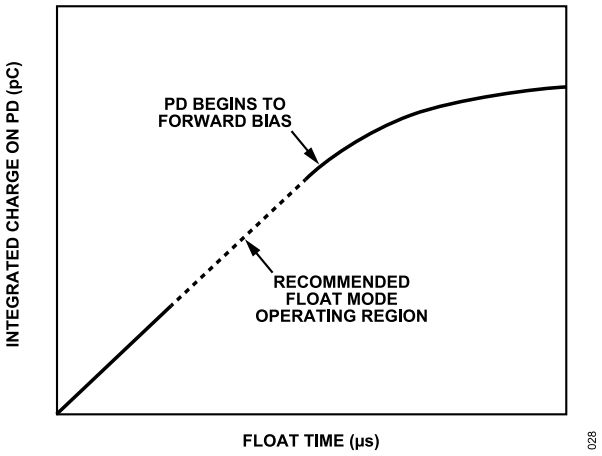

Figure 28. Integrated Charge on the Photodiode vs. Float Time

The maximum amount of charge that can be stored on the photodiode capacitance and remain in the linear operating region of the sensor is estimated by

$$Q = C_{PD} V$$

where:
Q is the integrated charge.
C_{PD} is the capacitance of the photodiode.
V is the amount of voltage change across the photodiode before the photodiode becomes nonlinear.

For a typical discrete optical design using a 7 mm^2 photodiode with 70 pF capacitance and 450 mV of headroom, the maximum amount

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of charge that can be stored on the photodiode capacitance is 31.5 pC.

In addition, consider the maximum amount of charge the integrator of the ADPD4200 can integrate. The integrator can integrate up to 7.6 pC. When this charge is referred back to the input, consider the TIA gain. When the TIA gain is at 200 kΩ, the input referred charge is at a 1:1 ratio to the integrated charge on the integrator. For 100 kΩ gain, it is 2:1. For 50 kΩ gain, it is 4:1. For 25 kΩ gain, it is 8:1.

For the previous example using a photodiode with 70 pF capacitance, use a 50 kΩ TIA gain and set the float timing such that, for a single pulse, the output of the ADC is at 70% of full scale, which is a typical operating condition. Under these operating conditions, 5.3 pC integrates per pulse by the integrator for 21.2 pC of charge accumulated on the photodiode capacitance. The amount of time to accumulate charge on C_{PD} is inversely proportional to CTR. TIA gain settings of 100 kΩ or 200 kΩ may be required based on the CTR of the measurement and how much charge can be accumulated in a given amount of time. Ultimately, the type of measurement being made (ambient or pulsed LED), the photodiode capacitance, and the CTR of the system determine the float times.

Pulse Connect Modulation

Pulse connect modulation is useful for ambient light measurements or any other sensor measurements that do not require a synchronous stimulus. This mode works by preconditioning the sensor to some level selected by the PRECON_x bits and then only connecting the sensor to the input of the TIA during the modulation pulse. When not connected to the TIA, the sensor is connected to a low input impedance node at the TIA_VREF voltage. Any sensor current during this time is directed into the AFE. Therefore, no charge accumulates on the sensor. This lack of charge accumulation is in contrast to float mode, which fully disconnects the sensor between modulation pulses. The MOD_TYPE_x bits must be set to 0x2 for pulse connect mode. The advantage of using this mode for nonsynchronous sensor measurements is that it allows the user to take advantage of the noise performance benefits of the full signal path using the BPF and integrator. Figure 30 shows a timing diagram for pulse connect modulation type measurements.

Modulation of Stimulus Source

The ADPD4200 has operating modes that modulate the VC1 and VC2 signals. These modes are useful for providing a pulsed stimulus to the sensor being measured. For example, a bioimpedance measurement can be made where one electrode to the human is being pulsed by the VC1 or VC2 output and the response is measured on a second electrode connected to the TIA input. This mode is also useful for a capacitance measurement, as shown in Figure 29, where one of the VCx pins is connected to one side of the capacitor and the other side is connected to the TIA input.

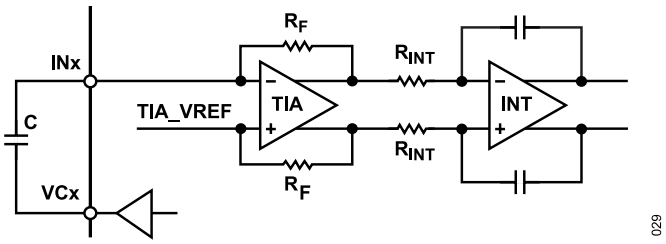

Figure 29. Modulate Stimulus for Capacitance Measurement

The BPF is bypassed for this measurement. When a stimulus pulse is provided on the VCx pin, the capacitor response is a positive spike on the rising edge that then settles back toward TIA_VREF, followed by a negative spike on the falling edge of the stimulus pulse. The integration sequence is centered such that the positive and negative integration sequences completely integrate the charge from the positive and negative TIA responses, respectively (see Figure 31).

Pulsing of the VC1 and VC2 pins is controlled by the VCx_PULSE_x, VCx_ALT_x, and VCx_SEL_x bits while timing of the modulation is controlled by the MOD_OFFSET_x and MOD_WIDTH_x bits. Table 20 shows the relevant registers for modulating the stimulus to the sensor.

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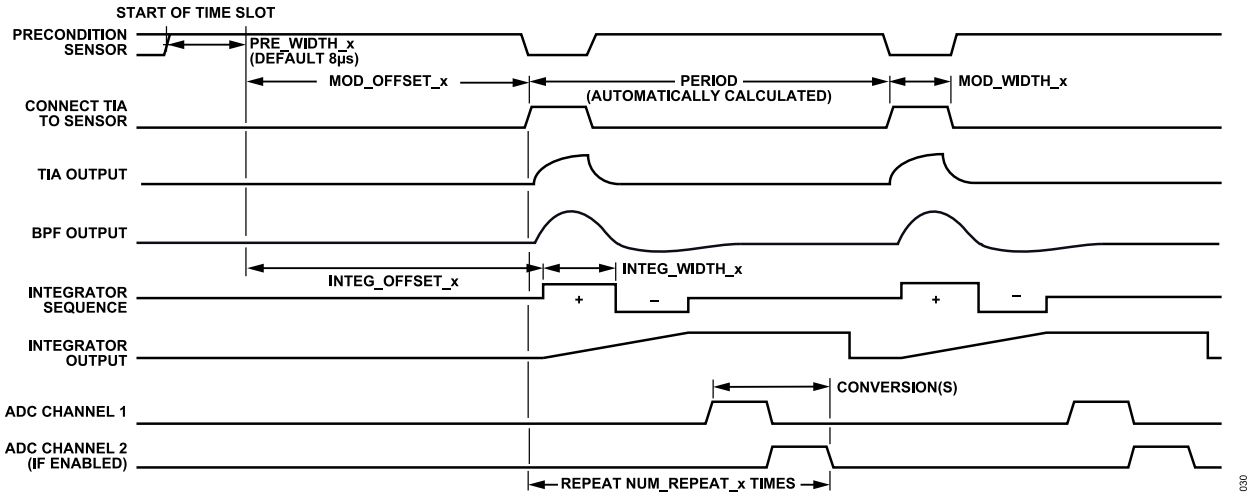

Figure 30. Timing Diagram for Pulse Connect Modulation

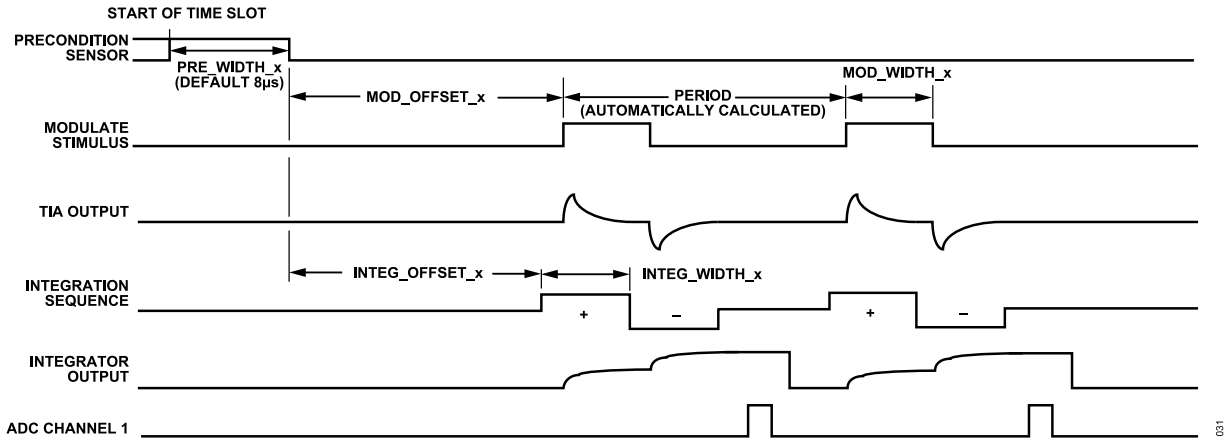

Figure 31. Timing Diagram for Modulate Stimulus Operation

Table 20. Modulate Stimulus Settings

Group	Time Slot A Register Address[1]	Bit Field Name	Description
Modulate Stimulus Set-up	0x0100, Bits[13:12]	SAMPLE_TYPE_x	Leave at the default setting (0) for default sampling mode.
	0x0101, Bits[8:0]	AFE_PATH_CFG_x	Set to 0x0E6 for TIA, integrator, and ADC. Bypass BPF.
	0x0102, Bits[15:12], 0x0102, Bits[3:0]	INPxx_x	Enable desired inputs.
	0x0103, Bits[14:12]	PRECON_x	Set to 0x5 to precondition sensor to TIA_VREF.
	0x0103, Bits[11:10], 0x0103, Bits[5:4]	VCx_PULSE_x	VCx pulse control. Set to 0x2 to pulse to the alternate voltage during a modulation pulse.
	0x0103, Bits[9:8], 0x0103, Bits[3:2]	VCx_ALT_x	Select the alternate state for VCx during the modulation pulse.
	0x0103, Bits[7:6], 0x0103 Bits[1:0]	VCx_SEL_x	Set to 0x1 to set VCx to TIA_VREF as primary state.
	0x0104, Bits[5:0]	TIA_GAIN_CHx_x	Select TIA gain.
	0x0104, Bits[9:8]	AFE_TRIM_VREF_x	Set to 0x2 to set TIA_VREF = 0.9 V.
Modulate Stimulus Timing	0x010C, Bits[7:0]	MOD_OFFSET_x	Sets start time of first modulation pulse in 1 µs increments.
	0x010C, Bits[15:8]	MOD_WIDTH_x	Sets width of modulation pulse in 1 µs increments. Typical values of 6 µs to 12 µs.

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Table 20. Modulate Stimulus Settings

Group	Time Slot A Register Address[1]	Bit Field Name	Description
	0x010A, Bits[4:0]	INTEG_WIDTH_x	Integration time in µs. Set to MOD_WIDTH_x + 1.
	0x010B, Bits[12:0]	INTEG_OFFSET_x	Integration sequence start time. Set to MOD_OFFSET_x – 1 and then sweep INTEG_OFFSET_x[4:0] in 31.25 ns steps to find optimal operating point.
	0x0107, Bits[15:8]	NUM_INT_x	Set to 1 for a single integration per ADC conversion.
	0x0107, Bits[7:0]	NUM_REPEAT_x	Number of sequence repeats. SNR increases as √n, where n = NUM_REPEAT_x × NUM_INT_x.

[1] This is the Time Slot A register address. Add 0x020 for the identical register address for each subsequent time slot. For example, Register 0x0100 is the location for SAMPLE_TYPE_A. For Time Slot B, this register is at Address 0x0120. For Time Slot C, this register is at Address 0x0140. For Time Slot D, this register is at Address 0x0160, and so on.

MULTIPLE INTEGRATION MODE

Multiple integration mode provides multiple analog integrations of incoming charge per ADC conversion. This mode is most useful when there is a small response that uses a small amount of the available dynamic range per stimuli event. Multiple integration mode allows multiple integrations of charge prior to an ADC conversion so that a larger amount of the available dynamic range of the integrator is utilized.

Figure 32 shows multiple integration mode using the LED as the stimulus. The number of LED pulses and subsequent integrations of charge from the photodiode response is determined by the setting of the NUM_INT_x bits. Following the final integration, there is a single ADC conversion. This process is repeated NUM_REPEAT_x times.

Prior to setting the number of integrations using the NUM_INT_x bits, determine the optimal TIA gain and LED current setting. When the TIA gain and LED current are set, measure how much of the integrator dynamic range is used to integrate the charge created by a single LED pulse. If the amount of integrator dynamic range used for a single pulse is less than half the available dynamic range, it may be desirable to use multiple integrations prior to an ADC conversion. For example, if the amount of integrator dynamic range used for a single pulse is 1/8 of the available dynamic range, set NUM_INT_x to 0x6 to use six pulses and integrations, using most of the available dynamic range (75%) per ADC conversion while leaving 25% of headroom for margin so that the integrator does not saturate as the input level varies. As each pulse is applied to the LED, the charge from the response is integrated and held. The charge from the response to each subsequent pulse is added to the previous total integrated charge, as shown in Figure 32, until NUM_INT_x integrations are reached.

In multiple integration mode, the minimum period is automatically calculated. In the example shown, the minimum period is calculated at 2 × INTEG_WIDTH_x so that subsequent pulses occur immediately following the completion of the previous integration. Extra time is automatically added to accommodate the ADC conversions at the end of NUM_INT_x integrations.

Use NUM_REPEAT_x to increase the iterations to improve the overall SNR. The entire multiple integration per ADC conversion process repeats NUM_REPEAT_x number of times. Increasing NUM_REPEAT_x serves the same purpose as multiple pulses in continuous connect mode, where n pulses improve the SNR by √n. In multiple integration mode, the SNR increases by √n, where n = NUM_REPEAT_x. The total number of LED pulses in this mode is equal to NUM_INT_x × NUM_REPEAT_x.

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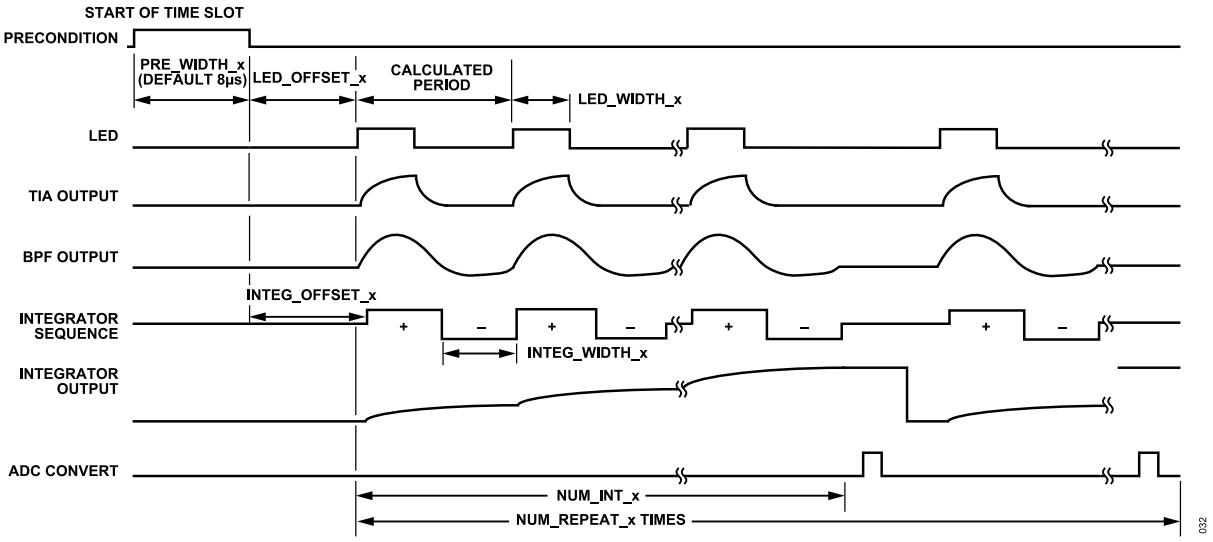

Figure 32. Multiple Integration Mode with LED as Stimulus

Table 21. Relevant Settings for Multiple Integration Mode

Group	Time Slot A Register Address[1]	Bit Field Name	Description
Multiple Integration Mode Using LED as Stimulus	0x0100, Bits[13:12]	SAMPLE_TYPE_x	Leave at the default setting (0) for default sampling mode.
	0x0101, Bits[8:0]	AFE_PATH_CFG_x	Set to 0x0DA for TIA, BPF, integrator, and ADC.
	0x0102, Bits[15:12], 0x0103, Bits[3:0]	INPxx_x	Enable desired inputs.
	0x0103, Bits[14:12]	PRECON_x	Set to 0x5 to precondition anode of the photodiode to TIA_VREF.
	0x0103, Bits[7:6], 0x0103, Bits[1:0]	VCx_SEL_x	Set to 0x2 to set ~250 mV reverse bias across photodiode.
	0x0104, Bits[5:0]	TIA_GAIN_CHx_x	Select TIA gain.
	0x0104, Bits[9:8]	AFE_TRIM_VREF_x	Set to 0x3 to set TIA_VREF = 1.27 V for maximum dynamic range.
Timing	0x0107, Bits[15:8]	NUM_INT_x	Set to a number that utilizes most of the dynamic range of integrator available, leaving some margin for fluctuations in input level.
	0x0107, Bits[7:0]	NUM_REPEAT_x	Set NUM_REPEAT_x to the number of times to repeat the multiple integration sequence. SNR increases by a factor of √(NUM_REPEAT_x). Total number of pulses is equal to NUM_REPEAT_x × NUM_INT_x.
	0x010A, Bits[4:0]	INTEG_WIDTH_x	Integration time in µs. Set to LED_WIDTH_x + 1.
	0x010B, Bits[12:0]	INTEG_OFFSET_x	Integration sequence start time = INTEG_OFFSET_x. Optimize as described in the Optimizing Position of Integration Sequence section.
LED Settings	0x0105, Bit 15, 0x0105, Bit 7, 0x0106, Bit 15, and 0x0106, Bit 7	LED_DRIVESIDEx_x	Select LED for time slot used.
	0x0105, Bits[14:8], 0x0105, Bits[6:0], 0x0106, Bits[14:8], 0x0106, Bits[6:0]	LED_CURRENTx_x	Set LED current for selected LED.
	0x0109, Bits[7:0]	LED_OFFSET_x	Sets start time of first LED pulse in 1 µs increments and 0x10 default (16 µs).
	0x0109, Bits[15:8]	LED_WIDTH_x	Sets width of LED pulse in 1 µs increments, and 2 µs or 3 µs recommended.

[1] This is the Time Slot A register address. Add 0x020 for the identical register address for each subsequent time slot. For example, Register 0x0100 is the location for SAMPLE_TYPE_A. For Time Slot B, this register is at Address 0x0120. For Time Slot C, this register is at Address 0x0140. For Time Slot D, this register is at Address 0x0160, and so on.

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DIGITAL INTEGRATION MODE

The ADPD4200 supports a digital integration mode to accommodate sensors that require longer pulses than can be supported in the typical analog integration modes. Digital integration mode allows the system to use a larger LED duty cycle than the analog integration modes, which may result in the highest achievable levels of SNR.

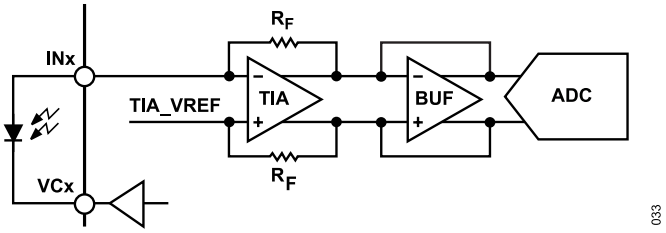

Figure 33. Signal Path for Digital Integration Mode

In digital integration mode, the BPF is bypassed and the integrator is configured as a buffer, resulting in the signal path shown in Figure 33. Digital integration regions are configured by the user and separated into lit and dark regions. The LED is pulsed in the lit region, and the LED is off in the dark region. ADC samples are taken at 1 µs intervals within the lit and dark regions and are then digitally integrated. The integration of the ADC samples from the dark region is subtracted from the integration of the ADC samples from the lit region and the result is written into the relevant signal output data registers. The sum of the samples from just the dark region is available in the dark output data registers. Both signal and dark values can be written to the FIFO.

The ADPD4200 support one-region and two-region digital integration modes. In one-region digital integration mode, an equal number of dark and lit samples are taken where all of the dark samples are taken in the dark region just prior to the lit region. One-region digital integration mode is illustrated in the timing diagram in Figure 34. In two-region digital integration mode, an equal number of dark and lit samples are taken. However, the dark region is split such that half of the samples are taken in the dark region prior to the lit region, and the other half is taken in the dark region following the lit region. The two-region digital integration mode results in higher ambient light rejection than the one-region digital integration mode in situations with a varying ambient light level. A timing diagram for two-region digital integration mode is shown in Figure 35.

Table 22 shows the relevant register settings for the digital integration modes of operation. Note that only a single channel can be used in digital integration mode. Two channels are not supported for digital integration mode of operation. The MIN_PERIOD_x bits must also be manually set with the correct period because the minimum period is not automatically calculated in digital integration mode.

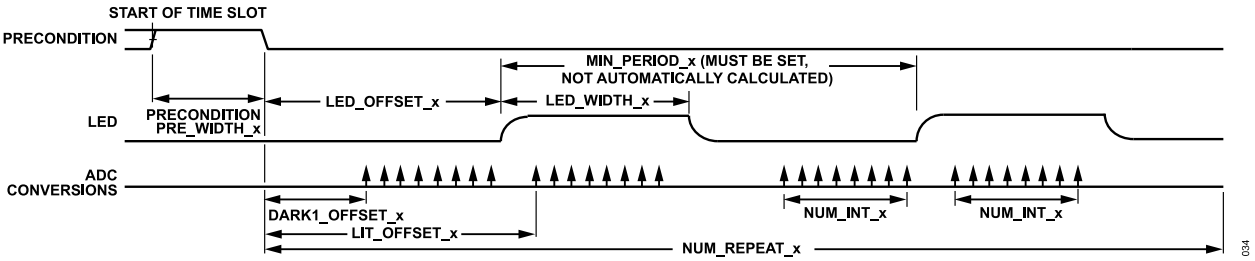

Figure 34. One-Region Digital Integration Mode Timing Diagram

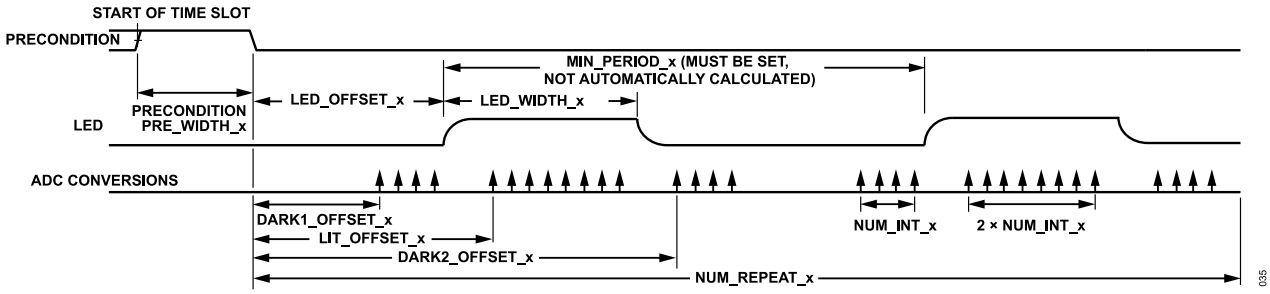

Figure 35. Two-Region Digital Integration Mode Timing Diagram

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Table 22. Relevant Settings for Digital Integration Modes

Group	Time Slot A Register Address[1]	Bit Field Name	Description
Signal Path Setup	0x0100, Bits[13:12]	SAMPLE_TYPE_x	Set to 0x1 for one-region digital integration mode. Set to 0x2 for two-region digital integration mode.
	0x0101, Bits[8:0]	AFE_PATH_CFG_x	Set to 0x0E6 for TIA, integrator, and ADC. Bypass BPF. Integrator is automatically configured as a buffer when one-region or two-region digital integration mode is selected.
	0x0102, Bits[15:12], 0x0102, Bits[3:0]	INPxx_x	Enable desired inputs.
	0x0103, Bits[14:12]	PRECON_x	Set to 0x5 to precondition anode of photodiode to TIA_VREF.
	0x0103, Bits[7:6], 0x0103, Bits[1:0]	VCx_SEL_x	Set to 0x2 to set ~250 mV reverse bias across photodiode.
	0x0104, Bits[5:0]	TIA_GAIN_CHx_x	Select TIA gain.
	0x0104, Bits[9:8]	AFE_TRIM_VREF_x	Set to 0x3 to set TIA_VREF = 1.265 V.
Timing	0x0107, Bits[15:8]	NUM_INT_x	Set to the number of desired ADC conversions in the dark and lit regions.
	0x0107, Bits[7:0]	NUM_REPEAT_x	Number of sequence repeats.
	0x0108, Bits[9:0]	MIN_PERIOD_x	Set the period. Automatic period calculation is not supported in digital integration mode.
	0x0113, Bits[8:0]	LIT_OFFSET_x	Set to the time of the first ADC conversion in the lit region.
	0x0114, Bits[6:0]	DARK1_OFFSET_x	Set to the time of the first ADC conversion in the Dark 1 region.
	0x0114, Bits[15:7]	DARK2_OFFSET_x	Set to the time of the first ADC conversion in the Dark 2 region. Only used in two-region digital integration mode.
LED Settings	0x0105, Bit 15, 0x0105, Bit 7, 0x0106, Bit 15, 0x0106, Bit 7	LED_DRIVESIDEx_x	Select LED for time slot used.
	0x0105, Bits[14:8], 0x0105, Bits[6:0], 0x0106, Bits[14:8], 0x0106, Bits[6:0]	LED_CURRENTx_x	Set LED current for selected LED.
	0x0109, Bits[7:0]	LED_OFFSET_x	Sets start time of first LED pulse in 1 µs increments.
	0x0109, Bits[15:8]	LED_WIDTH_x	Sets width of LED pulse in 1 µs increments.

[1] This is the Time Slot A register address. Add 0x020 for the identical register address for each subsequent time slot. For example, Register 0x0100 is the location for SAMPLE_TYPE_A. For Time Slot B, this register is at Address 0x0120. For Time Slot C, this register is at Address 0x0140. For Time Slot D, this register is at Address 0x0160, and so on.

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Timing Recommendations for Digital Integration Modes

When setting the timing for digital integration mode, it is important to place the ADC samples such that the signal being sampled is given time to settle prior to the sample being taken. The settling time of the input signal is affected by the photodiode capacitance and the TIA settling time. Figure 36 shows an example of proper placement of the ADC sampling edges. Calculations for the offset values are as follows:

DARK1_OFFSET_x = (*LED_OFFSET_x* – (*NUM_INT_x* + 1))

Add 1 to the number of ADC conversions such that there is 1 µs of margin added to the placement of the Dark 1 region samples with respect to the beginning of the LED pulse.

LIT_OFFSET_x = (*LED_OFFSET_x* + t_D)

where t_D is the delay built into the offset setting to allow settling time of the signal. This value must be characterized in the final application.

DARK2_OFFSET_x = (*LED_OFFSET_x* + *LED_WIDTH_x* + t_D)

This setting only applies to two-region digital integration mode.

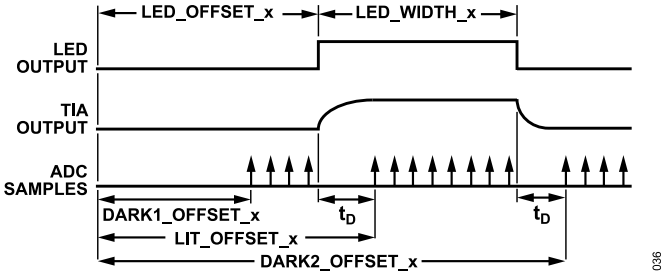

Figure 36. Proper Placement of ADC Sampling Edges in Digital Integration Mode

TIA ADC MODE

Figure 37 shows the TIA ADC mode, which bypasses the BPF and routes the TIA output through a buffer directly into the ADC. TIA ADC mode is useful in applications, such as ambient light sensing, and measuring of other dc signals, such as leakage resistance. In photodiode measurement applications using the BPF, all background light is blocked from the signal chain and, therefore, cannot be measured. TIA ADC mode can measure the amount of background and ambient light. This mode can also measure currents from other dc sources, such as leakage resistance.

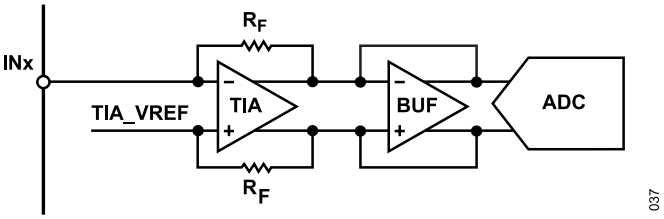

Figure 37. TIA ADC Mode Block Diagram

When the devices are in TIA ADC mode, the BPF is bypassed, and the integrator stage is reconfigured as a buffer. If both Channel 1 and Channel 2 are enabled in a single time slot, the ADC samples Channel 1 and then Channel 2 in sequential order in 1 µs intervals.

The recommended TIA ADC mode is one in which the BPF is bypassed, and the integrator is configured as an inverting buffer. This mode is enabled by writing 0x0E6 to AFE_PATH_CFG_x (Register 0x0101, Bits[8:0] for Time Slot A) to enable a signal path that includes the TIA, integrator, and ADC. Additionally, to configure the integrator as a buffer, set AFE_INT_C_BUF_x (Register 0x010A, Bit 11 for Time Slot A). With the ADC offset registers, ADC_OFF1_x and ADC_OFF2_x, set to 0 and TIA_VREF set to 1.265 V, the output of the ADC is at ~3000 codes for a single pulse and a zero input current condition. As the input current from the photodiode increases, the ADC output increases toward 16,384 LSBs.

When configuring the integrator as a buffer, there is the option of either using a gain of 1 or a gain of 0.7. Using the gain of 0.7 increases the usable dynamic range at the input to the TIA. However, it is possible to overrange the ADC in this configuration, and care must be taken to not saturate the ADC. To set the buffer gain, use the CHx_TRIM_INT_x bits. Setting CHx_TRIM_ INT_x to 00 or 01 sets a gain of 1. Setting CHx_TRIM_INT_x to 10 or 11 configures the buffer with a gain of 0.7.

Calculate the ADC output (ADC_{OUT}) as follows:

$$ADC_{OUT} = 8192 - (((2 \times TIA\_VREF - 2 \times I_{INPUT\_TIA} \times R_F - 1.8\ \ V)/146\ \ \mu V/LSB) \times Buffer\ \ Gain) \quad (3)$$

where:
TIA_VREF is the internal voltage reference signal for the TIA (the default value is 1.265 V).
I_{INPUT_TIA} is the input current to the TIA.
R_F is the TIA feedback resistor.
Buffer Gain is either 0.7 or 1 based on the setting of the CHx_TRIM_INT_x bits.

Equation 3 is an approximation and does not account for internal offsets and gain errors. The calculation also assumes that the ADC offset registers are set to 0.

Configuring a one time slot in TIA ADC mode is useful for monitoring ambient and pulsed signals at the same time. The ambient signal is monitored during the time slot configured for TIA ADC

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mode, while the pulsed signal, with the ambient signal rejected, is monitored in the time slot configured for measuring the desired LED pulsed signal.

Protecting Against TIA Saturation in Normal Operation

One of the reasons to monitor TIA ADC mode is to protect against environments that can cause saturation. One concern when operating in high light conditions, especially with larger photodiodes, is that the TIA stage can become saturated while the ADPD4200 continues to communicate data. The resulting saturation is not typical. The TIA, based on its settings, can only handle a certain level of photodiode current. Based on the way the ADPD4200 is configured, if there is a current level from the photodiode that is larger than the TIA can handle, the TIA output during the LED pulse effectively extends the current pulse, making it wider. The AFE timing is then violated because the positive portion of the BPF output extends into the negative section of the integration window. Thus, the photo signal is subtracted from itself, causing the output signal to decrease when the effective light signal increases.

To measure the response from the TIA and verify that this stage is not saturating, place the device in TIA ADC mode and slightly modify the timing. Specifically, sweep INTEG_OFFSET_x until a maximum is achieved. This procedure aligns the ADC sampling time with the LED pulse to measure the total amount of light falling on the photodetector (for example, background light and LED pulse).

If this minimum value is below 16,384 LSBs, the TIA is not saturated. However, take care, because even if the result is not 16,384 LSBs, operating the device near saturation can quickly result in saturation if light conditions change. A safe operating region is typically at ¾ full scale and lower. The ADC resolution when operating in TIA ADC mode with a buffer gain = 1 is shown in Table 23. These codes are not the same as in modes with the BPF and integrator enabled because the BPF and integrator are not unity-gain elements.

Table 23. ADC Resolution in TIA ADC Mode

TIA Gain (kΩ)	ADC Resolution (nA/LSB)
12.5	5.84
25	2.92
50	1.46
100	0.73
200	0.37

ECG MEASUREMENT WITH THE ADPD4200

The ADPD4200 can be used for ECG applications with the simple addition of an external RC network as shown in Figure 38. The electrical equivalent model for a dry electrode is shown along with an RC circuit, external to the ADPD4200, consisting of two 500 kΩ resistors in series with the inputs and a 470 pF capacitor across the inputs, which serves as the sensing capacitor for the ECG signal.

The 500 kΩ resistors serve several purposes. For example, these resistors provide short-circuit protection to limit the current that can be injected into the body in the case of shorted input pins, to increase overall input impedance of the ECG measurement, and to improve common-mode rejection when there is an electrode imbalance. The ECG signal is integrated onto the sensing capacitor. The value of this capacitor is chosen such that an acceptable amount of SNR is achieved, and the resultant RC time constant created between the capacitor and the 200 kΩ resistor is such that at least three time constants per sampling period are realized to fully charge the capacitor.

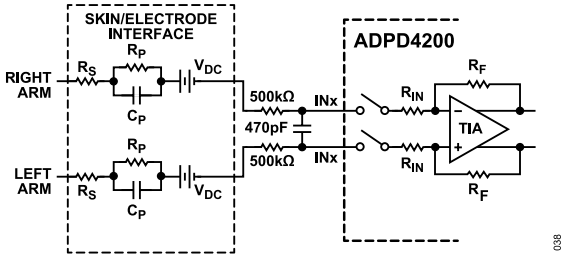

Figure 38. Circuit for Measuring Single-Lead ECG with the ADPD4200

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Sleep Float Mode

The recommended operating mode for an ECG measurement with the ADPD4200 is sleep float mode. In sleep float mode, a robust ECG measurement can be made regardless of whether low impedance wet electrodes or high impedance dry electrodes are used. Sleep float mode is also suitable for ECG measurements with large half cell potential mismatches.

In sleep float mode, the capacitor floats during other time slots and during sleep, accumulating charge from the ECG signal. The accumulated charge is then transferred into the integrator during a specified time slot. The device must be configured to float the inputs during the preconditioning period and during sleep. The inputs are connected to the external capacitor only during the charge transfer time. At all other times, the inputs are floating, resulting in a float time of $1/t_P$, where t_P is the sampling rate of the ADPD4200. For example, if the ADPD4200 is set up to sample at 300 Hz, the float time in sleep float mode is ~3.3 ms.

An advantage of using sleep float mode is reduced power consumption. While the sampling capacitor is floating, it is disconnected from the amplifier, and there is no need for the amplifier power to be on. Using sleep float mode can reduce power consumption by using the sleep time, when the amplifiers are powered down, to transfer the ECG signal from the body to the sampling capacitor. A timing diagram for sleep float mode is shown in Figure 39.

The relevant register settings for sleep float mode are shown in Table 24.

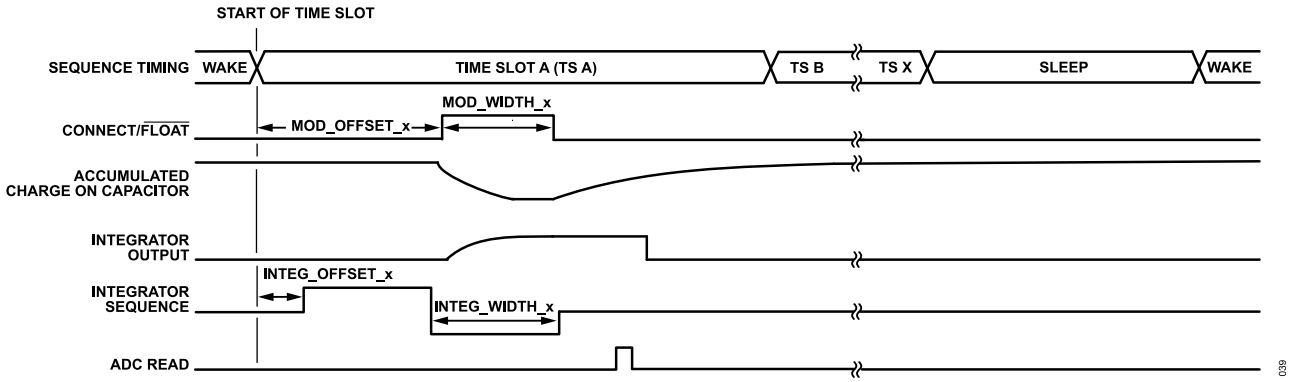

Figure 39. Sleep Float Mode Timing Diagram

Table 24. Relevant Configuration Registers for ECG Measurement Using Sleep Float Mode

Group	Time Slot A Register Address[1]	Bit Field Name	Description
Signal Path Setup	0x0100, Bits[13:12]	SAMPLE_TYPE_x	Leave at the default setting (0) for default sampling mode.
	0x0100, Bits[11:10]	INPUT_R_SELECT_x	Set to 0x0 for 500 Ω series input resistor.
	0x0101, Bits[8:0]	AFE_PATH_CFG_x	Set to 0x0E6 for TIA, integrator, and ADC. Bypass the BPF.
	0x0101, Bits[15:12]	PRE_WIDTH_x	Set to 0 to skip preconditioning period.
	0x0102, Bits[15:12], 0x0102, Bits[3:0]	INPxx_x	Set to 0x7 to enable desired inputs connected to Channel 1 as defined in PAIRxx.
	0x0103, Bits[14:12]	PRECON_x	Set to 0x0 to float the inputs during preconditioning.
	0x0020, Bits[15:12], 0x0020, Bits[3:0]	INP_SLEEP_xx	Set to 0x0 to float inputs during sleep.
	0x0021, Bit 3, 0x0021, Bit 0	PAIRxx	Set to 1 to configure selected inputs as a differential pair.
	0x0104, Bits[5:0]	TIA_GAIN_CHx_x	Select TIA gain.
	0x0104, Bits[9:8]	AFE_TRIM_VREF_x	Set to 0x2 to set TIA_VREF = 0.9 V.
Float Mode Configuration	0x0107, Bits[15:8]	NUM_INT_x	Set to 1 for a single integration per group of ADC conversions.
	0x0107, Bits[7:0]	NUM_REPEAT_x	Number of sequence repeats.
	0x0108, Bits[13:12]	MOD_TYPE_x	Set to 0x1 for float type operation.
	0x0108, Bits[9:0]	MIN_PERIOD_x	Set to 0. Minimum period is not applicable to sleep float mode with a single integration.
	0x010A, Bits[4:0]	INTEG_WIDTH_x	Integration time in µs. Set to MOD_WIDTH_x + 1.
	0x010A, Bits[14:12], 0x010A, Bits[10:8]	CHx_AMP_DISABLE_x	Set 0x010A, Bit 9 to 1 to power down the BPF for Channel 1, and Bit 13 to 1 to power down the BPF for Channel 2 if Channel 2 is enabled.
	0x010B, Bits[12:0]	INTEG_OFFSET_x	Integration sequence start time. Set to (MOD_OFFSET_x − INTEG_WIDTH_x – 250 ns).

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Table 24. Relevant Configuration Registers for ECG Measurement Using Sleep Float Mode

Group	Time Slot A Register Address[1]	Bit Field Name	Description
	0x010C, Bits[15:8]	MOD_WIDTH_x	Sets width of connect pulse in 1 µs increments, which is the time required to transfer the charge from the external capacitor. Set to approximately three time constants based on the time constant created between the external capacitor and the series input resistor (500 Ω or 6500 Ω based on setting of INPUT_R_SELECT_x).
	0x010C, Bits[7:0]	MOD_OFFSET_x	Sets start time of first connect pulse in 1 µs increments. Set to INTEG_WIDTH_x + 4.

[1] This is the Time Slot A register address. Add 0x020 for the identical register address for each subsequent time slot. For example, Register 0x0100 is the location for SAMPLE_TYPE_A. For Time Slot B, this register is at Address 0x0120. For Time Slot C, this register is at Address 0x0140. For Time Slot D, this register is at Address 0x0160, and so on.

Sleep Float Mode with Multiple Charge Transfers

When the electrode half cell potential mismatch becomes very large, on the order of hundreds of millivolts or greater, the half cell dc signal (V_{H-C}, see ECG Measurement with the ADPD4200) uses a significant amount of the dynamic range available for the ECG measurement. This half cell potential mismatch is a result of using electrodes of different materials, for example, stainless steel for one of the electrodes and titanium for a second electrode. The maximum amount of charge that the ADPD4200 can accommodate for a single sample is ~7.5 pC when using the 200 kΩ TIA gain setting. The maximum allowable charge per sample scales inversely with the gain of the TIA. The presence of a large dc signal creates excess charge on the sampling capacitor, which can saturate the input to the ADC. For example, a half cell potential mismatch of 100 mV adds an additional 47 pC of charge to the 470 pF capacitor.

To accommodate the half cell voltage without reducing the size of the sampling capacitor, the recommendation is to reduce the TIA gain to 50 kΩ or 100 kΩ, and to transfer the accumulated charge in multiple short transfers. For example, to transfer 47 pC of charge from the external capacitor to the internal integrator, set the TIA gain to 50 kΩ to accommodate 30 pC of charge per sample, and set the input resistor, R_{IN}, to 6.25 kΩ. Setting R_{IN} = 6.25 kΩ limits the rate of charge transfer into the TIA with an RC time constant of 2 × 6.25 kΩ × 470 pF = 5.9 µs.

Next, reduce the amount of time allowed to transfer the charge by using modulation pulses, which are some fraction of the time constant such that a smaller percentage of the overall charge is transferred and integrated per pulse to avoid saturating the TIA. Multiple transfer cycles are then used to fully discharge the sampling capacitor. The ADPD4200 automatically sums the results of the transfer cycles and report the total charge.

The timing for this mode is the same as shown in Figure 39 except the device is set up for multiple modulation pulses. All registers are set the same as for sleep float mode except the following:

- MOD_WIDTH_x and INTEG_WIDTH_x are shorter to accommodate shorter pulses.
- INPUT_R_SELECT_x = 1 to select the 6.25 kΩ input resistor.
- NUM_REPEAT_x is set to >1.

Lead Off Detection

To perform a lead off detection measurement, the ADPD4200 measures the impedance of the electrode contacts to determine whether one or more of the electrodes are not making contact with the skin. This measurement requires a separate electrode connected to an unused VCx pin that can provide a stimulus to the body. The RC network of the ECG measurement is also bypassed by wiring the electrodes directly to a separate set of inputs through 50 kΩ resistors. The response from the stimulus is measured from this separate set of inputs. Figure 40 shows a circuit that can be used for the lead off detection measurement. R_{BODY} is the resistance of the body.

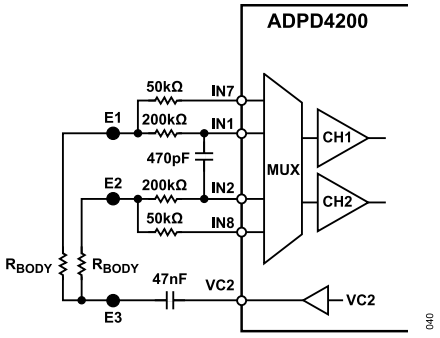

Figure 40. Circuit Used for Lead Off Detection Measurement

ECG and three-electrode lead off detection are measured as follows:

1. ECG is measured in Time Slot A as defined in the ECG Measurement with the ADPD4200 section.
2. Lead off detection of the ECG electrodes is taken in Time Slot B by making simultaneous single-ended impedance measurements of ECG Electrode 1 (E1) and Electrode 2 (E2) into Channel 1 and Channel 2, respectively, as shown in Figure 40. Note that the third electrode (E3) is used for biasing the body.

When both ECG electrodes, E1 and E2, are making contact with the skin during the measurement, an ECG signal is visible. The impedance measurements of the E1 and E2 electrodes have

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some readout indicating that contact is being made with the skin and current is flowing into the ADPD4200 through the body of low impedance when the stimulus is applied. When either ECG electrode stops making contact with the skin or is loose, there is no ECG signal in the acquired trace. When contact between both electrodes and the skin is restored, the ECG signal appears immediately. Because two inputs and two channels are allocated to detect the lead off condition for two electrodes, this measurement method can determine if one electrode loses contact with skin or both electrodes lose contact. This measurement can also detect which one of the electrodes loses contact with the skin if only one electrode loses contact.

Figure 41 shows a data plot of a lead off detection measurement during an ECG measurement using the circuit shown in Figure 40. When the ECG electrodes are making contact with the skin during the measurement, an ECG signal is clearly visible. The impedance measurements of the E1 and E2 electrodes show some value indicating that contact is being made with the skin and current is flowing into the ADPD4200 when the stimulus is applied. When either electrode stops making contact with the skin, 0 is read for that measurement indicating an open circuit, effectively a lead off condition. When contact between both electrodes and the skin is restored, the ECG signal is reacquired in less than 1 sec.

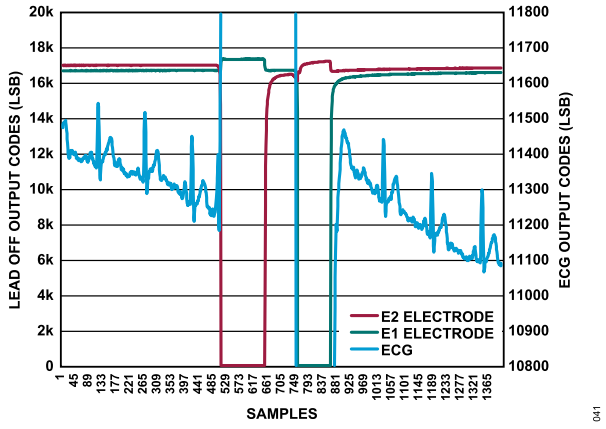

Figure 41. Lead Off Detection Measurement

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	**Name**	**Bits**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset**	**R/W**
0x0000	FIFO_STATUS	[15:8]	CLEAR_FIFO	INT_FIFO_UFLOW	INT_FIFO_OFLOW	Reserved		FIFO_BYTE_COUNT[10:8]			0x0000	R/W
		[7:0]	FIFO_BYTE_COUNT[7:0]									
0x0001	INT_STATUS_DATA	[15:8]	INT_FIFO_TH	Reserved			INT_DATA_L	INT_DATA_K	INT_DATA_J	INT_DATA_I	0x0000	R/W
		[7:0]	INT_DATA_H	INT_DATA_G	INT_DATA_F	INT_DATA_E	INT_DATA_D	INT_DATA_C	INT_DATA_B	INT_DATA_A		
0x0002	INT_STATUS_LEV0	[15:8]	Reserved				INT_LEV0_L	INT_LEV0_K	INT_LEV0_J	INT_LEV0_I	0x0000	R/W
		[7:0]	INT_LEV0_H	INT_LEV0_G	INT_LEV0_F	INT_LEV0_E	INT_LEV0_D	INT_LEV0_C	INT_LEV0_B	INT_LEV0_A		
0x0003	INT_STATUS_LEV1	[15:8]	Reserved				INT_LEV1_L	INT_LEV1_K	INT_LEV1_J	INT_LEV1_I	0x0000	R/W
		[7:0]	INT_LEV1_H	INT_LEV1_G	INT_LEV1_F	INT_LEV1_E	INT_LEV1_D	INT_LEV1_C	INT_LEV1_B	INT_LEV1_A		
0x0006	FIFO_TH	[15:8]	Reserved						FIFO_TH[9:8]		0x0000	R/W
		[7:0]	FIFO_TH[7:0]									
0x0007	INT_ACLEAR	[15:8]	INT_ACLEAR_FIFO	Reserved			INT_ACLEAR_DATA_L	INT_ACLEAR_DATA_K	INT_ACLEAR_DATA_J	INT_ACLEAR_DATA_I	0x8FFF	R/W
		[7:0]	INT_ACLEAR_DATA_H	INT_ACLEAR_DATA_G	INT_ACLEAR_DATA_F	INT_ACLEAR_DATA_E	INT_ACLEAR_DATA_D	INT_ACLEAR_DATA_C	INT_ACLEAR_DATA_B	INT_ACLEAR_DATA_A		
0x0008	CHIP_ID	[15:8]	Version								0x00C2	R
		[7:0]	CHIP_ID									
0x0009	OSC32M	[15:8]	Reserved								0x0090	R/W
		[7:0]	OSC_32M_FREQ_ADJ[7:0]									
0x000A	OSC32M_CAL	[15:8]	OSC_32M_CAL_START	OSC_32M_CAL_COUNT[14:8]							0x0000	R/W
		[7:0]	OSC_32M_CAL_COUNT[7:0]									
0x000B	OSC1M	[15:8]	Reserved					CLK_CAL_ENA	OSC_1M_FREQ_ADJ[9:8]		0x02B2	R/W
		[7:0]	OSC_1M_FREQ_ADJ[7:0]									
0x000C	OSC32K	[15:8]	CAPTURE_TIMESTAMP	Reserved							0x0012	R/W
		[7:0]	Reserved		OSC_32K_ADJUST[5:0]							
0x000D	TS_FREQ	[15:8]	TIMESLOT_PERIOD_L[15:8]								0x2710	R/W
		[7:0]	TIMESLOT_PERIOD_L[7:0]									
0x000E	TS_FREQH	[15:8]	Reserved								0x0000	R/W
		[7:0]	Reserved	TIMESLOT_PERIOD_H[7:0]								
0x000F	SYS_CTL	[15:8]	SW_RESET	Reserved					ALT_CLOCKS[1:0]		0x0000	R/W
		[7:0]	ALT_CLK_GPIO[1:0]		Reserved			LFOSC_SEL	OSC_1M_EN	OSC_32K_EN		
0x0010	OPMODE	[15:8]	Reserved				TIMESLOT_EN[3:0]				0x0000	R/W
		[7:0]	Reserved							OP_MODE		

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	**Name**	**Bits**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset**	**R/W**
0x0011	STAMP_L	[15:8]	TIMESTAMP_COUNT_L[15:8]								0x0000	R
		[7:0]	TIMESTAMP_COUNT_L[7:0]									
0x0012	STAMP_H	[15:8]	TIMESTAMP_COUNT_H[15:8]								0x0000	R
		[7:0]	TIMESTAMP_COUNT_H[7:0]									
0x0013	STAMP-DELTA	[15:8]	TIMESTAMP_SLOT_DELTA[15:8]								0x0000	R
		[7:0]	TIMESTAMP_SLOT_DELTA[7:0]									
0x0014	INT_ENABLE_XD	[15:8]	INTX_EN_FIFO_TH	INTX_EN_FIFO_UFLOW	INTX_EN_FIFO_OFLOW	Reserved	INTX_EN_DATA_L	INTX_EN_DATA_K	INTX_EN_DATA_J	INTX_EN_DATA_I	0x0000	R/W
		[7:0]	INTX_EN_DATA_H	INTX_EN_DATA_G	INTX_EN_DATA_F	INTX_EN_DATA_E	INTX_EN_DATA_D	INTX_EN_DATA_C	INTX_EN_DATA_B	INTX_EN_DATA_A		
0x0015	INT_ENABLE_YD	[15:8]	INTY_EN_FIFO_TH	INTY_EN_FIFO_UFLOW	INTY_EN_FIFO_OFLOW	Reserved	INTY_EN_DATA_L	INTY_EN_DATA_K	INTY_EN_DATA_J	INTY_EN_DATA_I	0x0000	R/W
		[7:0]	INTY_EN_DATA_H	INTY_EN_DATA_G	INTY_EN_DATA_F	INTY_EN_DATA_E	INTY_EN_DATA_D	INTY_EN_DATA_C	INTY_EN_DATA_B	INTY_EN_DATA_A		
0x0016	INT_ENABLE_XL0	[15:8]	Reserved				INTX_EN_LEV0_L	INTX_EN_LEV0_K	INTX_EN_LEV0_J	INTX_EN_LEV0_I	0x0000	R/W
		[7:0]	INTX_EN_LEV0_H	INTX_EN_LEV0_G	INTX_EN_LEV0_F	INTX_EN_LEV0_E	INTX_EN_LEV0_D	INTX_EN_LEV0_C	INTX_EN_LEV0_B	INTX_EN_LEV0_A		
0x0017	INT_ENABLE_XL1	[15:8]	Reserved				INTX_EN_LEV1_L	INTX_EN_LEV1_K	INTX_EN_LEV1_J	INTX_EN_LEV1_I	0x0000	R/W
		[7:0]	INTX_EN_LEV1_H	INTX_EN_LEV1_G	INTX_EN_LEV1_F	INTX_EN_LEV1_E	INTX_EN_LEV1_D	INTX_EN_LEV1_C	INTX_EN_LEV1_B	INTX_EN_LEV1_A		
0x001A	INT_ENABLE_YL0	[15:8]	Reserved				INTY_EN_LEV0_L	INTY_EN_LEV0_K	INTY_EN_LEV0_J	INTY_EN_LEV0_I	0x0000	R/W
		[7:0]	INTY_EN_LEV0_H	INTY_EN_LEV0_G	INTY_EN_LEV0_F	INTY_EN_LEV0_E	INTY_EN_LEV0_D	INTY_EN_LEV0_C	INTY_EN_LEV0_B	INTY_EN_LEV0_A		
0x001B	INT_ENABLE_YL1	[15:8]	Reserved				INTY_EN_LEV1_L	INTY_EN_LEV1_K	INTY_EN_LEV1_J	INTY_EN_LEV1_I	0x0000	R/W
		[7:0]	INTY_EN_LEV1_H	INTY_EN_LEV1_G	INTY_EN_LEV1_F	INTY_EN_LEV1_E	INTY_EN_LEV1_D	INTY_EN_LEV1_C	INTY_EN_LEV1_B	INTY_EN_LEV1_A		
0x001E	FIFO_STATUS_BYTES	[15:8]	Reserved								0x0000	R/W
		[7:0]	Reserved		ENA_STAT_LX	ENA_STAT_L1	ENA_STAT_L0	ENA_STAT_D2	ENA_STAT_D1	ENA_STAT_SUM		
0x0020	INPUT_SLEEP	[15:8]	INP_SLEEP_78[3:0]				Reserved				0x0000	R/W
		[7:0]	Reserved				INP_SLEEP_12[3:0]					
0x0021	INPUT_CFG	[15:8]	Reserved								0x0000	R/W
		[7:0]	VC2_SLEEP[1:0]		VC1_SLEEP[1:0]		PAIR78	Reserved		PAIR12		
0x0022	GPIO_CFG	[15:8]	GPIO_SLEW[1:0]		GPIO_DRV[1:0]		Reserved				0x0000	R/W
		[7:0]	Reserved		GPIO_PIN_CFG1[2:0]			GPIO_PIN_CFG0[2:0]				
0x0023	GPIO01	[15:8]	Reserved	GPIOOUT1[6:0]							0x0000	R/W
		[7:0]	Reserved	GPIOOUT0[6:0]								

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	**Name**	**Bits**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset**	**R/W**
0x0025	GPIO_IN	[15:8]	Reserved								0x0000	R
		[7:0]	Reserved				GPIO_INPUT[3:0]					
0x0026	GPIO_EXT	[15:8]	Reserved							TS_GPIO_SLEEP	0x0000	R/W
		[7:0]	TIMESTAMP_INV	TIMESTAMP_ALWAYS_EN	TIMESTAMP_GPIO[1:0]		Reserved	EXT_SYNC_EN	EXT_SYNC_GPIO[1:0]			
0x002E	DATA_HOLD_FLAG	[15:8]	Reserved				HOLD_REGS_L	HOLD_REGS_K	HOLD_REGS_J	HOLD_REGS_I	0x0000	R/W
		[7:0]	HOLD_REGS_H	HOLD_REGS_G	HOLD_REGS_F	HOLD_REGS_E	HOLD_REGS_D	HOLD_REGS_C	HOLD_REGS_B	HOLD_REGS_A		
0x002F	FIFO_DATA	[15:8]	FIFO_DATA[15:8]								0x0000	R
		[7:0]	FIFO_DATA[7:0]									
0x0030	SIGNAL1_L_A	[15:8]	SIGNAL1_L_A[15:8]								0x0000	R
		[7:0]	SIGNAL1_L_A[7:0]									
0x0031	SIGNAL1_H_A	[15:8]	SIGNAL1_H_A[15:8]								0x0000	R
		[7:0]	SIGNAL1_H_A[7:0]									
0x0032	SIGNAL2_L_A	[15:8]	SIGNAL2_L_A[15:8]								0x0000	R
		[7:0]	SIGNAL2_L_A[7:0]									
0x0033	SIGNAL2_H_A	[15:8]	SIGNAL2_H_A[15:8]								0x0000	R
		[7:0]	SIGNAL2_H_A[7:0]									
0x0034	DARK1_L_A	[15:8]	DARK1_L_A[15:8]								0x0000	R
		[7:0]	DARK1_L_A[7:0]									
0x0035	DARK1_H_A	[15:8]	DARK1_H_A[15:8]								0x0000	R
		[7:0]	DARK1_H_A[7:0]									
0x0036	DARK2_L_A	[15:8]	DARK2_L_A[15:8]								0x0000	R
		[7:0]	DARK2_L_A[7:0]									
0x0037	DARK2_H_A	[15:8]	DARK2_H_A[15:8]								0x0000	R
		[7:0]	DARK2_H_A[7:0]									
0x0038	SIGNAL1_L_B	[15:8]	SIGNAL1_L_B[15:8]								0x0000	R
		[7:0]	SIGNAL1_L_B[7:0]									
0x0039	SIGNAL1_H_B	[15:8]	SIGNAL1_H_B[15:8]								0x0000	R
		[7:0]	SIGNAL1_H_B[7:0]									
0x003A	SIGNAL2_L_B	[15:8]	SIGNAL2_L_B[15:8]								0x0000	R
		[7:0]	SIGNAL2_L_B[7:0]									
0x003B	SIGNAL2_H_B	[15:8]	SIGNAL2_H_B[15:8]								0x0000	R
		[7:0]	SIGNAL2_H_B[7:0]									
0x003C	DARK1_L_B	[15:8]	DARK1_L_B[15:8]								0x0000	R
		[7:0]	DARK1_L_B[7:0]									
0x003D	DARK1_H_B	[15:8]	DARK1_H_B[15:8]								0x0000	R

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
		[7:0]	DARK1_H_B[7:0]									
0x003E	DARK2_L_B	[15:8]	DARK2_L_B[15:8]								0x0000	R
		[7:0]	DARK2_L_B[7:0]									
0x003F	DARK2_H_B	[15:8]	DARK2_H_B[15:8]								0x0000	R
		[7:0]	DARK2_H_B[7:0]									
0x0040	SIGNAL1_L_C	[15:8]	SIGNAL1_L_C[15:8]								0x0000	R
		[7:0]	SIGNAL1_L_C[7:0]									
0x0041	SIGNAL1_H_C	[15:8]	SIGNAL1_H_C[15:8]								0x0000	R
		[7:0]	SIGNAL1_H_C[7:0]									
0x0042	SIGNAL2_L_C	[15:8]	SIGNAL2_L_C[15:8]								0x0000	R
		[7:0]	SIGNAL2_L_C[7:0]									
0x0043	SIGNAL2_H_C	[15:8]	SIGNAL2_H_C[15:8]								0x0000	R
		[7:0]	SIGNAL2_H_C[7:0]									
0x0044	DARK1_L_C	[15:8]	DARK1_L_C[15:8]								0x0000	R
		[7:0]	DARK1_L_C[7:0]									
0x0045	DARK1_H_C	[15:8]	DARK1_H_C[15:8]								0x0000	R
		[7:0]	DARK1_H_C[7:0]									
0x0046	DARK2_L_C	[15:8]	DARK2_L_C[15:8]								0x0000	R
		[7:0]	DARK2_L_C[7:0]									
0x0047	DARK2_H_C	[15:8]	DARK2_H_C[15:8]								0x0000	R
		[7:0]	DARK2_H_C[7:0]									
0x0048	SIGNAL1_L_D	[15:8]	SIGNAL1_L_D[15:8]								0x0000	R
		[7:0]	SIGNAL1_L_D[7:0]									
0x0049	SIGNAL1_H_D	[15:8]	SIGNAL1_H_D[15:8]								0x0000	R
		[7:0]	SIGNAL1_H_D[7:0]									
0x004A	SIGNAL2_L_D	[15:8]	SIGNAL2_L_D[15:8]								0x0000	R
		[7:0]	SIGNAL2_L_D[7:0]									
0x004B	SIGNAL2_H_D	[15:8]	SIGNAL2_H_D[15:8]								0x0000	R
		[7:0]	SIGNAL2_H_D[7:0]									
0x004C	DARK1_L_D	[15:8]	DARK1_L_D[15:8]								0x0000	R
		[7:0]	DARK1_L_D[7:0]									
0x004D	DARK1_H_D	[15:8]	DARK1_H_D[15:8]								0x0000	R
		[7:0]	DARK1_H_D[7:0]									
0x004E	DARK2_L_D	[15:8]	DARK2_L_D[15:8]								0x0000	R
		[7:0]	DARK2_L_D[7:0]									
0x004F	DARK2_H_D	[15:8]	DARK2_H_D[15:8]								0x0000	R
		[7:0]	DARK2_H_D[7:0]									
0x0050	SIGNAL1_L_E	[15:8]	SIGNAL1_L_E[15:8]								0x0000	R
		[7:0]	SIGNAL1_L_E[7:0]									

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	**Name**	**Bits**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset**	**R/W**
0x0051	SIGNAL1_H_E	[15:8]	SIGNAL1_H_E[15:8]								0x0000	R
		[7:0]	SIGNAL1_H_E[7:0]									
0x0052	SIGNAL2_L_E	[15:8]	SIGNAL2_L_E[15:8]								0x0000	R
		[7:0]	SIGNAL2_L_E[7:0]									
0x0053	SIGNAL2_H_E	[15:8]	SIGNAL2_H_E[15:8]								0x0000	R
		[7:0]	SIGNAL2_H_E[7:0]									
0x0054	DARK1_L_E	[15:8]	DARK1_L_E[15:8]								0x0000	R
		[7:0]	DARK1_L_E[7:0]									
0x0055	DARK1_H_E	[15:8]	DARK1_H_E[15:8]								0x0000	R
		[7:0]	DARK1_H_E[7:0]									
0x0056	DARK2_L_E	[15:8]	DARK2_L_E[15:8]								0x0000	R
		[7:0]	DARK2_L_E[7:0]									
0x0057	DARK2_H_E	[15:8]	DARK2_H_E[15:8]								0x0000	R
		[7:0]	DARK2_H_E[7:0]									
0x0058	SIGNAL1_L_F	[15:8]	SIGNAL1_L_F[15:8]								0x0000	R
		[7:0]	SIGNAL1_L_F[7:0]									
0x0059	SIGNAL1_H_F	[15:8]	SIGNAL1_H_F[15:8]								0x0000	R
		[7:0]	SIGNAL1_H_F[7:0]									
0x005A	SIGNAL2_L_F	[15:8]	SIGNAL2_L_F[15:8]								0x0000	R
		[7:0]	SIGNAL2_L_F[7:0]									
0x005B	SIGNAL2_H_F	[15:8]	SIGNAL2_H_F[15:8]								0x0000	R
		[7:0]	SIGNAL2_H_F[7:0]									
0x005C	DARK1_L_F	[15:8]	DARK1_L_F[15:8]								0x0000	R
		[7:0]	DARK1_L_F[7:0]									
0x005D	DARK1_H_F	[15:8]	DARK1_H_F[15:8]								0x0000	R
		[7:0]	DARK1_H_F[7:0]									
0x005E	DARK2_L_F	[15:8]	DARK2_L_F[15:8]								0x0000	R
		[7:0]	DARK2_L_F[7:0]									
0x005F	DARK2_H_F	[15:8]	DARK2_H_F[15:8]								0x0000	R
		[7:0]	DARK2_H_F[7:0]									
0x0060	SIGNAL1_L_G	[15:8]	SIGNAL1_L_G[15:8]								0x0000	R
		[7:0]	SIGNAL1_L_G[7:0]									
0x0061	SIGNAL1_H_G	[15:8]	SIGNAL1_H_G[15:8]								0x0000	R
		[7:0]	SIGNAL1_H_G[7:0]									
0x0062	SIGNAL2_L_G	[15:8]	SIGNAL2_L_G[15:8]								0x0000	R
		[7:0]	SIGNAL2_L_G[7:0]									
0x0063	SIGNAL2_H_G	[15:8]	SIGNAL2_H_G[15:8]								0x0000	R

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
		[7:0]	SIGNAL2_H_G[7:0]									
0x0064	DARK1_L_G	[15:8]	DARK1_L_G[15:8]								0x0000	R
		[7:0]	DARK1_L_G[7:0]									
0x0065	DARK1_H_G	[15:8]	DARK1_H_G[15:8]								0x0000	R
		[7:0]	DARK1_H_G[7:0]									
0x0066	DARK2_L_G	[15:8]	DARK2_L_G[15:8]								0x0000	R
		[7:0]	DARK2_L_G[7:0]									
0x0067	DARK2_H_G	[15:8]	DARK2_H_G[15:8]								0x0000	R
		[7:0]	DARK2_H_G[7:0]									
0x0068	SIGNAL1_L_H	[15:8]	SIGNAL1_L_H[15:8]								0x0000	R
		[7:0]	SIGNAL1_L_H[7:0]									
0x0069	SIGNAL1_H_H	[15:8]	SIGNAL1_H_H[15:8]								0x0000	R
		[7:0]	SIGNAL1_H_H[7:0]									
0x006A	SIGNAL2_L_H	[15:8]	SIGNAL2_L_H[15:8]								0x0000	R
		[7:0]	SIGNAL2_L_H[7:0]									
0x006B	SIGNAL2_H_H	[15:8]	SIGNAL2_H_H[15:8]								0x0000	R
		[7:0]	SIGNAL2_H_H[7:0]									
0x006C	DARK1_L_H	[15:8]	DARK1_L_H[15:8]								0x0000	R
		[7:0]	DARK1_L_H[7:0]									
0x006D	DARK1_H_H	[15:8]	DARK1_H_H[15:8]								0x0000	R
		[7:0]	DARK1_H_H[7:0]									
0x006E	DARK2_L_H	[15:8]	DARK2_L_H[15:8]								0x0000	R
		[7:0]	DARK2_L_H[7:0]									
0x006F	DARK2_H_H	[15:8]	DARK2_H_H[15:8]								0x0000	R
		[7:0]	DARK2_H_H[7:0]									
0x0070	SIGNAL1_L_I	[15:8]	SIGNAL1_L_I[15:8]								0x0000	R
		[7:0]	SIGNAL1_L_I[7:0]									
0x0071	SIGNAL1_H_I	[15:8]	SIGNAL1_H_I[15:8]								0x0000	R
		[7:0]	SIGNAL1_H_I[7:0]									
0x0072	SIGNAL2_L_I	[15:8]	SIGNAL2_L_I[15:8]								0x0000	R
		[7:0]	SIGNAL2_L_I[7:0]									
0x0073	SIGNAL2_H_I	[15:8]	SIGNAL2_H_I[15:8]								0x0000	R
		[7:0]	SIGNAL2_H_I[7:0]									
0x0074	DARK1_L_I	[15:8]	DARK1_L_I[15:8]								0x0000	R
		[7:0]	DARK1_L_I[7:0]									
0x0075	DARK1_H_I	[15:8]	DARK1_H_I[15:8]								0x0000	R
		[7:0]	DARK1_H_I[7:0]									
0x0076	DARK2_L_I	[15:8]	DARK2_L_I[15:8]								0x0000	R
		[7:0]	DARK2_L_I[7:0]									

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	**Name**	**Bits**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset**	**R/W**
0x0077	DARK2_H_I	[15:8]	DARK2_H_I[15:8]								0x0000	R
		[7:0]	DARK2_H_I[7:0]									
0x0078	SIGNAL1_L_J	[15:8]	SIGNAL1_L_J[15:8]								0x0000	R
		[7:0]	SIGNAL1_L_J[7:0]									
0x0079	SIGNAL1_H_J	[15:8]	SIGNAL1_H_J[15:8]								0x0000	R
		[7:0]	SIGNAL1_H_J[7:0]									
0x007A	SIGNAL2_L_J	[15:8]	SIGNAL2_L_J[15:8]								0x0000	R
		[7:0]	SIGNAL2_L_J[7:0]									
0x007B	SIGNAL2_H_J	[15:8]	SIGNAL2_H_J[15:8]								0x0000	R
		[7:0]	SIGNAL2_H_J[7:0]									
0x007C	DARK1_L_J	[15:8]	DARK1_L_J[15:8]								0x0000	R
		[7:0]	DARK1_L_J[7:0]									
0x007D	DARK1_H_J	[15:8]	DARK1_H_J[15:8]								0x0000	R
		[7:0]	DARK1_H_J[7:0]									
0x007E	DARK2_L_J	[15:8]	DARK2_L_J[15:8]								0x0000	R
		[7:0]	DARK2_L_J[7:0]									
0x007F	DARK2_H_J	[15:8]	DARK2_H_J[15:8]								0x0000	R
		[7:0]	DARK2_H_J[7:0]									
0x0080	SIGNAL1_L_K	[15:8]	SIGNAL1_L_K[15:8]								0x0000	R
		[7:0]	SIGNAL1_L_K[7:0]									
0x0081	SIGNAL1_H_K	[15:8]	SIGNAL1_H_K[15:8]								0x0000	R
		[7:0]	SIGNAL1_H_K[7:0]									
0x0082	SIGNAL2_L_K	[15:8]	SIGNAL2_L_K[15:8]								0x0000	R
		[7:0]	SIGNAL2_L_K[7:0]									
0x0083	SIGNAL2_H_K	[15:8]	SIGNAL2_H_K[15:8]								0x0000	R
		[7:0]	SIGNAL2_H_K[7:0]									
0x0084	DARK1_L_K	[15:8]	DARK1_L_K[15:8]								0x0000	R
		[7:0]	DARK1_L_K[7:0]									
0x0085	DARK1_H_K	[15:8]	DARK1_H_K[15:8]								0x0000	R
		[7:0]	DARK1_H_K[7:0]									
0x0086	DARK2_L_K	[15:8]	DARK2_L_K[15:8]								0x0000	R
		[7:0]	DARK2_L_K[7:0]									
0x0087	DARK2_H_K	[15:8]	DARK2_H_K[15:8]								0x0000	R
		[7:0]	DARK2_H_K[7:0]									
0x0088	SIGNAL1_L_L	[15:8]	SIGNAL1_L_L[15:8]								0x0000	R
		[7:0]	SIGNAL1_L_L[7:0]									
0x0089	SIGNAL1_H_L	[15:8]	SIGNAL1_H_L[15:8]								0x0000	R
		[7:0]	SIGNAL1_H_L[7:0]									

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	**Name**	**Bits**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset**	**R/W**
0x008A	SIGNAL2_L_L	[15:8]	SIGNAL2_L_L[15:8]								0x0000	R
		[7:0]	SIGNAL2_L_L[7:0]									
0x008B	SIGNAL2_H_L	[15:8]	SIGNAL2_H_L[15:8]								0x0000	R
		[7:0]	SIGNAL2_H_L[7:0]									
0x008C	DARK1_L_L	[15:8]	DARK1_L_L[15:8]								0x0000	R
		[7:0]	DARK1_L_L[7:0]									
0x008D	DARK1_H_L	[15:8]	DARK1_H_L[15:8]								0x0000	R
		[7:0]	DARK1_H_L[7:0]									
0x008E	DARK2_L_L	[15:8]	DARK2_L_L[15:8]								0x0000	R
		[7:0]	DARK2_L_L[7:0]									
0x008F	DARK2_H_L	[15:8]	DARK2_H_L[15:8]								0x0000	R
		[7:0]	DARK2_H_L[7:0]									
0x00B4	IO_ADJUST	[15:8]	Reserved (set to 0x00)								0x0050	R/W
		[7:0]	Reserved (set to 0x5)				SPI_SLEW[1:0]		SPI_DRV[1:0]			
0x0100	TS_CTRL_A	[15:8]	SUB SAMPLE_A	CH2_EN_A	SAMPLE_TYPE_A[1:0]		INPUT_R_SELECT_A[1:0]		TIMESLOT_OFFSET_A[9:8]		0x0000	R/W
		[7:0]	TIMESLOT_OFFSET_A[7:0]									
0x0101	TS_PATH_A	[15:8]	PRE_WIDTH_A[3:0]				Reserved		TS_GPIO_A	AFE_PATH_CFG_A[8]	0x40DA	R/W
		[7:0]	AFE_PATH_CFG_A[7:0]									
0x0102	INPUTS_A	[15:8]	INP78_A[3:0]				Reserved				0x0000	R/W
		[7:0]	Reserved				INP12_A[3:0]					
0x0103	CATHODE_A	[15:8]	Reserved	PRECON_A[2:0]			VC2_PULSE_A[1:0]		VC2_ALT_A[1:0]		0x0000	R/W
		[7:0]	VC2_SEL_A[1:0]		VC1_PULSE_A[1:0]		VC1_ALT_A[1:0]		VC1_SEL_A[1:0]			
0x0104	AFE_TRIM_A	[15:8]	Reserved	CH2_TRIM_INT_A[1:0]		CH1_TRIM_INT_A[1:0]		VREF_PULSE_A	AFE_TRIM_VREF_A[1:0]		0x03C0	R/W
		[7:0]	VREF_PULSE_VAL_A[1:0]		TIA_GAIN_CH2_A[2:0]			TIA_GAIN_CH1_A[2:0]				
0x0105	LED_POW12_A	[15:8]	LED_DRIVESIDE2_A	LED_CURRENT2_A[6:0]							0x0000	R/W
		[7:0]	LED_DRIVESIDE1_A	LED_CURRENT1_A[6:0]								
0x0106	LED_POW34_A	[15:8]	LED_DRIVESIDE4_A	LED_CURRENT4_A[6:0]							0x0000	R/W
		[7:0]	LED_DRIVESIDE3_A	LED_CURRENT3_A[6:0]								
0x0107	COUNTS_A	[15:8]	NUM_INT_A[7:0]								0x0101	R/W
		[7:0]	NUM_REPEAT_A[7:0]									
0x0108	PERIOD_A	[15:8]	Reserved		MOD_TYPE_A[1:0]		Reserved		MIN_PERIOD_A[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_A[7:0]									
0x0109	LED_PULSE_A	[15:8]	LED_WIDTH_A[7:0]								0x0210	R/W
		[7:0]	LED_OFFSET_A[7:0]									

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	**Name**	**Bits**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset**	**R/W**
0x010A	INTEG_SETUP_A	[15:8]	SINGLE_INTEG_A	CH2_AMP_DISABLE_A[2:0]			AFE_INT_C_BUF_A	CH1_AMP_DISABLE_A[2:0]			0x0003	R/W
		[7:0]	ADC_COUNT_A[1:0]		Reserved		INTEG_WIDTH_A[4:0]					
0x010B	INTEG_OS_A	[15:8]	Reserved				INTEG _OFFSET_A[12:8]				0x0214	R/W
		[7:0]	INTEG_OFFSET_A[7:0]									
0x010C	MOD_PULSE_A	[15:8]	MOD_WIDTH_A[7:0]								0x0001	R/W
		[7:0]	MOD_OFFSET_A[7:0]									
0x010D	PATTERN_A	[15:8]	LED_DISABLE_A[3:0]				MOD_DISABLE_A[3:0]				0x0000	R/W
		[7:0]	SUBTRACT_A[3:0]				REVERSE_INTEG_A[3:0]					
0x010E	ADC_OFF1_A	[15:8]	Reserved		CH1_ADC_ADJUST_A[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_A[7:0]									
0x010F	ADC_OFF2_A	[15:8]	ZERO_ADJUST_A	Reserved	CH2_ADC_ADJUST_A[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_A[7:0]									
0x0110	DATA_FORMAT_A	[15:8]	DARK_SHIFT_A[4:0]					DARK_SIZE_A[3:0]			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_A[4:0]					SIGNAL_SIZE_A[3:0]				
0x0112	DECIMATE_A	[15:8]	Reserved					DECIMATE_FACTOR_A[6:4]			0x0000	R/W
		[7:0]	DECIMATE_FACTOR_A[3:0]				DECIMATE_TYPE_A[3:0]					
0x0113	DIGINT_LIT_A	[15:8]	Reserved							LIT_OFFSET_A[8]	0x0026	R/W
		[7:0]	LIT_OFFSET_A[7:0]									
0x0114	DIGINT_DARK_A	[15:8]	DARK2_OFFSET_A[8:1]								0x2306	R/W
		[7:0]	DARK2_OFFSET_A[0]	DARK1_OFFSET_A[6:0]								
0x0115	THRESH_CFG_A	[15:8]	Reserved								0x0000	R/W
		[7:0]	THRESH1_CHAN_A	THRESH1_DIR_A	THRESH1_TYPE_A[1:0]		THRESH0_CHAN_A	THRESH0_DIR_A	THRESH0_TYPE_A[1:0]			
0x0116	THRESH0_A	[15:8]	Reserved			THRESH0_SHIFT_A[4:0]					0x0000	R/W
		[7:0]	THRESH0_VALUE_A[7:0]									
0x0117	THRESH1_A	[15:8]	Reserved			THRESH1_SHIFT_A[4:0]					0x0000	R/W
		[7:0]	THRESH1_VALUE_A[7:0]									
0x0120	TS_CTRL_B	[15:8]	SUB SAMPLE_B	CH2_EN_B	SAMPLE_TYPE_B[1:0]		INPUT_R_SELECT_B[1:0]		TIMESLOT_OFFSET_B[9:8]		0x0000	R/W
		[7:0]	TIMESLOT_OFFSET_B[7:0]									
0x0121	TS_PATH_B	[15:8]	PRE_WIDTH_B[3:0]				Reserved		TS_GPIO_B	AFE_PATH_CFG_B[8]	0x40DA	R/W
		[7:0]	AFE_PATH_CFG_B[7:0]									
0x0122	INPUTS_B	[15:8]	INP78_B[3:0]				Reserved				0x0000	R/W
		[7:0]	Reserved				INP12_B[3:0]					

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	**Name**	**Bits**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset**	**R/W**
0x0123	CATHODE_B	[15:8]	Reserved	PRECON_B[2:0]			VC2_PULSE_B[1:0]		VC2_ALT_B[1:0]		0x0000	R/W
		[7:0]	VC2_SEL_B[1:0]		VC1_PULSE_B[1:0]		VC1_ALT_B[1:0]		VC1_SEL_B[1:0]			
0x0124	AFE_TRIM_B	[15:8]	Reserved	CH2_TRIM_INT_B[1:0]		CH2_TRIM_INT_B[1:0]		VREF_ PULSE_B	AFE_TRIM_ VREF_B[1:0]		0x03C0	R/W
		[7:0]	VREF_PULSE_VAL_B[1:0]		TIA_GAIN_CH2_B[2:0]			TIA_GAIN_CH1_B[2:0]				
0x0125	LED_ POW12_B	[15:8]	LED_ DRIVESIDE2 _B	LED_CURRENT2_B[6:0]							0x0000	R/W
		[7:0]	LED_ DRIVESIDE1 _B	LED_CURRENT1_B[6:0]								
0x0126	LED_ POW34_B	[15:8]	LED_ DRIVESIDE4 _B	LED_CURRENT4_B[6:0]							0x0000	R/W
		[7:0]	LED_ DRIVESIDE3 _B	LED_CURRENT3_B[6:0]								
0x0127	COUNTS_B	[15:8]	NUM_INT_B[7:0]								0x0101	R/W
		[7:0]	NUM_REPEAT_B[7:0]									
0x0128	PERIOD_B	[15:8]	Reserved		MOD_TYPE_B[1:0]		Reserved		MIN_PERIOD_B[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_B[7:0]									
0x0129	LED_ PULSE_B	[15:8]	LED_WIDTH_B[7:0]								0x0210	R/W
		[7:0]	LED_OFFSET_B[7:0]									
0x012A	INTEG_ SETUP_B	[15:8]	SINGLE_ INTEG_B	CH2_AMP_DISABLE_B[2:0]			AFE_INT_C _BUF_B	CH1_AMP_DISABLE_B[2:0]			0x0003	R/W
		[7:0]	ADC_COUNT_B[1:0]		Reserved	INTEG_WIDTH_B[4:0]						
0x012B	INTEG_OS_ B	[15:8]	Reserved			INTEG_ OFFSET_B[12:8]					0x0214	R/W
		[7:0]	INTEG_OFFSET_B[7:0]									
0x012C	MOD_ PULSE_B	[15:8]	MOD_WIDTH_B[7:0]								0x0001	R/W
		[7:0]	MOD_OFFSET_B[7:0]									
0x012D	PATTERN_B	[15:8]	LED_DISABLE_B[3:0]				MOD_DISABLE_B[3:0]				0x0000	R/W
		[7:0]	SUBTRACT_B[3:0]				REVERSE_INTEG_B[3:0]					
0x012E	ADC_OFF1_ B	[15:8]	Reserved		CH1_ADC_ADJUST_B[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_B[7:0]									
0x012F	ADC_OFF2_ B	[15:8]	ZERO_ ADJUST_B	Reserved	CH2_ADC_ADJUST_B[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_B[7:0]									
0x0130	DATA_ FORMAT_B	[15:8]	DARK_SHIFT_B[4:0]					DARK_SIZE_B[2:0]			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_B[4:0]					SIGNAL_SIZE_B[2:0]				
0x0132	DECIMATE_ B	[15:8]	Reserved					DECIMATE_FACTOR_B[6:4]			0x0000	R/W
		[7:0]	DECIMATE_FACTOR_B[3:0]				DECIMATE_TYPE_B[3:0]					

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	**Name**	**Bits**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset**	**R/W**
0x0133	DIGINT_LIT_B	[15:8]	Reserved							LIT_OFFSET_B[8]	0x0026	R/W
		[7:0]	LIT_OFFSET_B[7:0]									
0x0134	DIGINT_DARK_B	[15:8]	DARK2_OFFSET_B[8:1]								0x2306	R/W
		[7:0]	DARK2_OFFSET_B[0]	DARK1_OFFSET_B[6:0]								
0x0135	THRESH_CFG_B	[15:8]	Reserved								0x0000	R/W
		[7:0]	THRESH1_CHAN_B	THRESH1_DIR_B	THRESH1_TYPE_B[1:0]		THRESH0_CHAN_B	THRESH0_DIR_B	THRESH0_TYPE_B[1:0]			
0x0136	THRESH0_B	[15:8]	Reserved			THRESH0_SHIFT_B[4:0]					0x0000	R/W
		[7:0]	THRESH0_VALUE_B[7:0]									
0x0137	THRESH1_B	[15:8]	Reserved			THRESH1_SHIFT_B[4:0]					0x0000	R/W
		[7:0]	THRESH1_VALUE_B[7:0]									
0x0140	TS_CTRL_C	[15:8]	SUB SAMPLE_C	CH2_EN_C	SAMPLE_TYPE_C[1:0]		INPUT_R_SELECT_C[1:0]		TIMESLOT_OFFSET_C[9:8]		0x0000	R/W
		[7:0]	TIMESLOT_OFFSET_C[7:0]									
0x0141	TS_PATH_C	[15:8]	PRE_WIDTH_C[3:0]				Reserved		TS_GPIO_C	AFE_PATH_CFG_C[8]	0x40DA	R/W
		[7:0]	AFE_PATH_CFG_C[7:0]									
0x0142	INPUTS_C	[15:8]	INP78_C[3:0]				Reserved				0x0000	R/W
		[7:0]	Reserved				INP12_C[3:0]					
0x0143	CATHODE_C	[15:8]	Reserved	PRECON_C[2:0]			VC2_PULSE_C[1:0]		VC2_ALT_C[1:0]		0x0000	R/W
		[7:0]	VC2_SEL_C[1:0]		VC1_PULSE_C[1:0]		VC1_ALT_C[1:0]		VC1_SEL_C[1:0]			
0x0144	AFE_TRIM_C	[15:8]	Reserved	CH2_TRIM_INT_C[1:0]		CH1_TRIM_INT_C[1:0]		VREF_PULSE_C	AFE_TRIM_VREF_C[1:0]		0x03C0	R/W
		[7:0]	VREF_PULSE_VAL_C[1:0]		TIA_GAIN_CH2_C[2:0]			TIA_GAIN_CH1_C[2:0]				
0x0145	LED_POW12_C	[15:8]	LED_DRIVESIDE2_C	LED_CURRENT2_C[6:0]							0x0000	R/W
		[7:0]	LED_DRIVESIDE1_C	LED_CURRENT1_C[6:0]								
0x0146	LED_POW34_C	[15:8]	LED_DRIVESIDE4_C	LED_CURRENT4_C[6:0]							0x0000	R/W
		[7:0]	LED_DRIVESIDE3_C	LED_CURRENT3_C[6:0]								
0x0147	COUNTS_C	[15:8]	NUM_INT_C[7:0]								0x0101	R/W
		[7:0]	NUM_REPEAT_C[7:0]									
0x0148	PERIOD_C	[15:8]	Reserved		MOD_TYPE_C[1:0]		Reserved		MIN_PERIOD_C[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_C[7:0]									
0x0149	LED_PULSE_C	[15:8]	LED_WIDTH_C[7:0]								0x0210	R/W

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	**Name**	**Bits**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset**	**R/W**
		[7:0]	LED_OFFSET_C[7:0]									
0x014A	INTEG_SETUP_C	[15:8]	SINGLE_INTEG_C	CH2_AMP_DISABLE_C[2:0]			AFE_INT_C_BUF_C	CH1_AMP_DISABLE_C[2:0]			0x0003	R/W
		[7:0]	ADC_COUNT_C[1:0]		Reserved	INTEG_WIDTH_C[4:0]						
0x014B	INTEG_OS_C	[15:8]	Reserved			INTEG_OFFSET_C[12:8]					0x0214	R/W
		[7:0]	INTEG_OFFSET_C[7:0]									
0x014C	MOD_PULSE_C	[15:8]	MOD_WIDTH_C[7:0]								0x0001	R/W
		[7:0]	MOD_OFFSET_C[7:0]									
0x014D	PATTERN_C	[15:8]	LED_DISABLE_C[3:0]				MOD_DISABLE_C[3:0]				0x0000	R/W
		[7:0]	SUBTRACT_C[3:0]				REVERSE_INTEG_C[3:0]					
0x014E	ADC_OFF1_C	[15:8]	Reserved		CH1_ADC_ADJUST_C[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_C[7:0]									
0x014F	ADC_OFF2_C	[15:8]	ZERO_ADJUST_C	Reserved	CH2_ADC_ADJUST_C[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_C[7:0]									
0x0150	DATA_FORMAT_C	[15:8]	DARK_SHIFT_C[4:0]					DARK_SIZE_C[2:0]			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_C[4:0]					SIGNAL_SIZE_C[2:0]				
0x0152	DECIMATE_C	[15:8]	Reserved					DECIMATE_FACTOR_C[6:4]			0x0000	R/W
		[7:0]	DECIMATE_FACTOR_C[3:0]				DECIMATE_TYPE_C[3:0]					
0x0153	DIGINT_LIT_C	[15:8]	Reserved							LIT_OFFSET_C[8]	0x0026	R/W
		[7:0]	LIT_OFFSET_C[7:0]									
0x0154	DIGINT_DARK_C	[15:8]	DARK2_OFFSET_C[8:1]								0x2306	R/W
		[7:0]	DARK2_OFFSET_C[0]	DARK1_OFFSET_C[6:0]								
0x0155	THRESH_CFG_C	[15:8]	Reserved								0x0000	R/W
		[7:0]	THRESH1_CHAN_C	THRESH1_DIR_C	THRESH1_TYPE_C[1:0]		THRESH0_CHAN_C	THRESH0_DIR_C	THRESH0_TYPE_C[1:0]			
0x0156	THRESH0_C	[15:8]	Reserved			THRESH0_SHIFT_C[4:0]					0x0000	R/W
		[7:0]	THRESH0_VALUE_C[7:0]									
0x0157	THRESH1_C	[15:8]	Reserved			THRESH1_SHIFT_C[4:0]					0x0000	R/W
		[7:0]	THRESH1_VALUE_C[7:0]									
0x0160	TS_CTRL_D	[15:8]	SUB SAMPLE_D	CH2_EN_D	SAMPLE_TYPE_D[1:0]		INPUT_R_SELECT_D[1:0]		TIMESLOT_OFFSET_D[9:8]		0x0000	R/W
		[7:0]	TIMESLOT_OFFSET_D[7:0]									
0x0161	TS_PATH_D	[15:8]	PRE_WIDTH_D[3:0]				Reserved		TS_GPIO_D	AFE_PATH_CFG_D[8]	0x40DA	R/W
		[7:0]	AFE_PATH_CFG_D[7:0]									
0x0162	INPUTS_D	[15:8]	INP78_D[3:0]				Reserved				0x0000	R/W

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	**Name**	**Bits**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset**	**R/W**
		[7:0]	Reserved				INP12_D[3:0]					
0x0163	CATHODE_D	[15:8]	Reserved	PRECON_D[2:0]			VC2_PULSE_D[1:0]		VC2_ALT_D[1:0]		0x0000	R/W
		[7:0]	VC2_SEL_D[1:0]		VC1_PULSE_D[1:0]		VC1_ALT_D[1:0]		VC1_SEL_D[1:0]			
0x0164	AFE_TRIM_D	[15:8]	Reserved	CH2_TRIM_INT_D[1:0]		CH1_TRIM_INT_D[1:0]		VREF_ PULSE_D	AFE_TRIM_VREF_ D[1:0]		0x03C0	R/W
		[7:0]	VREF_PULSE_VAL_D[1:0]		TIA_GAIN_CH2_D[2:0]			TIA_GAIN_CH1_D[2:0]				
0x0165	LED_ POW12_D	[15:8]	LED_ DRIVESIDE2 _D	LED_CURRENT2_D[6:0]							0x0000	R/W
		[7:0]	LED_ DRIVESIDE1 _D	LED_CURRENT1_D[6:0]								
0x0166	LED_ POW34_D	[15:8]	LED_ DRIVESIDE4 _D	LED_CURRENT4_D[6:0]							0x0000	R/W
		[7:0]	LED_ DRIVESIDE3 _D	LED_CURRENT3_D[6:0]								
0x0167	COUNTS_D	[15:8]	NUM_INT_D[7:0]								0x0101	R/W
		[7:0]	NUM_REPEAT_D[7:0]									
0x0168	PERIOD_D	[15:8]	Reserved		MOD_TYPE_D[1:0]		Reserved		MIN_PERIOD_D[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_D[7:0]									
0x0169	LED_ PULSE_D	[15:8]	LED_WIDTH_D[7:0]								0x0210	R/W
		[7:0]	LED_OFFSET_D[7:0]									
0x016A	INTEG_ SETUP_D	[15:8]	SINGLE_ INTEG_D	CH2_AMP_DISABLE_D[2:0]			AFE_INT_C _BUF_D	CH1_AMP_DISABLE_D[2:0]			0x0003	R/W
		[7:0]	ADC_COUNT_D[1:0]		Reserved	INTEG_WIDTH_D[4:0]						
0x016B	INTEG_OS_ D	[15:8]	Reserved			INTEG_ OFFSET_D[12:8]					0x0214	R/W
		[7:0]	INTEG_OFFSET_D[7:0]									
0x016C	MOD_ PULSE_D	[15:8]	MOD_WIDTH_D[7:0]								0x0001	R/W
		[7:0]	MOD_OFFSET_D[7:0]									
0x016D	PATTERN_D	[15:8]	LED_DISABLE_D[3:0]				MOD_DISABLE_D[3:0]				0x0000	R/W
		[7:0]	SUBTRACT_D[3:0]				REVERSE_INTEG_D[3:0]					
0x016E	ADC_OFF1_ D	[15:8]	Reserved		CH1_ADC_ADJUST_D[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_D[7:0]									
0x016F	ADC_OFF2_ D	[15:8]	ZERO_ ADJUST_D	Reserved	CH2_ADC_ADJUST_D[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_D[7:0]									
0x0170	DATA_ FORMAT_D	[15:8]	DARK_SHIFT_D[4:0]					DARK_SIZE_D[2:0]			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_D[4:0]					SIGNAL_SIZE_D[2:0]				
0x0172	DECIMATE_ D	[15:8]	Reserved					DECIMATE_FACTOR_D[6:4]			0x0000	R/W
		[7:0]	DECIMATE_FACTOR_D[3:0]				DECIMATE_TYPE_D[3:0]					

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	**Name**	**Bits**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset**	**R/W**
0x0173	DIGINT_LIT_D	[15:8]	Reserved							LIT_OFFSET_D[8]	0x0026	R/W
		[7:0]	LIT_OFFSET_D[7:0]									
0x0174	DIGINT_DARK_D	[15:8]	DARK2_OFFSET_D[8:1]								0x2306	R/W
		[7:0]	DARK2_OFFSET_D[0]	DARK1_OFFSET_D[6:0]								
0x0175	THRESH_CFG_D	[15:8]	Reserved								0x0000	R/W
		[7:0]	THRESH1_CHAN_D	THRESH1_DIR_D	THRESH1_TYPE_D[1:0]		THRESH0_CHAN_D	THRESH0_DIR_D	THRESH0_TYPE_D[1:0]			
0x0176	THRESH0_D	[15:8]	Reserved			THRESH0_SHIFT_D[4:0]					0x0000	R/W
		[7:0]	THRESH0_VALUE_D[7:0]									
0x0177	THRESH1_D	[15:8]	Reserved			THRESH1_SHIFT_D[4:0]					0x0000	R/W
		[7:0]	THRESH1_VALUE_D[7:0]									
0x0180	TS_CTRL_E	[15:8]	SUB SAMPLE_E	CH2_EN_E	SAMPLE_TYPE_E[1:0]		INPUT_R_SELECT_E[1:0]		TIMESLOT_OFFSET_E[9:8]		0x0000	R/W
		[7:0]	TIMESLOT_OFFSET_E[7:0]									
0x0181	TS_PATH_E	[15:8]	PRE_WIDTH_E[3:0]				Reserved		TS_GPIO_E	AFE_PATH_CFG_E[8]	0x40DA	R/W
		[7:0]	AFE_PATH_CFG_E[7:0]									
0x0182	INPUTS_E	[15:8]	INP78_E[3:0]				Reserved				0x0000	R/W
		[7:0]	Reserved				INP12_E[3:0]					
0x0183	CATHODE_E	[15:8]	Reserved	PRECON_E[2:0]			VC2_PULSE_E[1:0]		VC2_ALT_E[1:0]		0x0000	R/W
		[7:0]	VC2_SEL_E[1:0]		VC1_PULSE_E[1:0]		VC1_ALT_E[1:0]		VC1_SEL_E[1:0]			
0x0184	AFE_TRIM_E	[15:8]	Reserved	CH2_TRIM_INT_E[1:0]		CH1_TRIM_INT_E[1:0]		VREF_PULSE_E	AFE_TRIM_VREF_E[1:0]		0x03C0	R/W
		[7:0]	VREF_PULSE_VAL_E[1:0]		TIA_GAIN_CH2_E[2:0]			TIA_GAIN_CH1_E[2:0]				
0x0185	LED_POW12_E	[15:8]	LED_DRIVESIDE2_E	LED_CURRENT2_E[6:0]							0x0000	R/W
		[7:0]	LED_DRIVESIDE1_E	LED_CURRENT1_E[6:0]								
0x0186	LED_POW34_E	[15:8]	LED_DRIVESIDE4_E	LED_CURRENT4_E[6:0]							0x0000	R/W
		[7:0]	LED_DRIVESIDE3_E	LED_CURRENT3_E[6:0]								
0x0187	COUNTS_E	[15:8]	NUM_INT_E[7:0]								0x0101	R/W
		[7:0]	NUM_REPEAT_E[7:0]									
0x0188	PERIOD_E	[15:8]	Reserved		MOD_TYPE_E[1:0]		Reserved		MIN_PERIOD_E[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_E[7:0]									

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	**Name**	**Bits**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset**	**R/W**
0x0189	LED_PULSE_E	[15:8]	LED_WIDTH_E[7:0]								0x0210	R/W
		[7:0]	LED_OFFSET_E[7:0]									
0x018A	INTEG_SETUP_E	[15:8]	SINGLE_INTEG_E	CH2_AMP_DISABLE_E[2:0]			AFE_INT_C_BUF_E	CH1_AMP_DISABLE_E[2:0]			0x0003	R/W
		[7:0]	ADC_COUNT_E[1:0]		Reserved	INTEG_WIDTH_E[4:0]						
0x018B	INTEG_OS_E	[15:8]	Reserved			INTEG_ OFFSET_E[12:8]					0x0214	R/W
		[7:0]	INTEG_OFFSET_E[7:0]									
0x018C	MOD_PULSE_E	[15:8]	MOD_WIDTH_E[7:0]								0x0001	R/W
		[7:0]	MOD_OFFSET_E[7:0]									
0x018D	PATTERN_E	[15:8]	LED_DISABLE_E[3:0]				MOD_DISABLE_E[3:0]				0x0000	R/W
		[7:0]	SUBTRACT_E[3:0]				REVERSE_INTEG_E[3:0]					
0x018E	ADC_OFF1_E	[15:8]	Reserved		CH1_ADC_ADJUST_E[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_E[7:0]									
0x018F	ADC_OFF2_E	[15:8]	ZERO_ADJUST_E	Reserved	CH2_ADC_ADJUST_E[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_E[7:0]									
0x0190	DATA_FORMAT_E	[15:8]	DARK_SHIFT_E[4:0]					DARK_SIZE_E[2:0]			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_E[4:0]					SIGNAL_SIZE_E[2:0]				
0x0192	DECIMATE_E	[15:8]	Reserved					DECIMATE_FACTOR_E[6:4]			0x0000	R/W
		[7:0]	DECIMATE_FACTOR_E[3:0]				DECIMATE_TYPE_E[3:0]					
0x0193	DIGINT_LIT_E	[15:8]	Reserved							LIT_OFFSET_E[8]	0x0026	R/W
		[7:0]	LIT_OFFSET_E[7:0]									
0x0194	DIGINT_DARK_E	[15:8]	DARK2_OFFSET_E[8:1]								0x2306	R/W
		[7:0]	DARK2_OFFSET_E[0]	DARK1_OFFSET_E[6:0]								
0x0195	THRESH_CFG_E	[15:8]	Reserved								0x0000	R/W
		[7:0]	THRESH1_CHAN_E	THRESH1_DIR_E	THRESH1_TYPE_E[1:0]		THRESH0_CHAN_E	THRESH0_DIR_E	THRESH0_TYPE_E[1:0]			
0x0196	THRESH0_E	[15:8]	Reserved			THRESH0_SHIFT_E[4:0]					0x0000	R/W
		[7:0]	THRESH0_VALUE_E[7:0]									
0x0197	THRESH1_E	[15:8]	Reserved			THRESH1_SHIFT_E[4:0]					0x0000	R/W
		[7:0]	THRESH1_VALUE_E[7:0]									
0x01A0	TS_CTRL_F	[15:8]	SUB SAMPLE_F	CH2_EN_F	SAMPLE_TYPE_F[1:0]		INPUT_R_SELECT_F[1:0]		TIMESLOT_OFFSET_F[9:8]		0x0000	R/W
		[7:0]	TIMESLOT_OFFSET_F[7:0]									
0x01A1	TS_PATH_F	[15:8]	PRE_WIDTH_F[3:0]				Reserved		TS_GPIO_F	AFE_PATH_CFG_F[8]	0x40DA	R/W

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	**Name**	**Bits**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset**	**R/W**
		[7:0]	AFE_PATH_CFG_F[7:0]									
0x01A2	INPUTS_F	[15:8]	INP78_F[3:0]				Reserved				0x0000	R/W
		[7:0]	Reserved				INP12_F[3:0]					
0x01A3	CATHODE_F	[15:8]	Reserved	PRECON_F[2:0]			VC2_PULSE_F[1:0]		VC2_ALT_F[1:0]		0x0000	R/W
		[7:0]	VC2_SEL_F[1:0]		VC1_PULSE_F[1:0]		VC1_ALT_F[1:0]		VC1_SEL_F[1:0]			
0x01A4	AFE_TRIM_F	[15:8]	Reserved	CH2_TRIM_INT_F[1:0]		CH1_TRIM_INT_F[1:0]		VREF_PULSE_F	AFE_TRIM_VREF_F[1:0]		0x03C0	R/W
		[7:0]	VREF_PULSE_VAL_F[1:0]		TIA_GAIN_CH2_F[2:0]			TIA_GAIN_CH1_F[2:0]				
0x01A5	LED_POW12_F	[15:8]	LED_DRIVESIDE2_F	LED_CURRENT2_F[6:0]							0x0000	R/W
		[7:0]	LED_DRIVESIDE1_F	LED_CURRENT1_F[6:0]								
0x01A6	LED_POW34_F	[15:8]	LED_DRIVESIDE4_F	LED_CURRENT4_F[6:0]							0x0000	R/W
		[7:0]	LED_DRIVESIDE3_F	LED_CURRENT3_F[6:0]								
0x01A7	COUNTS_F	[15:8]	NUM_INT_F[7:0]								0x0101	R/W
		[7:0]	NUM_REPEAT_F[7:0]									
0x01A8	PERIOD_F	[15:8]	Reserved		MOD_TYPE_F[1:0]		Reserved		MIN_PERIOD_F[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_F[7:0]									
0x01A9	LED_PULSE_F	[15:8]	LED_WIDTH_F[7:0]								0x0210	R/W
		[7:0]	LED_OFFSET_F[7:0]									
0x01AA	INTEG_SETUP_F	[15:8]	SINGLE_INTEG_F	CH2_AMP_DISABLE_F[2:0]			AFE_INT_C_BUF_F	CH1_AMP_DISABLE_F[2:0]			0x0003	R/W
		[7:0]	ADC_COUNT_F[1:0]		Reserved		INTEG_WIDTH_F[4:0]					
0x01AB	INTEG_OS_F	[15:8]	Reserved			INTEG_ OFFSET_F[12:8]					0x0214	R/W
		[7:0]	INTEG_OFFSET_F[7:0]									
0x01AC	MOD_PULSE_F	[15:8]	MOD_WIDTH_F[7:0]								0x0001	R/W
		[7:0]	MOD_OFFSET_F[7:0]									
0x01AD	PATTERN_F	[15:8]	LED_DISABLE_F[3:0]				MOD_DISABLE_F[3:0]				0x0000	R/W
		[7:0]	SUBTRACT_F[3:0]				REVERSE_INTEG_F[3:0]					
0x01AE	ADC_OFF1_F	[15:8]	Reserved		CH1_ADC_ADJUST_F[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_F[7:0]									
0x01AF	ADC_OFF2_F	[15:8]	ZERO_ADJUST_F	Reserved	CH2_ADC_ADJUST_F[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_F[7:0]									
0x01B0	DATA_FORMAT_F	[15:8]	DARK_SHIFT_F[4:0]					DARK_SIZE_F[2:0]			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_F[4:0]					SIGNAL_SIZE_F[2:0]				

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	**Name**	**Bits**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset**	**R/W**
0x01B2	DECIMATE_F	[15:8]	Reserved					DECIMATE_FACTOR_F[6:4]			0x0000	R/W
		[7:0]	DECIMATE_FACTOR_F[3:0]				DECIMATE_TYPE_F[3:0]					
0x01B3	DIGINT_LIT_F	[15:8]	Reserved							LIT_OFFSET_F[8]	0x0026	R/W
		[7:0]	LIT_OFFSET_F[7:0]									
0x01B4	DIGINT_DARK_F	[15:8]	DARK2_OFFSET_F[8:1]								0x2306	R/W
		[7:0]	DARK2_OFFSET_F[0]	DARK1_OFFSET_F[6:0]								
0x01B5	THRESH_CFG_F	[15:8]	Reserved								0x0000	R/W
		[7:0]	THRESH1_CHAN_F	THRESH1_DIR_F	THRESH1_TYPE_F[1:0]		THRESH0_CHAN_F	THRESH0_DIR_F	THRESH0_TYPE_F[1:0]			
0x01B6	THRESH0_F	[15:8]	Reserved			THRESH0_SHIFT_F[4:0]					0x0000	R/W
		[7:0]	THRESH0_VALUE_F[7:0]									
0x01B7	THRESH1_F	[15:8]	Reserved			THRESH1_SHIFT_F[4:0]					0x0000	R/W
		[7:0]	THRESH1_VALUE_F[7:0]									
0x01C0	TS_CTRL_G	[15:8]	SUB SAMPLE_G	CH2_EN_G	SAMPLE_TYPE_G[1:0]		INPUT_R_SELECT_G[1:0]		TIMESLOT_OFFSET_G[9:8]		0x0000	R/W
		[7:0]	TIMESLOT_OFFSET_G[7:0]									
0x01C1	TS_PATH_G	[15:8]	PRE_WIDTH_G[3:0]				Reserved		TS_GPIO_G	AFE_PATH_CFG_G[8]	0x40DA	R/W
		[7:0]	AFE_PATH_CFG_G[7:0]									
0x01C2	INPUTS_G	[15:8]	INP78_G[3:0]				Reserved				0x0000	R/W
		[7:0]	Reserved				INP12_G[3:0]					
0x01C3	CATHODE_G	[15:8]	Reserved	PRECON_G[2:0]			VC2_PULSE_G[1:0]		VC2_ALT_G[1:0]		0x0000	R/W
		[7:0]	VC2_SEL_G[1:0]		VC1_PULSE_G[1:0]		VC1_ALT_G[1:0]		VC1_SEL_G[1:0]			
0x01C4	AFE_TRIM_G	[15:8]	Reserved	CH2_TRIM_INT_G[1:0]		CH1_TRIM_INT_G[1:0]		VREF_PULSE_G	AFE_TRIM_VREF_G[1:0]		0x03C0	R/W
		[7:0]	VREF_PULSE_VAL_G[1:0]		TIA_GAIN_CH2_G[2:0]			TIA_GAIN_CH1_G[2:0]				
0x01C5	LED_POW12_G	[15:8]	LED_DRIVESIDE2_G	LED_CURRENT2_G[6:0]							0x0000	R/W
		[7:0]	LED_DRIVESIDE1_G	LED_CURRENT1_G[6:0]								
0x01C6	LED_POW34_G	[15:8]	LED_DRIVESIDE4_G	LED_CURRENT4_G[6:0]							0x0000	R/W
		[7:0]	LED_DRIVESIDE3_G	LED_CURRENT3_G[6:0]								
0x01C7	COUNTS_G	[15:8]	NUM_INT_G[7:0]								0x0101	R/W
		[7:0]	NUM_REPEAT_G[7:0]									
0x01C8	PERIOD_G	[15:8]	Reserved		MOD_TYPE_G[1:0]		Reserved		MIN_PERIOD_G[9:8]		0x0000	R/W

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	**Name**	**Bits**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset**	**R/W**
		[7:0]	MIN_PERIOD_G[7:0]									
0x01C9	LED_PULSE_G	[15:8]	LED_WIDTH_G[7:0]								0x0210	R/W
		[7:0]	LED_OFFSET_G[7:0]									
0x01CA	INTEG_SETUP_G	[15:8]	SINGLE_INTEG_G	CH2_AMP_DISABLE_G[2:0]			AFE_INT_C_BUF_G	CH1_AMP_DISABLE_G[2:0]			0x0003	R/W
		[7:0]	ADC_COUNT_G[1:0]		Reserved	INTEG_WIDTH_G[4:0]						
0x01CB	INTEG_OS_G	[15:8]	Reserved			INTEG_ OFFSET_G[12:8]					0x0214	R/W
		[7:0]	INTEG_OFFSET_G[7:0]									
0x01CC	MOD_PULSE_G	[15:8]	MOD_WIDTH_G[7:0]								0x0001	R/W
		[7:0]	MOD_OFFSET_G[7:0]									
0x01CD	PATTERN_G	[15:8]	LED_DISABLE_G[3:0]				MOD_DISABLE_G[3:0]				0x0000	R/W
		[7:0]	SUBTRACT_G[3:0]				REVERSE_INTEG_G[3:0]					
0x01CE	ADC_OFF1_G	[15:8]	Reserved		CH1_ADC_ADJUST_G[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_G[7:0]									
0x01CF	ADC_OFF2_G	[15:8]	ZERO_ADJUST_G	Reserved	CH2_ADC_ADJUST_G[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_G[7:0]									
0x01D0	DATA_FORMAT_G	[15:8]	DARK_SHIFT_G[4:0]					DARK_SIZE_G[2:0]			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_G[4:0]					SIGNAL_SIZE_G[2:0]				
0x01D2	DECIMATE_G	[15:8]	Reserved					DECIMATE_FACTOR_G[6:4]			0x0000	R/W
		[7:0]	DECIMATE_FACTOR_G[3:0]				DECIMATE_TYPE_G[3:0]					
0x01D3	DIGINT_LIT_G	[15:8]	Reserved							LIT_OFFSET_G[8]	0x0026	R/W
		[7:0]	LIT_OFFSET_G[7:0]									
0x01D4	DIGINT_DARK_G	[15:8]	DARK2_OFFSET_G[8:1]								0x2306	R/W
		[7:0]	DARK2_OFFSET_G[0]	DARK1_OFFSET_G[6:0]								
0x01D5	THRESH_CFG_G	[15:8]	Reserved								0x0000	R/W
		[7:0]	THRESH1_CHAN_G	THRESH1_DIR_G	THRESH1_TYPE_G[1:0]		THRESH0_CHAN_G	THRESH0_DIR_G	THRESH0_TYPE_G[1:0]			
0x01D6	THRESH0_G	[15:8]	Reserved			THRESH0_SHIFT_G[4:0]					0x0000	R/W
		[7:0]	THRESH0_VALUE_G[7:0]									
0x01D7	THRESH1_G	[15:8]	Reserved			THRESH1_SHIFT_G[4:0]					0x0000	R/W
		[7:0]	THRESH1_VALUE_G[7:0]									
0x01E0	TS_CTRL_H	[15:8]	SUB SAMPLE_H	CH2_EN_H	SAMPLE_TYPE_H[1:0]		INPUT_R_SELECT_H[1:0]		TIMESLOT_OFFSET_H[9:8]		0x0000	R/W
		[7:0]	TIMESLOT_OFFSET_H[7:0]									

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	**Name**	**Bits**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset**	**R/W**
0x01E1	TS_PATH_H	[15:8]	PRE_WIDTH_H[3:0]				Reserved		TS_GPIO_H	AFE_PATH_CFG_H[8]	0x40DA	R/W
		[7:0]	AFE_PATH_CFG_H[7:0]									
0x01E2	INPUTS_H	[15:8]	INP78_H[3:0]				Reserved				0x0000	R/W
		[7:0]	Reserved				INP12_H[3:0]					
0x01E3	CATHODE_H	[15:8]	Reserved	PRECON_H[2:0]			VC2_PULSE_H[1:0]		VC2_ALT_H[1:0]		0x0000	R/W
		[7:0]	VC2_SEL_H[1:0]		VC1_PULSE_H[1:0]		VC1_ALT_H[1:0]		VC1_SEL_H[1:0]			
0x01E4	AFE_TRIM_H	[15:8]	Reserved	CH2_TRIM_INT_H[1:0]		CH1_TRIM_INT_H[1:0]		VREF_PULSE_H	AFE_TRIM_VREF_H[1:0]		0x03C0	R/W
		[7:0]	VREF_PULSE_VAL_H[1:0]		TIA_GAIN_CH2_H[2:0]			TIA_GAIN_CH1_H[2:0]				
0x01E5	LED_POW12_H	[15:8]	LED_DRIVESIDE2_H	LED_CURRENT2_H[6:0]							0x0000	R/W
		[7:0]	LED_DRIVESIDE1_H	LED_CURRENT1_H[6:0]								
0x01E6	LED_POW34_H	[15:8]	LED_DRIVESIDE4_H	LED_CURRENT4_H[6:0]							0x0000	R/W
		[7:0]	LED_DRIVESIDE3_H	LED_CURRENT3_H[6:0]								
0x01E7	COUNTS_H	[15:8]	NUM_INT_H[7:0]								0x0101	R/W
		[7:0]	NUM_REPEAT_H[7:0]									
0x01E8	PERIOD_H	[15:8]	Reserved		MOD_TYPE_H[1:0]		Reserved		MIN_PERIOD_H[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_H[7:0]									
0x01E9	LED_PULSE_H	[15:8]	LED_WIDTH_H[7:0]								0x0210	R/W
		[7:0]	LED_OFFSET_H[7:0]									
0x01EA	INTEG_SETUP_H	[15:8]	SINGLE_INTEG_H	CH2_AMP_DISABLE_H[2:0]			AFE_INT_C_BUF_H	CH1_AMP_DISABLE_H[2:0]			0x0003	R/W
		[7:0]	ADC_COUNT_H[1:0]		Reserved		INTEG_WIDTH_H[4:0]					
0x01EB	INTEG_OS_H	[15:8]	Reserved			INTEG_ OFFSET_H[12:8]					0x0214	R/W
		[7:0]	INTEG_OFFSET_H[7:0]									
0x01EC	MOD_PULSE_H	[15:8]	MOD_WIDTH_H[7:0]								0x0001	R/W
		[7:0]	MOD_OFFSET_H[7:0]									
0x01ED	PATTERN_H	[15:8]	LED_DISABLE_H[3:0]				MOD_DISABLE_H[3:0]				0x0000	R/W
		[7:0]	SUBTRACT_H[3:0]				REVERSE_INTEG_H[3:0]					
0x01EE	ADC_OFF1_H	[15:8]	Reserved		CH1_ADC_ADJUST_H[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_H[7:0]									
0x01EF	ADC_OFF2_H	[15:8]	ZERO_ADJUST_H	Reserved	CH2_ADC_ADJUST_H[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_H[7:0]									
0x01F0	DATA_FORMAT_H	[15:8]	DARK_SHIFT_H[4:0]					DARK_SIZE_H[2:0]			0x0003	R/W

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	**Name**	**Bits**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset**	**R/W**
		[7:0]	SIGNAL_SHIFT_H[4:0]					SIGNAL_SIZE_H[2:0]				
0x01F2	DECIMATE_H	[15:8]	Reserved					DECIMATE_FACTOR_H[6:4]			0x0000	R/W
		[7:0]	DECIMATE_FACTOR_H[3:0]				DECIMATE_TYPE_H[3:0]					
0x01F3	DIGINT_LIT_H	[15:8]	Reserved							LIT_OFFSET_H[8]	0x0026	R/W
		[7:0]	LIT_OFFSET_H[7:0]									
0x01F4	DIGINT_DARK_H	[15:8]	DARK2_OFFSET_H[8:1]								0x2306	R/W
		[7:0]	DARK2_OFFSET_H[0]	DARK1_OFFSET_H[6:0]								
0x01F5	THRESH_CFG_H	[15:8]	Reserved								0x0000	R/W
		[7:0]	THRESH1_CHAN_H	THRESH1_DIR_H	THRESH1_TYPE_H[1:0]		THRESH0_CHAN_H	THRESH0_DIR_H	THRESH0_TYPE_H[1:0]			
0x01F6	THRESH0_H	[15:8]	Reserved			THRESH0_SHIFT_H[4:0]					0x0000	R/W
		[7:0]	THRESH0_VALUE_H[7:0]									
0x01F7	THRESH1_H	[15:8]	Reserved			THRESH1_SHIFT_H[4:0]					0x0000	R/W
		[7:0]	THRESH1_VALUE_H[7:0]									
0x0200	TS_CTRL_I	[15:8]	SUB SAMPLE_I	CH2_EN_I	SAMPLE_TYPE_I[1:0]		INPUT_R_SELECT_I[1:0]		TIMESLOT_OFFSET_I[9:8]		0x0000	R/W
		[7:0]	TIMESLOT_OFFSET_I[7:0]									
0x0201	TS_PATH_I	[15:8]	PRE_WIDTH_I[3:0]				Reserved		TS_GPIO_I	AFE_PATH_CFG_I[8]	0x40DA	R/W
		[7:0]	AFE_PATH_CFG_I[7:0]									
0x0202	INPUTS_I	[15:8]	INP78_I[3:0]				Reserved				0x0000	R/W
		[7:0]	Reserved				INP12_I[3:0]					
0x0203	CATHODE_I	[15:8]	Reserved	PRECON_I[2:0]			VC2_PULSE_I[1:0]		VC2_ALT_I[1:0]		0x0000	R/W
		[7:0]	VC2_SEL_I[1:0]		VC1_PULSE_I[1:0]		VC1_ALT_I[1:0]		VC1_SEL_I[1:0]			
0x0204	AFE_TRIM_I	[15:8]	Reserved	CH2_TRIM_INT_I[1:0]		CH1_TRIM_INT_I[1:0]		VREF_PULSE_I	AFE_TRIM_VREF_I[1:0]		0x03C0	R/W
		[7:0]	VREF_PULSE_VAL_I[1:0]		TIA_GAIN_CH2_I[2:0]			TIA_GAIN_CH1_I[2:0]				
0x0205	LED_POW12_I	[15:8]	LED_DRIVESIDE2_I	LED_CURRENT2_I[6:0]							0x0000	R/W
		[7:0]	LED_DRIVESIDE1_I	LED_CURRENT1_I[6:0]								
0x0206	LED_POW34_I	[15:8]	LED_DRIVESIDE4_I	LED_CURRENT4_I[6:0]							0x0000	R/W
		[7:0]	LED_DRIVESIDE3_I	LED_CURRENT3_I[6:0]								
0x0207	COUNTS_I	[15:8]	NUM_INT_I[7:0]								0x0101	R/W

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	**Name**	**Bits**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset**	**R/W**
		[7:0]	NUM_REPEAT_I[7:0]									
0x0208	PERIOD_I	[15:8]	Reserved		MOD_TYPE_I[1:0]		Reserved		MIN_PERIOD_I[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_I[7:0]									
0x0209	LED_PULSE_I	[15:8]	LED_WIDTH_I[7:0]								0x0210	R/W
		[7:0]	LED_OFFSET_I[7:0]									
0x020A	INTEG_SETUP_I	[15:8]	SINGLE_INTEG_I	CH2_AMP_DISABLE_I[2:0]			AFE_INT_C_BUF_I	CH1_AMP_DISABLE_I[2:0]			0x0003	R/W
		[7:0]	ADC_COUNT_I[1:0]		Reserved	INTEG_WIDTH_I[4:0]						
0x020B	INTEG_OS_I	[15:8]	Reserved			INTEG_ OFFSET_I[12:8]					0x0214	R/W
		[7:0]	INTEG_OFFSET_I[7:0]									
0x020C	MOD_PULSE_I	[15:8]	MOD_WIDTH_I[7:0]								0x0001	R/W
		[7:0]	MOD_OFFSET_I[7:0]									
0x020D	PATTERN_I	[15:8]	LED_DISABLE_I[3:0]				MOD_DISABLE_I[3:0]				0x0000	R/W
		[7:0]	SUBTRACT_I[3:0]				REVERSE_INTEG_I[3:0]					
0x020E	ADC_OFF1_I	[15:8]	Reserved		CH1_ADC_ADJUST_I[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_I[7:0]									
0x020F	ADC_OFF2_I	[15:8]	ZERO_ADJUST_I	Reserved	CH2_ADC_ADJUST_I[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_I[7:0]									
0x0210	DATA_FORMAT_I	[15:8]	DARK_SHIFT_I[4:0]					DARK_SIZE_I[2:0]			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_I[4:0]					SIGNAL_SIZE_I[2:0]				
0x0212	DECIMATE_I	[15:8]	Reserved					DECIMATE_FACTOR_I[6:4]			0x0000	R/W
		[7:0]	DECIMATE_FACTOR_I[3:0]				DECIMATE_TYPE_I[3:0]					
0x0213	DIGINT_LIT_I	[15:8]	Reserved							LIT_OFFSET_I[8]	0x0026	R/W
		[7:0]	LIT_OFFSET_I[7:0]									
0x0214	DIGINT_DARK_I	[15:8]	DARK2_OFFSET_I[8:1]								0x2306	R/W
		[7:0]	DARK2_OFFSET_I[0]	DARK1_OFFSET_I[6:0]								
0x0215	THRESH_CFG_I	[15:8]	Reserved								0x0000	R/W
		[7:0]	THRESH1_CHAN_I	THRESH1_DIR_I	THRESH1_TYPE_I[1:0]		THRESH0_CHAN_I	THRESH0_DIR_I	THRESH0_TYPE_I[1:0]			
0x0216	THRESH0_I	[15:8]	Reserved			THRESH0_SHIFT_I[4:0]					0x0000	R/W
		[7:0]	THRESH0_VALUE_I[7:0]									
0x0217	THRESH1_I	[15:8]	Reserved			THRESH1_SHIFT_I[4:0]					0x0000	R/W
		[7:0]	THRESH1_VALUE_I[7:0]									
0x0220	TS_CTRL_J	[15:8]	SUB SAMPLE_J	CH2_EN_J	SAMPLE_TYPE_J[1:0]		INPUT_R_SELECT_J[1:0]		TIMESLOT_OFFSET_J[9:8]		0x0000	R/W
		[7:0]	TIMESLOT_OFFSET_J[7:0]									
0x0221	TS_PATH_J	[15:8]	PRE_WIDTH_J[3:0]				Reserved		TS_GPIO_J	AFE_PATH_CFG_J[8]	0x40DA	R/W

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	**Name**	**Bits**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset**	**R/W**
		[7:0]	AFE_PATH_CFG_J[7:0]									
0x0222	INPUTS_J	[15:8]	INP78_J[3:0]				Reserved				0x0000	R/W
		[7:0]	Reserved				INP12_J[3:0]					
0x0223	CATHODE_J	[15:8]	Reserved	PRECON_J[2:0]			VC2_PULSE_J[1:0]		VC2_ALT_J[1:0]		0x0000	R/W
		[7:0]	VC2_SEL_J[1:0]		VC1_PULSE_J[1:0]		VC1_ALT_J[1:0]		VC1_SEL_J[1:0]			
0x0224	AFE_TRIM_J	[15:8]	Reserved	CH2_TRIM_INT_J[1:0]		CH1_TRIM_INT_J[1:0]		VREF_PULSE_J	AFE_TRIM_VREF_J[1:0]		0x03C0	R/W
		[7:0]	VREF_PULSE_VAL_J[1:0]		TIA_GAIN_CH2_J[2:0]			TIA_GAIN_CH1_J[2:0]				
0x0225	LED_POW12_J	[15:8]	LED_DRIVESIDE2_J	LED_CURRENT2_J[6:0]							0x0000	R/W
		[7:0]	LED_DRIVESIDE1_J	LED_CURRENT1_J[6:0]								
0x0226	LED_POW34_J	[15:8]	LED_DRIVESIDE4_J	LED_CURRENT4_J[6:0]							0x0000	R/W
		[7:0]	LED_DRIVESIDE3_J	LED_CURRENT3_J[6:0]								
0x0227	COUNTS_J	[15:8]	NUM_INT_J[7:0]								0x0101	R/W
		[7:0]	NUM_REPEAT_J[7:0]									
0x0228	PERIOD_J	[15:8]	Reserved		MOD_TYPE_J[1:0]		Reserved		MIN_PERIOD_J[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_J[7:0]									
0x0229	LED_PULSE_J	[15:8]	LED_WIDTH_J[7:0]								0x0210	R/W
		[7:0]	LED_OFFSET_J[7:0]									
0x022A	INTEG_SETUP_J	[15:8]	SINGLE_INTEG_J	CH2_AMP_DISABLE_J[2:0]			AFE_INT_C_BUF_J	CH1_AMP_DISABLE_J[2:0]			0x0003	R/W
		[7:0]	ADC_COUNT_J[1:0]		Reserved	INTEG_WIDTH_J[4:0]						
0x022B	INTEG_OS_J	[15:8]	Reserved			INTEG_ OFFSET_J[12:8]					0x0214	R/W
		[7:0]	INTEG_OFFSET_J[7:0]									
0x022C	MOD_PULSE_J	[15:8]	MOD_WIDTH_J[7:0]								0x0001	R/W
		[7:0]	MOD_OFFSET_J[7:0]									
0x022D	PATTERN_J	[15:8]	LED_DISABLE_J[3:0]				MOD_DISABLE_J[3:0]				0x0000	R/W
		[7:0]	SUBTRACT_J[3:0]				REVERSE_INTEG_J[3:0]					
0x022E	ADC_OFF1_J	[15:8]	Reserved		CH1_ADC_ADJUST_J[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_J[7:0]									
0x022F	ADC_OFF2_J	[15:8]	ZERO_ADJUST_J	Reserved	CH2_ADC_ADJUST_J[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_J[7:0]									
0x0230	DATA_FORMAT_J	[15:8]	DARK_SHIFT_J[4:0]					DARK_SIZE_J[2:0]			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_J[4:0]					SIGNAL_SIZE_J[2:0]				
0x0232	DECIMATE_J	[15:8]	Reserved					DECIMATE_FACTOR_J[6:4]			0x0000	R/W
		[7:0]	DECIMATE_FACTOR_J[3:0]				DECIMATE_TYPE_J[3:0]					

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	**Name**	**Bits**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset**	**R/W**
0x0233	DIGINT_LIT_J	[15:8]	Reserved							LIT_OFFSET_J[8]	0x0026	R/W
		[7:0]	LIT_OFFSET_J[7:0]									
0x0234	DIGINT_DARK_J	[15:8]	DARK2_OFFSET_J[8:1]								0x2306	R/W
		[7:0]	DARK2_OFFSET_J[0]	DARK1_OFFSET_J[6:0]								
0x0235	THRESH_CFG_J	[15:8]	Reserved								0x0000	R/W
		[7:0]	THRESH1_CHAN_J	THRESH1_DIR_J	THRESH1_TYPE_J[1:0]		THRESH0_CHAN_J	THRESH0_DIR_J	THRESH0_TYPE_J[1:0]			
0x0236	THRESH0_J	[15:8]	Reserved			THRESH0_SHIFT_J[4:0]					0x0000	R/W
		[7:0]	THRESH0_VALUE_J[7:0]									
0x0237	THRESH1_J	[15:8]	Reserved			THRESH1_SHIFT_J[4:0]					0x0000	R/W
		[7:0]	THRESH1_VALUE_J[7:0]									
0x0240	TS_CTRL_K	[15:8]	SUB SAMPLE_K	CH2_EN_K	SAMPLE_TYPE_K[1:0]		INPUT_R_SELECT_K[1:0]		TIMESLOT_OFFSET_K[9:8]		0x0000	R/W
		[7:0]	TIMESLOT_OFFSET_K[7:0]									
0x0241	TS_PATH_K	[15:8]	PRE_WIDTH_K[3:0]				Reserved		TS_GPIO_K	AFE_PATH_CFG_K[8]	0x40DA	R/W
		[7:0]	AFE_PATH_CFG_K[7:0]									
0x0242	INPUTS_K	[15:8]	INP78_K[3:0]				Reserved				0x0000	R/W
		[7:0]	Reserved				INP12_K[3:0]					
0x0243	CATHODE_K	[15:8]	Reserved	PRECON_K[2:0]			VC2_PULSE_K[1:0]		VC2_ALT_K[1:0]		0x0000	R/W
		[7:0]	VC2_SEL_K[1:0]		VC1_PULSE_K[1:0]		VC1_ALT_K[1:0]		VC1_SEL_K[1:0]			
0x0244	AFE_TRIM_K	[15:8]	Reserved	CH2_TRIM_INT_K[1:0]		CH1_TRIM_INT_K[1:0]		VREF_PULSE_K	AFE_TRIM_VREF_K[1:0]		0x03C0	R/W
		[7:0]	VREF_PULSE_VAL_K[1:0]		TIA_GAIN_CH2_K[2:0]			TIA_GAIN_CH1_K[2:0]				
0x0245	LED_POW12_K	[15:8]	LED_DRIVESIDE2_K	LED_CURRENT2_K[6:0]							0x0000	R/W
		[7:0]	LED_DRIVESIDE1_K	LED_CURRENT1_K[6:0]								
0x0246	LED_POW34_K	[15:8]	LED_DRIVESIDE4_K	LED_CURRENT4_K[6:0]							0x0000	R/W
		[7:0]	LED_DRIVESIDE3_K	LED_CURRENT3_K[6:0]								
0x0247	COUNTS_K	[15:8]	NUM_INT_K[7:0]								0x0101	R/W
		[7:0]	NUM_REPEAT_K[7:0]									
0x0248	PERIOD_K	[15:8]	Reserved		MOD_TYPE_K[1:0]		Reserved		MIN_PERIOD_K[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_K[7:0]									
0x0249	LED_PULSE_K	[15:8]	LED_WIDTH_K[7:0]								0x0210	R/W

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	**Name**	**Bits**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset**	**R/W**
		[7:0]	LED_OFFSET_K[7:0]									
0x024A	INTEG_SETUP_K	[15:8]	SINGLE_INTEG_K	CH2_AMP_DISABLE_K[2:0]			AFE_INT_C_BUF_K	CH1_AMP_DISABLE_K[2:0]			0x0003	R/W
		[7:0]	ADC_COUNT_K[1:0]		Reserved		INTEG_WIDTH_K[4:0]					
0x024B	INTEG_OS_K	[15:8]	Reserved			INTEG_ OFFSET_K[12:8]					0x0214	R/W
		[7:0]	INTEG_OFFSET_K[7:0]									
0x024C	MOD_PULSE_K	[15:8]	MOD_WIDTH_K[7:0]								0x0001	R/W
		[7:0]	MOD_OFFSET_K[7:0]									
0x024D	PATTERN_K	[15:8]	LED_DISABLE_K[3:0]				MOD_DISABLE_K[3:0]				0x0000	R/W
		[7:0]	SUBTRACT_K[3:0]				REVERSE_INTEG_K[3:0]					
0x024E	ADC_OFF1_K	[15:8]	Reserved		CH1_ADC_ADJUST_K[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_K[7:0]									
0x024F	ADC_OFF2_K	[15:8]	ZERO_ADJUST_K	Reserved	CH2_ADC_ADJUST_K[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_K[7:0]									
0x0250	DATA_FORMAT_K	[15:8]	DARK_SHIFT_K[4:0]					DARK_SIZE_K[2:0]			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_K[4:0]					SIGNAL_SIZE_K[2:0]				
0x0252	DECIMATE_K	[15:8]	Reserved					DECIMATE_FACTOR_K[6:4]			0x0000	R/W
		[7:0]	DECIMATE_FACTOR_K[3:0]				DECIMATE_TYPE_K[3:0]					
0x0253	DIGINT_LIT_K	[15:8]	Reserved							LIT_OFFSET_K[8]	0x0026	R/W
		[7:0]	LIT_OFFSET_K[7:0]									
0x0254	DIGINT_DARK_K	[15:8]	DARK2_OFFSET_K[8:1]								0x2306	R/W
		[7:0]	DARK2_OFFSET_K[0]	DARK1_OFFSET_K[6:0]								
0x0255	THRESH_CFG_K	[15:8]	Reserved								0x0000	R/W
		[7:0]	THRESH1_CHAN_K	THRESH1_DIR_K	THRESH1_TYPE_K[1:0]		THRESH0_CHAN_K	THRESH0_DIR_K	THRESH0_TYPE_K[1:0]			
0x0256	THRESH0_K	[15:8]	Reserved			THRESH0_SHIFT_K[4:0]					0x0000	R/W
		[7:0]	THRESH0_VALUE_K[7:0]									
0x0257	THRESH1_K	[15:8]	Reserved			THRESH1_SHIFT_K[4:0]					0x0000	R/W
		[7:0]	THRESH1_VALUE_K[7:0]									
0x0260	TS_CTRL_L	[15:8]	SUB SAMPLE_L	CH2_EN_L	SAMPLE_TYPE_L[1:0]		INPUT_R_SELECT_L[1:0]		TIMESLOT_OFFSET_L[9:8]		0x0000	R/W
		[7:0]	TIMESLOT_OFFSET_L[7:0]									
0x0261	TS_PATH_L	[15:8]	PRE_WIDTH_L[3:0]				Reserved		TS_GPIO_L	AFE_PATH_CFG_L[8]	0x40DA	R/W
		[7:0]	AFE_PATH_CFG_L[7:0]									
0x0262	INPUTS_L	[15:8]	INP78_L[3:0]				Reserved				0x0000	R/W

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	**Name**	**Bits**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset**	**R/W**
		[7:0]	Reserved				INP12_L[3:0]					
0x0263	CATHODE_L	[15:8]	Reserved	PRECON_L[2:0]			VC2_PULSE_L[1:0]		VC2_ALT_L[1:0]		0x0000	R/W
		[7:0]	VC2_SEL_L[1:0]		VC1_PULSE_L[1:0]		VC1_ALT_L[1:0]		VC1_SEL_L[1:0]			
0x0264	AFE_TRIM_L	[15:8]	Reserved	CH2_TRIM_INT_L[1:0]		CH1_TRIM_INT_L[1:0]		VREF_ PULSE_L	AFE_TRIM_ VREF_L[1:0]		0x03C0	R/W
		[7:0]	VREF_PULSE_VAL_L[1:0]		TIA_GAIN_CH2_L[2:0]			TIA_GAIN_CH1_L[2:0]				
0x0265	LED_ POW12_L	[15:8]	LED_ DRIVESIDE2 _L	LED_CURRENT2_L[6:0]							0x0000	R/W
		[7:0]	LED_ DRIVESIDE1 _L	LED_CURRENT1_L[6:0]								
0x0266	LED_ POW34_L	[15:8]	LED_ DRIVESIDE4 _L	LED_CURRENT4_L[6:0]							0x0000	R/W
		[7:0]	LED_ DRIVESIDE3 _L	LED_CURRENT3_L[6:0]								
0x0267	COUNTS_L	[15:8]	NUM_INT_L[7:0]								0x0101	R/W
		[7:0]	NUM_REPEAT_L[7:0]									
0x0268	PERIOD_L	[15:8]	Reserved		MOD_TYPE_L[1:0]		Reserved		MIN_PERIOD_L[9:8]		0x0000	R/W
		[7:0]	MIN_PERIOD_L[7:0]									
0x0269	LED_PULSE _L	[15:8]	LED_WIDTH_L[7:0]								0x0210	R/W
		[7:0]	LED_OFFSET_L[7:0]									
0x026A	INTEG_ SETUP_L	[15:8]	SINGLE_ INTEG_L	CH2_AMP_DISABLE_L[2:0]			AFE_INT_C _BUF_L	CH1_AMP_DISABLE_L[2:0]			0x0003	R/W
		[7:0]	ADC_COUNT_L[1:0]		Reserved		INTEG_WIDTH_L[4:0]					
0x026B	INTEG_OS_L	[15:8]	Reserved				INTEG_ OFFSET_L[12:8]				0x0214	R/W
		[7:0]	INTEG_OFFSET_L[7:0]									
0x026C	MOD_ PULSE_L	[15:8]	MOD_WIDTH_L[7:0]								0x0001	R/W
		[7:0]	MOD_OFFSET_L[7:0]									
0x026D	PATTERN_L	[15:8]	LED_DISABLE_L[3:0]				MOD_DISABLE_L[3:0]				0x0000	R/W
		[7:0]	SUBTRACT_L[3:0]				REVERSE_INTEG_L[3:0]					
0x026E	ADC_OFF1_ L	[15:8]	Reserved		CH1_ADC_ADJUST_L[13:8]						0x0000	R/W
		[7:0]	CH1_ADC_ADJUST_L[7:0]									
0x026F	ADC_OFF2_ L	[15:8]	ZERO_ ADJUST_L	Reserved	CH2_ADC_ADJUST_L[13:8]						0x0000	R/W
		[7:0]	CH2_ADC_ADJUST_L[7:0]									
0x0270	DATA_ FORMAT_L	[15:8]	DARK_SHIFT_L[4:0]					DARK_SIZE_L[2:0]			0x0003	R/W
		[7:0]	SIGNAL_SHIFT_L[4:0]					SIGNAL_SIZE_L[2:0]				
0x0272	DECIMATE_L	[15:8]	Reserved					DECIMATE_FACTOR_L[6:4]			0x0000	R/W
		[7:0]	DECIMATE_FACTOR_L[3:0]				DECIMATE_TYPE_L[3:0]					
0x0273	DIGINT_LIT_ L	[15:8]	Reserved							LIT_ OFFSET_ L[8]	0x0026	R/W

REGISTER MAP

Table 25. Register Map Summary

			Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8		
Reg	**Name**	**Bits**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Reset**	**R/W**
		[7:0]	LIT_OFFSET_L[7:0]									
0x0274	DIGINT_DARK_L	[15:8]	DARK2_OFFSET_L[8:1]								0x2306	R/W
		[7:0]	DARK2_OFFSET_L[0]	DARK1_OFFSET_L[6:0]								
0x0275	THRESH_CFG_L	[15:8]	Reserved								0x0000	R/W
		[7:0]	THRESH1_CHAN_L	THRESH1_DIR_L	THRESH1_TYPE_L[1:0]		THRESH0_CHAN_L	THRESH0_DIR_L	THRESH0_TYPE_L[1:0]			
0x0276	THRESH0_L	[15:8]	Reserved			THRESH0_SHIFT_L[4:0]					0x0000	R/W
		[7:0]	THRESH0_VALUE_L[7:0]									
0x0277	THRESH1_L	[15:8]	Reserved			THRESH1_SHIFT_L[4:0]					0x0000	R/W
		[7:0]	THRESH1_VALUE_L[7:0]									

REGISTER DETAILS

GLOBAL CONFIGURATION REGISTERS

Table 26. Global Configuration Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x000D	TS_FREQ	[15:0]	TIMESLOT_PERIOD_L	Lower 16 bits of time slot period in low frequency oscillator cycles. The time slot rate is (low frequency oscillator frequency) ÷ (TIMESLOT_PERIOD_x). The default value operates at 100 Hz when using the 1 MHz low frequency oscillator.	0x2710	R/W
0x000E	TS_FREQH	[15:7]	Reserved	Reserved.	0x0	R
		[6:0]	TIMESLOT_PERIOD_H	Upper seven bits of time slot period in low frequency oscillator cycles. The time slot rate is (low frequency oscillator frequency) ÷ (TIMESLOT_PERIOD_x). The default value operates at 100 Hz when using the 1 MHz low frequency oscillator.	0x0	R/W
0x000F	SYS_CTL	15	SW_RESET	Software Reset. Write 1 to this bit to assert a software reset, which stops all AFE operations and resets the device to its default values. Software reset does not reset the SPI port.	0x0	R/W
		[14:10]	Reserved	Reserved.	0x0	R
		[9:8]	ALT_CLOCKS	External Clock Select. 00: use internal low frequency oscillator and high frequency oscillator. 01: use external low frequency oscillator. 02: use external high frequency oscillator and internal low frequency oscillator. 03: use external high frequency oscillator and generate low frequency oscillator from high frequency oscillator.	0x0	R/W
		[7:6]	ALT_CLK_GPIO	Alternate Clock GPIO Select. 00: use GPIO0 for alternate clock. 01: use GPIO1 for alternate clock.	0x0	R/W
		[5:3]	Reserved	Write 0x0.	0x0	R/W
		2	LFOSC_SEL	Selects low frequency oscillator. This bit selects between the 32 kHz and 1 MHz low speed oscillator. 0: use the 32 kHz oscillator as the low frequency clock. 1: use the 1 MHz oscillator as the low frequency clock.	0x0	R/W
		1	OSC_1M_EN	Enables 1 MHz low frequency oscillator. This bit turns on the 1 MHz low frequency oscillator, which must be left running during all operations while using this oscillator.	0x0	R/W
		0	OSC_32K_EN	Enables 32 kHz low frequency oscillator. This bit turns on the 32 kHz low frequency oscillator, which must be left running during all operations while using this oscillator.	0x0	R/W
0x0010	OPMODE	[15:12]	Reserved	Reserved.	0x0	R
		[11:8]	TIMESLOT_EN	Time Slot Enable Control. 0000: Time Slot Sequence A only. 0001: Time Slot Sequence AB. 0010: Time Slot Sequence ABC. 0011: Time Slot Sequence ABCD. 0100: Time Slot Sequence ABCDE. 0101: Time Slot Sequence ABCDEF. 0110: Time Slot Sequence ABCDEFG. 0111: Time Slot Sequence ABCDEFGH. 1000: Time Slot Sequence ABCDEFGHI. 1001: Time Slot Sequence ABCDEFGHIJ. 1010: Time Slot Sequence ABCDEFGHIJK. 1011: Time Slot Sequence ABCDEFGHIJKL.	0x0	R/W
		[7:1]	Reserved	Reserved.	0x0	R

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Table 26. Global Configuration Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
		0	OP_MODE	Operating Mode Selection. 0: standby. 1: go mode. Operate selected time slots.	0x0	R/W
0x0020	INPUT_SLEEP	[15:12]	INP_SLEEP_78	Input Pair Sleep State for IN7 and IN8 Inputs. 0x0: both inputs float. 0x1: floating short of IN7 to IN8. Only if PAIR78 is set to 1. 0x2: IN7 and IN8 connected to VC1. Also shorted together if PAIR78 is set to 1. 0x3: IN7 and IN8 connected to VC2. Also shorted together if PAIR78 is set to 1. 0x4: IN7 connected to VC1. IN8 floating. 0x5: IN7 connected to VC1. IN8 connected to VC2. 0x6: IN7 connected to VC2. IN8 floating. 0x7: IN7 connected to VC2. IN8 connected to VC1. 0x8: IN7 floating. IN8 connected to VC1. 0x9: IN7 floating. IN8 connected to VC2.	0x0	R/W
		[11:4]	Reserved	Reserved.	0x0	R
		[3:0]	INP_SLEEP_12	Input Pair Sleep State for IN1 and IN2 Inputs. 0x0: both inputs float. 0x1: floating short of IN1 to IN2. Only if PAIR12 is set to 1. 0x2: IN1 and IN2 connected to VC1. Also shorted together if PAIR12 is set to 1. 0x3: IN1 and IN2 connected to VC2. Also shorted together if PAIR12 is set to 1. 0x4: IN1 connected to VC1. IN2 floating. 0x5: IN1 connected to VC1. IN2 connected to VC2. 0x6: IN1 connected to VC2. IN2 floating. 0x7: IN1 connected to VC2. IN2 connected to VC1. 0x8: IN1 floating. IN2 connected to VC1. 0x9: IN1 floating. IN2 connected to VC2.	0x0	R/W
0x0021	INPUT_CFG	[15:8]	Reserved	Reserved.	0x0	R
		[7:6]	VC2_SLEEP	VC2 Sleep State. 0: VC2 set to AVDD during sleep. 1: VC2 set to ground during sleep. 10: VC2 floating during sleep.	0x0	R/W
		[5:4]	VC1_SLEEP	VC1 Sleep State. 0: VC1 set to AVDD during sleep. 1: VC1 set to ground during sleep. 10: VC1 floating during sleep.	0x0	R/W
		3	PAIR78	Input Pair Configuration. 0: IN7 and IN8 configured as two single-ended inputs. 1: IN7 and IN8 configured as a differential pair.	0x0	R/W
		[2:1]	Reserved	Reserved.	0x0	R
		0	PAIR12	Input Pair Configuration. 0: IN1 and IN2 configured as two single-ended inputs. 1: IN1 and IN2 configured as a differential pair.	0x0	R/W

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INTERRUPT STATUS AND CONTROL REGISTERS

Table 27. Interrupt Status and Control Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access[1]
0x0000	FIFO_STATUS	15	CLEAR_FIFO	Clear FIFO. Write a 1 to empty the FIFO while the FIFO is not being accessed, which resets FIFO_BYTE_COUNT and clears the INT_FIFO_OFLOW, INT_FIFO_UFLOW, and INT_FIFO_TH status bits.	0x0	R/W1C
		14	INT_FIFO_UFLOW	FIFO Underflow Error. This bit is set when the FIFO is read while empty. Write 1 to this bit to clear the interrupt. This bit is also cleared if the FIFO is cleared using the CLEAR_FIFO bit.	0x0	R/W1C
		13	INT_FIFO_OFLOW	FIFO Overflow Error. This bit is set when data was not written to the FIFO due to lack of space. Write 1 to this bit to clear the interrupt. This bit is also cleared if the FIFO is cleared with the CLEAR_FIFO bit.	0x0	R/W1C
		[12:11]	Reserved	Reserved.	0x0	R
		[10:0]	FIFO_BYTE_COUNT	This field indicates the number of bytes in the FIFO.	0x0	R
0x0001	INT_STATUS_DATA	15	INT_FIFO_TH	FIFO_TH Interrupt Status. This bit is set during a FIFO write when the number of bytes in the FIFO exceeds the FIFO_TH register value. Write 1 to this bit to clear this interrupt. This bit can also be automatically cleared when the FIFO_DATA register is read if the INT_ACLEAR_FIFO bit is set.	0x0	R/W1C
		[14:12]	Reserved	Reserved.	0x0	R
		11	INT_DATA_L	Time Slot L Data Register Interrupt Status. This bit is set every time the Time Slot L data registers are updated. Write 1 to this bit to clear the interrupt. The interrupt is cleared automatically when the Time Slot L data registers are read if the INT_ACLEAR_DATA_L bit is set.	0x0	R/W1C
		10	INT_DATA_K	Time Slot K Data Register Interrupt Status. This bit is set every time the Time Slot K data registers get updated. Write 1 to this bit to clear the interrupt. The interrupt is cleared automatically when the Time Slot K data registers are read if the INT_ACLEAR_DATA_K bit is set.	0x0	R/W1C
		9	INT_DATA_J	Time Slot J Data Register Interrupt Status. This bit is set every time the Time Slot J data registers are updated. Write 1 to this bit to clear the interrupt. The interrupt is cleared automatically when the Time Slot J data registers are read if the INT_ACLEAR_DATA_J bit is set.	0x0	R/W1C
		8	INT_DATA_I	Time Slot I Data Register Interrupt Status. This bit is set every time the Time Slot I data registers are updated. Write 1 to this bit to clear the interrupt. The interrupt is cleared automatically when the Time Slot I data registers are read if the INT_ACLEAR_DATA_I bit is set.	0x0	R/W1C
		7	INT_DATA_H	Time Slot H Data Register Interrupt Status. This bit is set every time the Time Slot H data registers are updated. Write 1 to this bit to clear the interrupt. The interrupt is cleared automatically when the Time Slot H data registers are read if the INT_ACLEAR_DATA_H bit is set.	0x0	R/W1C
		6	INT_DATA_G	Time Slot G Data Register Interrupt Status. This bit is set every time the Time Slot G data registers are updated. Write 1 to this bit to clear the interrupt. The interrupt is cleared automatically when the Time Slot G data registers are read if the INT_ACLEAR_DATA_G bit is set.	0x0	R/W1C
		5	INT_DATA_F	Time Slot F Data Register Interrupt Status. This bit is set every time the Time Slot F data registers are updated. Write 1 to this bit to clear the interrupt. The interrupt is cleared automatically when the Time Slot F data registers are read if the INT_ACLEAR_DATA_F bit is set.	0x0	R/W1C
		4	INT_DATA_E	Time Slot E Data Register Interrupt Status. This bit is set every time the Time Slot E data registers are updated. Write 1 to this bit to clear the interrupt. The interrupt is cleared automatically when the Time Slot E data registers are read if the INT_ACLEAR_DATA_E bit is set.	0x0	R/W1C

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Table 27. Interrupt Status and Control Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access[1]
		3	INT_DATA_D	Time Slot D Data Register Interrupt Status. This bit is set every time the Time Slot D data registers are updated. Write 1 to this bit to clear the interrupt. The interrupt is cleared automatically when the Time Slot D data registers are read if the INT_ACLEAR_DATA_D bit is set.	0x0	R/W1C
		2	INT_DATA_C	Time Slot C Data Register Interrupt Status. This bit is set every time the Time Slot C data registers are updated. Write 1 to this bit to clear the interrupt. The interrupt is cleared automatically when the Time Slot C data registers are read if the INT_ACLEAR_DATA_C bit is set.	0x0	R/W1C
		1	INT_DATA_B	Time Slot B Data Register Interrupt Status. This bit is set every time the Time Slot B data registers are updated. Write 1 to this bit to clear the interrupt. The interrupt is cleared automatically when the Time Slot B data registers are read if the INT_ACLEAR_DATA_B bit is set.	0x0	R/W1C
		0	INT_DATA_A	Time Slot A Data Register Interrupt Status. This bit is set every time the Time Slot A data registers are updated. Write 1 to this bit to clear the interrupt. The interrupt is cleared automatically when the Time Slot A data registers are read if the INT_ACLEAR_DATA_A bit is set.	0x0	R/W1C
0x0002	INT_STATUS_LEV0	[15:12]	Reserved	Reserved.	0x0	R
		11	INT_LEV0_L	Time Slot L Level 0 Interrupt Status. This bit is set during a data register update when the configured criteria is met.	0x0	R/W1C
		10	INT_LEV0_K	Time Slot K Level 0 Interrupt Status. This bit is set during a data register update when the configured criteria is met.	0x0	R/W1C
		9	INT_LEV0_J	Time Slot J Level 0 Interrupt Status. This bit is set during a data register update when the configured criteria is met.	0x0	R/W1C
		8	INT_LEV0_I	Time Slot I Level 0 Interrupt Status. This bit is set during a data register update when the configured criteria is met.	0x0	R/W1C
		7	INT_LEV0_H	Time Slot H Level 0 Interrupt Status. This bit is set during a data register update when the configured criteria is met.	0x0	R/W1C
		6	INT_LEV0_G	Time Slot G Level 0 Interrupt Status. This bit is set during a data register update when the configured criteria is met.	0x0	R/W1C
		5	INT_LEV0_F	Time Slot F Level 0 Interrupt Status. This bit is set during a data register update when the configured criteria is met.	0x0	R/W1C
		4	INT_LEV0_E	Time Slot E Level 0 Interrupt Status. This bit is set during a data register update when the configured criteria is met.	0x0	R/W1C
		3	INT_LEV0_D	Time Slot D Level 0 Interrupt Status. This bit is set during a data register update when the configured criteria is met.	0x0	R/W1C
		2	INT_LEV0_C	Time Slot C Level 0 Interrupt Status. This bit is set during a data register update when the configured criteria is met.	0x0	R/W1C
		1	INT_LEV0_B	Time Slot B Level 0 Interrupt Status. This bit is set during a data register update when the configured criteria is met.	0x0	R/W1C
		0	INT_LEV0_A	Time Slot A Level 0 Interrupt Status. This bit is set during a data register update when the configured criteria is met.	0x0	R/W1C
0x0003	INT_STATUS_LEV1	[15:12]	Reserved	Reserved.	0x0	R
		11	INT_LEV1_L	Time Slot L Level 1 Interrupt Status. This bit is set during a data register update when the configured criteria is met.	0x0	R/W1C
		10	INT_LEV1_K	Time Slot K Level 1 Interrupt Status. This bit is set during a data register update when the configured criteria is met.	0x0	R/W1C
		9	INT_LEV1_J	Time Slot J Level 1 Interrupt Status. This bit is set during a data register update when the configured criteria is met.	0x0	R/W1C
		8	INT_LEV1_I	Time Slot I Level 1 Interrupt Status. This bit is set during a data register update when the configured criteria is met.	0x0	R/W1C
		7	INT_LEV1_H	Time Slot H Level 1 Interrupt Status. This bit is set during a data register update when the configured criteria is met.	0x0	R/W1C

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Table 27. Interrupt Status and Control Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access[1]
		6	INT_LEV1_G	Time Slot G Level 1 Interrupt Status. This bit is set during a data register update when the configured criteria is met.	0x0	R/W1C
		5	INT_LEV1_F	Time Slot F Level 1 Interrupt Status. This bit is set during a data register update when the configured criteria is met.	0x0	R/W1C
		4	INT_LEV1_E	Time Slot E Level 1 Interrupt Status. This bit is set during a data register update when the configured criteria is met.	0x0	R/W1C
		3	INT_LEV1_D	Time Slot D Level 1 Interrupt Status. This bit is set during a data register update when the configured criteria is met.	0x0	R/W1C
		2	INT_LEV1_C	Time Slot C Level 1 Interrupt Status. This bit is set during a data register update when the configured criteria is met.	0x0	R/W1C
		1	INT_LEV1_B	Time Slot B Level 1 Interrupt Status. This bit is set during a data register update when the configured criteria is met.	0x0	R/W1C
		0	INT_LEV1_A	Time Slot A Level 1 Interrupt Status. This bit is set during a data register update when the configured criteria is met.	0x0	R/W1C
0x0007	INT_ACLEAR	15	INT_ACLEAR_FIFO	FIFO Threshold Interrupt Autoclear Enable. Set this bit to enable automatic clearing of the FIFO_TH interrupt each time the FIFO is read.	0x1	R/W
		[14:12]	Reserved	Reserved.	0x0	R
		11	INT_ACLEAR_DATA_L	Time Slot L Interrupt Autoclear Enable. Set this bit to enable automatic clearing of the INT_DATA_L interrupt each time the Time Slot L data registers are read.	0x1	R/W
		10	INT_ACLEAR_DATA_K	Time Slot K Interrupt Autoclear Enable. Set this bit to enable automatic clearing of the INT_DATA_K interrupt each time the Time Slot K data registers are read.	0x1	R/W
		9	INT_ACLEAR_DATA_J	Time Slot J Interrupt Autoclear Enable. Set this bit to enable automatic clearing of the INT_DATA_J interrupt each time the Time Slot J data registers are read.	0x1	R/W
		8	INT_ACLEAR_DATA_I	Time Slot I Interrupt Autoclear Enable. Set this bit to enable automatic clearing of the INT_DATA_I interrupt each time the Time Slot I data registers are read.	0x1	R/W
		7	INT_ACLEAR_DATA_H	Time Slot H Interrupt Autoclear Enable. Set this bit to enable automatic clearing of the INT_DATA_H interrupt each time the Time Slot H data registers are read.	0x1	R/W
		6	INT_ACLEAR_DATA_G	Time Slot G Interrupt Autoclear Enable. Set this bit to enable automatic clearing of the INT_DATA_G interrupt each time the Time Slot G data registers are read.	0x1	R/W
		5	INT_ACLEAR_DATA_F	Time Slot F Interrupt Autoclear Enable. Set this bit to enable automatic clearing of the INT_DATA_F interrupt each time the Time Slot F data registers are read.	0x1	R/W
		4	INT_ACLEAR_DATA_E	Time Slot E Interrupt Autoclear Enable. Set this bit to enable automatic clearing of the INT_DATA_E interrupt each time the Time Slot E data register is read.	0x1	R/W
		3	INT_ACLEAR_DATA_D	Time Slot D Interrupt Autoclear Enable. Set this bit to enable automatic clearing of the INT_DATA_D interrupt each time the Time Slot D data registers are read.	0x1	R/W
		2	INT_ACLEAR_DATA_C	Time Slot C Interrupt Autoclear Enable. Set this bit to enable automatic clearing of the INT_DATA_C interrupt each time the Time Slot C data registers are read.	0x1	R/W
		1	INT_ACLEAR_DATA_B	Time Slot B Interrupt Autoclear Enable. Set this bit to enable automatic clearing of the INT_DATA_B interrupt each time the Time Slot B data registers are read.	0x1	R/W

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Table 27. Interrupt Status and Control Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access[1]
		0	INT_ACLEAR_DATA_A	Time Slot A Interrupt Autoclear Enable. Set this bit to enable automatic clearing of the INT_DATA_A interrupt each time the Time Slot A data registers are read.	0x1	R/W
0x0014	INT_ENABLE_XD	15	INTX_EN_FIFO_TH	INT_FIFO_TH Interrupt Enable. Write a 1 to this bit to enable the drive of the FIFO threshold status on Interrupt X.	0x0	R/W
		14	INTX_EN_FIFO_UFLOW	INT_FIFO_UFLOW Interrupt Enable for Interrupt X. Write a 1 to this bit to enable drive of the FIFO underflow status on Interrupt X.	0x0	R/W
		13	INTX_EN_FIFO_OFLOW	INT_FIFO_OFLOW Interrupt Enable for Interrupt X. Write a 1 to this bit to enable drive of the FIFO overflow status on Interrupt X.	0x0	R/W
		12	Reserved	Reserved.	0x0	R
		11	INTX_EN_DATA_L	INT_DATA_L Interrupt Enable. Write a 1 to this bit to enable drive of INT_DATA_L status on Interrupt X.	0x0	R/W
		10	INTX_EN_DATA_K	INT_DATA_K Interrupt Enable. Write a 1 to this bit to enable drive of INT_DATA_K status on Interrupt X.	0x0	R/W
		9	INTX_EN_DATA_J	INT_DATA_J Interrupt Enable. Write a 1 to this bit to enable drive of INT_DATA_J status on Interrupt X.	0x0	R/W
		8	INTX_EN_DATA_I	INT_DATA_I Interrupt Enable. Write a 1 to this bit to enable drive of INT_DATA_I status on Interrupt X.	0x0	R/W
		7	INTX_EN_DATA_H	INT_DATA_H Interrupt Enable. Write a 1 to this bit to enable drive of INT_DATA_H status on Interrupt X.	0x0	R/W
		6	INTX_EN_DATA_G	INT_DATA_G Interrupt Enable. Write a 1 to this bit to enable drive of INT_DATA_G status on Interrupt X.	0x0	R/W
		5	INTX_EN_DATA_F	INT_DATA_F Interrupt Enable. Write a 1 to this bit to enable drive of INT_DATA_F status on Interrupt X.	0x0	R/W
		4	INTX_EN_DATA_E	INT_DATA_E Interrupt Enable. Write a 1 to this bit to enable drive of INT_DATA_E status on Interrupt X.	0x0	R/W
		3	INTX_EN_DATA_D	INT_DATA_D Interrupt Enable. Write a 1 to this bit to enable drive of INT_DATA_D status on Interrupt X.	0x0	R/W
		2	INTX_EN_DATA_C	INT_DATA_C Interrupt Enable. Write a 1 to this bit to enable drive of INT_DATA_C status on Interrupt X.	0x0	R/W
		1	INTX_EN_DATA_B	INT_DATA_B Interrupt Enable. Write a 1 to this bit to enable drive of INT_DATA_B status on Interrupt X.	0x0	R/W
		0	INTX_EN_DATA_A	INT_DATA_A Interrupt Enable. Write a 1 to this bit to enable drive of INT_DATA_A status on Interrupt X.	0x0	R/W
0x0015	INT_ENABLE_YD	15	INTY_EN_FIFO_TH	INT_FIFO_TH Interrupt Enable. Write a 1 to this bit to enable drive of the FIFO threshold status on Interrupt Y.	0x0	R/W
		14	INTY_EN_FIFO_UFLOW	INT_FIFO_UFLOW Interrupt Enable for Interrupt Y. Write a 1 to this bit to enable drive of the FIFO underflow status on Interrupt Y.	0x0	R/W
		13	INTY_EN_FIFO_OFLOW	INT_FIFO_OFLOW Interrupt Enable for Interrupt Y. Write a 1 to this bit to enable drive of the FIFO overflow status on Interrupt Y.	0x0	R/W
		12	Reserved	Reserved.	0x0	R
		11	INTY_EN_DATA_L	INT_DATA_L Interrupt Enable. Write a 1 to this bit to enable drive of INT_DATA_L status on Interrupt Y.	0x0	R/W
		10	INTY_EN_DATA_K	INT_DATA_K Interrupt Enable. Write a 1 to this bit to enable drive of INT_DATA_K status on Interrupt Y.	0x0	R/W
		9	INTY_EN_DATA_J	INT_DATA_J Interrupt Enable. Write a 1 to this bit to enable drive of INT_DATA_J status on Interrupt Y.	0x0	R/W
		8	INTY_EN_DATA_I	INT_DATA_I Interrupt Enable. Write a 1 to this bit to enable drive of INT_DATA_I status on Interrupt Y.	0x0	R/W
		7	INTY_EN_DATA_H	INT_DATA_H Interrupt Enable. Write a 1 to this bit to enable drive of INT_DATA_H status on Interrupt Y.	0x0	R/W

REGISTER DETAILS

Table 27. Interrupt Status and Control Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access[1]
		6	INTY_EN_DATA_G	INT_DATA_G Interrupt Enable. Write a 1 to this bit to enable drive of INT_DATA_G status on Interrupt Y.	0x0	R/W
		5	INTY_EN_DATA_F	INT_DATA_F Interrupt Enable. Write a 1 to this bit to enable drive of INT_DATA_F status on Interrupt Y.	0x0	R/W
		4	INTY_EN_DATA_E	INT_DATA_E Interrupt Enable. Write a 1 to this bit to enable drive of INT_DATA_E status on Interrupt Y.	0x0	R/W
		3	INTY_EN_DATA_D	INT_DATA_D Interrupt Enable. Write a 1 to this bit to enable drive of INT_DATA_D status on Interrupt Y.	0x0	R/W
		2	INTY_EN_DATA_C	INT_DATA_C Interrupt Enable. Write a 1 to this bit to enable drive of INT_DATA_C status on Interrupt Y.	0x0	R/W
		1	INTY_EN_DATA_B	INT_DATA_B Interrupt Enable. Write a 1 to this bit to enable drive of INT_DATA_B status on Interrupt Y.	0x0	R/W
		0	INTY_EN_DATA_A	INT_DATA_A Interrupt Enable. Write a 1 to this bit to enable drive of INT_DATA_A status on Interrupt Y.	0x0	R/W
0x0016	INT_ENABLE_XL0	[15:12]	Reserved	Reserved.	0x0	R
		11	INTX_EN_LEV0_L	INT_LEV0_L Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV0_L status on Interrupt X.	0x0	R/W
		10	INTX_EN_LEV0_K	INT_LEV0_K Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV0_K status on Interrupt X.	0x0	R/W
		9	INTX_EN_LEV0_J	INT_LEV0_J Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV0_J status on Interrupt X.	0x0	R/W
		8	INTX_EN_LEV0_I	INT_LEV0_I Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV0_I status on Interrupt X.	0x0	R/W
		7	INTX_EN_LEV0_H	INT_LEV0_H Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV0_H status on Interrupt X.	0x0	R/W
		6	INTX_EN_LEV0_G	INT_LEV0_G Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV0_G status on Interrupt X.	0x0	R/W
		5	INTX_EN_LEV0_F	INT_LEV0_F Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV0_F status on Interrupt X.	0x0	R/W
		4	INTX_EN_LEV0_E	INT_LEV0_E Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV0_E status on Interrupt X.	0x0	R/W
		3	INTX_EN_LEV0_D	INT_LEV0_D Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV0_D status on Interrupt X.	0x0	R/W
		2	INTX_EN_LEV0_C	INT_LEV0_C Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV0_C status on Interrupt X.	0x0	R/W
		1	INTX_EN_LEV0_B	INT_LEV0_B Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV0_B status on Interrupt X.	0x0	R/W
		0	INTX_EN_LEV0_A	INT_LEV0_A Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV0_A status on Interrupt X.	0x0	R/W
0x0017	INT_ENABLE_XL1	[15:12]	Reserved	Reserved.	0x0	R
		11	INTX_EN_LEV1_L	INT_LEV1_L Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV1_L status on Interrupt X.	0x0	R/W
		10	INTX_EN_LEV1_K	INT_LEV1_K Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV1_K status on Interrupt X.	0x0	R/W
		9	INTX_EN_LEV1_J	INT_LEV1_J Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV1_J status on Interrupt X.	0x0	R/W
		8	INTX_EN_LEV1_I	INT_LEV1_I Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV1_I status on Interrupt X.	0x0	R/W
		7	INTX_EN_LEV1_H	INT_LEV1_H Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV1_H status on Interrupt X.	0x0	R/W

REGISTER DETAILS

Table 27. Interrupt Status and Control Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access[1]
		6	INTX_EN_LEV1_G	INT_LEV1_G Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV1_G status on Interrupt X.	0x0	R/W
		5	INTX_EN_LEV1_F	INT_LEV1_F Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV1_F status on Interrupt X.	0x0	R/W
		4	INTX_EN_LEV1_E	INT_LEV1_E Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV1_E status on Interrupt X.	0x0	R/W
		3	INTX_EN_LEV1_D	INT_LEV1_D Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV1_D status on Interrupt X.	0x0	R/W
		2	INTX_EN_LEV1_C	INT_LEV1_C Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV1_C status on Interrupt X.	0x0	R/W
		1	INTX_EN_LEV1_B	INT_LEV1_B Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV1_B status on Interrupt X.	0x0	R/W
		0	INTX_EN_LEV1_A	INT_LEV1_A Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV1_A status on Interrupt X.	0x0	R/W
0x001A	INT_ENABLE_YL0	[15:12]	Reserved	Reserved.	0x0	R
		11	INTY_EN_LEV0_L	INT_LEV0_L Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV0_L status on Interrupt Y.	0x0	R/W
		10	INTY_EN_LEV0_K	INT_LEV0_K Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV0_K status on Interrupt Y.	0x0	R/W
		9	INTY_EN_LEV0_J	INT_LEV0_J Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV0_J status on Interrupt Y.	0x0	R/W
		8	INTY_EN_LEV0_I	INT_LEV0_I Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV0_I status on Interrupt Y.	0x0	R/W
		7	INTY_EN_LEV0_H	INT_LEV0_H Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV0_H status on Interrupt Y.	0x0	R/W
		6	INTY_EN_LEV0_G	INT_LEV0_G Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV0_G status on Interrupt Y.	0x0	R/W
		5	INTY_EN_LEV0_F	INT_LEV0_F Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV0_F status on Interrupt Y.	0x0	R/W
		4	INTY_EN_LEV0_E	INT_LEV0_E Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV0_E status on Interrupt Y.	0x0	R/W
		3	INTY_EN_LEV0_D	INT_LEV0_D Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV0_D status on Interrupt Y.	0x0	R/W
		2	INTY_EN_LEV0_C	INT_LEV0_C Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV0_C status on Interrupt Y.	0x0	R/W
		1	INTY_EN_LEV0_B	INT_LEV0_B Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV0_B status on Interrupt Y.	0x0	R/W
		0	INTY_EN_LEV0_A	INT_LEV0_A Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV0_A status on Interrupt Y.	0x0	R/W
0x001B	INT_ENABLE_YL1	[15:12]	Reserved	Reserved.	0x0	R
		11	INTY_EN_LEV1_L	INT_LEV1_L Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV1_L status on Interrupt Y.	0x0	R/W
		10	INTY_EN_LEV1_K	INT_LEV1_K Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV1_K status on Interrupt Y.	0x0	R/W
		9	INTY_EN_LEV1_J	INT_LEV1_J Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV1_J status on Interrupt Y.	0x0	R/W
		8	INTY_EN_LEV1_I	INT_LEV1_I Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV1_I status on Interrupt Y.	0x0	R/W
		7	INTY_EN_LEV1_H	INT_LEV1_H Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV1_H status on Interrupt Y.	0x0	R/W

REGISTER DETAILS

Table 27. Interrupt Status and Control Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access[1]
		6	INTY_EN_LEV1_G	INT_LEV1_G Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV1_G status on Interrupt Y.	0x0	R/W
		5	INTY_EN_LEV1_F	INT_LEV1_F Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV1_F status on Interrupt Y.	0x0	R/W
		4	INTY_EN_LEV1_E	INT_LEV1_E Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV1_E status on Interrupt Y.	0x0	R/W
		3	INTY_EN_LEV1_D	INT_LEV1_D Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV1_D status on Interrupt Y.	0x0	R/W
		2	INTY_EN_LEV1_C	INT_LEV1_C Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV1_C status on Interrupt Y.	0x0	R/W
		1	INTY_EN_LEV1_B	INT_LEV1_B Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV1_B status on Interrupt Y.	0x0	R/W
		0	INTY_EN_LEV1_A	INT_LEV1_A Interrupt Enable. Write a 1 to this bit to enable drive of INT_LEV1_A status on Interrupt Y.	0x0	R/W
0x001E	FIFO_STATUS_BYTES	[15:6]	Reserved	Reserved.	0x0	R
		5	ENA_STAT_LX	Enable Level 0 and Level 1 interrupt status byte for Time Slot I through Time Slot L. This byte contains the interrupt status for the Level 0 and Level 1 interrupts for Time Slot I through Time Slot L.	0x0	R/W
		4	ENA_STAT_L1	Enable Level 1 interrupt status byte for Time Slot A through Time Slot H. This byte contains the interrupt status for the Level 1 interrupts for Time Slot A through Time Slot H.	0x0	R/W
		3	ENA_STAT_L0	Enable Level 0 interrupt status byte for Time Slot A through Time Slot H. This byte contains the interrupt status for Level Interrupt 0 for Time Slot A through Time Slot H.	0x0	R/W
		2	ENA_STAT_D2	Enable data interrupt status byte for Time Slot I through Time Slot L. This byte contains the data interrupt status for Time Slot I through Time Slot L.	0x0	R/W
		1	ENA_STAT_D1	Enable data interrupt status byte for Time Slot A through Time Slot H. This byte is the data interrupt status for Time Slot A through Time Slot H.	0x0	R/W
		0	ENA_STAT_SUM	Enable status summary byte. When enabled write a status byte containing the summary pattern to the FIFO following the last enabled time slot data.	0x0	R/W

[1] R/W1C means write 1 to clear.

THRESHOLD SETUP AND CONTROL REGISTERS

Table 28. Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x0006	FIFO_TH	[15:10]	Reserved	Reserved.	0x00	R
		[9:0]	FIFO_TH	FIFO Interrupt Generation Threshold. Generate FIFO interrupt during a FIFO write when the number of bytes in the FIFO exceeds this value. The FIFO is 512 bytes. Therefore, the maximum value for FIFO_TH is 0x1FF.	0x000	R/W
0x0115	THRESH_CFG_A	[15:8]	Reserved	Reserved.	0x0	R
0x0135	THRESH_CFG_B	7	THRESH1_CHAN_x	Select channel for Level 1 interrupt.	0x0	R/W
0x0155	THRESH_CFG_C			0: use Channel 1.		
0x0175	THRESH_CFG_D			1: use Channel 2.		
0x0195	THRESH_CFG_E	6	THRESH1_DIR_x	Direction of Comparison for Level 1 Interrupt.	0x0	R/W
0x01B5	THRESH_CFG_F			0: set when below Level 1 interrupt threshold.		
0x01D5	THRESH_CFG_G			1: set when above Level 1 interrupt threshold.		

REGISTER DETAILS

Table 28. Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x01F5 0x0215 0x0235 0x0255 0x0275	THRESH_CFG_H THRESH_CFG_I THRESH_CFG_J THRESH_CFG_K THRESH_CFG_L	[5:4]	THRESH1_TYPE_x	Type of Comparison for Level 1 Interrupt. 0: off (no comparison). 1: compare to signal. 10: compare to dark. 11: reserved.	0x0	R/W
		3	THRESH0_CHAN_x	Select channel for Level 0 interrupt. 0: use Channel 1. 1: use Channel 2.	0x0	R/W
		2	THRESH0_DIR_x	Direction of Comparison for Level 0 Interrupt. 0: set when below Level 0 interrupt threshold. 1: set when above Level 0 interrupt threshold.	0x0	R/W
		[1:0]	THRESH0_TYPE_x	Type of Comparison for Level 0 Interrupt. 0: off (no comparison). 1: compare to signal. 10: compare to dark. 11: reserved.	0x0	R/W
0x0116	THRESH0_A	[15:13]	Reserved	Reserved.	0x0	R
0x0136 0x0156	THRESH0_B THRESH0_C	[12:8]	THRESH0_SHIFT_x	Shift for Level 0 Interrupt Comparison Threshold. Shift THRESH0_VALUE_x by this amount before comparing.	0x0	R/W
0x0176 0x0196 0x01B6 0x01D6 0x01F6 0x0216 0x0236 0x0256 0x0276	THRESH0_D THRESH0_E THRESH0_F THRESH0_G THRESH0_H THRESH0_I THRESH0_J THRESH0_K THRESH0_L	[7:0]	THRESH0_VALUE_x	Value for Level 0 Interrupt Comparison Threshold.	0x0	R/W
0x0117	THRESH1_A	[15:13]	Reserved	Reserved.	0x0	R
0x0137 0x0157	THRESH1_B THRESH1_C	[12:8]	THRESH1_SHIFT_x	Shift for Level 1 Interrupt Comparison Threshold. Shift THRESH1_VALUE_x by this amount before comparing.	0x0	R/W
0x0177 0x0197 0x01B7 0x01D7 0x01F7 0x0217 0x0237 0x0257 0x0277	THRESH1_D THRESH1_E THRESH1_F THRESH1_G THRESH1_H THRESH1_I THRESH1_J THRESH1_K THRESH1_L	[7:0]	THRESH1_VALUE_x	Value for Level 1 Interrupt Comparison Threshold.	0x0	R/W

REGISTER DETAILS

CLOCK AND TIMESTAMP SETUP AND CONTROL REGISTERS

Table 29. Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x0009	OSC32M	[15:8]	Reserved	Reserved.	0x0	R
		[7:0]	OSC_32M_FREQ_ADJ	High Frequency Oscillator Frequency Control. 0x00 is the lowest frequency, and 0xFF is maximum frequency.	0x90	R/W
0x000A	OSC32M_CAL	15	OSC_32M_CAL_START	Start High Frequency Oscillator Calibration Cycle. Writing a 1 to this bit causes the high frequency oscillator calibration cycle to occur. 32 MHz oscillator cycles are counted during 128 low frequency oscillator cycles if using the 1 MHz low frequency oscillator, or 32 low frequency oscillator cycles if using the 32 kHz low frequency oscillator. The OSC_32M_CAL_COUNT bit field is updated with the count. The calibration circuit clears the OSC_32M_CAL_START bit when the calibration cycle is completed.	0x0	R/W
		[14:0]	OSC_32M_CAL_COUNT	High Frequency Oscillator Calibration Count. This bit field contains the total number of 32 MHz cycles that occurred during the last high frequency oscillator calibration cycle.	0x0	R
0x000B	OSC1M	[15:11]	Reserved	Reserved.	0x0	R
		10	CLK_CAL_ENA	Enables clock for oscillator calibration. When set to 0 (default), the oscillator calibration circuitry is disabled. Set this bit to 1 to turn on the oscillator calibration circuitry.	0x0	R/W
		[9:0]	OSC_1M_FREQ_ADJ	Low Frequency Oscillator Frequency Control. 0x000 is the lowest frequency, and 0x3FF is maximum frequency.	0x2B2	R/W
0x000C	OSC32K	15	CAPTURE_TIMESTAMP	Enable time stamp capture. This bit field is used to activate the time stamp capture function. When set, the next rising edge on the time stamp input (defaults to GPIO0) causes a time stamp capture. This bit field is cleared when the time stamp occurs.	0x0	R/W
		[14:6]	Reserved	Reserved.	0x0	R
		[5:0]	OSC_32K_ADJUST	32 kHz Oscillator Trim. 00 0000: maximum frequency. 01 0010: default frequency. 11 1111: minimum frequency.	0x12	R/W
0x0011	STAMP_L	[15:0]	TIMESTAMP_COUNT_L	Count at last time stamp. Lower 16 bits.	0x0	R
0x0012	STAMP_H	[15:0]	TIMESTAMP_COUNT_H	Count at last time stamp. Upper 16 bits.	0x0	R
0x0013	STAMPDELTA	[15:0]	TIMESTAMP_SLOT_DELTA	Count remaining until next time slot start.	0x0	R

SYSTEM REGISTERS

Table 30. Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x0008	CHIP_ID	[15:8]	Version	Mask version.	0x0	R
		[7:0]	CHIP_ID	Chip ID.	0xC0	R
0x002E	DATA_HOLD_FLAG	[15:12]	Reserved	Reserved.	0x0	R
		11	HOLD_REGS_L	Prevents update of Time Slot L data registers. 0: allows data register update. 1: holds current contents of data register.	0x0	R/W
		10	HOLD_REGS_K	Prevents update of time Slot K data registers. 0: allows data register update. 1: holds current contents of data register.	0x0	R/W
		9	HOLD_REGS_J	Prevents update of Time Slot J data registers. 0: allows data register update. 1: holds current contents of data register.	0x0	R/W

REGISTER DETAILS

Table 30. Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
		8	HOLD_REGS_I	Prevents update of Time Slot I data registers. 0: allows data register update. 1: holds current contents of data register.	0x0	R/W
		7	HOLD_REGS_H	Prevents update of Time Slot H data registers. 0: allows data register update. 1: holds current contents of data register.	0x0	R/W
		6	HOLD_REGS_G	Prevents update of Time Slot G data registers. 0: allows data register update. 1: holds current contents of data register.	0x0	R/W
		5	HOLD_REGS_F	Prevents update of Time Slot F data registers. 0: allows data register update. 1: holds current contents of data register.	0x0	R/W
		4	HOLD_REGS_E	Prevents update of Time Slot E data registers. 0: allows data register update. 1: holds current contents of data register.	0x0	R/W
		3	HOLD_REGS_D	Prevents update of Time Slot D data registers. 0: allows data register update. 1: holds current contents of data register.	0x0	R/W
		2	HOLD_REGS_C	Prevents update of Time Slot C data registers. 0: allows data register update. 1: holds current contents of data register.	0x0	R/W
		1	HOLD_REGS_B	Prevents update of Time Slot B data registers. 0: allows data register update. 1: holds current contents of data register.	0x0	R/W
		0	HOLD_REGS_A	Prevents update of Time Slot A data registers. 0: allows data register update. 1: holds current contents of data register.	0x0	R/W

INPUT AND OUTPUT SETUP AND CONTROL REGISTERS

Table 31. Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x0022	GPIO_CFG	[15:14]	GPIO_SLEW	Slew Control for GPIOx Pins. 0: slowest. 1: slow. 10: fastest. 11: fast.	0x0	R/W
		[13:12]	GPIO_DRV	Drive Control for GPIOx Pins. 0: medium. 1: weak. 10: strong. 11: strong.	0x0	R/W
		[11:6]	Reserved	Reserved.	0x0	R
		[5:3]	GPIO_PIN_CFG1	GPIO1 Pin Configuration. 000: disabled (tristate, input buffer off). 001: enabled input. 010: output—normal. 011: output—inverted. 100: pull-down only—normal.	0x0	R/W

REGISTER DETAILS

Table 31. Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
				101: pull-down only—inverted. 110: pull-up only—normal. 111: pull-up only—inverted.		
		[2:0]	GPIO_PIN_CFG0	GPIO0 Pin Configuration. 000: disabled (tristate, input buffer off). 001: enabled input. 010: output—normal. 011: output—inverted. 100: pull-down only—normal. 101: pull-down only—inverted. 110: pull-up only—normal. 111: pull-up only—inverted.	0x0	R/W
0x0023	GPIO01	15	Reserved	Reserved.	0x0	R
		[14:8]	GPIOOUT1	GPIO1 Output Signal Select. 0x00: Output Logic 0. 0x01: Output Logic 1. 0x02: Interrupt X. 0x03: Interrupt Y. 0x08: LED1A amplifier enabled. 0x09: LED2A amplifier enabled. 0x0A: LED3A amplifier enabled. 0x0B: LED4A amplifier enabled. 0x0C: any LED amplifier enabled. 0x0F: 32 MHz oscillator output divided by 64 (500 kHz). 0x10: time slot specific output pattern defined by TS_GPIO_x and TS_GPIO_SLEEP bits. 0x11: in sleep state. 0x16: low frequency oscillator output. 0x17: 32 MHz oscillator output. 0x18: 32 MHz oscillator output divided by 32 (1 MHz). 0x20: Time Slot A active. 0x21: Time Slot B active. 0x22: Time Slot C active. 0x23: Time Slot D active. 0x24: Time Slot E active. 0x25: Time Slot F active 0x26: Time Slot G active. 0x27: Time Slot H active. 0x28: Time Slot I active. 0x29: Time Slot J active. 0x2A: Time Slot K active. 0x2B: Time Slot L active. 0x30: Time Slot A LED pulse. 0x31: Time Slot B LED pulse. 0x32: Time Slot C LED pulse. 0x33: Time Slot D LED pulse. 0x34: Time Slot E LED pulse. 0x35: Time Slot F LED pulse. 0x36: Time Slot G LED pulse.	0x0	R/W

REGISTER DETAILS

Table 31. Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
				0x37: Time Slot H LED pulse. 0x38: Time Slot I LED pulse. 0x39: Time Slot J LED pulse. 0x3A: Time Slot K LED pulse. 0x3B: Time Slot L LED pulse. 0x3F: any time slot LED pulse. 0x40: Time Slot A modulation pulse. 0x41: Time Slot B modulation pulse. 0x42: Time Slot C modulation pulse. 0x43: Time Slot D modulation pulse. 0x44: Time Slot E modulation pulse. 0x45: Time Slot F modulation pulse. 0x46: Time Slot G modulation pulse. 0x47: Time Slot H modulation pulse. 0x48: Time Slot I modulation pulse. 0x49: Time Slot J modulation pulse. 0x4A: Time Slot K modulation pulse. 0x4B: Time Slot L modulation pulse. 0x4F: any time slot modulation pulse. 0x50: output data cycle occurred in Time Slot A, which is useful when synchronizing an external device to a decimated data rate from the ADPD4200 0x51: output data cycle occurred in Time Slot B. 0x52: output data cycle occurred in Time Slot C. 0x53: output data cycle occurred in Time Slot D. 0x54: output data cycle occurred in Time Slot E. 0x55: output data cycle occurred in Time Slot F. 0x56: output data cycle occurred in Time Slot G. 0x57: output data cycle occurred in Time Slot H. 0x58: output data cycle occurred in Time Slot I. 0x59: output data cycle occurred in Time Slot J. 0x5A: output data cycle occurred in Time Slot K. 0x5B: output data cycle occurred in Time Slot L. 0x5F: output data cycle occurred in any time slot.		
		7	Reserved	Reserved.	0x0	R
		[6:0]	GPIOOUT0	GPIO0 Output Signal Select. Options are identical to those described in GPIOOUT1.	0x0	R/W
0x0025	GPIO_IN	[15:4]	Reserved	Reserved.	0x0	R
		[3:0]	GPIO_INPUT	GPIO Input Value (If Enabled). Read back the value present on any GPIOx enabled as an input. Bit 0 is GPIO0, and Bit 1 is GPIO1.	0x0	R
0x0026	GPIO_EXT	[15:9]	Reserved	Reserved.	0x0	R
		8	TS_GPIO_SLEEP	When GPIOOUTx is set to 0x10, the GPIO returns to the TS_GPIO_SLEEP value at the end of the time slot and during sleep.	0x0	R/W
		7	TIMESTAMP_INV	Time Stamp Trigger Invert. 0: time stamp trigger is rising edge. 1: time stamp trigger is falling edge.	0x0	R/W
		6	TIMESTAMP_ALWAYS_EN	Enable time stamp always on. When set, do not automatically clear CAPTURE_TIMESTAMP. This bit provides an always activated time stamp.	0x0	R/W
		[5:4]	TIMESTAMP_GPIO	Time Stamp GPIOx Select. 0x0: use GPIO0 for time stamp (default).	0x0	R/W

REGISTER DETAILS

Table 31. Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
				0x1: use GPIO1 for time stamp.		
		3	Reserved	Reserved.	0x0	R/W
		2	EXT_SYNC_EN	External Sync Enable. When enabled, use the GPIO selected by EXT_SYNC_GPIO to trigger samples rather than the period counter.	0x0	R/W
		[1:0]	EXT_SYNC_GPIO	External Synchronization GPIOx Select. 00: use GPIO0 for external synchronization 01: use GPIO1 for external synchronization.	0x0	R/W
0x00B4	IO_ADJUST	[15:4]	Reserved	Set to 0x005.	0x005	R/W
		[3:2]	SPI_SLEW	Slew Control for SPI Pins. 0: slowest. 1: slow. 10: fastest. 11: fast.	0x0	R/W
		[1:0]	SPI_DRV	Drive Control for SPI Pins. 0: medium. 1: weak. 10: strong. 11: strong.	0x0	R/W

TIME SLOT CONFIGURATION REGISTERS

Table 32. Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x0100 0x0120 0x0140	TS_CTRL_A TS_CTRL_B TS_CTRL_C	15	SUBSAMPLE_x	Subsample using DECIMATE_FACTOR_x. When this bit is set, operate the selected time slot only once per (DECIMATE_FACTOR_x + 1) time slot sequences.	0x0	R/W
0x0160 0x0180 0x01A0	TS_CTRL_D TS_CTRL_E TS_CTRL_F	14	CH2_EN_x	Channel 2 Enable. 0: Channel 2 disabled. 1: Channel 2 enabled.	0x0	R/W
0x01C0 0x01E0 0x0200 0x0220 0x0240	TS_CTRL_G TS_CTRL_H TS_CTRL_I TS_CTRL_J TS_CTRL_K	[13:12]	SAMPLE_TYPE_x	Time Slot x Sampling Type. 00: standard sampling modes. 01: one-region digital integration mode. 10: two-region digital integration mode. 11: impulse response mode.	0x0	R/W
0x0260	TS_CTRL_L	[11:10]	INPUT_R_SELECT_x	Input Resistor (R_{IN}) Select. 00: 500 Ω. 01: 6.25 kΩ. 10: reserved. 11: reserved.	0x0	R/W
		[9:0]	TIMESLOT_OFFSET_x	Time Slot x Offset in 64 × Number of 1 MHz Low Frequency Oscillator Cycles or 2 × Number of 32 kHz Low Frequency Oscillator Cycles.	0x0	R/W
0x0101 0x0121 0x0141	TS_PATH_A TS_PATH_B TS_PATH_C	[15:12]	PRE_WIDTH_x	Preconditioning Duration for Time Slot x. This value is in 2 µs increments. A value of 0 skips the preconditioning state. Default is 8 µs.	0x4	R/W
0x0161	TS_PATH_D	[11:10]	Reserved	Write 0x0.	0x0	R
0x0181 0x01A1 0x01C1 0x01E1	TS_PATH_E TS_PATH_F TS _PATH_G TS_PATH_H	9	TS_GPIO_x	Time Slot Specific Value for Time Slot x. When GPIOOUTx is set to 0x10 and TS_GPIO_x is set to 1, the GPIO selected by GPIOOUTx outputs a 1 while the time slot selected by TS_GPIO_x is active. The GPIO returns to the TS_GPIO_SLEEP value at the end of the time slot.	0x0	R/W

REGISTER DETAILS

Table 32. Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x0201 0x0221 0x0241 0x0261	TS_PATH_I TS_PATH_J TS_PATH_K TS_PATH_L	[8:0]	AFE_PATH_CFG_x	Signal Path Selection. 0x0DA: TIA, BPF, integrator, and ADC. 0x0E6: TIA, integrator, and ADC. 0x106: TIA and ADC. 0x101: ADC. 0x0E1: buffer and ADC.	0x0DA	R/W
0x0102 0x0122 0x0142 0x0162 0x0182 0x01A2 0x01C2 0x01E2 0x0202 0x0222 0x0242 0x0262	INPUTS_A INPUTS_B INPUTS_C INPUTS_D INPUTS_E INPUTS_F INPUTS_G INPUTS_H INPUTS_I INPUTS_J INPUTS_K INPUTS_L	[15:12]	INP78_x	IN7 and IN8 Input Pair Enable. 0000: input pair disabled. IN7 and IN8 disconnected. 0001: IN7 connected to Channel 1. IN8 disconnected. 0010: IN7 connected to Channel 2. IN8 disconnected. 0011: IN7 disconnected. IN8 connected to Channel 1. 0100: IN7 disconnected. IN8 connected to Channel 2. 0101: IN7 connected to Channel 1. IN8 connected to Channel 2. 0110: IN7 connected to Channel 2. IN8 connected to Channel 1. 0111: IN7 and IN8 connected to Channel 1. Single-ended or differentially based on PAIR78. 1000: IN7 and IN8 connected to Channel 2. Single-ended or differentially based on PAIR78.	0x0	R/W
		[11:4]	Reserved	Reserved.	0x0	R
		[3:0]	INP12_x	IN1 and IN2 Input Pair Enable. 0000: input pair disabled. IN1 and IN2 disconnected. 0001: IN1 connected to Channel 1. IN2 disconnected. 0010: IN1 connected to Channel 2. IN2 disconnected. 0011: IN1 disconnected. IN2 connected to Channel 1. 0100: IN1 disconnected. IN2 connected to Channel 2. 0101: IN1 connected to Channel 1. IN2 connected to Channel 2. 0110: IN1 connected to Channel 2. IN2 connected to Channel 1. 0111: IN1 and IN2 connected to Channel 1. Single-ended or differentially based on PAIR12. 1000: IN1 and IN2 connected to Channel 2. Single-ended or differentially based on PAIR12.	0x0	R/W
0x0103	CATHODE_A	15	Reserved	Reserved.	0x0	R
0x0123 0x0143 0x0163 0x0183 0x01A3 0x01C3 0x01E3 0x0203 0x0223	CATHODE_B CATHODE_C CATHODE_D CATHODE_E CATHODE_F CATHODE_G CATHODE_H CATHODE_I CATHODE_J	[14:12]	PRECON_x	Precondition Value for Enabled Inputs During Time Slot x. 000: float input(s). 001: precondition to VC1. 010: precondition to VC2. 011: precondition to V_{ICM}. Used when inputs are configured differentially. 100: precondition with TIA input. 101: precondition with TIA_VREF. 110: precondition by shorting differential pair.	0x0	R/W
0x0243 0x0263	CATHODE_K CATHODE_L	[11:10]	VC2_PULSE_x	VC2 Pulse Control for Time Slot x. 00: no pulsing. 01: alternate VC2 on each subsequent Time Slot x. 10: pulse to alternate value specified in VC2_ALT_x using modulation pulse.	0x0	R/W
		[9:8]	VC2_ALT_x	VC2 Alternate Pulsed State for Time Slot x. 00: V_{DD}. 01: TIA_VREF.	0x0	R/W

REGISTER DETAILS

Table 32. Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
				10: TIA_VREF + 250 mV. 11: GND.		
		[7:6]	VC2_SEL_x	VC2 Active State for Time Slot x. 00: V_{DD}. 01: TIA_VREF. 10: TIA_VREF + 250 mV. 11: GND.	0x0	R/W
		[5:4]	VC1_PULSE_x	VC1 Pulse Control for Time Slot x. 00: no pulsing. 01: alternate VC1 on each subsequent Time Slot x. 10: pulse to alternate value specified in VC1_ALT_x using modulation pulse.	0x0	R/W
		[3:2]	VC1_ALT_x	VC1 Alternate Pulsed State for Time Slot x. 00: V_{DD}. 01: TIA_VREF. 10: TIA_VREF + 250 mV. 11: GND.	0x0	R/W
		[1:0]	VC1_SEL_x	VC1 Active State for Time Slot x. 00: V_{DD}. 01: TIA_VREF. 10: TIA_VREF + 250 mV. 11: GND.	0x0	R/W
0x0104	AFE_TRIM_A	15	Reserved	Reserved	0x0	R/W
0x0124	AFE_TRIM_B	[13:12]	CH2_TRIM_INT_x	Sets the integrator input resistor when AFE_INT_C_BUF_x = 0. Sets the buffer gain when AFE_INT_C_BUF_x = 1.	0x0	R/W
0x0144	AFE_TRIM_C					
0x0164	AFE_TRIM_D			**AFE_INT_C_BUF_x = 0** / **AFE_INT_C_BUF_x = 1**		
0x0184	AFE_TRIM_E			00: 400 kΩ. / 00: gain = 1.		
0x01A4	AFE_TRIM_F			01: 200 kΩ. / 01: gain = 1.		
0x01C4	AFE_TRIM_G			10: 100 kΩ. / 10: gain = 0.7.		
0x01E4	AFE_TRIM_H			11: 100 kΩ. / 11: gain = 0.7.		
0x0204	AFE_TRIM_I	[12:11]	CH1_TRIM_INT_x	Sets the integrator input resistor when AFE_INT_C_BUF_x = 0. Sets the buffer gain when AFE_INT_C_BUF_x = 1.	0x0	R/W
0x0224	AFE_TRIM_J					
0x0244	AFE_TRIM_K			**AFE_INT_C_BUF_x = 0** / **AFE_INT_C_BUF_x = 1**		
0x0264	AFE_TRIM_L			00: 400 kΩ. / 00: gain = 1.		
				01: 200 kΩ. / 01: gain = 1.		
				10: 100 kΩ. / 10: gain = 0.7.		
				11: 100 kΩ. / 11: gain = 0.7.		
		10	VREF_PULSE_x	TIA_VREF Pulse Control. 0: no pulsing. 1: pulse TIA_VREF based on modulation pulse.	0x0	R/W
		[9:8]	AFE_TRIM_VREF_x	Voltage Select for TIA_VREF. 00: TIA_VREF = 1.1385 V. 01: TIA_VREF = 1.012 V. 10: TIA_VREF = 0.8855 V. 11: TIA_VREF = 1.265 V.	0x3	R/W
		[7:6]	VREF_PULSE_VAL_x	TIA_VREF Pulse Alternate Value. 00: modulate TIA_VREF = 1.1385 V. 01: modulate TIA_VREF = 1.012 V.	0x3	R/W

REGISTER DETAILS

Table 32. Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
				10: modulate TIA_VREF = 0.8855 V. 11: modulate TIA_VREF = 1.265 V.		
		[5:3]	TIA_GAIN_CH2_x	TIA Resistor Gain Setting for Channel 2. 000: 200 kΩ. 001: 100 kΩ. 010: 50 kΩ. 011: 25 kΩ. 100: 12.5 kΩ.	0x0	R/W
		[2:0]	TIA_GAIN_CH1_x	TIA Resistor Gain Setting for Channel 1. 000: 200 kΩ. 001: 100 kΩ. 010: 50 kΩ. 011: 25 kΩ. 100: 12.5 kΩ.	0x0	R/W
0x010D 0x012D 0x014D	PATTERN_A PATTERN_B PATTERN_C	[15:12]	LED_DISABLE_x	Four-Pulse LED Disable Pattern. Set to 1 to disable the LED pulse in the matching position in a group of four pulses. The LSB maps to the first pulse.	0x0	R/W
0x016D 0x018D 0x01AD	PATTERN_D PATTERN_E PATTERN_F	[11:8]	MOD_DISABLE_x	Four-Pulse Modulation Disable Pattern. Set to 1 to disable the modulation pulse in the matching position in a group of four pulses. The LSB maps to the first pulse.	0x0	R/W
0x01CD 0x01ED 0x020D	PATTERN_G PATTERN_H PATTERN_I	[7:4]	SUBTRACT_x	Four-Pulse Subtract Pattern. Set to 1 to negate the math operation in the matching position in a group of four pulses. The LSB maps to the first pulse.	0x0	R/W
0x022D 0x024D 0x026D	PATTERN_J PATTERN_K PATTERN_L	[3:0]	REVERSE_INTEG_x	Four-Pulse Integration Reverse Pattern. Set to 1 to reverse the integrator positive and/or negative pulse order in the matching position in a group of four pulses. The LSB maps to the first pulse.	0x0	R/W
0x0110 0x0130 0x0150	DATA_FORMAT_A DATA_FORMAT_B DATA_FORMAT_C	[15:11]	DARK_SHIFT_x	Number of Bits to Shift the Dark Data to the Right Before Writing to the FIFO for Time Slot x. Selectable between 0 bits and 32 bits.	0x0	R/W
0x0170 0x0190	DATA_FORMAT_D DATA_FORMAT_E	[10:8]	DARK_SIZE_x	Number of Bytes of Dark Data to be Written to the FIFO for Time Slot x. Selectable between 0 bytes and four bytes.	0x0	R/W
0x01B0 0x01D0 0x01F0	DATA_FORMAT_F DATA_FORMAT_G DATA_FORMAT_H	[7:3]	SIGNAL_SHIFT_x	Number of Bits to Shift the Signal Data to the Right Before Writing to the FIFO for Time Slot x. Selectable between 0 bits and 32 bits.	0x0	R/W
0x0210 0x0230 0x0250 0x0270	DATA_FORMAT_I DATA_FORMAT_J DATA_FORMAT_K DATA_FORMAT_L	[2:0]	SIGNAL_SIZE_x	Number of Bytes of Signal Data to be Written to the FIFO for Time Slot x. Selectable between 0 bytes and four bytes.	0x3	R/W
0x0112	DECIMATE_A	[15:11]	Reserved	Write 0x0.	0x0	R
0x0132 0x0152	DECIMATE_B DECIMATE_C	[10:4]	DECIMATE_FACTOR_x	Decimate Sample Divider. Output data rate is sample rate ÷ (DECIMATE_FACTOR_x + 1). Decimate by 1 to 128.	0x0	R/W
0x0172 0x0192 0x01B2 0x01D2 0x01F2 0x0212 0x0232	DECIMATE_D DECIMATE_E DECIMATE_F DECIMATE_G DECIMATE_H DECIMATE_I DECIMATE_J	[3:0]	DECIMATE_TYPE_x	Decimation Type Select. 0: block sum, CIC first order. 1: signal uses CIC second order. 10: signal uses CIC third order. 11: signal uses CIC fourth order. 100: reserved.	0x0	R/W

REGISTER DETAILS

Table 32. Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x0252	DECIMATE_K					
0x0272	DECIMATE_L					

AFE TIMING SETUP REGISTERS

Table 33. Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x0107 0x0127 0x0147 0x0167	COUNTS_A COUNTS_B COUNTS_C COUNTS_D	[15:8]	NUM_INT_x	Number of ADC Cycles or Acquisition Width. Number of analog integration cycles per ADC conversion or the acquisition width for digital integration and impulse mode. A setting of 0 is not allowed.	0x1	R/W
0x0187 0x01A7 0x01C7 0x01E7 0x0207 0x0227 0x0247 0x0267	COUNTS_E COUNTS_F COUNTS_G COUNTS_H COUNTS_I COUNTS_J COUNTS_K COUNTS_L	[7:0]	NUM_REPEAT_x	Number of Sequence Repeats. Total number of pulses = NUM_INT_x × NUM_REPEAT_x. A setting of 0 is not allowed.	0x1	R/W
0x0108	PERIOD_A	[15:14]	Reserved	Reserved.	0x0	R
0x0128 0x0148 0x0168 0x0188 0x01A8 0x01C8 0x01E8 0x0208	PERIOD_B PERIOD_C PERIOD_D PERIOD_E PERIOD_F PERIOD_G PERIOD_H PERIOD_I	[13:12]	MOD_TYPE_x	Modulation Connection Type. 00: TIA is continuously connected to input after precondition. No connection modulation. 01: Float type operation. Pulse connection from input to TIA with modulation pulse, floating between pulses. 10: Nonfloat type connection modulation. Pulse connection from input to TIA. Connect to precondition value between pulses.	0x0	R/W
0x0228	PERIOD_J	[11:10]	Reserved	Reserved.	0x0	R
0x0248 0x0268	PERIOD_K PERIOD_L	[9:0]	MIN_PERIOD_x	Minimum Period for Pulse Repetition in µs. Override for the automatically calculated period. Used in float type operations to set the float time of the second and subsequent floats using the formula: Float Time = MIN_PERIOD_x – MOD_WIDTH_x.	0x0	R/W
0x010A 0x012A 0x014A	INTEG_SETUP_A INTEG_SETUP_B INTEG_SETUP_C	15	SINGLE_INTEG_x	Use single integrator pulse. 0: use both generated integrator clocks. 1: skip the second integrator clock.	0x0	R/W
0x016A 0x018A 0x01AA 0x01CA	INTEG_SETUP_D INTEG_SETUP_E INTEG_SETUP_F INTEG_SETUP_G	[14:12]	CH2_AMP_DISABLE_x	Amplifier disables for power control. Set the appropriate bit to disable the Channel 2 amplifier in Time Slot x. 0: TIA. 1: band-pass filter. 2: integrator.	0x0	R/W
0x01EA	INTEG_SETUP_H	11	AFE_INT_C_BUF_x	Set to 1 to configure the integrator as a buffer in Time Slot x.	0x0	R/W
0x020A 0x022A 0x024A 0x026A	INTEG_SETUP_I INTEG_SETUP_J INTEG_SETUP_K INTEG_SETUP_L	[10:8]	CH1_AMP_DISABLE_x	Amplifier disables for power control. Set the appropriate bit to disable the Channel 1 amplifier in Time Slot x. 0: TIA. 1: band-pass filter. 2: integrator.	0x0	R/W
		[7:6]	ADC_COUNT_x	ADC Conversions per Pulse. Number of conversions = ADC_COUNT + 1.	0x0	R/W
		5	Reserved	Reserved.	0x0	R

REGISTER DETAILS

Table 33. Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
		[4:0]	INTEG_WIDTH_A	Integrator Clock Width in µs. Must be >0.	0x3	R/W
0x010B	INTEG_OS_A	[15:13]	Reserved	Reserved.	0x0	R
0x012B	INTEG_OS_B	[12:0]	INTEG_ OFFSET_x	Integrator Clock Offset for Time Slot x in 31.25 ns Increments per LSB. Must be >1 µs (0x0020).	0x0214	R/W
0x014B	INTEG_OS_C					
0x016B	INTEG_OS_D					
0x018B	INTEG_OS_E					
0x01AB	INTEG_OS_F					
0x01CB	INTEG_OS_G					
0x01EB	INTEG_OS_H					
0x020B	INTEG_OS_I					
0x022B	INTEG_OS_J					
0x024B	INTEG_OS_K					
0x026B	INTEG_OS_L					
0x010C	MOD_PULSE_A	[15:8]	MOD_WIDTH_x	Modulation Pulse Width for Time Slot x in µs. 0 = disable.	0x0	R/W
0x012C	MOD_PULSE_B	[7:0]	MOD_OFFSET_x	Modulation Pulse Offset for Time Slot x in µs. Must be >0.	0x1	R/W
0x014C	MOD_PULSE_C					
0x016C	MOD_PULSE_D					
0x018C	MOD_PULSE_E					
0x01AC	MOD_PULSE_F					
0x01CC	MOD_PULSE_G					
0x01EC	MOD_PULSE_H					
0x020C	MOD_PULSE_I					
0x022C	MOD_PULSE_J					
0x024C	MOD_PULSE_K					
0x026C	MOD_PULSE_L					
0x0113	DIGINT_LIT_A	[15:9]	Reserved	Reserved.	0x0	R
0x0133	DIGINT_LIT_B	[8:0]	LIT_OFFSET_x	Digital Integration Mode, Acquisition Window Lit Offset in µs for Time Slot x. Also, impulse response mode offset. Must be >0.	0x26	R/W
0x0153	DIGINT_LIT_C					
0x0173	DIGINT_LIT_D					
0x0193	DIGINT_LIT_E					
0x01B3	DIGINT_LIT_F					
0x01D3	DIGINT_LIT_G					
0x01F3	DIGINT_LIT_H					
0x0213	DIGINT_LIT_I					
0x0233	DIGINT_LIT_J					
0x0253	DIGINT_LIT_K					
0x0273	DIGINT_LIT_L					
0x0114	DIGINT_DARK_A	[15:7]	DARK2_OFFSET_x	Digital Integration Mode, Acquisition Window Dark Offset 2 for Time Slot x in µs. Must be >0.	0x046	R/W
0x0134	DIGINT_DARK_B					
0x0154	DIGINT_DARK_C	[6:0]	DARK1_OFFSET_x	Digital Integration Mode, Acquisition Window Dark Offset 1 for Time Slot x in µs. Must be >0.	0x6	R/W
0x0174	DIGINT_DARK_D					
0x0194	DIGINT_DARK_E					
0x01B4	DIGINT_DARK_F					
0x01D4	DIGINT_DARK_G					
0x01F4	DIGINT_DARK_H					
0x0214	DIGINT_DARK_I					
0x0234	DIGINT_DARK_J					
0x0254	DIGINT_DARK_K					

REGISTER DETAILS

Table 33. Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x0274	DIGINT_DARK_L					

LED CONTROL AND TIMING REGISTERS

Table 34. Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x0105 0x0125 0x0145	LED_POW12_A LED_POW12_B LED_POW12_C	15	LED_DRIVESIDE2_x	LED Output Select for LED2x. 0: drive LED on Output LED2A.	0x0	R/W
0x0165 0x0185 0x01A5	LED_POW12_D LED_POW12_E LED_POW12_F	[14:8]	LED_CURRENT2_x	LED Current Setting for LED2A Output. Set to 0 to disable. Output current varies monotonically from 2 mA to 200 mA for values between 0x01 and 0x7F.	0x0	R/W
0x01C5 0x01E5 0x0205	LED_POW12_G LED_POW12_H LED_POW12_I	7	LED_DRIVESIDE1_x	LED Output Select for LED1x. 0: drive LED on Output LED1A.	0x0	R/W
0x0225 0x0245 0x0265	LED_POW12_J LED_POW12_K LED_POW12_L	[6:0]	LED_CURRENT1_x	LED Current Setting for LED1A Output. Set to 0 to disable. Output current varies monotonically from 2 mA to 200 mA for values between 0x01 and 0x7F.	0x0	R/W
0x0106 0x0126 0x0146	LED_POW34_A LED_POW34_B LED_POW34_C	15	LED_DRIVESIDE4_x	LED Output Select for LED4x. 0: drive LED on Output LED4A.	0x0	R/W
0x0166 0x0186 0x01A6	LED_POW34_D LED_POW34_E LED_POW34_F	[14:8]	LED_CURRENT4_x	LED Current Setting for LED4A Output. Set to 0 to disable. Output current varies monotonically from 2 mA to 200 mA for values between 0x01 and 0x7F.	0x0	R/W
0x01C6 0x01E6 0x0206	LED_POW34_G LED_POW34_H LED_POW34_I	7	LED_DRIVESIDE3_x	LED Output Select for LED3x. 0: drive LED on Output LED3A.	0x0	R/W
0x0226 0x0246 0x0266	LED_POW34_J LED_POW34_K LED_POW34_L	[6:0]	LED_CURRENT3_x	LED Current Setting for LED3A Output. Set to 0 to disable. Output current varies monotonically from 2 mA to 200 mA for values between 0x01 and 0x7F.	0x0	R/W
0x0109	LED_PULSE_A	[15:8]	LED_WIDTH_x	LED Pulse Width in µs. 0 = disable.	0x2	R/W
0x0129 0x0149 0x0169 0x0189 0x01A9 0x01C9 0x01E9 0x0209 0x0229 0x0249 0x0269	LED_PULSE_B LED_PULSE_C LED_PULSE_D LED_PULSE_E LED_PULSE_F LED_PULSE_G LED_PULSE_H LED_PULSE_I LED_PULSE_J LED_PULSE_K LED_PULSE_L	[7:0]	LED_OFFSET_x	LED Pulse Offset in µs. Set to a minimum of 16 µs (0x10). Must be >0.	0x10	R/W

REGISTER DETAILS

ADC OFFSET REGISTERS

Table 35. Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x010E	ADC_OFF1_A	[15:14]	Reserved	Reserved.	0x0	R
0x012E	ADC_OFF1_B	[13:0]	CH1_ADC_ADJUST_x	Adjustment to ADC Value. This value is subtracted from the ADC value for Channel 1 in Time Slot x. Set to 0 for chop and float modes.	0x0	R/W
0x014E	ADC_OFF1_C					
0x016E	ADC_OFF1_D					
0x018E	ADC_OFF1_E					
0x01AE	ADC_OFF1_F					
0x01CE	ADC_OFF1_G					
0x01EE	ADC_OFF1_H					
0x020E	ADC_OFF1_I					
0x022E	ADC_OFF1_J					
0x024E	ADC_OFF1_K					
0x026E	ADC_OFF1_L					
0x010F	ADC_OFF2_A	15	ZERO_ADJUST_x	Additive Offset for Signal Value. Set to 1 to add 2048 to the signal value prior to clipping positive.	0x0	R/W
0x012F	ADC_OFF2_B	14	Reserved	Reserved.		
0x014F	ADC_OFF2_C	[13:0]	CH2_ADC_ADJUST_x	Adjustment to ADC Value. This value is subtracted from the ADC value for Channel 2 in Time Slot x. Set to 0 for chop and float modes.	0x0	R/W
0x016F	ADC_OFF2_D					
0x018F	ADC_OFF2_E					
0x01AF	ADC_OFF2_F					
0x01CF	ADC_OFF2_G					
0x01EF	ADC_OFF2_H					
0x020F	ADC_OFF2_I					
0x022F	ADC_OFF2_J					
0x024F	ADC_OFF2_K					
0x026F	ADC_OFF2_L					

OUTPUT DATA REGISTERS

Table 36. Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x002F	FIFO_DATA	[15:0]	FIFO_DATA	FIFO Data Port.	0x0	R
0x0030	SIGNAL1_L_A	[15:0]	SIGNAL1_L_A	Signal Channel 1 lower half Time Slot A	0x0	R
0x0031	SIGNAL1_H_A	[15:0]	SIGNAL1_H_A	Signal Channel 1 upper half Time Slot A	0x0	R
0x0032	SIGNAL2_L_A	[15:0]	SIGNAL2_L_A	Signal Channel 2 lower half Time Slot A	0x0	R
0x0033	SIGNAL2_H_A	[15:0]	SIGNAL2_H_A	Signal Channel 2 upper half Time Slot A	0x0	R
0x0034	DARK1_L_A	[15:0]	DARK1_L_A	Dark Channel 1 value lower half Time Slot A	0x0	R
0x0035	DARK1_H_A	[15:0]	DARK1_H_A	Dark Channel 1 value upper half Time Slot A	0x0	R
0x0036	DARK2_L_A	[15:0]	DARK2_L_A	Dark Channel 2 value lower half Time Slot A	0x0	R
0x0037	DARK2_H_A	[15:0]	DARK2_H_A	Dark Channel 2 value upper half Time Slot A	0x0	R
0x0038	SIGNAL1_L_B	[15:0]	SIGNAL1_L_B	Signal Channel 1 lower half Time Slot B	0x0	R
0x0039	SIGNAL1_H_B	[15:0]	SIGNAL1_H_B	Signal Channel 1 upper half Time Slot B	0x0	R
0x003A	SIGNAL2_L_B	[15:0]	SIGNAL2_L_B	Signal Channel 2 lower half Time Slot B	0x0	R
0x003B	SIGNAL2_H_B	[15:0]	SIGNAL2_H_B	Signal Channel 2 upper half Time Slot B	0x0	R
0x003C	DARK1_L_B	[15:0]	DARK1_L_B	Dark Channel 1 value lower half Time Slot B	0x0	R
0x003D	DARK1_H_B	[15:0]	DARK1_H_B	Dark Channel 1 value upper half Time Slot B	0x0	R
0x003E	DARK2_L_B	[15:0]	DARK2_L_B	Dark Channel 2 value lower half Time Slot B	0x0	R
0x003F	DARK2_H_B	[15:0]	DARK2_H_B	Dark Channel 2 value upper half Time Slot B	0x0	R

REGISTER DETAILS

Table 36. Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x0040	SIGNAL1_L_C	[15:0]	SIGNAL1_L_C	Signal Channel 1 lower half Time Slot C	0x0	R
0x0041	SIGNAL1_H_C	[15:0]	SIGNAL1_H_C	Signal Channel 1 upper half Time Slot C	0x0	R
0x0042	SIGNAL2_L_C	[15:0]	SIGNAL2_L_C	Signal Channel 2 lower half Time Slot C	0x0	R
0x0043	SIGNAL2_H_C	[15:0]	SIGNAL2_H_C	Signal Channel 2 upper half Time Slot C	0x0	R
0x0044	DARK1_L_C	[15:0]	DARK1_L_C	Dark Channel 1 value lower half Time Slot C	0x0	R
0x0045	DARK1_H_C	[15:0]	DARK1_H_C	Dark Channel 1 value upper half Time Slot C	0x0	R
0x0046	DARK2_L_C	[15:0]	DARK2_L_C	Dark Channel 2 value lower half Time Slot C	0x0	R
0x0047	DARK2_H_C	[15:0]	DARK2_H_C	Dark Channel 2 value upper half Time Slot C	0x0	R
0x0048	SIGNAL1_L_D	[15:0]	SIGNAL1_L_D	Signal Channel 1 lower half Time Slot D	0x0	R
0x0049	SIGNAL1_H_D	[15:0]	SIGNAL1_H_D	Signal Channel 1 upper half Time Slot D	0x0	R
0x004A	SIGNAL2_L_D	[15:0]	SIGNAL2_L_D	Signal Channel 2 lower half Time Slot D	0x0	R
0x004B	SIGNAL2_H_D	[15:0]	SIGNAL2_H_D	Signal Channel 2 upper half Time Slot D	0x0	R
0x004C	DARK1_L_D	[15:0]	DARK1_L_D	Dark Channel 1 value lower half Time Slot D	0x0	R
0x004D	DARK1_H_D	[15:0]	DARK1_H_D	Dark Channel 1 value upper half Time Slot D	0x0	R
0x004E	DARK2_L_D	[15:0]	DARK2_L_D	Dark Channel 2 value lower half Time Slot D	0x0	R
0x004F	DARK2_H_D	[15:0]	DARK2_H_D	Dark Channel 2 value upper half Time Slot D	0x0	R
0x0050	SIGNAL1_L_E	[15:0]	SIGNAL1_L_E	Signal Channel 1 lower half Time Slot E	0x0	R
0x0051	SIGNAL1_H_E	[15:0]	SIGNAL1_H_E	Signal Channel 1 upper half Time Slot E	0x0	R
0x0052	SIGNAL2_L_E	[15:0]	SIGNAL2_L_E	Signal Channel 2 lower half Time Slot E	0x0	R
0x0053	SIGNAL2_H_E	[15:0]	SIGNAL2_H_E	Signal Channel 2 upper half Time Slot E	0x0	R
0x0054	DARK1_L_E	[15:0]	DARK1_L_E	Dark Channel 1 value lower half Time Slot E	0x0	R
0x0055	DARK1_H_E	[15:0]	DARK1_H_E	Dark Channel 1 value upper half Time Slot E	0x0	R
0x0056	DARK2_L_E	[15:0]	DARK2_L_E	Dark Channel 2 value lower half Time Slot E	0x0	R
0x0057	DARK2_H_E	[15:0]	DARK2_H_E	Dark Channel 2 value upper half Time Slot E	0x0	R
0x0058	SIGNAL1_L_F	[15:0]	SIGNAL1_L_F	Signal Channel 1 lower half Time Slot F	0x0	R
0x0059	SIGNAL1_H_F	[15:0]	SIGNAL1_H_F	Signal Channel 1 upper half Time Slot F	0x0	R
0x005A	SIGNAL2_L_F	[15:0]	SIGNAL2_L_F	Signal Channel 2 lower half Time Slot F	0x0	R
0x005B	SIGNAL2_H_F	[15:0]	SIGNAL2_H_F	Signal Channel 2 upper half Time Slot F	0x0	R
0x005C	DARK1_L_F	[15:0]	DARK1_L_F	Dark Channel 1 value lower half Time Slot F	0x0	R
0x005D	DARK1_H_F	[15:0]	DARK1_H_F	Dark Channel 1 value upper half Time Slot F	0x0	R
0x005E	DARK2_L_F	[15:0]	DARK2_L_F	Dark Channel 2 value lower half Time Slot F	0x0	R
0x005F	DARK2_H_F	[15:0]	DARK2_H_F	Dark Channel 2 value upper half Time Slot F	0x0	R
0x0060	SIGNAL1_L_G	[15:0]	SIGNAL1_L_G	Signal Channel 1 lower half Time Slot G	0x0	R
0x0061	SIGNAL1_H_G	[15:0]	SIGNAL1_H_G	Signal Channel 1 upper half Time Slot G	0x0	R
0x0062	SIGNAL2_L_G	[15:0]	SIGNAL2_L_G	Signal Channel 2 lower half Time Slot G	0x0	R
0x0063	SIGNAL2_H_G	[15:0]	SIGNAL2_H_G	Signal Channel 2 upper half Time Slot G	0x0	R
0x0064	DARK1_L_G	[15:0]	DARK1_L_G	Dark Channel 1 value lower half Time Slot G	0x0	R
0x0065	DARK1_H_G	[15:0]	DARK1_H_G	Dark Channel 1 value upper half Time Slot G	0x0	R
0x0066	DARK2_L_G	[15:0]	DARK2_L_G	Dark Channel 2 value lower half Time Slot G	0x0	R
0x0067	DARK2_H_G	[15:0]	DARK2_H_G	Dark Channel 2 value upper half Time Slot G	0x0	R
0x0068	SIGNAL1_L_H	[15:0]	SIGNAL1_L_H	Signal Channel 1 lower half Time Slot H	0x0	R
0x0069	SIGNAL1_H_H	[15:0]	SIGNAL1_H_H	Signal Channel 1 upper half Time Slot H	0x0	R
0x006A	SIGNAL2_L_H	[15:0]	SIGNAL2_L_H	Signal Channel 2 lower half Time Slot H	0x0	R
0x006B	SIGNAL2_H_H	[15:0]	SIGNAL2_H_H	Signal Channel 2 upper half Time Slot H	0x0	R
0x006C	DARK1_L_H	[15:0]	DARK1_L_H	Dark Channel 1 value lower half Time Slot H	0x0	R
0x006D	DARK1_H_H	[15:0]	DARK1_H_H	Dark Channel 1 value upper half Time Slot H	0x0	R
0x006E	DARK2_L_H	[15:0]	DARK2_L_H	Dark Channel 2 value lower half Time Slot H	0x0	R
0x006F	DARK2_H_H	[15:0]	DARK2_H_H	Dark Channel 2 value upper half Time Slot H	0x0	R

REGISTER DETAILS

Table 36. Register Details

Addr	Name	Bits	Bit Name	Description	Reset	Access
0x0070	SIGNAL1_L_I	[15:0]	SIGNAL1_L_I	Signal Channel 1 lower half Time Slot I	0x0	R
0x0071	SIGNAL1_H_I	[15:0]	SIGNAL1_H_I	Signal Channel 1 upper half Time Slot I	0x0	R
0x0072	SIGNAL2_L_I	[15:0]	SIGNAL2_L_I	Signal Channel 2 lower half Time Slot I	0x0	R
0x0073	SIGNAL2_H_I	[15:0]	SIGNAL2_H_I	Signal Channel 2 upper half Time Slot I	0x0	R
0x0074	DARK1_L_I	[15:0]	DARK1_L_I	Dark Channel 1 value lower half Time Slot I	0x0	R
0x0075	DARK1_H_I	[15:0]	DARK1_H_I	Dark Channel 1 value upper half Time Slot I	0x0	R
0x0076	DARK2_L_I	[15:0]	DARK2_L_I	Dark Channel 2 value lower half Time Slot I	0x0	R
0x0077	DARK2_H_I	[15:0]	DARK2_H_I	Dark Channel 2 value upper half Time Slot I	0x0	R
0x0078	SIGNAL1_L_J	[15:0]	SIGNAL1_L_J	Signal Channel 1 lower half Time Slot J	0x0	R
0x0079	SIGNAL1_H_J	[15:0]	SIGNAL1_H_J	Signal Channel 1 upper half Time Slot J	0x0	R
0x007A	SIGNAL2_L_J	[15:0]	SIGNAL2_L_J	Signal Channel 2 lower half Time Slot J	0x0	R
0x007B	SIGNAL2_H_J	[15:0]	SIGNAL2_H_J	Signal Channel 2 upper half Time Slot J	0x0	R
0x007C	DARK1_L_J	[15:0]	DARK1_L_J	Dark Channel 1 value lower half Time Slot J	0x0	R
0x007D	DARK1_H_J	[15:0]	DARK1_H_J	Dark Channel 1 value upper half Time Slot J	0x0	R
0x007E	DARK2_L_J	[15:0]	DARK2_L_J	Dark Channel 2 value lower half Time Slot J	0x0	R
0x007F	DARK2_H_J	[15:0]	DARK2_H_J	Dark Channel 2 value upper half Time Slot J	0x0	R
0x0080	SIGNAL1_L_K	[15:0]	SIGNAL1_L_K	Signal Channel 1 lower half Time Slot K	0x0	R
0x0081	SIGNAL1_H_K	[15:0]	SIGNAL1_H_K	Signal Channel 1 upper half Time Slot K	0x0	R
0x0082	SIGNAL2_L_K	[15:0]	SIGNAL2_L_K	Signal Channel 2 lower half Time Slot K	0x0	R
0x0083	SIGNAL2_H_K	[15:0]	SIGNAL2_H_K	Signal Channel 2 upper half Time Slot K	0x0	R
0x0084	DARK1_L_K	[15:0]	DARK1_L_K	Dark Channel 1 value lower half Time Slot K	0x0	R
0x0085	DARK1_H_K	[15:0]	DARK1_H_K	Dark Channel 1 value upper half Time Slot K	0x0	R
0x0086	DARK2_L_K	[15:0]	DARK2_L_K	Dark Channel 2 value lower half Time Slot K	0x0	R
0x0087	DARK2_H_K	[15:0]	DARK2_H_K	Dark Channel 2 value upper half Time Slot K	0x0	R
0x0088	SIGNAL1_L_L	[15:0]	SIGNAL1_L_L	Signal Channel 1 lower half Time Slot L	0x0	R
0x0089	SIGNAL1_H_L	[15:0]	SIGNAL1_H_L	Signal Channel 1 upper half Time Slot L	0x0	R
0x008A	SIGNAL2_L_L	[15:0]	SIGNAL2_L_L	Signal Channel 2 lower half Time Slot L	0x0	R
0x008B	SIGNAL2_H_L	[15:0]	SIGNAL2_H_L	Signal Channel 2 upper half Time Slot L	0x0	R
0x008C	DARK1_L_L	[15:0]	DARK1_L_L	Dark Channel 1 value lower half Time Slot L	0x0	R
0x008D	DARK1_H_L	[15:0]	DARK1_H_L	Dark Channel 1 value upper half Time Slot L	0x0	R
0x008E	DARK2_L_L	[15:0]	DARK2_L_L	Dark Channel 2 value lower half Time Slot L	0x0	R
0x008F	DARK2_H_L	[15:0]	DARK2_H_L	Dark Channel 2 value upper half Time Slot L	0x0	R

OUTLINE DIMENSIONS

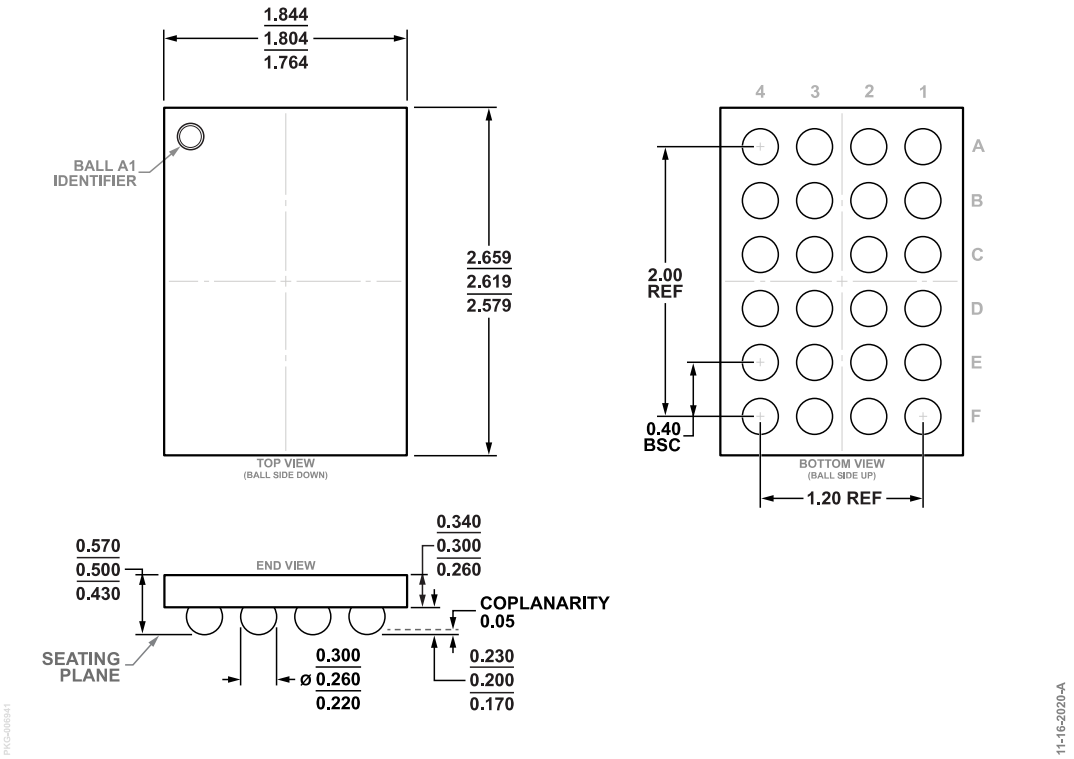

Figure 42. 24-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-24-5)
Dimensions shown in millimeters

Updated: February 18, 2022

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADPD4200BCBZR7	-40°C to +85°C	CHIPS W/SOLDER BUMPS/WLCSP	Reel, 1500	CB-24-5

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1, 2]	Description
EVAL-ADPD4200Z-PPG	Evaluation Board
EVAL-ADPDUCZ	Microcontroller Board

[1] Z = RoHS-Compliant Part.

[2] The EVAL-ADPDUCZ is the microcontroller board, ordered separately, which is required to interface with the EVAL-ADPD4200Z-PPG evaluation board.

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