

## ADuC7020 Evaluation Board Reference Guide MicroConverter<sup>®</sup> ADuC7020 Development System

by Aude Richard

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### OVERVIEW

The ADuC7020 evaluation board has the following features:

- 2-layer PCB (4" × 5" form factor)
- 9 V power supply regulated to 3.3 V on board
- 4-pin UART header to connect to RS232 interface cable
- 20-pin standard JTAG connector to connect to ULINK emulator
- Demonstration circuit
- 32.768 kHz watch crystal to drive the PLL clock
- ADR291 2.5 V external reference chip
- Reset/Download/IRQ0 push-buttons
- Power indicator/general-purpose LEDs
- Access to all ADC inputs and DAC outputs from external header. All device ports are brought out to external header pins.
- Surface-mount and through-hole general-purpose prototype area

### Notes

1. This document refers to the MicroConverter ADuC7020 Evaluation Board Rev. A.
2. All references in this document to physical orientation of components on the board are made with respect to a component side view of the board, with the prototype area appearing in the bottom of the board.
3. The board is laid out to minimize coupling between the analog and digital sections of the board. The ground plane is split with the analog section on the left-hand side and a digital plane on the right-hand side of the board. The regulated 3.3 V power supply is routed directly to the digital section, and is filtered before being routed into the analog section of the board.

REV. 0

### FEATURES

#### Power Supply

The user should connect the 9 V power supply via the 2.1 mm input power socket (J5). The input connector is configured as CENTER NEGATIVE, i.e., GND on the center pin and 9 V on the outer shield.

This 9 V supply is regulated via a linear voltage regulator (U5). The 3.3 V regulator output is used to directly drive the digital side of the board. The 3.3 V supply is also filtered, and is then used to supply the analog side of the board.

When on, the red LED (D3) indicates that a valid 3.3 V supply is being driven from the regulator circuit. All active components are decoupled with 0.1  $\mu$ F at device supply pins to ground.

#### RS232 Interface

The ADuC7020 (U1) P1.1 and P1.0 lines are connected to the RS232 interface cable via connector (J1). The interface cable generates the required level shifting to allow direct connection to a PC serial port. Ensure that the cable supplied is connected to the board correctly, i.e., DV<sub>DD</sub> is connected to DV<sub>DD</sub>, and DGND is connected to DGND.

#### Emulation Interface

Nonintrusive emulation and download are possible on the ADuC7020 via JTAG by connecting the ULINK emulator to the J4 connector.

#### Crystal Circuit

The board is fitted with a 32.768 kHz crystal from which the on-chip PLL circuit can generate a 45 MHz clock.

#### External Reference (ADR291)

The external 2.5 V reference chip (U2) has two functions. It is provided on the evaluation board to demonstrate the external reference option of the ADuC7020, but its main purpose is to generate the V<sub>OCM</sub> voltage of the differential amplifier, if required.

#### Reset/Download/IRQ0 Push-Buttons

A RESET push-button is provided to allow the user to manually reset the part. When inserted, the RESET pin of the ADuC7020 is pulled to DGND. Because the RESET pin on the ADuC7020 is Schmitt-triggered internally, there is no need to use an external Schmitt trigger on this pin.

When inserted, the IRQ0 push-button switch drives

P0.4/IRQ0 high. This can be used to initiate an external interrupt 0.

To enter serial download mode, the user must pull the P0.0/BM pin low while reset is toggled. On the evaluation board, serial download mode can be easily initiated by holding down the serial download push-button (S2) while inserting and releasing the reset button (S3), as illustrated in Figure 1.

### Power Indicator/General-Purpose LEDs

A red power LED (D3) is used to indicate that a sufficient supply is available on the board. A general-purpose LED (D2) is directly connected to P4.2 of the ADuC7020. When P4.2 is cleared, the LED is turned on; when P4.2 is set, the LED is turned off.

### Analog I/O Connections

All analog I/O connections are brought out on header J3.

ADC0 and ADC1 are buffered using an AD8606 to evaluate single-ended and pseudo differential mode. A potentiometer can be connected to ADC0 buffered. ADC3 and ADC4 can be buffered with a single-ended-to-differential op amp on board, with the AD8132 used to evaluate the ADC in fully differential mode.

ADC2 is not buffered. Be sure to follow the data sheet recommendations when connecting signals to this input.

DAC1 can be used to control the brightness of the green LED, D1, when connected via the S1 switch.

### General-Purpose Prototype Area

A general-purpose prototype area is provided at the bottom of the evaluation board for adding external components as required in the user's application. As can be seen from the layout, AV<sub>DD</sub>, AGND, V<sub>DDIO</sub>, and DGND tracks are provided in this prototype area.

### DIP SWITCH LINK OPTIONS

#### S1-1 V<sub>REF</sub>

**Function:** Connects the output of the 2.5 V external reference (ADR291) to the V<sub>REF</sub> pin (Pin 35) of the ADuC7020.

**Use:** *Slide S1-1 to the ON position* to connect the external reference to the ADuC7020.

*Slide S1-1 to the OFF position* to use the internal 2.5 V reference or a different external reference on the V<sub>REF</sub> pin of the J3 header.

#### S1-2 V<sub>OCM</sub>

**Function:** Connects 1.67 V to the V<sub>OCM</sub> pin of the AD8132. No extra dc voltage is required on the board to use the ADC in differential mode.

**Use:** *Slide S1-2 to the ON position* to connect V<sub>OCM</sub> of the differential amplifier to 1.67 V, divided output of the ADR291 reference.

*Slide S1-2 to the OFF position* to use a different voltage for V<sub>OCM</sub> by connecting a dc voltage to the V<sub>OCM</sub> pin of the J3 header. Note that V<sub>OCM</sub> value is dependent on reference value, as shown in Table I.

Table I. V<sub>OCM</sub> Range

V <sub>REF</sub>	V <sub>OCM min</sub>	V <sub>OCM max</sub>
2.5 V	1.25 V	2.05 V
2.048 V	1.024 V	2.276 V
1.25 V	0.75 V	2.55 V

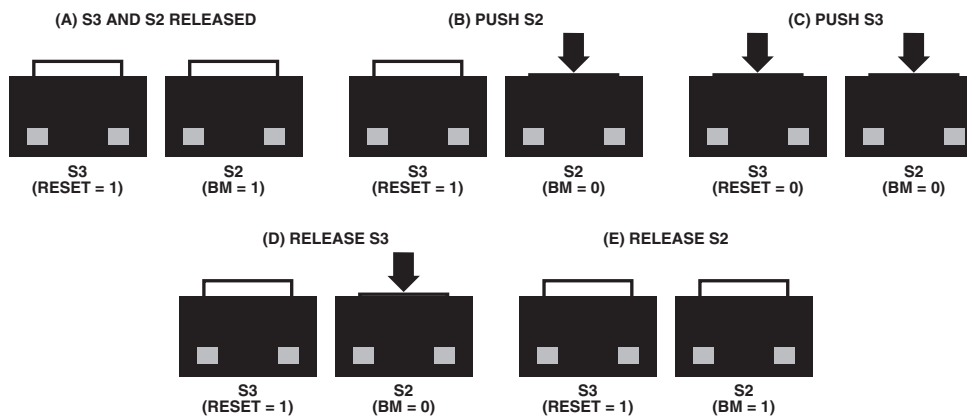


Figure 1. Entering Serial Download Mode on the Evaluation Board

**S1-3 POT**

**Function:** Connects the potentiometer output to ADC0. This input is buffered by an AD8606. This is for demonstration purposes.

**Use:** **Slide S1-3 to the ON position** to connect the potentiometer to the op amp of the ADC0 input channel.

**Slide S1-3 to the OFF position** to use the ADC0 input on the J3 header.

**S1-4 ADC3**

**Function:** Brings out ADC3 (Pin 1) on the J3 header.

**Use:** **Slide S1-6 to the ON position** to connect ADC3 of the J3 header directly to the ADC3 pin (Pin 1) of the ADuC7020.

**Slide S1-6 to the OFF Position** to disconnect ADC3 of the J3 header from the ADC3 pin (Pin 1) of the ADuC7020.

**S1-5 VIN-**

**Function:** Connects -OUT of the single-ended-to-differential op amp (AD8132) to ADC3. S1-5 and S1-6 must be used together when VIN- is in the ON position; VIN+ must also be in the ON position to use the differential op amp on channels ADC3 and ADC4.

**Use:** **Slide S1-5 to the ON position** to connect -OUT of the AD8132 to ADC3.

**Slide S1-5 to the OFF position** to use ADC3 without the AD8132.

**S1-6 VIN+**

**Function:** Connects +OUT of the single-ended-to-differential op amp (AD8132) to ADC4. When VIN+ is in the ON position, VIN- must also be in the ON position to use the differential op amp on channels ADC3 and ADC4.

**Use:** **Slide S1-6 to the ON position** to connect +OUT of AD8132 to ADC4.

**Slide S1-6 to the OFF position** to use ADC4 without the AD8132.

**S1-7 ADC4**

**Use:** **Slide S1-6 to the ON position** to connect ADC4 of the J3 header directly to the ADC4 pin (Pin 2) of the ADuC7020.

**Slide S1-6 to the OFF position** to disconnect ADC4 of the J3 header from the ADC4 pin (Pin 2) of the ADuC7020.

**S1-8 LED**

**Function:** Connects the DAC1 output to the green LED of the demo circuit, D1.

**Use:** **Slide S1-7 to the ON position** to connect the DAC1 output to D1.

**Slide S1-7 to the OFF position** to use the DAC1 output on the J3 header.

**EXTERNAL CONNECTORS****J3 Analog I/O Connector**

The analog I/O connector J3 provides external connections for all ADC inputs, reference inputs, and DAC outputs. The pinout of the connector is shown in Table II.

Table II. Pin Functions for Analog I/O Connector J3

Pin No.	Pin Description
J3-1	AV <sub>DD</sub>
J3-2	AGND
J3-3	V <sub>REF</sub>
J3-4	ADC0
J3-5	ADC1
J3-6	ADC2
J3-7	ADC3
J3-8	ADC4
J3-9	V <sub>DIFF</sub>
J3-10	V <sub>OCM</sub>
J3-11	DAC0
J3-12	DAC1
J3-13	DAC2
J3-14	DAC3

**J5 Power Supply Connection**

J5 allows for the connection between the evaluation board and the 9 V power supply provided in the ADuC7020 development system.

**J4 Emulation Connector**

J4 provides a connection of the evaluation board to the PC via a USB cable and ULINK provided in the ADuC7020 development system.

**J1 Serial Interface Connector**

J1 provides a simple connection of the evaluation board to the PC via a PC serial port cable provided with the ADuC7020 development system.

**J6 I<sup>2</sup>C<sup>®</sup> Interface Connector**

J6 provides a simple access to the two I<sup>2</sup>C interfaces of the ADuC7020.

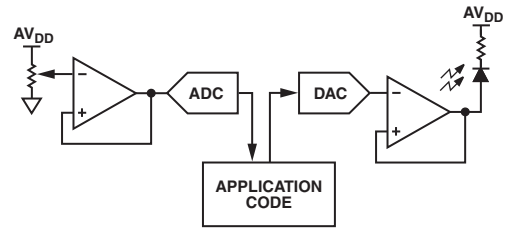
## J2 Digital I/O Connector

The digital I/O connector J2 provides external connections for all GPIOs. The pinout of the connector with pin function descriptions is shown in Table III.

**Table III. Pin Functions for Digital I/O Connector J2**

Pin No.	Pin Description
J2-1	<b>DGND</b>
J2-2	<b>P4.2</b> PLAO[10]
J2-3	<b>P1.0</b> SIN/SCL/PLAI[0]
J2-4	<b>P1.1</b> SOUT/SDA/PLAI[1]
J2-5	<b>P1.2</b> RTS/PLAI[2]
J2-6	<b>P1.3</b> CTS/PLAI[3]
J2-7	<b>P1.4</b> RI/CLK/PLAI[4]
J2-8	<b>P1.5</b> DCD/MISO/PLAI[5]
J2-9	<b>P1.6</b> DSR/MOSI/PLAI[6]
J2-10	<b>P1.7</b> DTR/CSL/PLAO[0]
J2-11	<b>P0.7</b> ECLK/SIN/PLAO[4]
J2-12	<b>P2.0</b> CONV/SOUT/PLAO[5]
J2-13	<b>P0.5</b> IRQ1/ADC <sub>BUSY</sub> /PLAO[2]
J2-14	<b>P0.4</b> IRQ0/ PLAO[1]
J2-15	<b>P0.3</b> TRST/ADC <sub>BUSY</sub>
J2-16	<b>P0.6</b> MRST/PLAO[3]
J2-17	<b>P0.0</b> CMP/PLAI[7]
J2-18	<b>DGND</b>

## POTENTIOMETER DEMONSTRATION CIRCUIT



*Figure 2. Circuit Diagram of the RTD Circuit*

Using the sample code in `\code\adc\pot.c`, the variation in the potentiometer resistance can be seen on the output LED. Note that the internal reference and external reference are 2.5 V, which gives an ADC input range of 0 V to 2.5 V in single-ended mode. The potentiometer can give a voltage between 0 V and  $AV_{DD} = 3.3$  V.

## ADuC7020 EVALUATION BOARD PARTS LIST

Component	Qty.	Part	Description	Order No.	Order From
EVAL-ADuC7020QS QuickStart™ PCB	1	PCB-1	2-Sided Surface-Mount PCB		
PCB Stand-Off	4	Stand-Off	Stick-On Mounting Feet	148-922	Farnell
U1	1	ADuC7020	MicroConverter (64-CSP)	ADuC7020CP	ADI
U2	1	ADR291	Band Gap Reference	ADR291ER	ADI
U3	1	AD8132	Differential Op Amp	AD8132ARM	ADI
U4	1	AD8606	Dual Op Amp, (8-Lead SOIC)	AD8606AR	ADI
U5	1	ADP3333	Fixed 3.3 V Linear Voltage Regulator	ADP3333ARM3.3	ADI
Y1	1	32.768 kHz	Watch Crystal	316-0312	Farnell
S1	1	SW\8-DIP	8-Way DIP Switch	566-718	Farnell
S2, S3, S4	3	Push-Button Switch	PCB-Mounted Push-Button Switch	177-807	Farnell
D1, D2, D3	3	LED	1.8 mm Miniature LED	515-620	Farnell
D4	1	PRLL4002	Diode	BAV103DITR-ND	Digi-Key
C1, C5, C13, C15, C18, C22, C23	7	10 $\mu$ F	Surface-Mount Tantalum Cap, Taj-B Case	197-130	Farnell
C2-C4, C6, C12, C14, C16, C17	8	0.1 $\mu$ F	Surface-Mount Ceramic Cap, 0603 Case	317-287	Farnell
C7, C8	2	22 pF	Surface-Mount Ceramic Cap, 0603 Case	722-005	Farnell
C11, C19	2	470 nF	Surface-Mount Ceramic Cap, 0603 Case	318-8851	Farnell
R1	1	10 k $\Omega$ Potentiometer	0.25 W, 4 Series, 4 mm Square Sealed	307-1741	Farnell
R2	1	100 $\Omega$	Surface-Mount Resistor, 0603 Case	911-732	Farnell
R3	1	200 $\Omega$	Surface-Mount Resistor, 0603 Case	321-7978	Farnell
R4	1	49.9 $\Omega$	Surface-Mount Resistor, 0805 Case	422-1825	Farnell
R5, R6, R8, R9	4	348 $\Omega$	Surface-Mount Resistor, 0603 Case	422-2570	Farnell
R7	1	24.9 $\Omega$	Surface-Mount Resistor, 0805 Case	422-1539	Farnell
R10, R11	2	60.4 $\Omega$	Surface-Mount Resistor, 0805 Case	422-1904	Farnell
R12, R18, R20	2	270 $\Omega$	Surface-Mount Resistor, 0603 Case	613-022	Farnell
R13, R14	2	0 $\Omega$	Surface-Mount Resistor, 0603 Case	772-227	Farnell
R15-R17	4	1 k $\Omega$	Surface-Mount Resistor, 0603 Case	911-239	Farnell
R19	1	1.5 $\Omega$	Surface-Mount Resistor, 0603 Case	758-267	Farnell
R21, R22, R24	3	100 k $\Omega$	Surface-Mount Resistor, 0603 Case	911-471	Farnell
L1	1	Ferrite Bead	Surface-Mount Inductor, 1206 Case	581-094	Farnell
J1	1	4-Pin Header	4-Pin 90° Single Row Header	TSM-104-02-T-SH	Samtec
J2	1	18-Pin Header	18-Pin Straight Single Row Header	TSM-118-01-T-SV	Samtec
J3	1	14-Pin Header	14-Pin Straight Single Row Header	TSM-114-01-T-SV	Samtec
J4	1	20-Pin Header	20-Pin Connector	IMP-BV(SMT)-20	Imperial-Connect
J5	1		PCB-Mounted Socket (2 mm Pin Diameter)	KLD-SMT2-0202-A	Kycon

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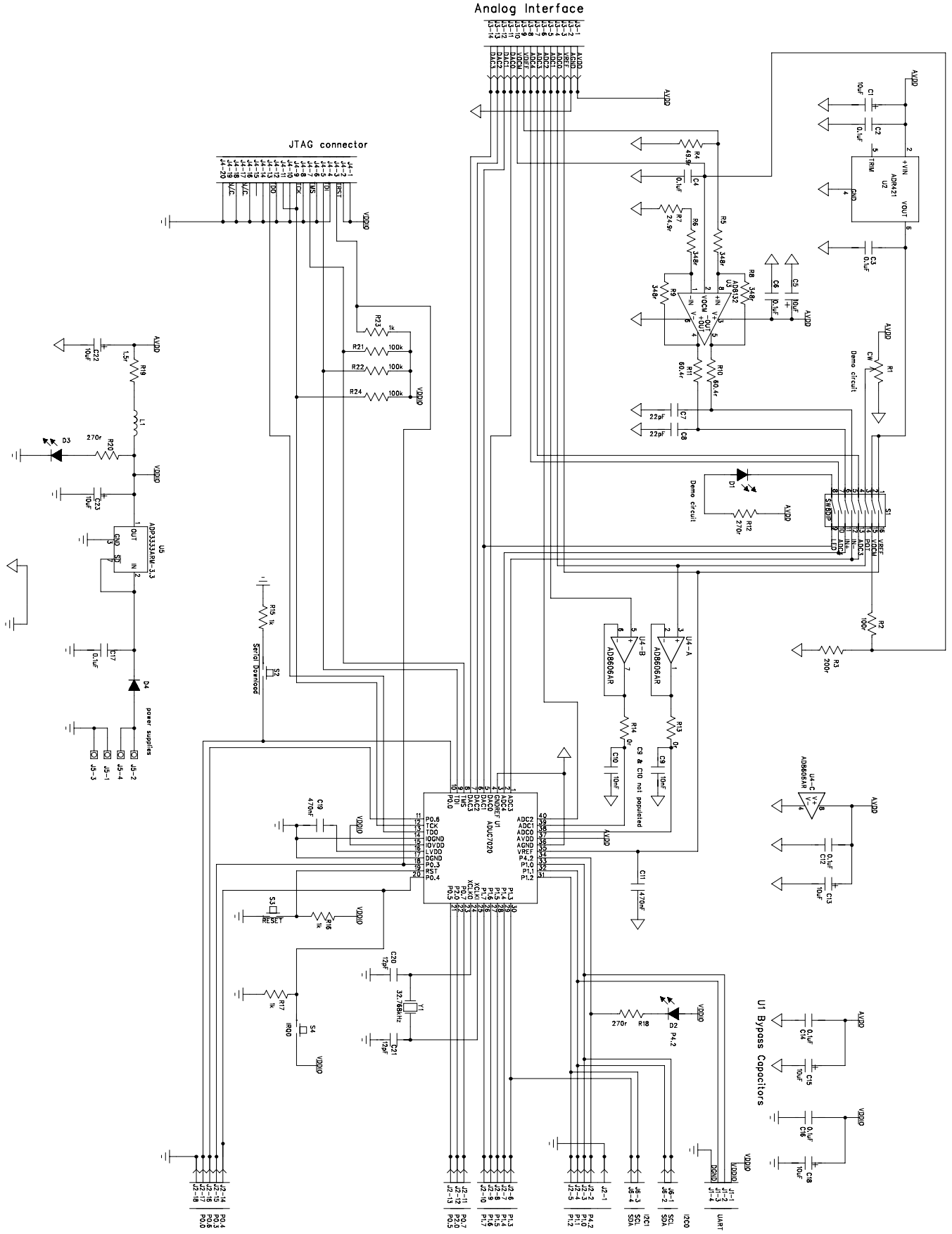
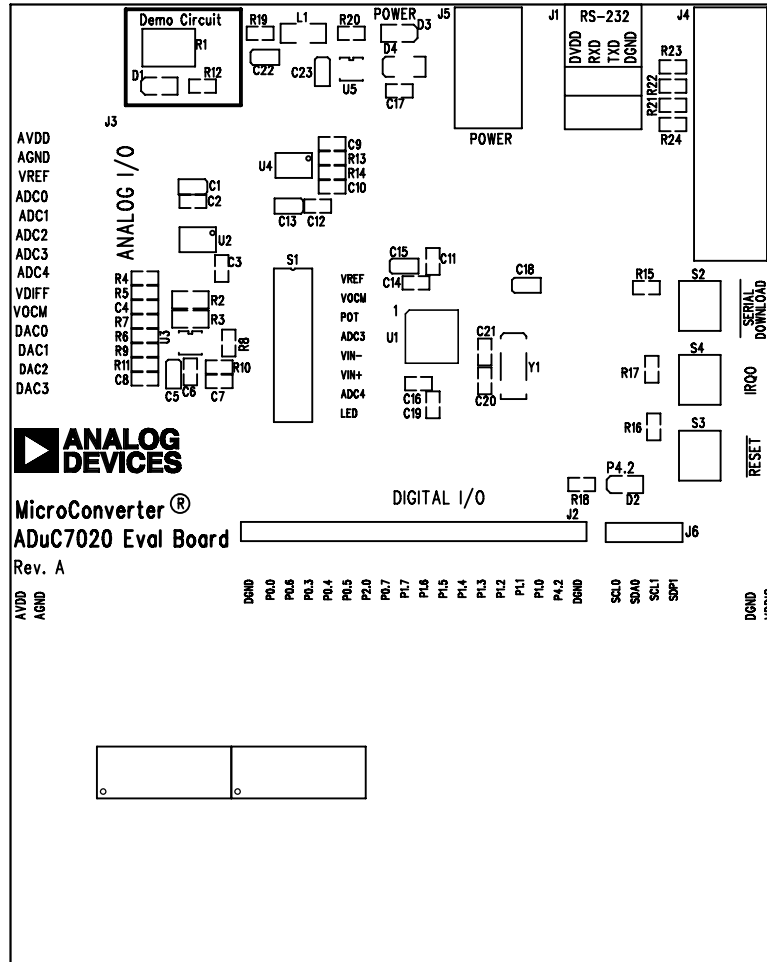


Figure 3. ADuC7020 Evaluation Board Schematic



ADuC7020 EVALUATION BOARD Rev. A- Component Side View

Silkscreen Top

Figure 4. ADuC7020 Evaluation Board Silkscreen





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