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**Devices Connected/Referenced**

<a href="#">AD5422</a>	16-Bit Current and Voltage Output DAC
<a href="#">AD5700-1</a>	Low Power HART Modem with Internal RC Oscillator
<a href="#">ADP2441</a>	36 V, 1 A, Synchronous, Step-Down DC-to-DC Regulator
<a href="#">ADuM3471</a>	Quad Isolator with Integrated Transformer Driver and PWM Controller
<a href="#">ADuM3482</a>	Small, 3.75 kV rms Quad Digital Isolator

## Fully Isolated, Single Channel Voltage and 4 mA to 20 mA Output with HART Connectivity

### EVALUATION AND DESIGN SUPPORT

#### Circuit Evaluation Boards

[CN0321 Evaluation Board \(EVAL-CN0321-SDPZ\)](#)

[System Demonstration Platform \(EVAL-SDP-CB1Z\)](#)

#### Design and Integration Files

[Schematics](#), [Layout Files](#), [Bill of Materials](#)

### CIRCUIT FUNCTION AND BENEFITS

This circuit provides a complete, fully isolated, analog output channel suitable for programmable logic controllers (PLCs) and distributed control system (DCS) modules that require standard 4 mA to 20 mA HART<sup>®1</sup>-compatible current outputs and unipolar or bipolar output voltage ranges. It provides a flexible building block for channel-to-channel isolated PLC/DCS output modules or any other industrial application that requires a fully isolated analog output. The circuit also includes external protection on the analog output terminals.

The [AD5422](#) 16-bit digital-to-analog converter (DAC) is software configurable and provides all the necessary current and voltage outputs.

The [AD5700-1](#), the industry's lowest power and smallest footprint HART-compliant IC modem, is used in conjunction with the [AD5422](#) to form a complete HART-compatible 4 mA to 20 mA solution. The [AD5700-1](#) includes a precision internal oscillator that provides additional space savings, especially in channel-to-channel isolated applications.

PLC/DCS solutions must be isolated from the local system controller to protect against ground loops and to ensure robustness against external events. Traditional solutions use discrete ICs for both power and digital isolation. When multichannel isolation is needed, the cost and space of providing discrete power solutions becomes a big disadvantage. Solutions based on optoisolators typically have reasonable output regulation but require additional external components, thereby increasing board area. Power modules are often bulky and can provide poor output regulation. The circuit in Figure 1 uses the [ADuM347x](#) family of isolators and power regulation circuitry along with associated feedback isolation. External transformers are used to transfer power across the isolation barrier.

The [ADuM3482](#) provides the UART signal isolation for the [AD5700-1](#).

The [ADP2441](#), 36 V step-down dc-to-dc regulator, accepts an industrial standard 24 V supply, with wide tolerance on the input voltage. It steps this down to 5 V to power all controller side circuitry. The circuit also includes standard external protection on the 24 V supply terminals, as well as protection against dc overvoltage of +36 V down to -28 V.

<sup>1</sup> HART is a registered trademark of the HART Communication Foundation.

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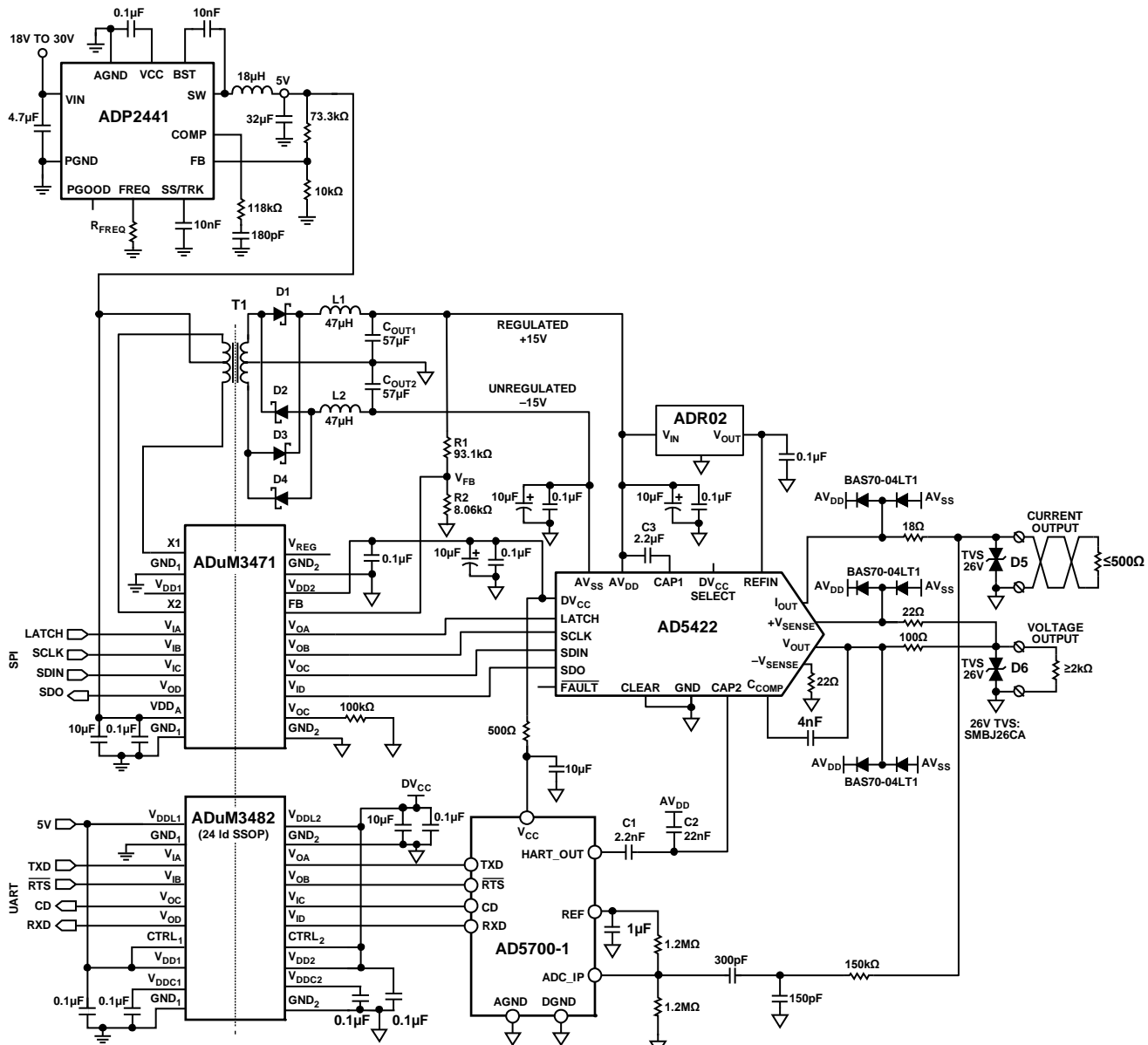


Figure 1. Functional Block Diagram (Simplified Schematic: All Connections and Decoupling Not Shown)

## CIRCUIT DESCRIPTION

### Analog Output

For industrial control modules, standard analog output voltage and current ranges include  $\pm 5$  V,  $\pm 10$  V, 0 V to +5 V, 0 V to +10 V, +4 mA to +20 mA, and 0 mA to +20 mA. The [AD5422](#) is a precision, fully integrated 16-bit DAC that offers a programmable current source and programmable voltage output designed to meet the requirements of industrial process control applications.

The [AD5422](#) provides all the output ranges previously listed, with the current output ranges and voltage output ranges available on separate pins. An overrange feature of 10% is available on all the voltage ranges, and a 0 mA to 20 mA overrange is available on the current output. Analog outputs are short- and open-circuit protected.

The [AD5422](#) has an on-board 10 ppm/ $^{\circ}$ C reference. For higher performance over temperature, this design uses an [ADR02](#) reference. The [ADR02](#) is a 5 V precision reference that allows for an input voltage of up to 36 V. It has a 0.05% maximum accuracy error and a 3 ppm/ $^{\circ}$ C maximum temperature drift. This drift contributes approximately 0.02% error across the industrial temperature range.

The [AD5422](#) allows for an internal or external precision, current setting resistor for the current output circuitry. This design uses the internal current sensing resistor option; however, even higher accuracy can be achieved by using a precision external 15 k $\Omega$  resistor.

By leaving the DV<sub>CC</sub> SELECT pin of the [AD5422](#) floating, an internal 4.5 V power supply is connected to the DV<sub>CC</sub> pin which is used as a digital power supply for the [AD5700-1](#) and the field side of the isolators. Alternatively, the 5 V output low dropout (LDO) regulator on the [ADuM3471](#) can be used. The LDO provides a tighter regulated 5 V rail; however, it does not allow for dc overvoltages of greater than 20 V due to the absolute maximum ratings on the regulator input pin of the [ADuM3471](#).

The output connector configuration for the [EVAL-CN0321-SDPZ](#) hardware is shown in Table 1.

**Table 1. Output Terminals**

Terminal Name	Output Type
OUT2	Voltage output ranges
GND	Ground
OUT1	Current output ranges

### HART Compatibility

The [AD5700-1](#) is used in conjunction with the [AD5422](#) to form a complete HART-compatible 4 mA to 20 mA solution. The [AD5700-1](#) 0.5% precision internal oscillator provides significant space savings in channel-to-channel isolated applications where a clock crystal would otherwise be needed per channel. The crystal would typically be bigger than the [AD5700-1](#) IC itself; therefore, the internal oscillator results in significant space saving.

The HART modem output is attenuated by C1 and C2 and ac-coupled into the [AD5422](#) via the CAP2 pin. Additional information can be found in the [AN-1065 Application Note](#). Circuit Note [CN-0278](#) describes an alternate HART coupling method using the R<sub>SET</sub> pin that offers greater power supply rejection; however, it requires an external precision current setting resistor.

### Isolated Power

The voltage output headroom required by the [AD5422](#) is 0.8 V maximum, and the current output needs a 2.5 V headroom maximum. Therefore, a >12.5 V supply is required to output a 20 mA current through a 500 Ω load. In this design, the minimum supply voltage (overtemperature) is no lower than 13.5 V, which allows for some additional headroom.

The [ADuM347x](#) devices are quad-channel digital isolators with integrated pulse-width modulation (PWM) controllers and low impedance transformer drivers (X1 and X2). The only additional components required for an isolated dc-to-dc converter are a transformer and simple full-wave diode rectifier. The devices provide up to 2 W of regulated, isolated power when supplied from a 5.0 V or 3.3 V input, which eliminates the need for a separate isolated dc-to-dc converter.

The *iCoupler*® chip-scale transformer technology is used to isolate the logic signals, and the integrated transformer driver with isolated secondary side control provides high efficiency for the isolated dc-to-dc converter. The internal oscillator frequency is adjustable from 200 kHz to 1 MHz and is determined by the R<sub>OC</sub> value. When R<sub>OC</sub> = 100 kΩ, the switching frequency is 500 kHz.

The [ADuM3471](#) regulation is from the positive 15 V supply. The feedback for regulation is from the divider network (R1 and R2). The resistors are chosen such that the feedback voltage is 1.25 V when the output voltage is 15 V. The feedback voltage is compared with the [ADuM3471](#) internal feedback setpoint voltage of 1.25 V. Regulation is achieved by varying the duty cycle of the PWM signals driving the external transformer.

The negative supply is loosely regulated and could potentially be as low as -26.4 V if unloaded. For this reason, a 25 V Zener diode was placed on the negative supply. This diode draws a small current from the supply when it is lightly loaded; however, it ensures that it clamps at around 25 V.

Another approach is to use an isolation transformer with a 4:1 turns ratio; when it is unloaded, the negative rail does not go as low. In applications that require higher compliance voltages or very low power dissipation, a different power supply design should be considered.

### Input Power

The circuit in Figure 1 is powered by a 24 V supply. The [ADP2441](#) is used to step the 24 V down to 5 V to supply all controller side circuitry.

The [ADP2441](#) has a wide tolerance on its input supply, making it ideal for accepting a 24 V industrial supply. Because the [ADP2441](#) can accept up to 36 V, reliable transient protection of the supply input is also more easily achieved.

The [ADP2441](#) also features a number of other safety/reliability functions, such as undervoltage lockout (UVLO), a precision enable feature, a power good pin, and overcurrent limit protection. It can achieve up to 90% efficiency for an input of 24 V and an output of 5 V.

### Isolation

The [ADuM3471](#) power isolation circuitry includes four fully isolated voltage channels with a 2.5 kV isolation rating. These four channels are used to isolate the four data lines (SCLK, LATCH, SDIN, and SDO) of the [AD5422](#). Isolation of the SDO line is not essential for the operation of the circuit; however, it does allow access to diagnostic and fault features, as well as register readback.

The [ADuM3482](#) is a 3.75 kV quad channel digital isolator in a small 20-lead SSOP package (7.2 mm × 7.8 mm). The [ADuM3482](#) core operates between 3.0 V and 5.5 V, whereas the I/O supply can range from 1.8 V to 5.5 V. These devices can be used to interface directly with 1.8 V logic. This isolator is used to isolate the UART signals for the [AD5700-1](#) HART modem.

Further information on *iCoupler* products is available at [www.analog.com/icouplers](http://www.analog.com/icouplers).

### DC Overvoltage Protection

The circuit in Figure 1 allows for continuous +36 V and –28 V dc overvoltage protection. This means the circuit is protected in cases where a dc power supply line is accidentally connected to the output.

During an overvoltage condition, the supplies are pulled up or down via the external protection diodes. The resistance between these diodes and the output terminals limits the peak current.

The maximum/minimum voltage on the output terminals is limited by the breakdown voltage on any circuitry connected to the output or power supplies. The current and voltage outputs of the [AD5422](#) can tolerate +48 V down to –28 V. The  $AV_{SS}$  input can tolerate –28 V, and the  $AV_{DD}$  can tolerate +48 V. The [ADR02](#) reference can tolerate 36 V on its supply. The  $ADC_{IP}$  pin of the [AD5700-1](#) is protected by a 150 k $\Omega$  resistor that limits any current, followed by a 300 pF capacitor to block any dc current. Do not expose other ICs to higher voltages during the dc overvoltage condition.

### Transient Voltage Protection

The [AD5422](#) contains ESD protection diodes that prevent damage from normal handling. The industrial control environment can, however, subject I/O circuits to much higher transients. To protect the [AD5422](#) from excessively high voltage transients, external power diodes and a surge current limiting resistor may be required, as is shown in Figure 1.

The constraint on the resistor value in the current output path, shown in Figure 1 as 18  $\Omega$ , is that during normal operation, the output level at  $I_{OUT}$  must remain within its voltage compliance limit of  $AV_{DD} - 2.5$  V, and the two protection diodes and resistor must have the appropriate power ratings. With 18  $\Omega$ , for a 4 mA to 20 mA output, the compliance limit at the terminal is decreased by  $V = I_{MAX} \times R = 0.36$  V.

The constraint on the resistor value in the voltage output path, shown in Figure 1 as 100  $\Omega$ , is that there must be 0.8 V headroom over the output voltage. The effect of this resistor can be minimized by using the  $+V_{SENSE}$  input. Shown in Figure 1, the  $+V_{SENSE}$  input is protected by a 22  $\Omega$  resistor. There is also a corresponding 22  $\Omega$  resistor on the  $-V_{SENSE}$  path. These two 22  $\Omega$  resistors cause some absolute gain error that may need to be calibrated out at room temperature; the reason for this error is that there is only about 70 k $\Omega$  impedance in the internal feedback circuitry of the [AD5422](#). The advantage of sensing the voltage at the output and not at the  $V_{OUT}$  pin of the [AD5422](#) is that the protection resistor for the  $V_{OUT}$  pin has a varying voltage across it, depending on the load current drawn. Sensing at the terminal avoids this error source.

Further protection is provided with transient voltage suppressors (TVS) or transorbs. These are available as both unidirectional and bidirectional suppressors and in a wide range of standoff and breakdown voltage ratings. Size the TVS with the lowest breakdown voltage possible while not conducting in the functional range of the current output. As previously discussed, it is recommended that all remotely connected nodes be protected.

### COMMON VARIATIONS

This circuit is proven to work well with good stability and accuracy with the component values shown. When the application needs the 4 mA to 20 mA current output only, a single-supply scheme can be used. In this case, the positive  $AV_{DD}$  supply for the [AD5422](#) can be 24 V, for example, and the output compliance is  $24$  V  $-$   $2.5$  V =  $21.5$  V. With an output current of 20 mA, a load resistance as high as 1 k $\Omega$  is possible.

For applications not requiring 16-bit resolution, the 12-bit [AD5412](#) is available. For applications that require only current outputs, the [AD5420](#) (16-bit) and [AD5410](#) (12-bit) are available.

For applications that require voltage and current outputs on the same terminal, see [Circuit Note CN-0278](#) for a technique.

If overvoltage protection is not required, a reference with a lower maximum supply voltage can be used such as the [ADR4550](#) or the [ADR445](#).

The [ADuM347x](#) isolators ([ADuM3470](#), [ADuM3471](#), [ADuM3472](#), [ADuM3473](#), and [ADuM3474](#)) provide four independent isolation channels in a variety of input/output channel configurations. These devices are also available with either a maximum data rate of 1 Mbps (A grade) or 25 Mbps (C grade).

The [AD5700](#) modem can be used instead of the [AD5700-1](#); however, either an external crystal or a CMOS clock is required.

### CIRCUIT EVALUATION AND TEST

#### Equipment Required

The following equipment is required:

- The [EVAL-SDP-CB1Z](#) system demonstration platform (SDP-B)
- The [EVAL-CN0321-SDPZ](#) evaluation board and software
- A PC (Windows® 32-bit or 64-bit)
- A 24 V power supply
- A precision voltmeter, such as Agilent 34410A
- A digital test filter (such as the HCF\_TOOL-31 available from the HART Communication Foundation)
- A 500  $\Omega$  precision load resistor
- An oscilloscope, Tektronix DS1012B or equivalent

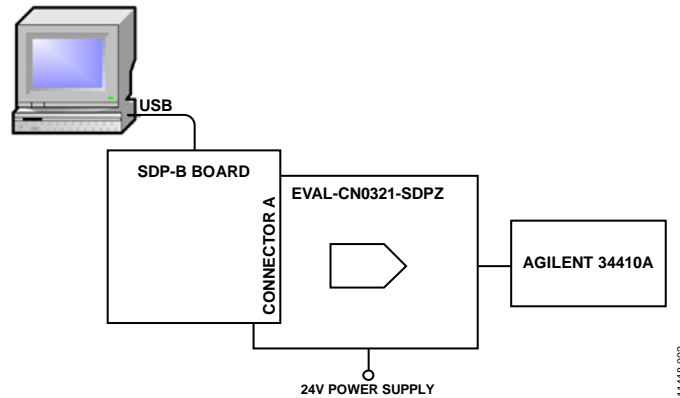


Figure 2. Test Setup Functional Diagram

### Test Setup Functional Diagram

A diagram of the test setup is shown in Figure 2.

### Software Installation

The evaluation kit includes self-installing software on a CD. The software is compatible with Windows XP (SP2), Vista (32-bit and 64-bit) or Windows 7 (32-bit and 64-bit). If the setup file does not run automatically, run the **setup.exe** file from the CD.

Install the evaluation software before connecting the evaluation board and SDP board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

1. Connect the [EVAL-SDP-CB1Z](#) via the USB port of the PC using the supplied cable.
2. Connect the [EVAL-CN0321-SDPZ](#) evaluation board to Connector A. If Connector B is used, the UART of the [EVAL-SDP-CB1Z](#) will not function as required.
3. Power up the [EVAL-CN0321-SDPZ](#) by applying 24 V to the J1 connector.
4. Start the [EVAL-CN0321-SDPZ](#) software and proceed through any dialog boxes that appear. This completes the installation.

### Software

The main software window is shown in Figure 3. Click **Advanced** for more options for configuring the [AD5422](#).

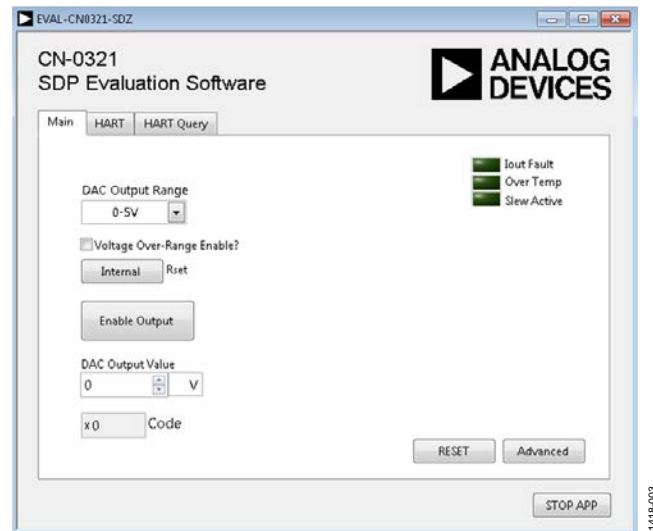


Figure 3. Main Software Window

For HART communications, ensure a current output range is enabled and then select the **HART** tab. From the **HART** tab, data can be entered into the **Command** box and sent over the 4 mA to 20 mA loop, and the software can be set to poll for any data on the 4 mA to 20 mA loop. Alternately, by selecting the **HART Query** tab, a connected HART-compatible actuator can be queried for its device address and device type.

**Absolute Accuracy Performance**

The specification for the total unadjusted error (TUE) for the AD5422 in current output mode using the internal R<sub>SET</sub> is 0.08% FSR typical at 25°C.

The total error of the ADR02 reference (B grade) is 0.06% maximum at 25°C.

Table 2 shows the measured current output error of the circuit for the 4 mA to 20 mA range.

**Table 2. Measured Current Output Error (4 mA to 20 mA Range)**

Code (Hex)	Current at Output (mA)	Error (%FSR)
0000	3.992	-0.049
4000	7.995	-0.034
8000	11.997	-0.018
B000	16.000	+0.001
FFFF	20.003	+0.020

The results are well within the expected values.

Similarly, for voltage output mode, the AD5422 TUE is 0.01% FSR typical at 25°C.

The ADR02 reference error (B grade) is 0.06% maximum at 25°C.

Table 3 shows the measured voltage output error for the circuit in the ±10 V output range.

**Table 3. Measured Voltage Output Error (±10 V Range)**

Code (Hex)	Voltage at Output (V)	Error (%FSR)
0000	-10.010	-0.050
4000	-5.005	-0.023
8000	+0.001	+0.003
B000	+5.006	+0.031
FFFF	+10.011	+0.057

The voltage output shown in Table 3 also includes the error in the circuit for the 22 Ω protection resistors on the +V<sub>SENSE</sub> and -V<sub>SENSE</sub> inputs of the AD5422. The +V<sub>SENSE</sub> and -V<sub>SENSE</sub> inputs are internally connected to a ~70 kΩ feedback resistor. The additional 22 Ω resistors externally add a gain error of roughly 22 kΩ/70 kΩ, or 0.031%. This initial error can be removed by calibration.

**Integral Nonlinearity (INL) Performance**

The INL of the AD5422 was tested using both linear supplies and the isolated dc-to-dc switching supplies to ensure no loss in system accuracy was incurred because of the switching supplies. Figure 4 shows the INL for both the linear supplies and the switching supplies. There is no noticeable performance loss when using the switching supplies as compared to the linear supplies.

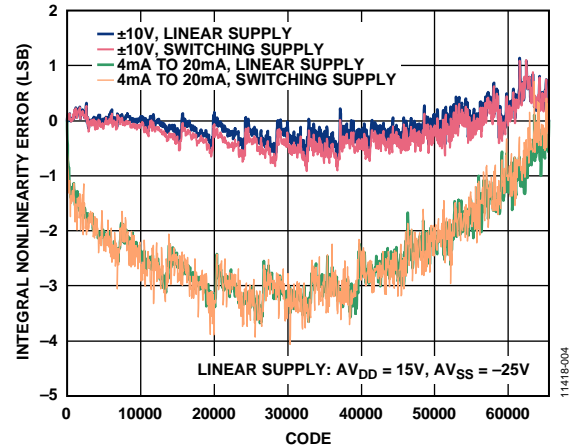


Figure 4. Measured INL of Circuit with Linear and Switching Supply

The average output noise was also tested and compared over time when using a linear supply and switching supply, as shown in Figure 5. Note that there is a slight offset in output noise measured over time. This offset is not much larger than 1 LSB and could be introduced by a slightly different measurement setup or the drift in the reference during the time between the two measurements.

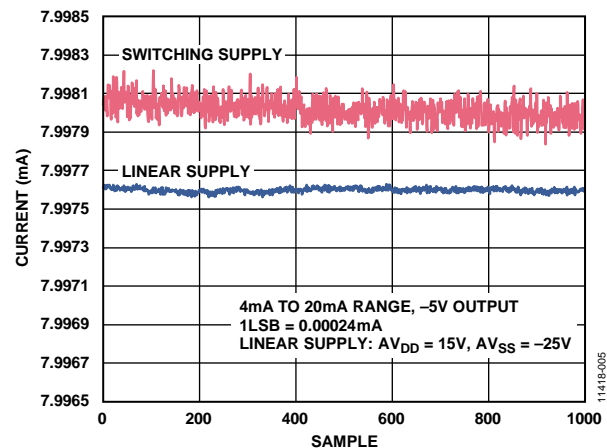


Figure 5. Measured Average DAC Output Noise, 1000 Sample, Meter Set to NPLC = 1

**HART Compliance**

For the circuit in Figure 1 to be HART-compliant, it must meet the HART physical layer specifications. There are a number of physical layer specifications included in the HART specification documents. For evaluating the performance of the hardware, the output noise during silence and the analog rate of change test were used.

### Output Noise During Silence Test

When a HART device is not transmitting (silence), it should not couple noise onto the network. Excessive noise may interfere with the reception of HART signals by the device itself or other devices on the network.

The voltage noise measured across a 500 Ω load in the loop must contain no more than 2.2 mV rms of combined broadband and correlated noise in the HART extended frequency band. In addition, the noise must not exceed 138 mV rms outside the HART extended frequency band.

This noise was measured by a true rms meter connected across the 500 Ω load. This noise was measured directly for the out-of-band noise and measured through the HCF\_TOOL-31 filter for the in-band noise. An oscilloscope was also used to examine the noise waveform.

The captured noise waveform is shown in Figure 6, and the results are summarized in Table 4.

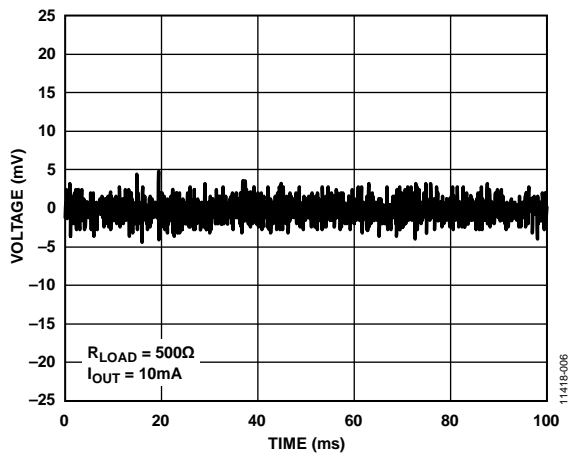


Figure 6. Output Noise During Silence Waveform

Table 4. Output Noise During Silence

Output Noise	Measured (mV)	
Outside Extended Frequency Range	0.6	<138
Inside Extended Frequency Range	0.126	<2.2

### Analog Rate of Change

The analog rate of change test ensures that when a device regulates the analog output current, the maximum rate of change of the analog current does not interfere with HART communications. Step changes in current disrupt HART signaling.

The worst-case change in the analog output current must not produce a disturbance higher than 15 mV peak, measured across a 500 Ω load in the HART extended frequency band.

The AD5422 DAC and output driver are relatively fast. Therefore, to meet the required system specifications, the output current change is limited by the hardware slew rate limit using capacitors on the CAP1 and CAP2 pins of the AD5422 and the digital slew rate control feature of the AD5422. This is outlined in more detail in the AN-1065 Application Note.

This test was performed using an oscilloscope coupled to a 500 Ω load through the HCF\_TOOL-31 filter.

The result is shown in Figure 7. The 4 mA and 20 mA output line (see blue line in Figure 7) shows the periodic steps between 4 mA and 20 mA, sensed directly across a 500 Ω load. The output of the filter × 10 line (see red line in Figure 7) is the signal captured on the HCF\_TOOL-31 filter output, amplified 10×, within the 150 mV peak limits.

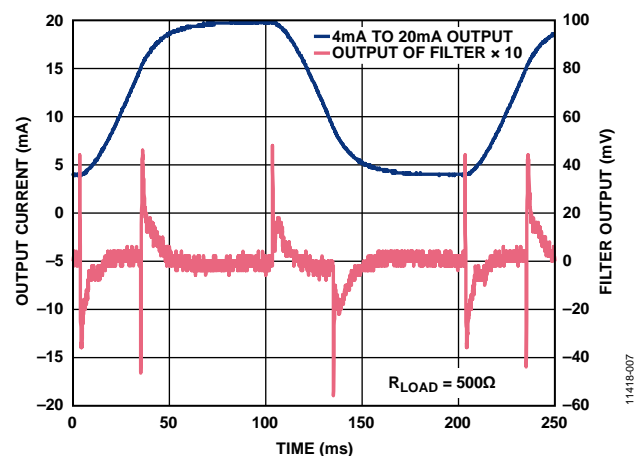


Figure 7. Analog Rate of Change Waveform

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CN-0321 Design Support Package:

<http://www.analog.com/CN0321-DesignSupport>

CN-0270, Complete 4 mA to 20 mA HART Solution

CN-0278, *Complete 4 mA to 20 mA HART Solution with Additional Voltage Output Capability*

Maurice Egan, *Configuring the AD5420 for HART Communication Compliance*, Application Note AN-1065, Analog Devices.

HART® Communication Foundation

**Data Sheets and Evaluation Boards**

[AD5422 Data Sheet](#)

[AD5700-1 Data Sheet](#)

[ADP2441 Data Sheet](#)

[ADuM3471 Data Sheet](#)

[ADuM3482 Data Sheet](#)

[System Demonstration Platform \(EVAL-SDP-CB1Z\)](#)

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