Circuits from the Lab® Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0369.

Devices Connected/Referenced	
ADL5801	High IP3,10 MHz to 6 GHz, Active Mixer
HMC512	VCO with Fo/2 & Divide-by-4 SMT, 9.6 GHz to 10.8 GHz
ADF4355-2	Microwave Wideband Synthesizer with Integrated VCO
AD8065	High Performance, 145 MHz FastFET Op Amp
ADP151	Ultralow Noise, 200 mA, CMOS Linear Regulator
ADM7150	800 mA Ultralow Noise, High PSRR, RF Linear Regulator
ADF4002	Phase Detector/PLL Frequency Synthesizer

Translation Phase Locked Loop Synthesizer with Low Phase Noise

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

- **CN-0369 Circuit Evaluation Board (EVAL-CN0369-SDPZ)**
- **System Demonstration Platforms (EVAL-SDP-CS1Z)**
- **ADL5801 Evaluation Board (ADL5801-EVALZ)**
- **ADF4355-2 Evaluation Board (EV-ADF4355-2SD1Z)**

Design and Integration Files

- **Schematics, Layout Files, Bill of Materials**

CIRCUIT FUNCTION AND BENEFITS

The circuit block diagram shown in Figure 1 is a low phase noise translation loop synthesizer (also known as an offset loop). This circuit translates the lower 100 MHz reference frequency of the ADF4002 phase locked loop (PLL) up to a higher frequency range of 5.0 GHz to 5.4 GHz, as determined by the frequency of the local oscillator (LO).

The translation loop synthesizer has very low phase noise (<50 fs) in contrast to a synthesizer using only a PLL. The low phase noise is because of the very low N value used by the ADF4002 integer-N PLL, which controls the voltage controlled oscillator (VCO). In this example, the ADF4002 phase frequency detector (PFD) runs at 100 MHz, and N = 1, yielding phase noise performance that is not limited by the N value of the PLL.

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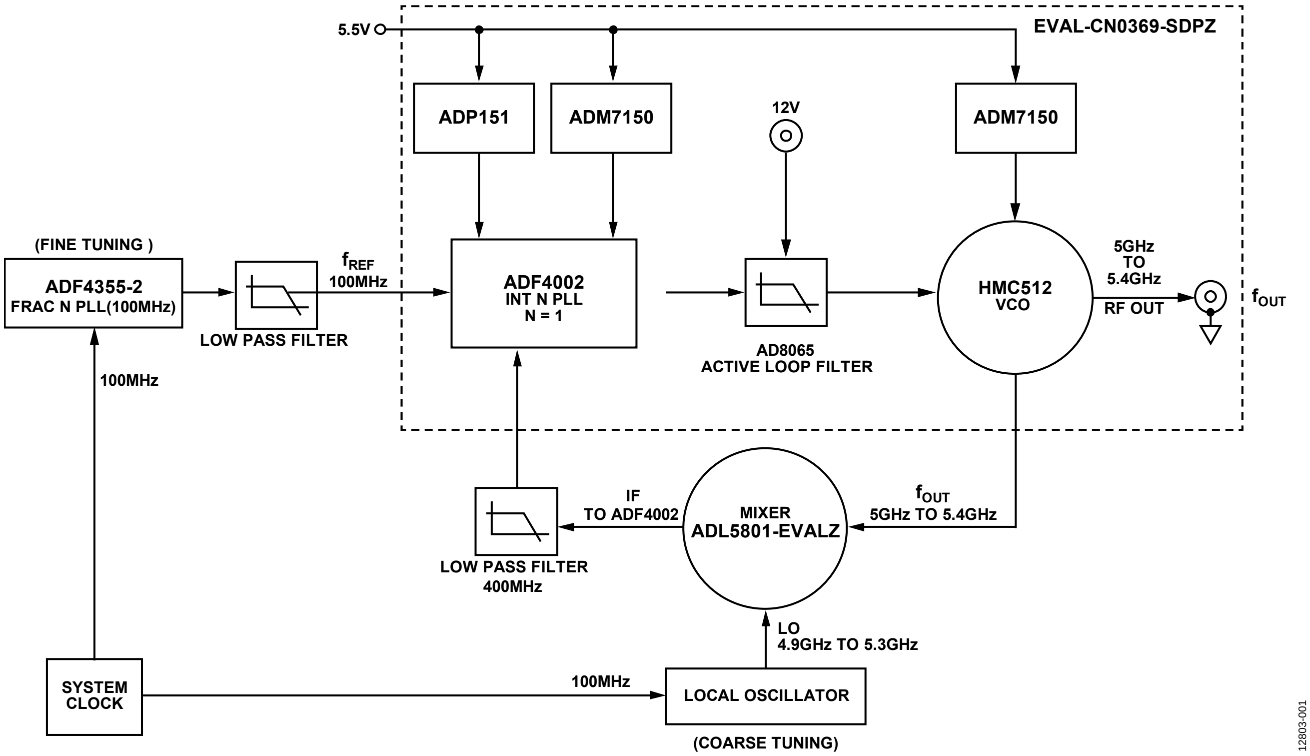

Figure 1. Block Diagram of the Translation Loop Synthesizer

CIRCUIT DESCRIPTION

In a standard PLL and VCO frequency synthesizer system, low phase noise is generally the primary objective. The phase noise in a PLL can be described as having two components: a flat noise component known as the PLL figure of merit (FOM), and a 1/f noise profile component known as the PLL 1/f, or flicker noise.

The PLL noise floor, PN_{TOT1}, is given by

$$PN_{TOT1} = PN_{SYNTH} + 20\log_{10}(N) + 10\log_{10}(f_{PFD}) \quad (1)$$

where:
PN_{SYNTH} is the synthesizer FOM and is device specific.
N is the divider used by the PLL.
f_{PFD} is the frequency of the phase frequency detector.

A PLL whose N value = 1 has a noise floor of $10\log_{10}(f_{PFD})$.

The PLL 1/f noise, PN_{TOT2}, is given by

$$PN_{TOT2} = PN_{1/f} + 20\log_{10}(f_{RF}/1\text{ GHz}) + 10\log_{10}(10\text{ kHz}/f) \quad (2)$$

where:
$PN_{1/f}$ is the data sheet PLL 1/f noise at an offset of 10 kHz from the output RF frequency (normalised to a 1 GHz output).
f_{RF} is the output RF frequency.

The total PLL noise, PN_{TOT}, is given by

$$PN_{TOT} = \sqrt{(PN_{TOT1})^2 + (PN_{TOT2})^2} \quad (3)$$

This equation indicates that the noise sources add in root-sum-square fashion; therefore, the larger noise source dominates.

A PLL with a very low N value has a phase noise dominated by the PLL 1/f noise.

The translation loop synthesizer decouples the required channel spacing from the N divider value to optimize the phase noise of the PLL. In this translation loop synthesizer example, N = 1.

The translation loop synthesizer in Figure 1 locks the higher frequency 4.8 GHz to 5.2 GHz VCO to the 100 MHz f_{REF} signal. The ADL5801 mixer and the LO together perform the divider function of this PLL.

With the LO in the feedback loop, the balance equation at the ADF4002 PLL becomes

$$f_{REF}/R = (f_{OUT} - f_{LO})/N$$

where N and R are the N and R divider values (in this circuit, R = 1 and N = 1).

The output frequency is therefore given by

$$f_{OUT} = f_{LO} + f_{REF}$$

ADF4355-2 Fractional-N Synthesizer

The ADF4355-2 in this circuit provides the reference frequency (f_{REF}) for the translation loop as shown in Figure 2.

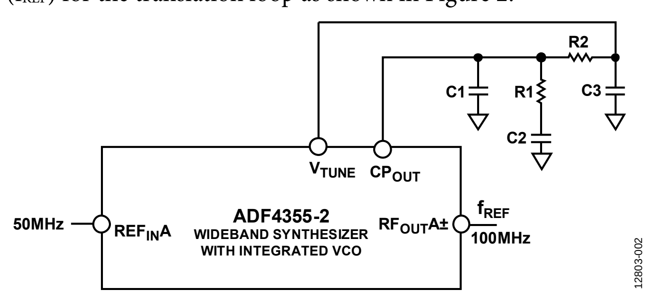

Figure 2. ADF4355-2 and Loop Filter

The ADF4355-2 is a wideband synthesizer with an integrated VCO providing an output frequency range from 55 MHz to 4400 MHz. The ADF4355-2 uses a high-resolution 38-bit modulus that allows very fine frequency resolution with no residual frequency error. The ADF4355-2 in this circuit uses a PFD of 50 MHz, and a loop bandwidth of 100 kHz. The Analog Devices ADIsimPLL tool was used to design and simulate the loop filter. Figure 3 shows the phase noise performance simulated by ADIsimPLL. A loop bandwidth (LBW) of 100 kHz was used, which is sufficient to allow the ADF4355-2 to provide the fine frequency tuning required.

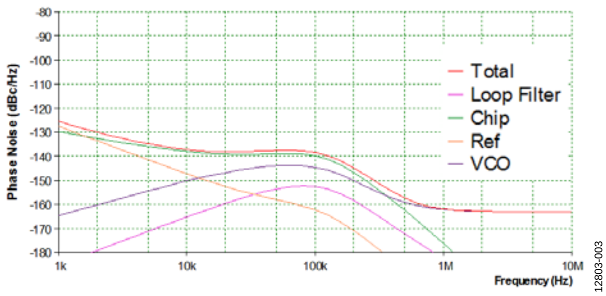

Figure 3. ADF4355-2 Simulated Output Phase Noise at 100 MHz from ADIsimPLL

The ADF4355-2 in this design operates with an internal VCO frequency of 6400 MHz. This high VCO frequency is divided by the maximum divider value of 64 to generate the 100 MHz RF output frequency. Adding a divider to the output of the VCO results in a 6 dB improvement in phase noise for each divide by 2. The divided VCO output contains harmonics inherent to the division process. A 100 MHz low pass filter is inserted at the RF output of the ADF4355-2 to filter these harmonics.

The simulated phase noise at an offset of 10 kHz is −137 dBc. The ADF4355-2 is the reference of choice for this translation loop because of its very low phase noise performance and very fine output frequency resolution.

Figure 4 shows a phase noise plot taken at the RFOUTA of the EV-ADF4355-2SD1Z.

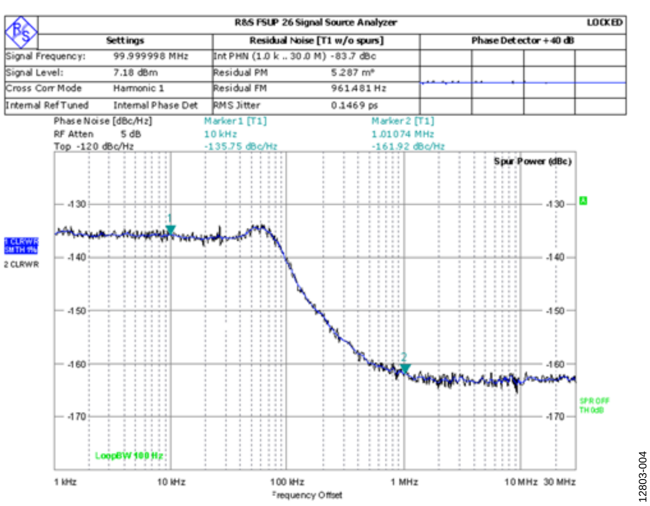

Figure 4. ADF4355-2, f_{OUT} = 100 MHz

ADF4002 Translation Loop Frequency Synthesizer

The ADF4002 is the translation loop frequency synthesizer, operating at a high PFD frequency of 100 MHz and a minimum N = 1. Operating at a high PFD frequency decreases the reference spurs and lowers N and thus phase noise. The translation loop frequency synthesizer uses integer-N PLL operation instead of fractional-N for better spurious performance. The ADF4002 meets the requirements for integer-N operation, a low minimum N value, and good phase noise performance. Fractional-N is not required because fine tuning is provided by the reference source. In this circuit, the RF input of the ADF4002 is driven by the 100 MHz IF output of the ADL5801 mixer.

The supply voltage for the ADF4002 internal charge pump is 5 V. However, many wideband VCOs require a tuning voltage of up to 18 V. A tuning voltage of 2 V to 12 V is required to drive the 9.6 GHZ to 10.8 GHz VCO. To accommodate this, an active loop filter is required. The active filter multiplies the output tuning range of the ADF4002 by the gain of the op amp.

The ADF4002 supports a programmable charge pump current feature that allows the user to modify the loop filter dynamics without changing the physical components. In this circuit, the LBW is 1 MHz using a charge pump current of 5 mA. The charge pump current can be modified to reduce or increase the LBW without physically changing the loop filter components.

Active Filter Using the AD8065

The AD8065 op amp has a 24 V supply voltage range, a gain bandwidth product (GBP) of approximately 145 MHz, and low noise (7 nV/√Hz). These features make it ideal for an active filter. For this application, a supply voltage of 12 V for the AD8065 is sufficient to provide the required output swing.

For most PLL applications, a phase margin of 45° to 55° is recommended to maintain a stable loop and to minimize settling time. In an active loop filter, that is, when there is an op amp in a loop filter, an additional pole occurs at the unity gain frequency (or gain bandwidth product) of the op amp. This additional pole adds extra phase lag; therefore, depending on the frequency of the pole, it can render the loop unstable.

The higher the ratio of GBP to LBW, the less phase lag. For example, Table 1 shows that a GBP/LBW ratio of 10 reduces the phase margin by 5.7°. If the GBP/LBW ratio is too low, the phase margin also becomes too low and results in an unstable loop.

Table 1. Phase Lag as a Function of GBP:LBW Ratio

GBP/LBW Ratio	Extra Phase Lag (°)
5 (such as GBP = 1 MHz, LBW = 200 kHz)	11.3
10	5.7
20	2.9

This circuit uses a 1 MHz LBW; therefore, the 145 MHz GBP of the AD8065 results in negligible phase lag (GBP/LBW = 145).

The AD8065 also acts as a buffer to mitigate the input capacitance of the VCO.

HMC512 VCO

The ADF4002 PLL locks the 100 MHz reference frequency to the HMC512 VCO frequency. The HMC512 has a primary frequency range from 9.6 GHz to 10.8 GHz. In this circuit, RFOUT/2 is used for the output signal (f_{OUT}) as well as the feedback RF to the mixer. High reverse isolation is required between the RF output (f_{OUT}) and the mixer to minimize LO to RF leakage. Choosing a VCO with a half frequency output provides reverse isolation. The typical RFOUT/2 power level of 8 dBm requires a 6 dB attenuation pad to reduce the power level to the mixer RF input recommended levels; in effect giving an additional 6 dB of reverse isolation.

The wide loop filter bandwidth high passes the VCO noise within the loop filter bandwidth. Outside the loop filter bandwidth, the VCO noise dominates. Therefore, a low noise VCO is required to achieve the low phase noise benefits from the circuit. The low noise of −110 dBc/Hz at 100 kHz along with the half frequency output of the HMC512 makes it a component of choice as the VCO to generate a 5.0 GHz to 5.4 GHz output in this circuit.

Local Oscillator and ADL5801 Mixer

The mixer selection for the translation loop must meet the following requirements:

- Operates in the required frequency range
- LO power levels matching the LO source
- High RF to LO isolation
- Low noise figure

The ADL5801 meets these requirements.

Figure 5 shows a block diagram of the ADL5801 mixer and the local oscillator. In general, an active mixer such as the ADL5801 (10 MHz to 6000 MHz) provides the required wideband operation, 35 dB to 40 dB of port to port isolation, and allows a typical −6 dBm to 0 dBm LO drive. The LO leakage degrades the spectral purity of the output signal. A low LO drive plus port to port isolation minimize LO to RF and LO to IF leakage.

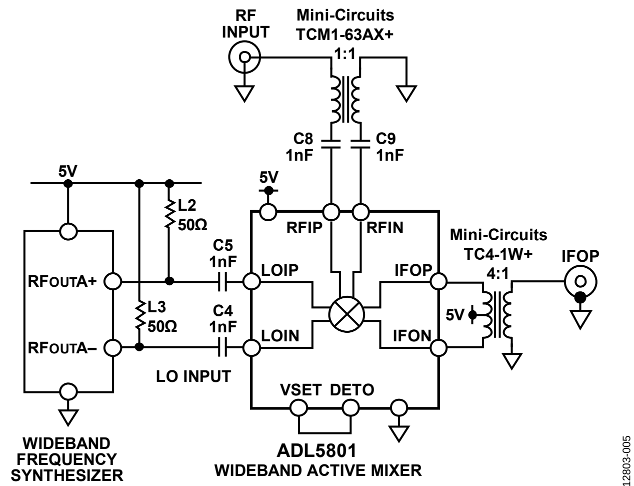

Figure 5. ADL5801 Mixer LO input

The local oscillator provides the coarse output frequency tuning in steps of 100 MHz with very low phase noise. For this circuit evaluation, the LO function is provided by a bench signal generator, such as the R&S SMA100.

Translation Loop Design and Performance

The core of this translation loop is the EVAL-CN0369-SDPZ board. Figure 6 shows a block diagram of the EVAL-CN0369-SDPZ, which uses the ADF4002 PLL, the AD8065 active loop filter, and the HMC512 VCO. The loop filter components for the active loop filter are shown in this diagram. ADIsimPLL is used to design the active loop filter.

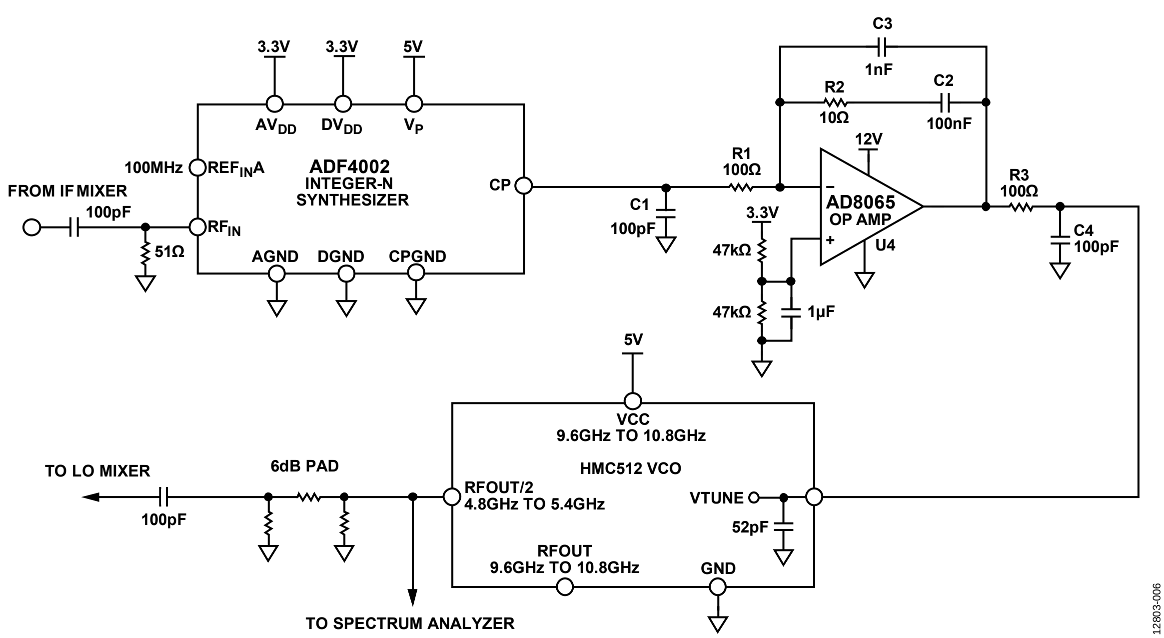

Figure 6. Block Diagram of EVAL-CN0369-SDPZ

The ADIsimPLL software is also used to design the loop filter of the translation loop PLL.

The simplest way to design a translation loop using ADIsimPLL is to replace the VCO/mixer/filter block with an equivalent VCO. If the VCO used tunes from 5.0 GHz to 5.4 GHz with K_V = 150 MHz/V, and the user mixes it with a 4.9 GHz to 5.3 GHz local oscillator, the PLL sees a VCO that tunes from 400 MHz to 100 MHz with K_V = 150 MHz/V.

Figure 7 shows the ADIsimPLL simulated phase noise and corresponding schematic using the ADF4002, and indicates that the PLL loop locks at 100 MHz with a minimum increase in the phase noise floor.

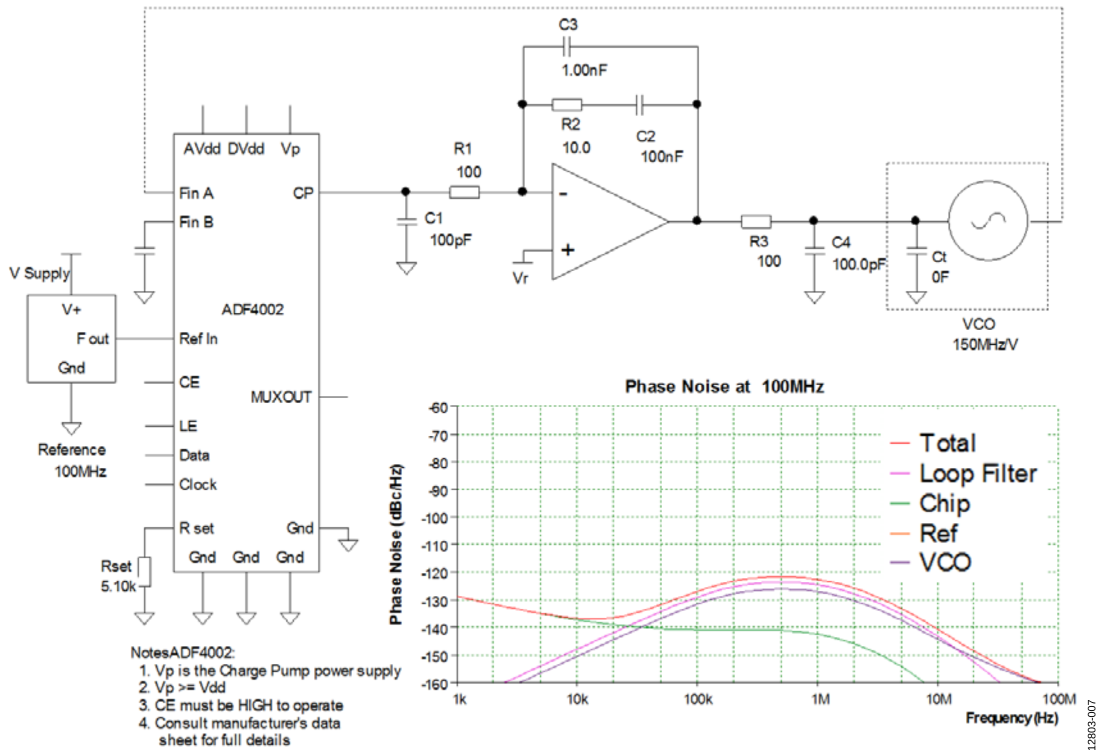

Figure 7. ADIsimPLL Schematic and Simulated Phase Noise for ADF4002 PLL

Translation Loop: Measured Phase Noise Results vs. Standalone PLL

Using the configuration shown in Figure 1, the f_{OUT} rms jitter measures less than 50 fs, as shown in Table 2.

In Table 2, f_{REF} is the reference input to the EVAL-CN0369-SDPZ from the ADF4255-2 evaluation board. The f_{REF} provides the fine tuning for the translation loop. The local oscillator is the LO to the ADL5801-EVALZ mixer evaluation board and provides the coarse tuning for the translation loop. f_{OUT} is the VCO/2 RF output from the EVAL-CN0369-SDPZ.

Table 2. Phase Noise of Translation Loop PLL of Figure 1

f_{REF} (MHz)	Local Oscillator (MHz)	f_{OUT} Frequency (MHz)	f_{OUT} RMS Jitter (fs)
100.00	5300.00	5400.00	43
100.00	5200.00	5300.00	39
100.00	5100.00	5200.00	43
101.01	5100.00	5201.11	43

Figure 8 is a phase noise plot of the f_{OUT} from the translation loop. The reference (f_{REF}) input used in Figure 8 is 101.011 MHz to show the fine tuning performance of the translation loop. The f_{OUT} rms jitter in Figure 8 measures less than 39 fs integrated from 1 kHz to 30 MHz.

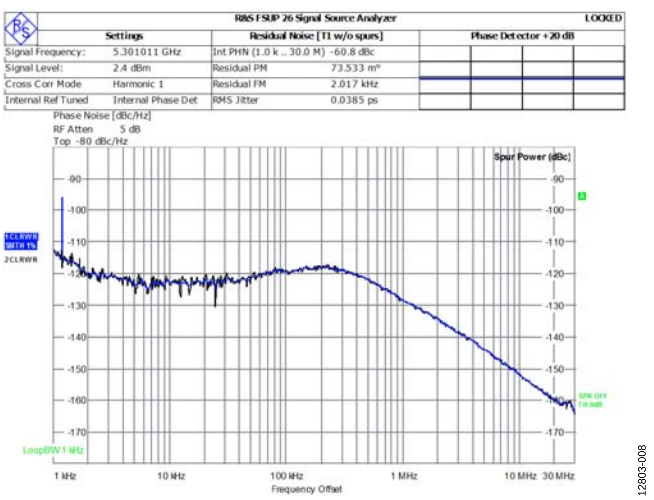

Figure 8. Phase Plot of the Translation Loop f_{OUT}

The f_{OUT} rms jitter measures between 200 fs and 250 fs using the ADF4355-2 as a stand-lone PLL to generate similar frequencies, as shown in Table 3.

For the Table 3 data, f_{REF} is the low noise REFIN source for the EV-ADF4355-2SD1Z evaluation board. f_{OUT} is the RFOUTA(+) of the EV-ADF4355-2SD1Z. RFOUTA(−) is connected to a 50 Ω terminator.

Table 3. Phase Noise of ADF4355-2-Based Standalone PLL

f_{REF} (MHz)	f_{OUT} Frequency (MHz)	f_{OUT} RMS Jitter (fs)
100.00	5400.00	202
100.00	5300.00	220
100.00	5200.00	243
100.00	5201.11	222

CIRCUIT EVALUATION AND TEST

This circuit uses the EVAL-CN0369-SDPZ circuit board, the EV-ADF4355-2SD1Z evaluation board, and the ADL5801-EVALZ evaluation board. The two EVAL-SDP-CS1Z system demonstration platform (SDP-S) boards are used with the EVAL-CN0369-SDPZ circuit board and the EV-ADF4355-2SD1Z evaluation board. The two boards have a 120-pin mating connectors, allowing quick setup and evaluation of the circuit performance. The SDP-S board connected to the EVAL-CN0369-SDPZ circuit board is used with the integer-N evaluation software to program the ADF4002 on-chip registers. The SDP-S board connected to the EV-ADF4355-2SD1Z board is used with the ADF4355-2 evaluation software to program the ADF4355-2 on-chip registers.

A complete set of documentation for the EVAl-CN0369-SDPZ board including schematics, layout files, and bill of materials can be found in the CN-0369 Design Support package at www.analog.com/CN0369-DesignSupport.

Getting Started

Refer to the EVAL-CN0369-SDPZ user guide (UG-806) for software installation and test setup.

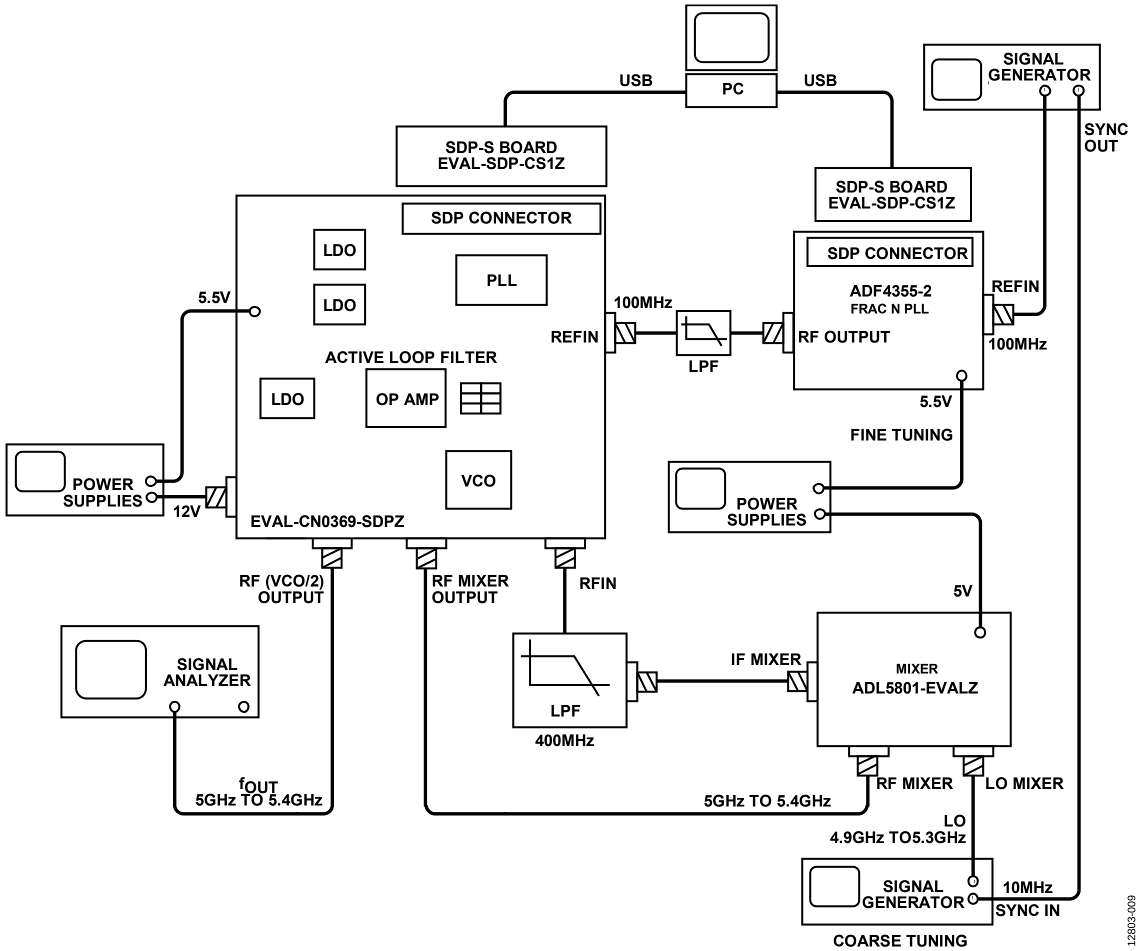

Figure 9. Block Diagram of the Test Setup

Equipment Needed

The following equipment is needed:

- PC with a USB port and Windows® XP, Windows Vista (32-bit), or Windows 7 (32-bit)
- EVAL-CN0369-SDPZ circuit evaluation board
- EV-ADF4355-2SD1Z evaluation board
- Two EVAL-SDP-CS1Z SDP-S boards
- Integer-N v7 and the ADF4355 evaluation software
- Power supplies: 5 V, 5.5 V, and 12 V
- Two RF signal source (R&S SMA100 or equivalent)
- Spectrum analyzer (Agilent FSUP or equivalent)
- TTE 400 MHz low pass filter (or equivalent)
- Mini Circuits 100 MHz low pass filter (or equivalent)

Functional Block Diagram

See Figure 1 for the block diagram. A block diagram of the test setup is shown in Figure 9.

Setup and Test

After setting up the equipment, use standard RF test methods to measure the phase noise and phase jitter of the circuit.

Figure 10. EVAL-CN0369-SDPZ PCB Photo

LEARN MORE

CN-0369 Design Support Package: www.analog.com/CN0369-DesignSupport

EVAL-CN0369-SDPZ User Guide (UG-806)

EV-ADF4355-2SD1Z User Guide (UG-804)

EVAL-SDP-CS1Z System Development Platform User Guide

MT-031 Tutorial. *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*. Analog Devices.

MT-086 Tutorial. *Fundamentals of Phase Locked Loops (PLLs)*. Analog Devices.

MT-101 Tutorial. *Decoupling Techniques*. Analog Devices.

ADIsimPLL Design Tool

AN-30. *Ask the Application Engineer-30, PLL Synthesizers*. Analog Devices

Data Sheets and Evaluation Boards

EVAL-CN0369-SDPZ Evaluation Board

ADL5801-EVALZ Evaluation Board

EV-ADF4355-2SD1Z Evaluation Board

EVAL-SDP-CS1Z System Development Platform

ADF4002 Data Sheet

AD8065 Data Sheet

HMC512 Data Sheet

ADL5801 Data Sheet

ADF4355-2 Data Sheet

REVISION HISTORY

11/2016—Revision 0: Initial Version

ANALOG DEVICES