Circuits from the Lab® Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0422.

Devices Connected/Referenced	
ADN4654	5 kV RMS/3.75 kV RMS, 1.1 Gbps, Dual-Channel LVDS Isolator
ADuM1250	Hot Swappable, Dual I^2C Isolator
ADuM5020	Low Emission Isolated DC-to-DC Converter
ADP7104	20 V, 500 mA, Low Noise, CMOS LDO
ADP5302	500 mA, Ultralow Power Step-Down Regulator

Galvanic Isolation of the HDMI 1.3a Protocol Using *i*Coupler® Isolation Technology

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN-0422 Circuit Evaluation Board (EVAL-CN0422-EBZ)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The requirement to add galvanic isolation to a high speed interface has traditionally been a nontrivial task. Data rates above 250 Mbps are beyond the capabilities of optocouplers and most digital isolators, forcing the system designer towards more complex technologies such as optical fiber. Analog Devices, Inc., *i*Coupler® technology isolates the low voltage differential signaling (LVDS) physical layer at data rates in excess of 1 Gbps, reducing complexity in systems where both isolation and high bandwidth are required. The interface between a surgical scope and the display monitor is one example where galvanic isolation is required.

The circuit shown in Figure 1 provides a completely isolated connection between a High-Definition Multimedia Interface (HDMI) source and HDMI sink device. Both signal and power isolation ensure a safe and noise immune connection between an HDMI source (for example, a medical endoscope or machine defect monitoring camera) and HDMI sink (for example, a camera control module or industrial display).

Isolation in the CN-0422 circuit increases system safety and robustness by providing protection against electrical line surges and breaks the ground connection between bus and digital pins, thereby removing possible ground loops within the system.

Several versions of the HDMI standard are available. The circuit shown in Figure 1 is compliant to Version 1.3a of the HDMI standard. Figure 1 includes isolation of high speed, transition minimized differential signaling (TMDS) clock and data lines, which are implemented with current mode logic (CML) on the physical layer.

The circuit shown in Figure 1 also provides bidirectional isolation of the consumer electronics control (CEC), hot plug detect (HPD), and display data channel (DDC) signals. Isolated power is provided to the high speed and bidirectional data isolators. The CN-0422 circuit also provides 275 mW of isolated power to the HDMI sink device, as required by the HDMI Version 1.3a standard.

The system can transparently isolate a HDMI interface that is configured for resolutions of up to 1280p × 720p (720p) at 60 Hz and is rated to a withstand voltage of 2500 V per UL 1577.

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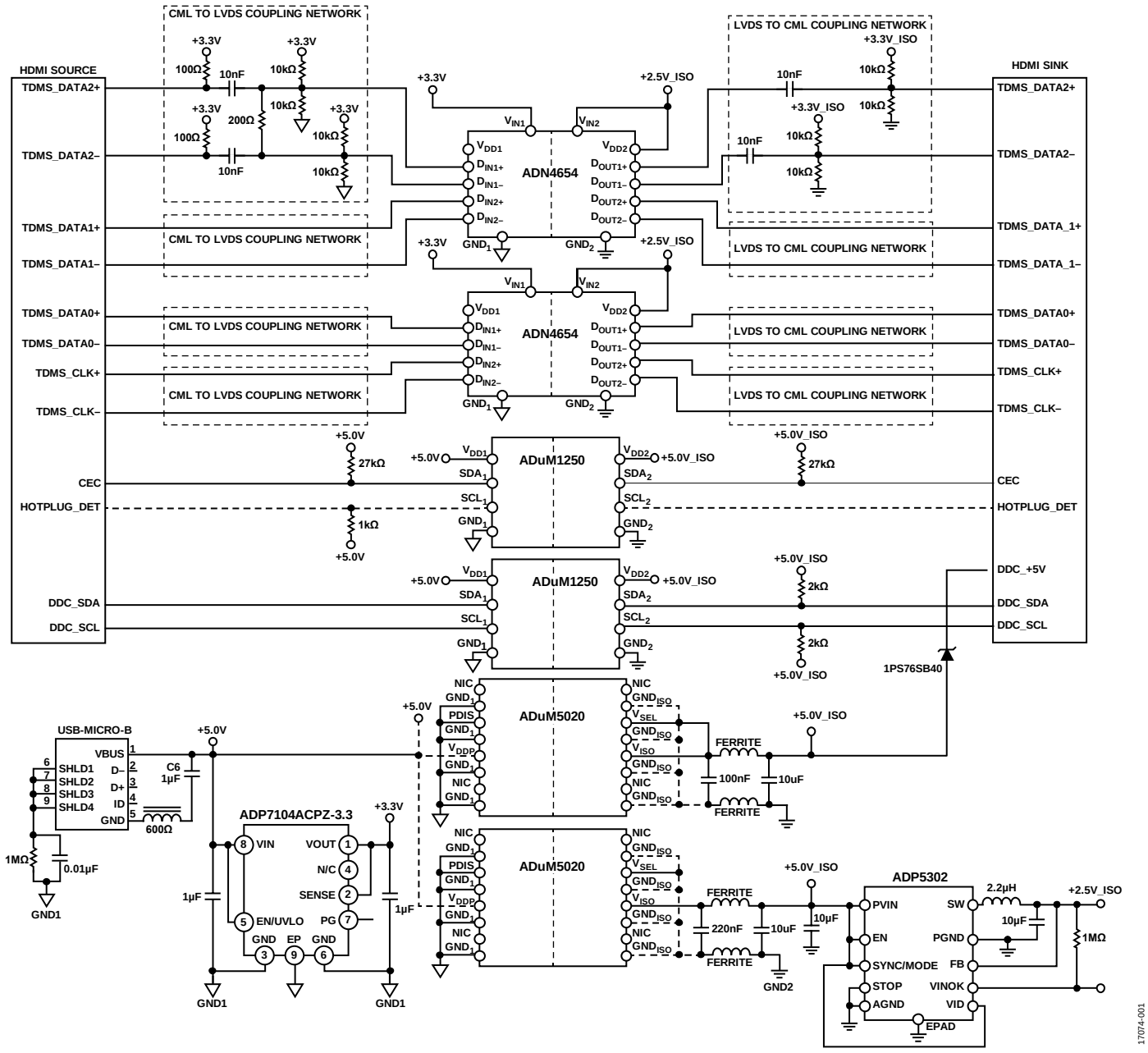

Figure 1. Simplified Circuit Diagram for EVAL-CN0422-EBZ

CIRCUIT DESCRIPTION

Figure 2 shows a simplified block diagram of the power isolation and the isolation of the HDMI Version 1.3a signals. Number 1 through Number 5 show the start-up communication sequence through the ADN4654, ADuM1250, and ADuM5020 devices between the HDMI source and HDMI sink.

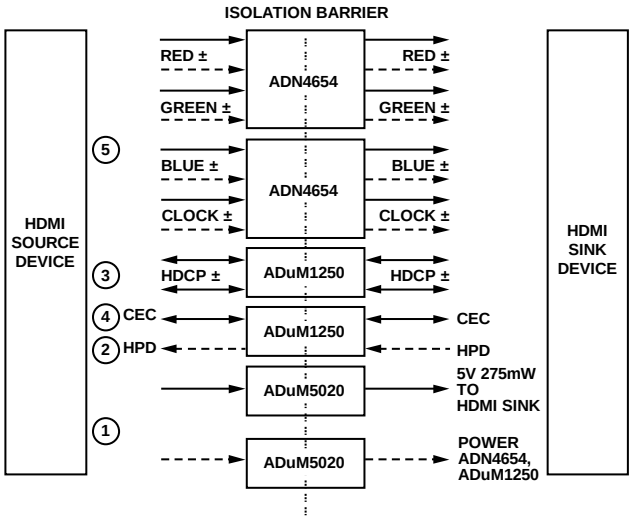

Figure 2. Isolated HDMI Signal Flow Diagram

Step 1: Power

The HDMI Version 1.3a standard states that the HDMI source must be able to provide 55 mA at 5 V to the HDMI sink device. To meet this requirement with an isolated design, CN-0422 uses an ADuM5020 *iso*Power dc-to-dc converter (see Figure 1). Isolated power is provided to the HDMI sink via the DDC + 5 V line, as well as to the two ADuM1250 I²C isolators. A second ADuM5020 device provides isolated power to the secondary side of the ADN4654 via a 2.5 V buck regulator, the ADP5302.

Step 2: Hot Plug Detect (HPD)

When the HDMI source and sink devices are connected to EVAL-CN0422-EBZ via HDMI cables, a start-up communication sequence is initiated through the HPD signal. The sink device pulls the HPD signal high via the ADuM1250 I²C isolator to indicate to the source that it is ready to accept commands through the display data channel (DDC).

Step 3: Display Data Channel (DDC)

The bidirectional DDC uses the I²C protocol that operates at 100 kHz nominal, and a maximum 400 kHz data rate. The HDMI source device uses the DDC to read the extended display identification data (EDID) from the sink device, via the bidirectional ADuM1250 I²C isolator. The HDMI source uses the EDID to determine what audio/video formats are possible at the HDMI sink. The DDC channel is also used in the implementation of High-bandwidth Digital Content Protection (HDCP).

Step 4: Consumer Electronics Control (CEC)

The CEC uses a protocol with a physical layer that is similar to I²C and operates at 200 Hz. The CEC protocol provides high level control functions, via the ADuM1250 I²C isolator, between all of the audio-visual products in a user's environment. The CEC allows the user to command and control up to 15 CEC enabled devices connected through HDMI (for example remote control of a television to set up a DVD player).

Step 5: Transition Minimized Differential Signaling (TMDS)

The TMDS signals consist of three data pairs and one clock pair: Data 0±, Data 1±, Data 2±, and Clock±. The three differential data pairs transmit 10 bits per clock period and carry the high speed video and audio data. The TMDS clock and data lines are implemented with CML on the physical layer.

The coupling networks shown in Figure 1 allow reliable translation between CML and LVDS voltage levels. Following coupling between the CML and the low voltage differential signal (LVDS) physical layer, the ADN4654 1.1 Gbps LVDS isolator is used to isolate the TMDS signals.

For CML to LVDS coupling, use 100 Ω pull-up resistors to correctly terminate the CML signals from the HDMI source. Coupling capacitors (10 nF) are required to remove the CML dc common-mode voltage. Terminating the ADN4654 LVDS inputs requires 200 Ω differential resistance. To bias the ADN4654 inputs, use the 10 kΩ pull-up resistors to 3.3 V and the 10 kΩ pull-down resistors to ground.

For LVDS to CML coupling, use 10 nF capacitors to remove the dc common-mode voltage of the ADN4654 LVDS outputs. CML inputs at the HDMI sink typically require biasing to the common-mode voltage of the CML receiver. Because internal biasing is not included on-chip at the HDMI sink device, biasing must be implemented at the printed circuit board (PCB) level. To bias the inputs to the CML receiver at the HDMI sink device, use the 10 kΩ pull-up resistors to isolated 3.3 V and the 10 kΩ pull-down resistors to isolated ground.

COMMON VARIATIONS

Other Versions of HDMI

HDMI Ethernet audio control (HEAC) compliance is required for more recent versions of the HDMI standard (more recent than HDMI V1.3a). The circuit described in Figure 1 and Figure 2 does not include isolation of HEAC signaling for Ethernet (internet) sharing between devices.

5 kV Isolated Solution

The CN-0422 reference circuit is rated to 2500 V rms per UL 1577, which is suitable for functional isolation or in some safety applications. For medical applications, this design meets the withstand voltage and creepage requirements for 1 means of

patient protection (MOPP) or 1 means of operator protection (MOOP) in 250 V rms systems.

Each of the digital isolators used in this design are also available with increased creepage and a 5000 V withstand rating. Table 1 shows the relevant devices to select for applications where 5 kV of galvanic isolation is required. This 5 kV design meets IEC 60601-1 requirements for 2 means of operator protection (MOOP) in 250 V rms systems, 1 means of patient protection (MOPP) in 250 V rms systems, or 2 MOPP in 125 V rms systems.

Table 1. Comparison of Isolation Ratings

Isolation Voltage	2.5 kV	5 kV
Minimum Creepage	4.01 mm	7.8 mm
DC-to-DC Converter	ADuM5020-5BRWZ	ADuM6020-5BRIZ
High Speed Isolators	ADN4654BRSZ	ADN4654BRWZ
I^2C Isolators	ADuM1250ARZ	ADuM2250ARWZ

CIRCUIT EVALUATION AND TEST

Common-Mode Transient Immunity

Common-mode transient immunity (CMTI) refers to the ability of an isolator to reject fast common-mode transients. The CMTI is defined as the maximum common-mode voltage slew rate, or transient, that can be tolerated between system ground (Ground 1) and isolated ground (Ground 2) while still maintaining bit error free communication.

CMTI is important because high slew rate transients can couple across the parasitic capacitance of the isolation barrier, corrupting data. The ADuM1250 and ADN4654 are robust digital isolators with good CMTI performance, specified to operate correctly and without data corruption in the presence of common-mode transients greater than 25,000 V/µs.

System Compliance Test

This section describes a HDMI source compliance test performed using the EVAL-CN0422-EBZ. Fourteen compliance tests were passed using the EVAL-CN0422-EBZ outputs, including clock jitter, eye diagrams and jitter for data channels, rise and fall times for clock and data channels, and maximum/minimum clock duty cycles.

Figure 3, Figure 4, Figure 5, and Figure 6 document the HDMI source compliance testing performed and the test results. Figure 3 and Figure 4 show the HDMI source compliance test eye diagrams for 720p × 576p, 60 Hz and 1280p × 720p, and 60 Hz HDMI resolutions, respectively.

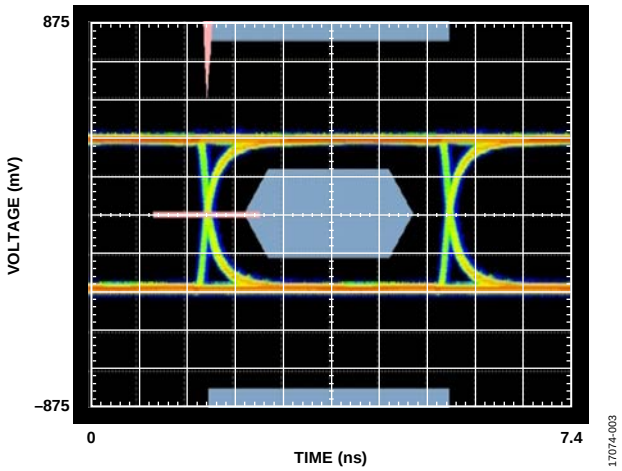

Figure 3. HDMI Source Compliance Test Eye Diagram, 576p

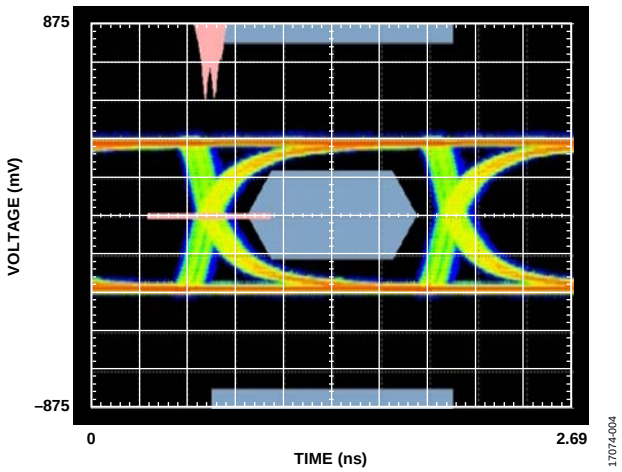

Figure 4. HDMI Source Compliance Test Eye Diagram, 720p

Figure 5 and Figure 6 show the corresponding HDMI source compliance test reports for 720p × 576p, 60Hz and 1280p × 720p, 60 Hz HDMI resolutions, respectively.

Setup Configuration

Oscilloscope Info	MSO70804C - 7.6.1 Build 5*
TDSHT3 Version	5.3.2 Build 47

Device Configuration

Device Details	HDMI Device
Clock Frequency(Mhz)	27.0275
Resolution	720x576p
Refresh Rate	60Hz

Compliance Summary

Total Tests Supported	9
Tests Completed	14
Pass	14
Fail	0

Test Summary

Index	Test Name	Lanes	Spec Range	Meas Value	Result
1	7-9 : Source Clock Jitter	CK	Clock Jitter < 0.25*Tbit;	0.053*Tbit	Pass
2	7-10 : Source Eye Diagram	CK - D0	Data Jitter < 0.3*Tbit;	0.08*Tbit	Pass
3	7-10 : Source Eye Diagram	CK - D1	Data Jitter < 0.3*Tbit;	0.05*Tbit	Pass
4	7-10 : Source Eye Diagram	CK - D2	Data Jitter < 0.3*Tbit;	0.05*Tbit	Pass
5	7-4 : Source Rise Time	CK	75.00ps < TRISE;	287.07ps	Pass
6	7-4 : Source Rise Time	D0	75.00ps < TRISE;	274.12ps	Pass
7	7-4 : Source Rise Time	D1	75.00ps < TRISE;	263.64ps	Pass
8	7-4 : Source Rise Time	D2	75.00ps < TRISE;	271.35ps	Pass
9	7-4 : Source Fall Time	CK	75.00ps < TFALL;	276.43ps	Pass
10	7-4 : Source Fall Time	D0	75.00ps < TFALL;	257.08ps	Pass
11	7-4 : Source Fall Time	D1	75.00ps < TFALL;	253.42ps	Pass
12	7-4 : Source Fall Time	D2	75.00ps < TFALL;	265.41ps	Pass
13	7-8 : Max Duty Cycle	CK	Max Duty Cycle < 60.0%;	50.54%	Pass
14	7-8 : Min Duty Cycle	CK	40.0% < Min Duty Cycle;	49.46%	Pass

17074-005

Figure 5. HDMI Source Compliance Test Report, 576p

Setup Configuration

Oscilloscope Info	MSO72504D - 7.3.0 Build 9
TDSHT3 Version	5.2.8 Build 30

Device Configuration

Device Details	HDMI Device
Clock Frequency(Mhz)	74.2511
Resolution	1280x720p
Refresh Rate	60Hz

Compliance Summary

Total Tests Supported	9
Tests Completed	14
Pass	14
Fail	0

Test Summary

Index	Test Name	Lanes	Spec Range	Meas Value	Result
1	7-9 : Source Clock Jitter	CK	Clock Jitter < 0.25*Tbit;	0.084*Tbit	Pass
2	7-10 : Source Eye Diagram	CK - D0	Data Jitter < 0.3*Tbit;	0.2*Tbit	Pass
3	7-10 : Source Eye Diagram	CK - D1	Data Jitter < 0.3*Tbit;	0.17*Tbit	Pass
4	7-10 : Source Eye Diagram	CK - D2	Data Jitter < 0.3*Tbit;	0.16*Tbit	Pass
5	7-4 : Source Rise Time	CK	75.00ps < TRISE;	197.34ps	Pass
6	7-4 : Source Rise Time	D0	75.00ps < TRISE;	194.97ps	Pass
7	7-4 : Source Rise Time	D1	75.00ps < TRISE;	219.13ps	Pass
8	7-4 : Source Rise Time	D2	75.00ps < TRISE;	195.30ps	Pass
9	7-4 : Source Fall Time	CK	75.00ps < TFALL;	193.93ps	Pass
10	7-4 : Source Fall Time	D0	75.00ps < TFALL;	191.48ps	Pass
11	7-4 : Source Fall Time	D1	75.00ps < TFALL;	199.49ps	Pass
12	7-4 : Source Fall Time	D2	75.00ps < TFALL;	189.05ps	Pass
13	7-8 : Max Duty Cycle	CK	Max Duty Cycle < 60.0%;	51.08%	Pass
14	7-8 : Min Duty Cycle	CK	40.0% < Min Duty Cycle;	49.3%	Pass

17074-006

Figure 6. HDMI Source Compliance Test Report, 720p

System Compatibility Test

A system compatibility test is performed using the Analog Devices EVAL-ADV7625-SMZ evaluation board. The ADV7625 is a 3 GHz HDMI 5:2 crosspoint transceiver. The system compatibility test demonstrates the zero loss in visual quality when comparing the galvanically isolated display to a standard nonisolated display.

Equipment Needed for System Compatibility Test

The following equipment is needed to perform the system compatibility test:

- HDMI audio and video source (DVD player)
- EVAL-CN0422-EBZ circuit evaluation board
- EVAL-ADV7625-SMZ video evaluation board
- Power supply: 5 V, 3.6 A power supply or 5 V wall wart
- 4 HDMI cables, length 1 m each
- USB to RS-232 cable.
- Two monitors/displays with HDMI input

Getting Started

Reference the EVAL-ADV7625-SMZ user guide (UG-603) when working with the EVAL-ADV7625-SMZ video evaluation board.

Power up the EVAL-ADV7625-SMZ and connect a USB-to-RS-232 cable from your laptop to the connector, P1. Install a jumper across J15 on the EVAL-ADV7625-SMZ while programming the board. For complete setup details see the CN-0422 User Guide.

Configure a terminal window as per instructions found in the UG-603 user guide (115,200 baud, eight data bits, no parity, one stop bit, no flow control). Type the commands, **hdmia a** and **hdmia b** to set up a 1:2 HDMI splitter mode from RxA to TxA, and RxA to TxB.

Functional Block Diagram

Figure 7 shows a block diagram for the HDMI system compatibility test.

The EVAL-ADV7625-SMZ accepts one HDMI input from the source and generates two identical HDMI outputs. The EVAL-CN0422-EBZ is connected between the EVAL-ADV7625-SMZ Output 1 and sink (Display 1), and compared to a second channel with the EVAL-ADV7625-SMZ Output 2 and sink (Display 2) connected directly together.

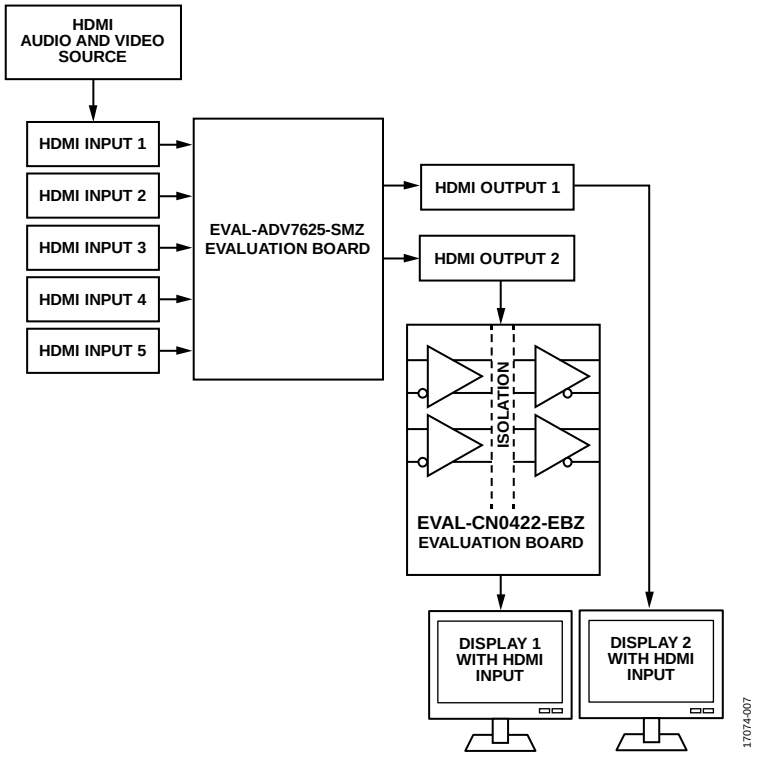

Figure 7. HDMI System Compatibility Test

Test

After the EVAL-ADV7625-SMZ is configured, take the following steps:

1. Connect an HDMI video and audio source to the EVAL-ADV7625-SMZ RxA input.
2. Connect 5 V power from a wall wart to J5 on the EVAL-CN0422-EBZ via a micro USB Type B cable.
3. Connect the input HDMI connector on the underside of the EVAL-CN0422-EBZ circuit evaluation board to the EVAL-ADV7625-SMZ TxA output.
4. Connect the HDMI output (J4) of the EVAL-CN0422-EBZ to an HDMI display (Display 1).
5. Connect the EVAL-ADV7625-SMZ TxB output to an HDMI display (Display 2).

The HDMI video/audio source appears on both displays. Observing both displays confirms that the isolated HDMI is transparent; Display 1 and Display 2 are visually identical.

LEARN MORE

CN-0422 Design Support Package:
www.analog.com/CN0422-DesignSupport

High-Definition Multimedia Interface (HDMI). www.hdmi.org.

Data Sheets and Evaluation Boards

ADN4654 Data Sheet

EVAL-ADN4654 Evaluation Board

ADuM1250 Data Sheet

EVAL-ADuM1250EBZ Evaluation Board

ADuM2250 Data Sheet

ADuM5020 Data Sheet

EVAL-ADuM5020EBZ Evaluation Board

EVAL-ADV7625-SMZ Evaluation Board

ADuM6020 Data Sheet

REVISION HISTORY

4/2019—Revision 0: Initial Version

I^2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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