

Evaluating the **LTC6227** and **LTC6229** Low Distortion, Rail-to-Rail Output Op Amps

FEATURES

- Enables efficient prototyping
- User defined circuit configuration
- Edge mounted SMA connector provisions
- Simplified connection to test equipment and other circuits
- RoHS compliant

EVALUATION KIT CONTENTS

EVAL-LTC6227MS8E or EVAL-LTC6229MS8E

EQUIPMENT NEEDED

- Dual output dc power supply
- Dual-channel signal generator
- Oscilloscope
- 3 banana plug to grabber cables
- 4 SMA to BNC male cables

EVALUATION BOARD PHOTOGRAPHS



Figure 1. EVAL-LTC6227MS8E/EVAL-LTC6229MS8E, Primary Side



Figure 2. EVAL-LTC6227MS8E/EVAL-LTC6229MS8E, Secondary Side

GENERAL DESCRIPTION

The EVAL-LTC6227MS8E/EVAL-LTC6229MS8E allow the evaluation of the **LTC6227** and **LTC6229**, 8-lead, dual-channel, micro small outline package (MSOP) op amps. The EVAL-LTC6227MS8E and the EVAL-LTC6229MS8E are prepopulated boards on a buffer configuration with a post low-pass filter. This configuration allows the **LTC6227** and **LTC6229** to be used as high speed analog-to-digital converter (ADC) drivers. The EVAL-LTC6227MS8E/EVAL-LTC6229MS8E support other typical configurations of the op amps, and are configured and have provisions for typical applications of the **LTC6227** and the **LTC6229**, including high speed, low voltage, low noise, in-amp, and as an active filter. The exposed paddle pin is already shorted to the VEE turret pin, which is required for the device. The 4-layer EVAL-LTC6227MS8E/EVAL-LTC6229MS8E accept edge mounted, Subminiature Version A (SMA) connectors on both inputs and outputs to provide an efficient connection to the test equipment and other circuitry. In addition, the EVAL-

LTC6227MS8E/EVAL-LTC6229MS8E have sufficient test points for both signal pins and groundings.

Optimized power and ground planes ensure low noise and high speed operation. Component placement and power supply bypassing are optimized for maximum circuit flexibility and performance. The EVAL-LTC6227MS8E/EVAL-LTC6229MS8E accept C0402 or C0603 surface-mount technology (SMT) components and C1206 bypass capacitors for C5 and C6.

All components are placed on the primary side of the EVAL-LTC6227MS8E/EVAL-LTC6229MS8E, and no components are placed on the secondary side. The EVAL-LTC6227MS8E and EVAL-LTC6229MS8E evaluation boards are identical except for the on-board devices.

For full details on the **LTC6227** and the **LTC6229**, see the **LTC6227** and the **LTC6229** data sheets, which must be consulted in conjunction with this user guide when using the EVAL-LTC6227MS8E/EVAL-LTC6229MS8E.

TABLE OF CONTENTS

Features	1	Using the Evaluation Board for Testing	3
Evaluation Kit Contents.....	1	Evaluation Board Hardware.....	4
Equipment Needed.....	1	Power Supply Bypassing.....	4
Evaluation Board Photographs	1	Evaluation Board Stack Up	4
General Description	1	Evaluation Board Schematic and Artwork.....	5
Revision History	2	Ordering Information.....	7
Evaluation Board Quick Start Procedures	3	Bill of Materials.....	7
Power Supply Consideration.....	3		
Initial Board Configuration	3		

REVISION HISTORY

8/2020—Rev. 0 to Rev. A

Added EVAL-LTC6227MS8E	Universal
Added LTC6227	Universal
Changes to Figure 1 and General Description Section	1
Changes to Using the Evaluation Board for Testing Section	3
Changes to Table 1.....	7

12/2019—Revision 0: Initial Version

EVALUATION BOARD QUICK START PROCEDURES

The following sections outline the basic prepopulated configuration of the EVAL-LTC6227MS8E/EVAL-LTC6229MS8E required to test the basic functionality of the [LTC6227](#) or the [LTC6229](#).

POWER SUPPLY CONSIDERATION

Use the turret pins (VCC, VEE, and GND) to power up the EVAL-LTC6227MS8E/EVAL-LTC6229MS8E. Use the correct polarity and voltage level to avoid reverse polarity and overvoltage, which can permanently damage the EVAL-LTC6227MS8E/EVAL-LTC6229MS8E.

INITIAL BOARD CONFIGURATION

To test the basic functionality of the EVAL-LTC6227MS8E/EVAL-LTC6229MS8E and the [LTC6227](#) or the [LTC6229](#), take the following steps:

1. Ensure that all equipment is powered down, including the power supply and the signal generator.
2. Use a banana plug to grabber cable to connect the positive supply, ground, and negative supply to the VCC, GND, and VEE turret pins, respectively.
3. Use an SMA to Bayonet Neill-Concelman (BNC) connector to connect the on-board SMA connector test point, labeled VIN1P, on the J3 connector to a signal generator channel.
4. Use an SMA to BNC connector to connect the on-board SMA connector test point, VIN2P, on the J6 connector to another signal generator channel.
5. Use an SMA to BNC connector to connect the on-board SMA connector test point, VOUT1, on the J1 connector to an oscilloscope channel.
6. Use an SMA to BNC connector to connect the on-board SMA connector test point, VOUT2, on the J4 connector to another oscilloscope channel.

USING THE EVALUATION BOARD FOR TESTING

When the procedure in the Initial Board Configuration section is complete, implement the following settings and verify the expected output:

1. Set the power supply to +5 V for the positive supply and –5 V for the negative supply.
2. Select the output waveform for both the signal generator channels to a sine wave with a frequency of 1 kHz and a peak-to-peak voltage of 2 V.
3. Set the output load of the signal generator to a high-Z load.
4. Set the oscilloscope termination to 1 M Ω and observe the oscilloscope frequency and the peak-to-peak voltage.
5. When all equipment is set up, turn on the power supply and check the voltage and current consumption of the EVAL-LTC6227MS8E/EVAL-LTC6229MS8E. The expected current consumption is approximately 12 mA for the [LTC6227](#) and 36 mA for the [LTC6229](#), and the current drawn from the supply must not exceed 16 mA or 45 mA, respectively.
6. Turn on the signal generator when the power supply turns on.
7. Observe the output at the oscilloscope. The output of VOUT1 and VOUT2 is a sine wave with a frequency of 1 kHz, and a peak-to-peak voltage of approximately 2 V.

EVALUATION BOARD HARDWARE

POWER SUPPLY BYPASSING

External bypass capacitors, such as C5 and C6, are provided for low level frequency bypassing at the amplifier power pins. Additional capacitors (C3, C4, and C7 to C12) are provided for additional higher level frequency bypassing (see Figure 3).

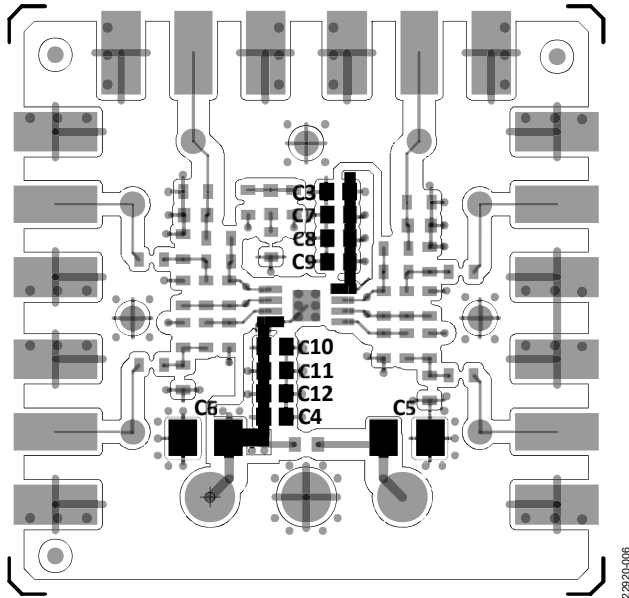


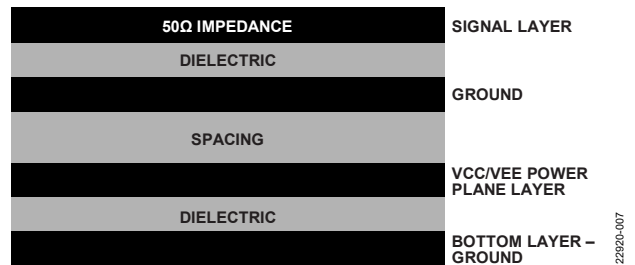
Figure 3. Bypass Capacitor Locations

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EVALUATION BOARD STACK UP

The 4-layer board design of the EVAL-LTC6227MS8E/EVAL-LTC6229MS8E (see Figure 4) provides optimized high speed and low noise performance. The upper ground layer is spaced to provide 50 Ω controlled impedance with the signal layer to optimize high frequency performance.

The VCC/VEE power plane layer is in between the two ground layers to provide mechanical stability and distributed interplanar capacitance between the power plane layer and the ground layer.



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Figure 4. Stack Up

EVALUATION BOARD SCHEMATIC AND ARTWORK

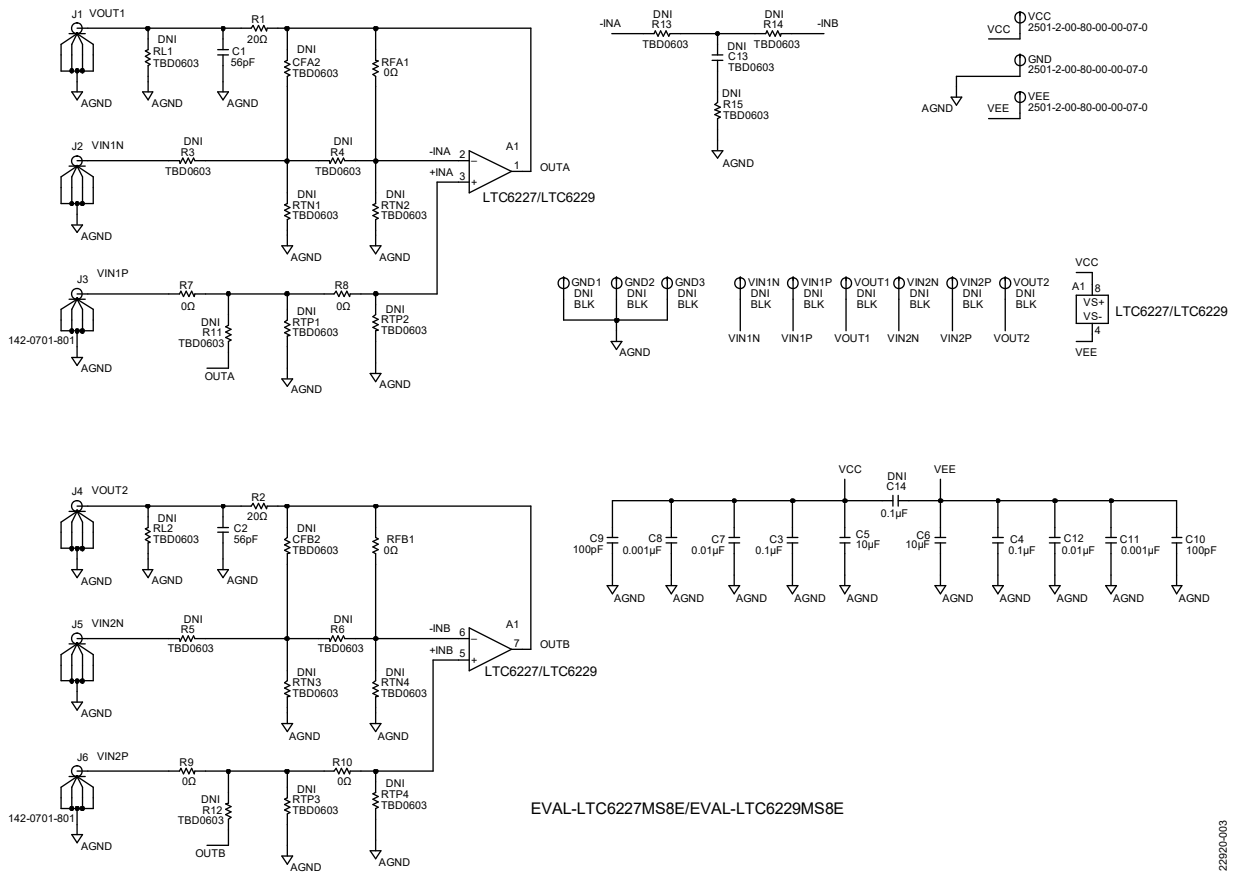
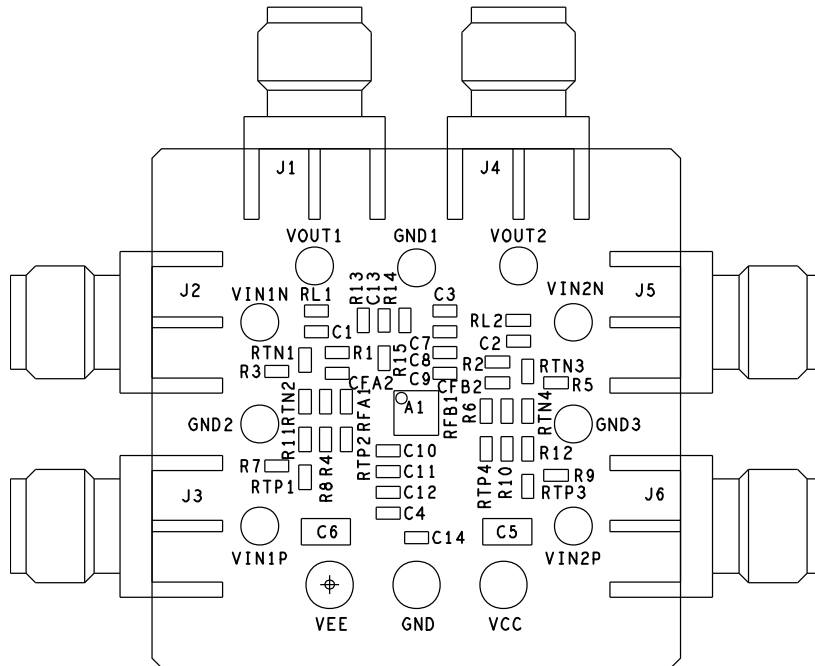
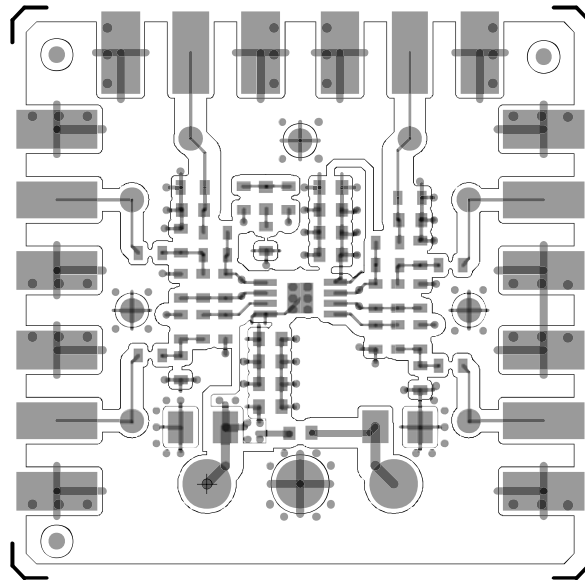


Figure 5. EVAL-LTC6227MS8E/EVAL-LTC6229MS8E Schematic



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Figure 6. EVAL-LTC6227MS8E/EVAL-LTC6229MS8E Assembly Drawing, Primary Side



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Figure 7. EVAL-LTC6227MS8E/EVAL-LTC6229MS8E Layout Pattern, Primary Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 1.

Qty	Reference Designator	Description	Part Number
1	A1	Rail-to-rail output op amp, LTC6227 or LTC6229	LTC6227MS8E#PBF or LTC6229MS8E#PBF
2	C1, C2	Capacitors, 68 pF (LTC6227) or 56 pF (LTC6229), C0603	223887000000
2	C3, C4	Capacitors, 0.1 μF, C0603	06035C104KAT2A
2	C5, C6	Capacitors, 10 μF, C1206	GMK316AB7106KL-TR
2	C7, C12	Capacitors, 0.01 μF, C0603	CC0603KRX7R9BB103
2	C8, C11	Capacitors, 0.001 μF, C0603	CC0603KRX7R9BB102
2	C9, C10	Capacitors, 100 pF, C0603	C0603C101K5RAC
1	C13	Capacitor, user defined, do not install, C0603/C0402	Not applicable
1	C14	Capacitor, 0.1 μF, do not install, C0603/C0402	Not applicable
21	CFA2, CFB2, R3 to R6, R11 to R15, RL1, RL2, RTN1 to RTN4, RTP1 to RTP4	Resistors, user defined, do not install, R0603/R0402	Not applicable
3	GND, VCC, VEE	Terminal turrets	2501-2-00-80-00-00-07-0
9	GND1 to GND3, VIN1N, VIN2N, VIN1P, VIN2P, VOUT1, VOUT2	Test points, do not install	5001
6	J1 to J6	SMA end launch connectors	142-0701-801
2	R1, R2	Resistors, 33 Ω (LTC6227) or 20 Ω (LTC6229), R0603	P0603E20R0BBT
6	R7 to R10, RFA1, RFB1	Resistors, 0 Ω, R0603	MC0603WG00000T5E-TC



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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