Digital Input 2 W Class-D Audio Power Amplifier

Data Sheet **SSM2519**

FEATURES

- **Filterless digital input Class-D amplifier**
- **Standalone operation or I²C control**
- **Serial digital audio interface supports common formats: I²S, left justified, right justified, TDM1-16, and PCM**
- **2.31 W into 4 Ω and 1.35 W into 8 Ω at 5 V supply with 1% THD + N**
- **Available in 12-ball 1.4 mm × 1.7 mm × 0.4 mm pitch WLCSP**
- **Efficiency 90% at full scale into 8 Ω**
- **9 mW loaded idle power at 1.8 V/3.6 V**
- **SNR = 98 dB, A-weighted**
- **PSRR = 80 dB at 217 Hz, dither input**
- **Supports wide range of sample rates: 8.0 kHz to 48.0 kHz**
- **Autosample rate and MCLK rate detection**
- **No BCLK required for operation**
- **2.5 V to 5.5 V PV_{DD} speaker operating supply voltage**
- **1.5 V to 3.6 V V_{DD} operating voltage**
- **Pop and click suppression**
- **Short-circuit and thermal protection with autorecovery**
- **Smart power-down when no input signal detected**
- **Power-on reset**
- **Low EMI emissions**

APPLICATIONS

- **Mobile phones**
- **Portable media players**
- **Laptop PCs**
- **Wireless speakers**
- **Portable gaming**
- **Navigation systems**

FUNCTIONAL BLOCK DIAGRAM

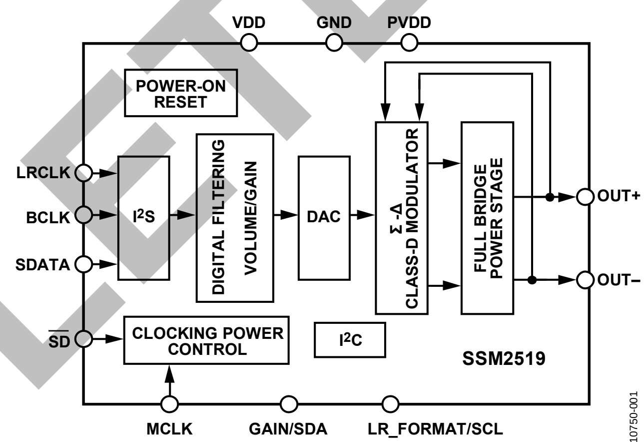

Figure 1.

GENERAL DESCRIPTION

The SSM2519 is a digital input, Class-D power amplifier that combines a digital-to-analog converter (DAC) and a sigma-delta (Σ-Δ) Class-D modulator. This unique architecture enables extremely low, real-world power consumption from digital audio sources with excellent audio performance. The SSM2519 is ideal for power sensitive applications, such as mobile phones and portable media players, where system noise can corrupt small analog signals such as those sent to an analog input audio amplifier.

Using the SSM2519, audio data can be transmitted to the amplifier over a standard digital audio serial interface, thereby significantly reducing the effect of noise sources such as GSM interference or other digital signals on the transmitted audio. The closed-loop digital input design retains the benefits of a completely digital amplifier, yet enables very good PSRR and audio performance. The three-level, Σ-Δ Class-D modulator is designed to provide the least amount of EMI interference, the lowest quiescent power dissipation, and the highest audio efficiency without sacrificing audio quality.

Input is provided via a serial audio interface, programmable to accept all common audio formats including I²S, left justified (LJ), right justified (RJ), TDM, and PCM. The SSM2519 is designed to operate with or without a control interface such as I²C, which is typically required for this type of device. Several control pins offer selection of operation when I²C control is not used. The SSM2519 can accept a variety of input MCLK frequencies and can use BCLK as the clock source in some configurations. Both the input sample rate and MCLK rates are automatically detected.

The architecture of the SSM2519 provides a solution that offers lower power and higher performance than existing DAC plus Class-D solutions. Its digital interface also offers a better system solution for other products whose sole audio source is digital, such as wireless speakers, laptop PCs, portable digital televisions, and navigation systems.

The SSM2519 is specified over the industrial temperature range of −40°C to +85°C. It has built-in thermal shutdown and output short-circuit protection. It is available in a 12-ball, 1.4 mm × 1.7 mm wafer level chip scale package (WLCSP).

Rev. 0

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REVISION HISTORY

7/12—Revision 0: Initial Version

SPECIFICATIONS

All conditions at PV_{DD} = 5.0 V; V_{DD} = 1.8 V; f_S = 48 kHz; MCLK = 128 × f_S; T_A = 25°C; R_L = 8 Ω + 15 μH; default I^2C settings; volume control 0 dB setting, unless otherwise noted.

PERFORMANCE SPECIFICATIONS

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS						
Output Power	P_{OUT}	R_L = 4 Ω, THD + N = 1%, f = 1 kHz, BW = 20 kHz, PV_{DD} = 5.0 V		2.31		W
		R_L = 4 Ω, THD + N = 10%, f = 1 kHz, BW = 20 kHz, PV_{DD} = 5.0 V		2.75		W
		R_L = 8 Ω, THD + N = 1%, f = 1 kHz, BW = 20 kHz, PV_{DD} = 5.0 V		1.35		W
		R_L = 8 Ω, THD + N = 10%, f = 1 kHz, BW = 20 kHz, PV_{DD} = 5.0 V		1.68		W
		R_L = 4 Ω, THD + N = 1%, f = 1 kHz, BW = 20 kHz, PV_{DD} = 3.6 V		1.13		W
		R_L = 4 Ω, THD + N = 10%, f = 1 kHz, BW = 20 kHz, PV_{DD} = 3.6 V		1.4		W
		R_L = 8 Ω, THD + N = 1%, f = 1 kHz, BW = 20 kHz, PV_{DD} = 3.6 V		0.69		W
		R_L = 8 Ω, THD + N = 10%, f = 1 kHz, BW = 20 kHz, PV_{DD} = 3.6 V		0.85		W
		R_L = 4 Ω, THD + N = 1%, f = 1 kHz, BW = 20 kHz, PV_{DD} = 2.5 V		0.48		W
		R_L = 4 Ω, THD + N = 10%, f = 1 kHz, BW = 20 kHz, PV_{DD} = 2.5 V		0.6		W
		R_L = 8 Ω, THD + N = 1%, f = 1 kHz, BW = 20 kHz, PV_{DD} = 2.5 V		0.31		W
		R_L = 8 Ω, THD + N = 10%, f = 1 kHz, BW = 20 kHz, PV_{DD} = 2.5 V		0.39		W
Efficiency	η	P_{OUT} = 2 W, 4 Ω, PV_{DD} = 5.0 V		84		%
		P_{OUT} = 1.4 W, 8 Ω, PV_{DD} = 5.0 V, normal operation		90.2		%
Total Harmonic Distortion Plus Noise	THD + N	P_{OUT} = 1 W into 8 Ω, f = 1 kHz, PV_{DD} = 5.0 V		0.03		%
		P_{OUT} = 0.5 W into 8 Ω, f = 1 kHz, PV_{DD} = 3.6 V		0.03		%
Average Switching Frequency	f_{SW}			305		kHz
Differential Output Offset	V_{OOS}			1		mV
Power Supply Rejection Ratio	$PSRR_{DC}$	PV_{DD} = 2.5 V to 5.0 V	70	82		dB
	$PSRR_{GSM}$	V_{RIPPLE} = 100 mV rms at 217 Hz, dither input		80		dB
Supply Current, PVDD	I_{PVDD}	Dither input, 8 Ω + 15 μH load, PV_{DD} = 5.0 V		2.64		mA
		Dither input, 8 Ω + 15 μH load, PV_{DD} = 3.6 V		2.24		mA
		Dither input, 8 Ω + 15 μH load, PV_{DD} = 2.5 V		2.02		mA
		Dither input, 8 Ω + 15 μH load, PV_{DD} = 3.6 V (DAC_LPM = 0 and AMP_LPM = 0)		2.5		mA
		Hardware shutdown		200		nA
Supply Current, VDD	I_{VDD}	Dither input, V_{DD} = 3.3 V		1.14		mA
		Dither input, V_{DD} = 1.8 V		0.6		mA
		Software shutdown, clock present, V_{DD} = 1.8 V		86		μA
		Software shutdown, clock removed, V_{DD} = 1.8 V		5		μA
		Hardware shutdown		200		nA
Output Noise Voltage	e_n	PV_{DD} = 5.0 V, f = 20 Hz to 20 kHz, dither input, A-weighted		37		μV
		PV_{DD} = 3.6 V, f = 20 Hz to 20 kHz, dither input, A-weighted, gain = 3.6 V		41		μV
Signal-to-Noise Ratio	SNR	A-weighted reference to 0 dBFS, PV_{DD} = 5.0 V		98		dB
Closed-Loop Gain	Gain	0 dBFS input, BTL output, f = 1 kHz				
		Gain = 5.0 V		4.94		V pk
		Gain = 4.2 V		4.21		V pk
		Gain = 3.6 V		3.69		V pk
		Gain = 2 V		1.98		V pk

POWER SUPPLY REQUIREMENTS

Table 2.

Parameter	Min	Typ	Max	Unit
PV_{DD}	2.5	3.6	5.5	V
V_{DD}	1.5	1.8	3.6	V

DIGITAL INPUT/OUTPUT

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT VOLTAGE					
High (V_{IH})	$0.7 \times V_{DD}$		3.6	V	MCLK, BCLK, LRCLK, SDATA
	1.35		5.5	V	$\overline{SD}$, SDA, SCL
Low (V_{IL})	−0.3		$+0.3 \times V_{DD}$	V	MCLK, BCLK, LRCLK, SDATA
	−0.3		+0.35	V	$\overline{SD}$, SDA, SCL
INPUT LEAKAGE CURRENT					
High (I_{IH})			1	µA	Excluding MCLK
Low (I_{IL})			1	µA	Excluding MCLK and bidirectional pin
MCLK INPUT LEAKAGE CURRENT					
High (I_{IH})			3	µA	
Low (I_{IL})			3	µA	
INPUT CAPACITANCE			5	pF	

DIGITAL TIMING

All timing specifications are given for the default setting (I^2S mode) of the serial input port.

Table 4.

	Limit			
Parameter	Min	Max	Unit	Description
MASTER CLOCK				
t_{MP}	74	136	ns	MCLK period, $256 \times f_S$ mode (MCS = b0010)
t_{MP}	148	271	ns	MCLK period, $128 \times f_S$ mode (MCS = b0001)
SERIAL PORT				
t_{BIL}	40		ns	BCLK low pulse width
t_{BIH}	40		ns	BCLK high pulse width
t_{LIS}	10		ns	Setup time from LRCLK or SDATA edge to BCLK rising edge
t_{LIH}	10		ns	Hold time from BCLK rising edge to LRCLK or SDATA edge
t_{SIS}	10		ns	SDATA setup time to BCLK rising
t_{SIH}	10		ns	SDATA hold time from BCLK rising
I^2C PORT				
f_{SCL}		400	kHz	SCL frequency
t_{SCLH}	0.6		µs	SCL high
t_{SCLL}	1.3		µs	SCL low
t_{SCS}	0.6		µs	Setup time; relevant for repeated start condition
t_{SCH}	0.6		µs	Hold time; after this period, the first clock is generated
t_{DS}	100		ns	Data setup time
t_{SCR}		300	ns	SCL rise time
t_{SCF}		300	ns	SCL fall time
t_{SDR}		300	ns	SDA rise time
t_{SDF}		300	ns	SDA fall time
t_{BFT}	0.6		µs	Bus-free time (time between stop and start)

Digital Timing Diagrams

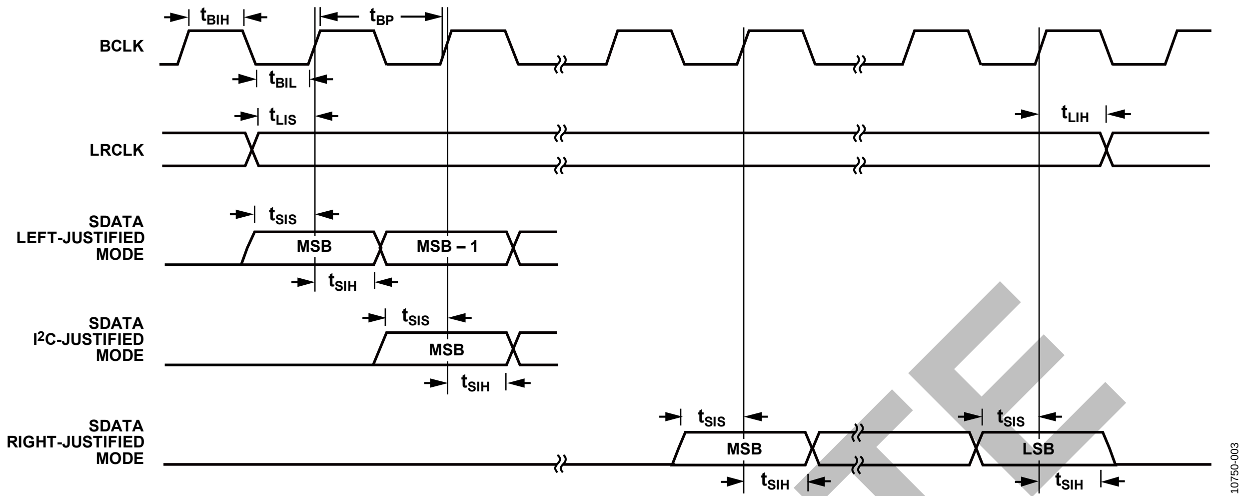

Figure 2. Serial Input Port Timing

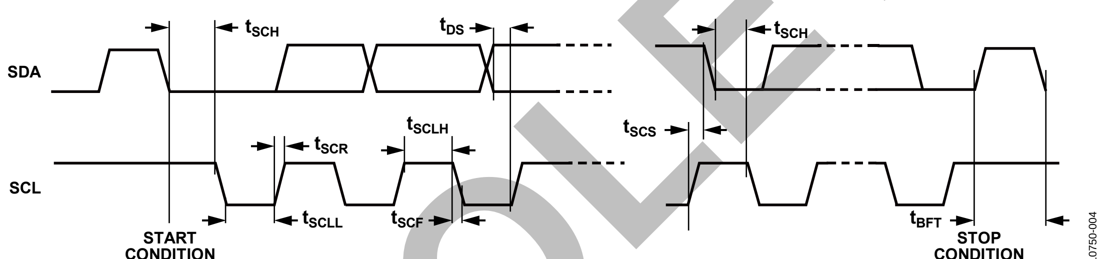

Figure 3. I²C Port Timing

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
PVDD Supply Voltage	−0.3 V to 6 V
VDD Supply Voltage	−0.3 V to 3.6 V
Input Voltage (MCLK, BCLK, $\overline{SD}$, LRCLK, LR_FORMAT, GAIN, SDATA)	−0.3 V to 3.6 V
ESD Susceptibility	4 kV
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to 7absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
12-ball, 1.4 mm × 1.7 mm WLCSP	56.1	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

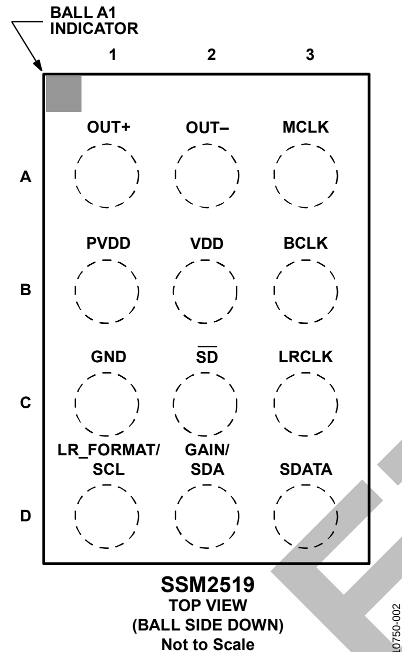

Figure 4. Pin Configuration—Top View

Table 7. Pin Function Descriptions

Ball Number	Pin Name	Function[1]	Description
A1	OUT+	O	Amplifier Output Positive
A2	OUT−	O	Amplifier Output Negative
A3	MCLK	I	Serial Audio Interface Master Clock
B1	PVDD	P	2.5 V to 5.5 V Amplifier Power
B2	VDD	P	1.5 V to 3.6 V Digital and Analog Power
B3	BCLK	I	I^{2}S Bit Clock/Generated BCLK Rate Select
C1	GND	P	Ground
C2	$\overline{SD}$	I	Power-Down Control—Active Low
C3	LRCLK	I	I^{2}S Left/Right Frame Clock
D1	LR_FORMAT/SCL	I	Left/Right Channel Selection and Serial Format Selection/I^{2}C Clock
D2	GAIN/SDA	I/O	Digital and Analog Gain Selection/I^{2}C Serial Data
D3	SDATA	I	I^{2}S Serial Data

[1] I = input, O = output, P = power.

TYPICAL PERFORMANCE CHARACTERISTICS

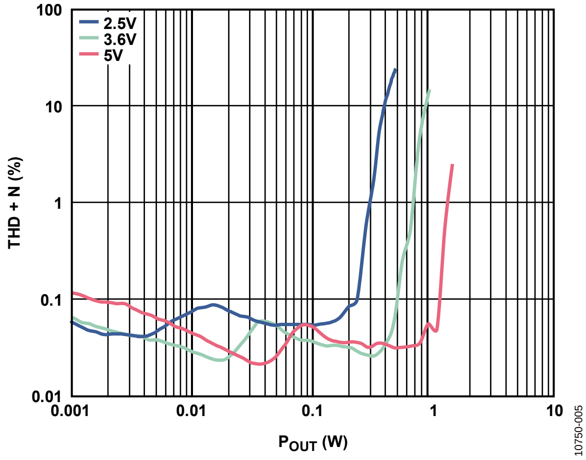

Figure 5. THD + N vs. Output Power into 8 Ω, 5.0 V Gain Setting

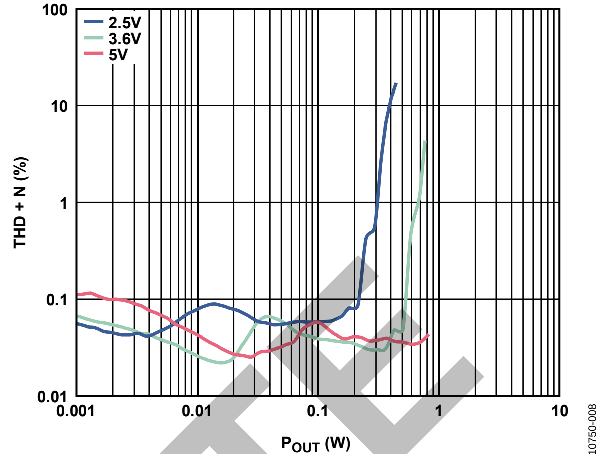

Figure 8. THD + N vs. Output Power into 8 Ω, 3.6 V Gain Setting

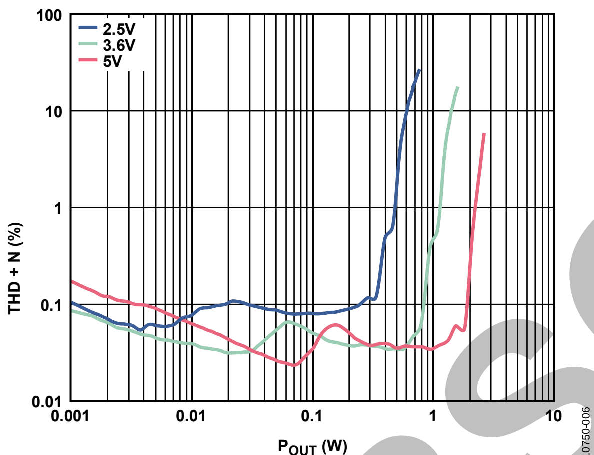

Figure 6. THD + N vs. Output Power into 4 Ω, 5.0 V Gain Setting

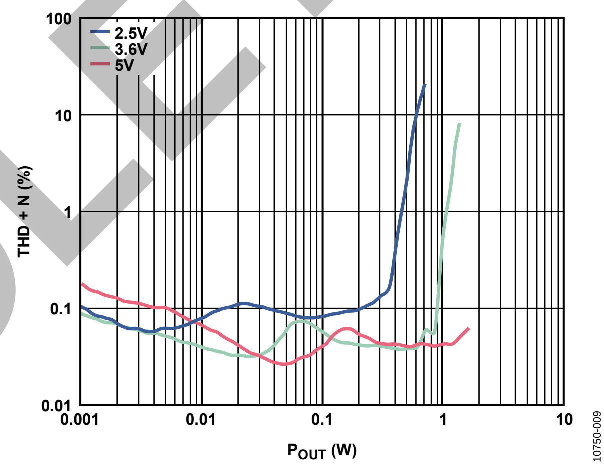

Figure 9. THD + N vs. Output Power into 4 Ω, 3.6 V Gain Setting

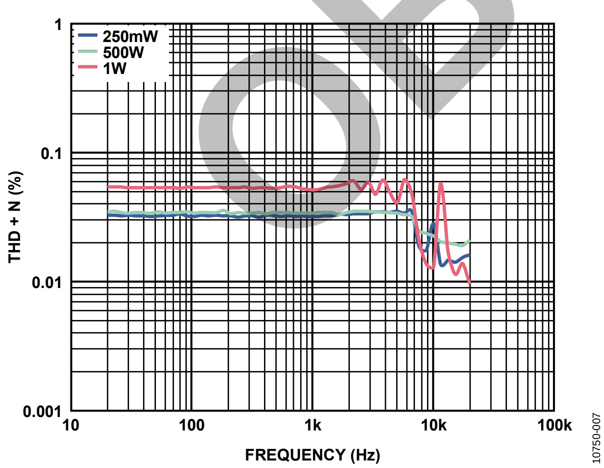

Figure 7. THD + N vs. Frequency into 8 Ω, PV_{DD} = 5.0 V

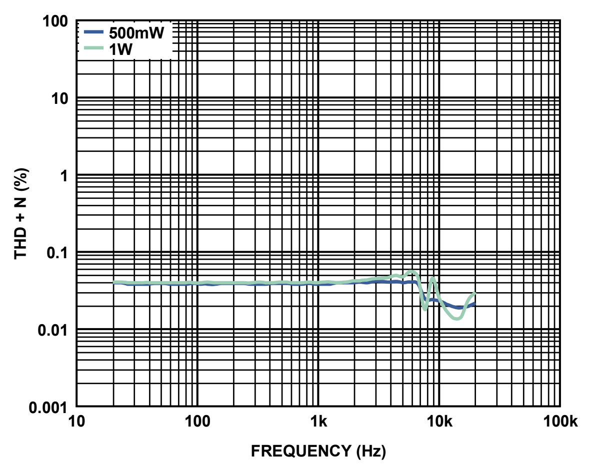

Figure 10. THD + N vs. Frequency into 4 Ω, PV_{DD} = 5.0 V

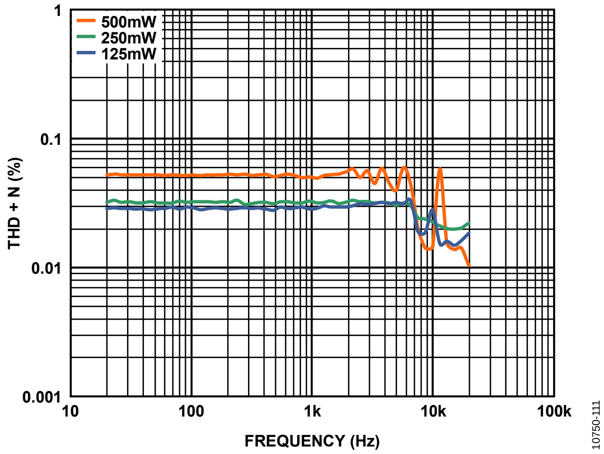

Figure 11. THD + N vs. Frequency into 8 Ω, PV_{DD} = 3.6 V

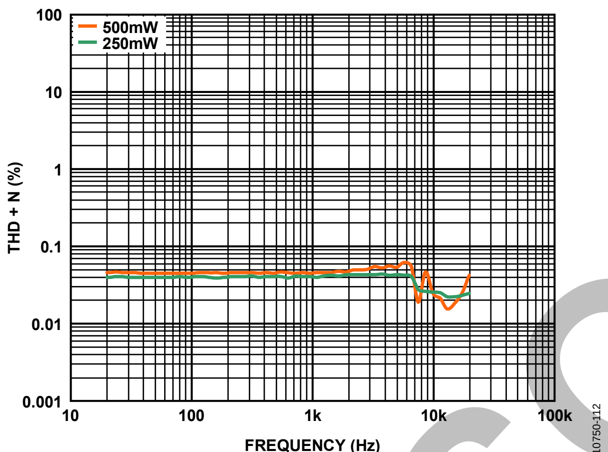

Figure 12. THD + N vs. Frequency into 4 Ω, PV_{DD} = 3.6 V

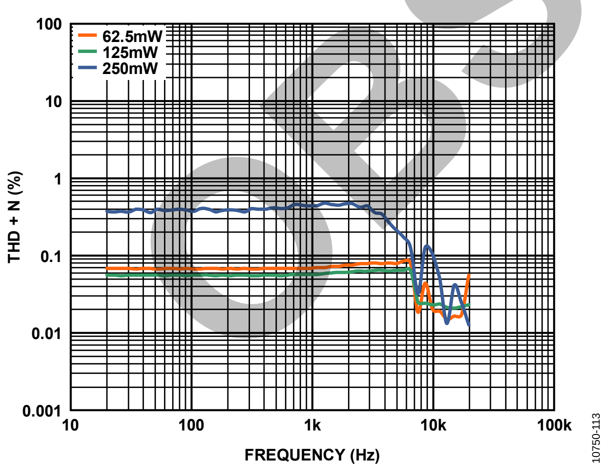

Figure 13. THD + N vs. Frequency into 8 Ω, PV_{DD} = 2.5 V

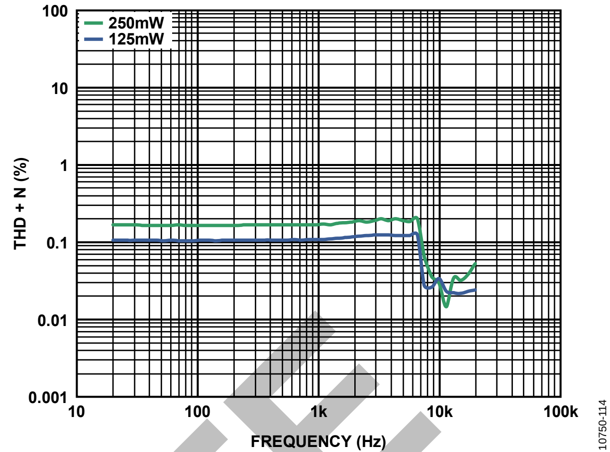

Figure 14. THD + N vs. Frequency into 4 Ω, PV_{DD} = 2.5 V

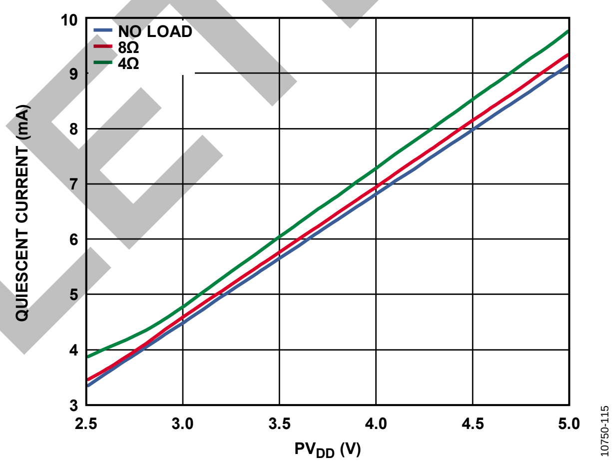

Figure 15. Quiescent Current vs. Supply Voltage PV_{DD}

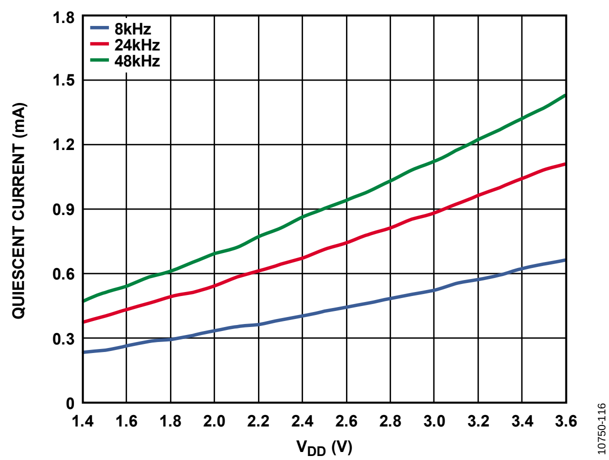

Figure 16. Quiescent Current vs. Supply Voltage V_{DD}

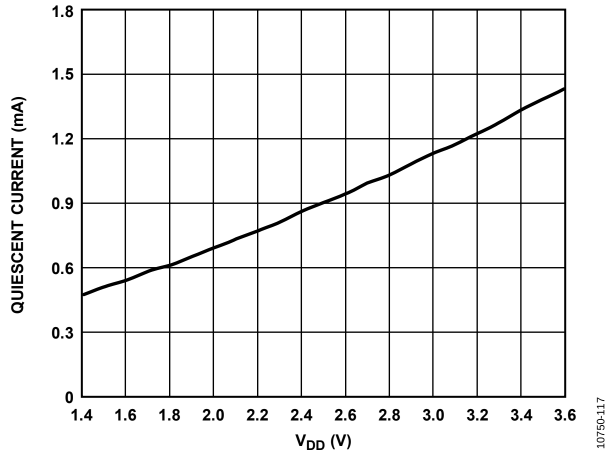

Figure 17. Quiescent Current vs. Supply Voltage V_{DD}

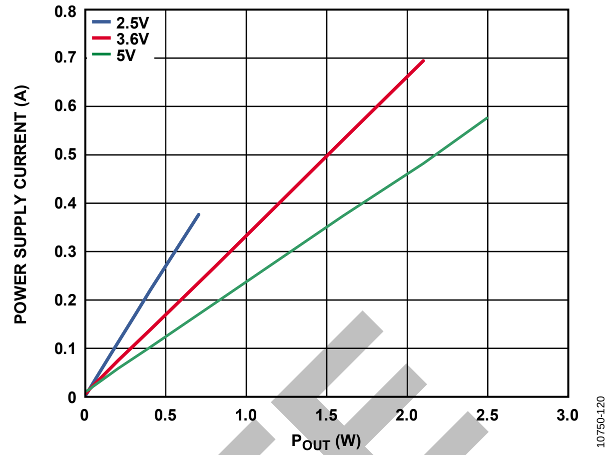

Figure 20. Power Supply Current vs. P_{OUT}, 4 Ω

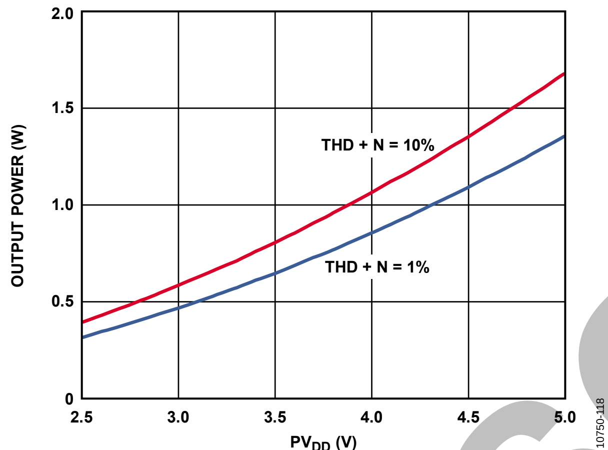

Figure 18. Maximum Output Power vs. PV_{DD}
(f_{IN} = 1 kHz, R_L = 8 Ω)

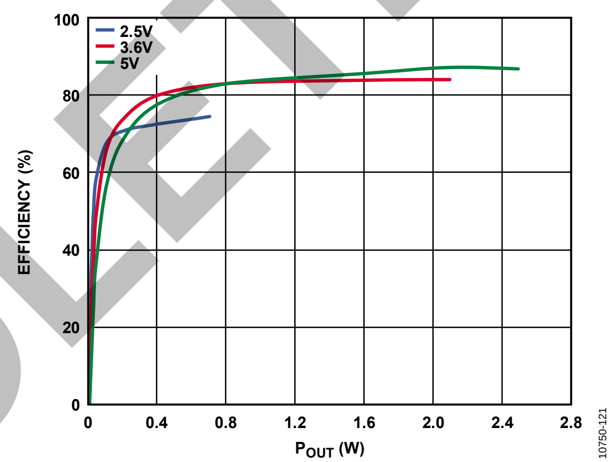

Figure 21. Class-D Efficiency vs. P_{OUT}, 4 Ω

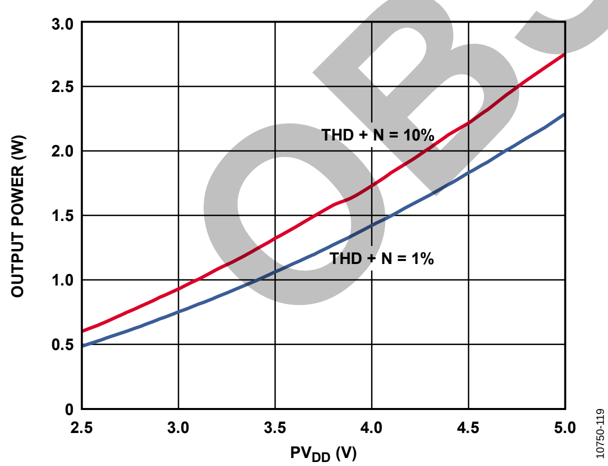

Figure 19. Maximum Output Power vs. PV_{DD}
(f_{IN} = 1 kHz, R_L = 4 Ω)

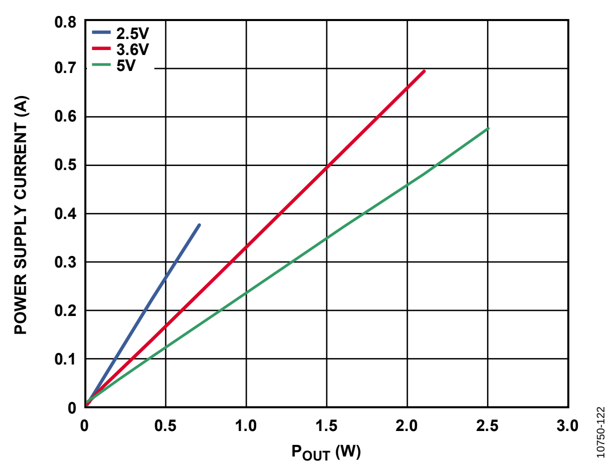

Figure 22. Power Supply Current vs. P_{OUT}, 8 Ω

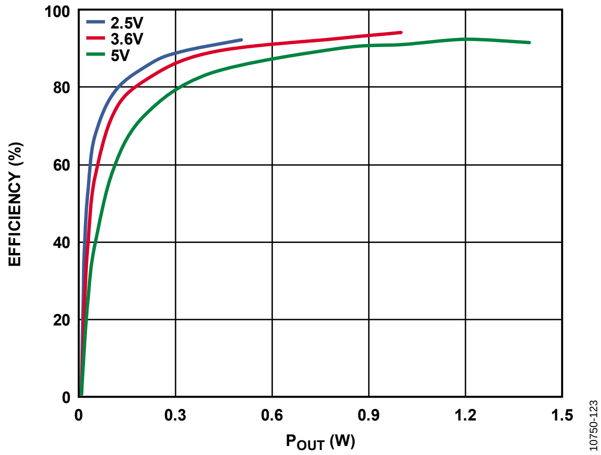

Figure 23. Class-D Efficiency vs. P_{OUT}, 8 Ω

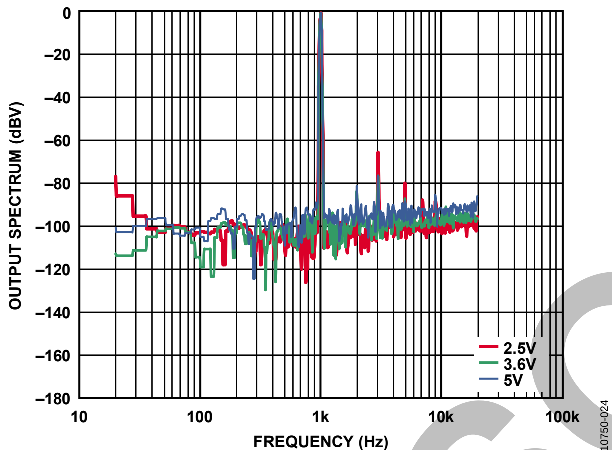

Figure 24. Output Spectrum, 100 mW, 8 Ω

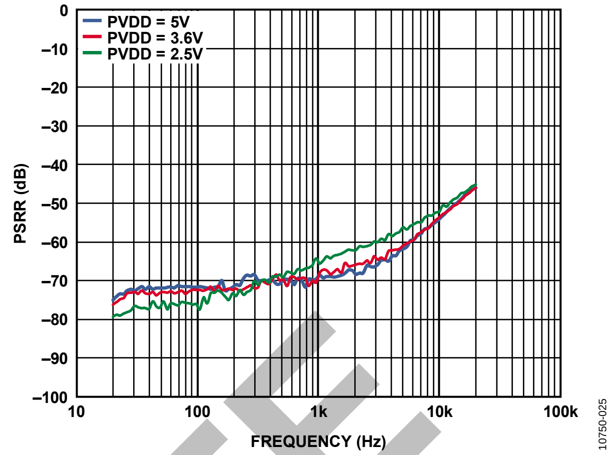

Figure 25. PSRR vs. Frequency

THEORY OF OPERATION

OVERVIEW

The SSM2519 is a fully integrated digital switching audio amplifier. The SSM2519 receives digital audio inputs and produces the PDM differential switching outputs using an internal power stage. The part has built-in protections against overtemperature as well as overcurrent. The SSM2519 also has built-in soft turn-on and soft turn-off for pop and click suppression.

STANDALONE AND I²C OPERATIONAL MODE

The SSM2519 supports both standalone and I²C control modes. The setting on the $\overline{SD}$ pin determines which mode is used.

Table 8. $\overline{SD}$ Pin Settings

$\overline{SD}$ Pin	Operation
Tie to VDD Through 20 kΩ	I²C
Connect to VDD Without 20 kΩ	Standalone mode
Connect to GND (Shorted or with 20 kΩ)	Shutdown mode

MASTER AND BIT CLOCK

The SSM2519 requires an external clock present at the MCLK input pin to operate. This clock must be fully synchronous with the incoming digital audio on the serial interface. Internal to the IC, a clock frequency of 2.048 MHz to 24.576 MHz is required. This internal clock is derived from the external MCLK by dividing, passing through, or doubling in frequency the external MCLK signal.

Different rates for MCLK are supported at different sample rates. Refer to Table 9 for all available options. The MCLK rate as well as sample rate can be automatically detected by setting the AMCS and ASR bits in Register 0x01, or they can be manually set (MCS bits in Register 0x00, and FS bits in Register 0x02) if AMCS or ASR is cleared.

When in standalone mode or in I²C mode and auto clock rate detection is enabled (Register 0x01, Bit 1, AMCS = 1), the internal clock generation circuitry is automatically configured. When autosample rate detection is disabled (AMCS = 0), the MCS bits in Register 0x00 must be set with the correct value to generate the internal clock.

When the SSM2519 has entered its power-down state, it is possible to gate this clock to conserve additional system power. However, a master clock must be present for the audio amplifier to operate.

If the serial interface bit clock (BCLK) is in the range of acceptable internal master clock frequencies (between 2.048 MHz and 6.144 MHz), it can serve as both master clock and the bit clock. Setting NO_BCLK (Bit 5 of Register 0x00) routes the signal on the MCLK pin to serve as the internal bit clock as well. In this case, tie the BCLK pin to ground.

Table 9. Supported MCLK Rate for Different Sample Frequencies

Sample Rates	Supported MCLK Rates	Supported MCLK Frequencies
8 kHz to 12 kHz	$256 \times f_S/512 \times f_S/1024 \times f_S/1536 \times f_S/2048 \times f_S$	2.048 MHz to 24.576 MHz
16 kHz to 24 kHz	$128 \times f_S/256 \times f_S/512 \times f_S/768 \times f_S/1024 \times f_S$	2.048 MHz to 24.576 MHz
32 kHz to 48 kHz	$64 \times f_S/128 \times f_S/256 \times f_S/384 \times f_S/512 \times f_S$	2.048 MHz to 24.576 MHz
8 kHz to 12 kHz	$400 \times f_S/800 \times f_S/1600 \times f_S$	3.2 MHz to 19.2 MHz
16 kHz to 24 kHz	$200 \times f_S/400 \times f_S/800 \times f_S$	3.2 MHz to 19.2 MHz
32 kHz to 48 kHz	$100 \times f_S/200 \times f_S/400 \times f_S$	3.2 MHz to 19.2 MHz

Table 10. Master Clock Select (MCS) Bit Settings: MCLK, Ratio, and Frequency

Input Sample Rate	Ratio/ MCLK	Setting 0, b0000	Setting 1, b0001	Setting 2, b0010	Setting 3, b0011	Setting 4, b0100	Setting 5, b0101	Setting 6, b0110	Setting 7, b0111	Setting 8, b1000
8 kHz	Ratio	256 × f_S[1]	512 × f_S	1024 × f_S	1536 × f_S	2048 × f_S	3072 × f_S	400 × f_S	800 × f_S	1600 × f_S
	MCLK	2.048 MHz	4.096 MHz	8.192 MHz	12.288 MHz	16.384 MHz	24.576 MHz	3.20 MHz	6.40 MHz	12.80 MHz
11.025 kHz	Ratio	256 × f_S[1]	512 × f_S	1024 × f_S	1536 × f_S	2048 × f_S	3072 × f_S	400 × f_S	800 × f_S	1600 × f_S
	MCLK	2.822 MHz	5.6448 MHz	11.2896 MHz	16.9344 MHz	22.5792 MHz	33.8688 MHz	4.41 MHz	8.82 MHz	17.64 MHz
12 kHz	Ratio	256 × f_S[1]	512 × f_S	1024 × f_S	1536 × f_S	2048 × f_S	3072 × f_S	400 × f_S	800 × f_S	1600 × f_S
	MCLK	3.072 MHz	6.144 MHz	12.288 MHz	18.432 MHz	24.576 MHz	38.864 MHz	4.80 MHz	9.60 MHz	19.20 MHz
16 kHz	Ratio	128 × f_S[1]	256 × f_S	384 × f_S	768 × f_S	1024 × f_S	1536 × f_S	200 × f_S	400 × f_S	800 × f_S
	MCLK	2.048 MHz	4.096 MHz	8.192 MHz	12.288 MHz	16.384 MHz	24.576 MHz	3.20 MHz	6.40 MHz	12.80 MHz
22.05 kHz	Ratio	128 × f_S[1]	256 × f_S	512 × f_S	768 × f_S	1024 × f_S	1536 × f_S	200 × f_S	400 × f_S	800 × f_S
	MCLK	2.822 MHz	5.6448 MHz	11.2896 MHz	16.9344 MHz	22.5792 MHz	33.8688 MHz	4.41 MHz	8.82 MHz	17.64 MHz
24 kHz	Ratio	128 × f_S[1]	256 × f_S	512 × f_S	768 × f_S	1024 × f_S	1536 × f_S	200 × f_S	400 × f_S	800 × f_S
	MCLK	3.072 MHz	6.144 MHz	12.288 MHz	18.432 MHz	24.576 MHz	38.864 MHz	4.80 MHz	9.60 MHz	19.20 MHz
32 kHz	Ratio	64 × f_S[1]	128 × f_S	256 × f_S	384 × f_S	512 × f_S	768 × f_S	100 × f_S	200 × f_S	400 × f_S
	MCLK	2.048 MHz	4.096 MHz	8.192 MHz	12.288 MHz	16.384 MHz	24.576 MHz	3.20 MHz	6.40 MHz	12.80 MHz
44.1 kHz	Ratio	64 × f_S[1]	128 × f_S	256 × f_S	384 × f_S	512 × f_S	768 × f_S	100 × f_S	200 × f_S	400 × f_S
	MCLK	2.822 MHz	5.6448 MHz	11.2896 MHz	16.9344 MHz	22.5792 MHz	33.8688 MHz	4.41 MHz	8.82 MHz	17.64 MHz
48 kHz	Ratio	64 × f_S[1]	128 × f_S	256 × f_S	384 × f_S	512 × f_S	768 × f_S	100 × f_S	200 × f_S	400 × f_S
	MCLK	3.072 MHz	6.144 MHz	12.288 MHz	18.432 MHz	24.576 MHz	38.864 MHz	4.80 MHz	9.60 MHz	19.20 MHz

[1] When using MCS = 0/64 f_S mode, the chip automatically operates in low power mode.

DIGITAL INPUT SERIAL AUDIO INTERFACE

It is capable of receiving stereo I²S, left justified, or right justified data. Mono, stereo, and multichannel PCM/TDM interface formats are available. The data and interface formats are selected by adjusting the SDATA_FMT and SAI bits in Register 0x02. Note that, when operating in right justified mode, the proper data width must be chosen. The BCLK signal does not have to be provided to the SSM2519. It can internally generate the appropriate BCLK signal. To operate without a BCLK, the BCLK pin should be tied to VDD or GND to select the appropriate BCLK rate for the SDATA input.

Table 11. BCLK Pin Connection Options

BCLK Pin	Generation	BCLK Rate
Connected to External Clock Source	External	Any
Tied to VDD	Internal	16 bit clocks/channel
Tied to GND	Internal	32 bit clocks/channel

When the SSM2519 is set up in standalone mode, a subset of serial interface formats are available. Selection of these serial formats and input channel are determined by the LR_FORMAT pin.

Table 12. LR_FORMAT Pin Configuration Controls

LR_FORMAT Pin Configuration	Serial Format/Channel Select
Tie to VDD	I²S/left channel
Tie to VDD Through 150 kΩ	Special gain case[1] (I²S/left channel)
Tie to VDD Through 47 kΩ	PCM/left channel
Tie to VDD Through 15 kΩ	LJ/left channel
Tie to GND	I²S/right channel

[1] See Table 14.

CHANNEL MAPPING

Stereo audio formats and TDM formats with two, four, eight, or 16 channels are available. In these modes, the amplifier audio can be chosen from any of the available TDM slots using the CH_SEL bits in Register 0x04. For most digital interface formats, many of these options are not present. For example, in stereo modes, only Channel 0 and Channel 1 are valid, and in four-slot TDM mode, only Channel 0, Channel 1, Channel 2, and Channel 3 are valid.

POWER SUPPLIES

The SSM2519 has two internal power supplies that must be provided. PVDD supplies power to the full-bridge power stage of MOSFETs and its associated drive, control, and protection circuitry. PVDD can operate from 2.5 V to 5.5 V and must be present to obtain audio output. Lowering the PVDD supply results in lower output power and correspondingly lower power consumption. This does not affect audio performance.

VDD provides power to the digital logic, analog components, and I/O circuitry. VDD can operate from 1.5 V to 3.6 V and must be provided to obtain audio output. Lowering the supply voltage results in lower power consumption, but does not result in lower audio performance.

POWER CONTROL

The IC starts up in software power-down mode, where all blocks except for the I²C interface are disabled. To fully power up the amplifier, clear SPWDN (Bit 0 of Register 0x00). In addition to the software power-down, the software master mute control (M_MUTE) is enabled at the initial state of the amplifier; therefore, no audio is output until Bit 0 of Register 0x06 is cleared.

The SSM2519 contains a smart power-down feature that, when enabled, analyzes the incoming digital audio and, if the audio is zero for 512 consecutive samples, regardless of sample rate, places the IC in the smart power-down state. In this state, all circuitry except the I²S ports are placed in a low power state. After this state is entered, the I²S input and master clock (MCLK) can be removed to place the part in its lowest power state. When a single nonzero input is received, the SSM2519 leaves this state and resumes normal operation.

The SSM2519 can also be powered down to its lowest power state by pulling the $\overline{\text{SD}}$ pin low.

POWER-ON RESET/VOLTAGE SUPERVISOR

The SSM2519 includes an internal power-on reset and voltage supervisor circuit. This circuit provides an internal reset to all circuitry during initial power-up. It also monitors the power supplies to the IC, mutes the output, and issues a reset when the voltages fall below the minimum operating range. This is done to ensure that no damage occurs due to low voltage operation and that no pops can occur under nearly any power removal condition.

A soft reset of the chip can be issued through I²C by setting Bit 7 of Register 0x00 (S_RST).

LOW POWER MODES

Two low power modes are available. If DAC_LPM (Bit 5 of Register 0x01) is set, the digital-to-analog converter (DAC) runs at half speed, reducing the quiescent current. This half speed mode is also active when the MCS setting (Bits[4:1] of Register 0x00) is set to its lowest value (MCS = 0000) because the slowest acceptable MCLK rates can only support half speed DAC operation.

If AMP_LPM (Bit 6 of Register 0x01) is set, the Σ-Δ modulator runs in a special mode that offers lower quiescent current when the output power is small, at the expense of slightly degraded audio performance.

VOLUME CONTROL

The SSM2519 has a digital volume control. There are 255 levels available, providing a range from +24 dB to −71.25 dB in 0.375 dB increments. This is a soft volume control, meaning that the gain is adjusted continuously from one value to another. This continuously adjusted gain prevents the audible pop that occurs with an instantaneous gain adjustment.

ANALOG GAIN

The SSM2519 has selectable digital and analog gain. Selection of these gains occurs via the GAIN pin. The analog gain settings are optimized for operation at 2.5 V, 3.6 V, 4.2 V, or 5 V PVDD.

Table 13. GAIN Pin Configuration Control

GAIN Pin Configuration	Analog Gain/Digital Gain
Tie to VDD	5 V optimized analog/0 dB digital gain
Tie to VDD Through 150 kΩ	5 V optimized analog/6 dB digital gain
Tie to VDD Through 47 kΩ	4.2 V optimized analog/0 dB digital gain
Tie to VDD Through 15 kΩ	3.6 V optimized analog/−3 dB digital gain
Tie to GND	3.6 V optimized analog/0 dB digital gain

Table 14. Special Gain Case (LR_FORMAT Tied to VDD Through 150 kΩ) GAIN Pin Configuration Control

GAIN Pin Configuration	Analog Gain/Digital Gain
Tie to VDD	2.5 V optimized analog/−6.75 dB digital gain
Tie to GND	3.6 V optimized analog/0 dB digital gain

FAULT DETECTION AND RECOVERY

Two fault conditions are detected by the SSM2519 fault detection system: overcurrent and overtemperature. When either of these is detected, the amplifier shuts down and a read-only I²C bit is set to indicate the cause of the shutdown. The OC and OT fault indicators are Bit 6 and Bit 5, respectively, of Register 0x07. An autorecovery feature can be enabled for temperature faults, current faults, or both, depending on the state of ARCV (Bits[1:0] of Register 0x07).

DIGITAL AUDIO FORMATS

STEREO MODE

0x02[4:2], SAI = 0 (stereo: I²S, LJ, RJ)
0x02[6:5], SDATA_FMT = 0 (I²S), 1 (LJ), 2 (RJ 24-bit), 3 (RJ 16-bit)

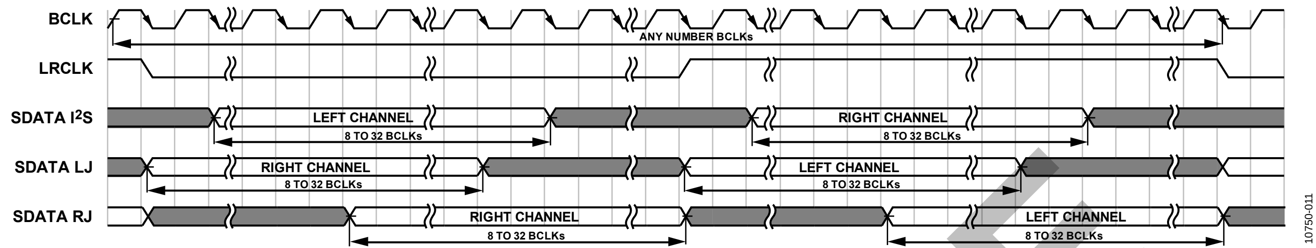

Figure 26. Stereo Modes: I²S, Left Justified, and Right Justified

TDM, 50% DUTY CYCLE MODE

0x02[4:2], SAI = 1 (2 channels), 2 (4 channels), 3 (8 channels), 4 (16 channels)
0x02[6:5], SDATA_FMT = 0 (I²S), 1 (LJ), 2 (RJ 24-bit), 3 (RJ 16-bit)
0x03[1], BCLK_EDGE = 0 (rising BCLK edge used)
0x03[6], LRCLK_MODE = 0 (50% duty cycl LRCLK)
0x03[3:2], SLOT_WIDTH = 0 (32 BCLK cycles), 1 (24 BCLK cycles), 2 (16 BCLK cycles)

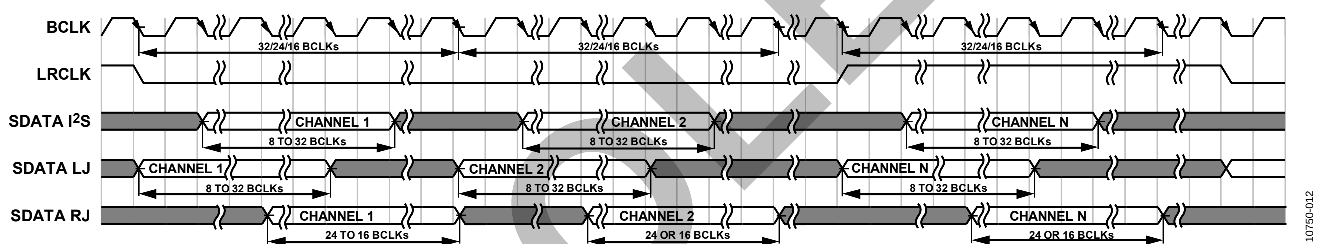

Figure 27. TDM Modes with 50% Duty Cycle LRCLK

TDM, PULSE MODE

0x02[4:2], SAI = 1 (2 channels), 2 (4 channels), 3 (8 channels), 4 (16 channels)
0x02[6:5], SDATA_FMT = 0 (I²S), 1 (LJ), 2 (RJ 24-bit), 3 (RJ 16-bit)
0x03[1], BCLK_EDGE = 0 (rising BCLK edge used)
0x03[6], LRCLK_MODE = 1 (pulse mode LRCLK)
0x03[3:2], SLOT_WIDTH = 0 (32 BCLK cycles), 1 (24 BCLK cycles), 2 (16 BCLK cycles)

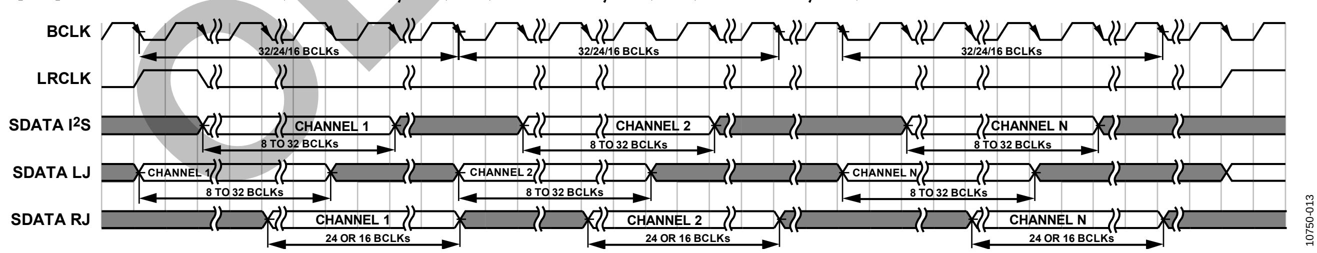

Figure 28. TDM Modes with Pulse Mode LRCLK

PCM, MULTICHANNEL MODE

0x02[4:2], SAI = 1 (2 channels), 2 (4 channels), 3 (8 channels), 4 (16 channels)
0x02[6:5], SDATA_FMT = 0 (I^2S), 1 (LJ), 2 (RJ 24-bit), 3 (RJ 16-bit)
0x03[1], BCLK_EDGE = 1 (falling BCLK edge used)
0x03[6], LRCLK_MODE = 1 (pulse mode LRCLK)
0x03[3:2], SLOT_WIDTH = 0 (32 cycles), 1 (24 cycles), 2 (16 cycles)

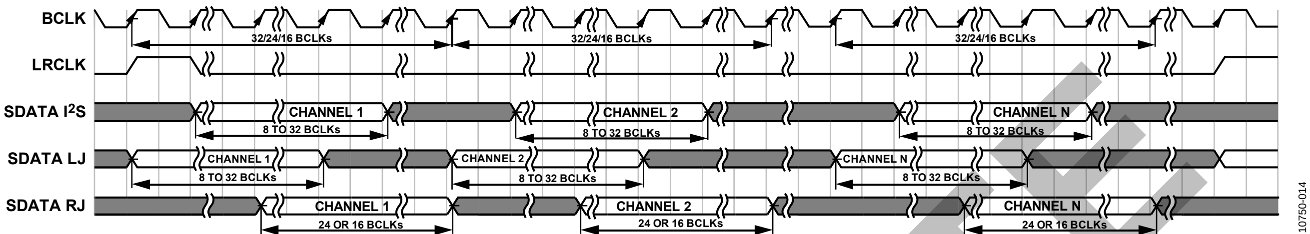

Figure 29. Multichannel PCM Modes

PCM, MONO MODE

0x02[4:2], SAI = 5
0x02[6:5], SDATA_FMT = 0 (I^2S), 1 (LJ), 2 (RJ 24-bit), 3 (RJ 16-bit)
0x03[1], BCLK_EDGE = 1 (falling BCLK edge used)
0x03[6], LRCLK_MODE = 1 (pulse mode LRCLK)

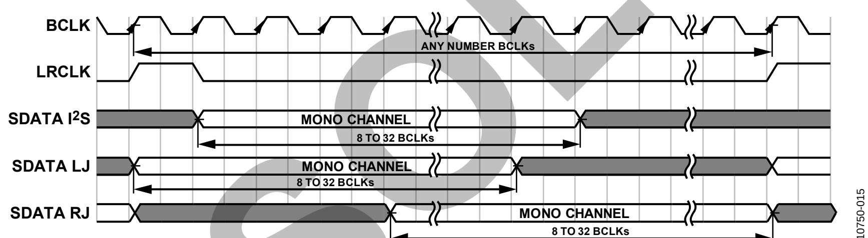

Figure 30. Mono PCM Modes

I^{2}C CONFIGURATION INTERFACE

OVERVIEW

The SSM2519 supports a 2-wire serial (I^{2}C-compatible) microprocessor bus driving multiple peripherals. Two pins, serial data (SDA) and serial clock (SCL), carry information between the SSM2519 and the system I^{2}C master controller. The SSM2519 is always a slave on the bus, meaning it cannot initiate a data transfer. Each slave device is recognized by a unique device address. The device address byte format is shown in Figure 31. The address resides in the first seven bits of the I^{2}C write. The LSB (Bit 7) of this byte sets either a read or write operation.

Logic Level 1 corresponds to a read operation, and Logic Level 0 corresponds to a write operation. The full byte addresses are shown in Figure 31, where the subaddresses are automatically incremented at word boundaries and can be used for writing large amounts of data to contiguous memory locations. This increment happens automatically after a single word write, unless a stop condition is encountered. A data transfer is always terminated by a stop condition.

Both SDA and SCL should have a 2.2 kΩ pull-up resistor on the lines connected to them.

The device address is 0x70.

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1	1	1	0	0	0	0	$R/\overline{W}$

10750-016

Figure 31. I^{2}C Device Address Byte Format

Addressing

Initially, each device on the I^{2}C bus is in an idle state, monitoring the SDA and SCL lines for a start condition and the proper address. The I^{2}C master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address/data stream follows. All devices on the bus respond to the start condition and shift the next eight bits (the 7-bit address plus the $R/\overline{W}$ bit) MSB first. The device that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This ninth bit is known as an acknowledge bit. All other devices withdraw from the bus at this point and return to the idle condition. The $R/\overline{W}$ bit determines the direction of the data. A Logic 0 on the LSB of the first byte means that the master writes information to the peripheral, whereas a Logic 1 means that the master reads information from the peripheral after writing the subaddress and repeating the start address. A data transfer takes place until a stop condition is encountered. A stop condition occurs when SDA transitions from low to high while SCL is held high. The timing for the I^{2}C port is shown in Figure 3.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, the SSM2519 immediately jumps to the idle condition. During a given SCL high period, the user should issue only one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the SSM2519 does not issue an acknowledge and returns to the idle condition. If the user exceeds the highest subaddress while in auto-increment mode, one of two actions is taken. In read mode, the SSM2519 outputs the highest subaddress register contents until the master device issues a no acknowledge, indicating the end of a read. A no acknowledge condition is where the SDA line is not pulled low on the ninth clock pulse of SCL. If the highest subaddress location is reached while in write mode, the data for the invalid byte is not loaded into any subaddress register, a no acknowledge is issued by the SSM2519, and the part returns to the idle condition.

I^{2}C Read and Write Operations

Figure 33 shows the timing of a single-word write operation. Every ninth clock, the SSM2519 issues an acknowledge by pulling SDA low.

Figure 34 shows the timing of a burst mode write sequence. This figure shows an example where the target destination registers are two bytes. The SSM2519 knows to increment its subaddress register every byte because the requested subaddress corresponds to a register or memory area with a byte word length.

The timing of a single-word read operation is shown in Figure 35. Note that the first $R/\overline{W}$ bit is 0, indicating a write operation. This is because the subaddress still needs to be written to set up the internal address. After the SSM2519 acknowledges the receipt of the subaddress, the master must issue a repeated start command followed by the chip address byte with the $R/\overline{W}$ bit set to 1 (read). This causes the SSM2519 SDA to reverse and begin driving data back to the master. The master then responds every ninth pulse with an acknowledge pulse to the SSM2519.

Figure 36 shows the timing of a burst mode read sequence. This figure shows an example where the target destination registers are two bytes. The SSM2519 knows to increment its subaddress register at every byte because the requested subaddress corresponds to a register or memory area with a byte word length.

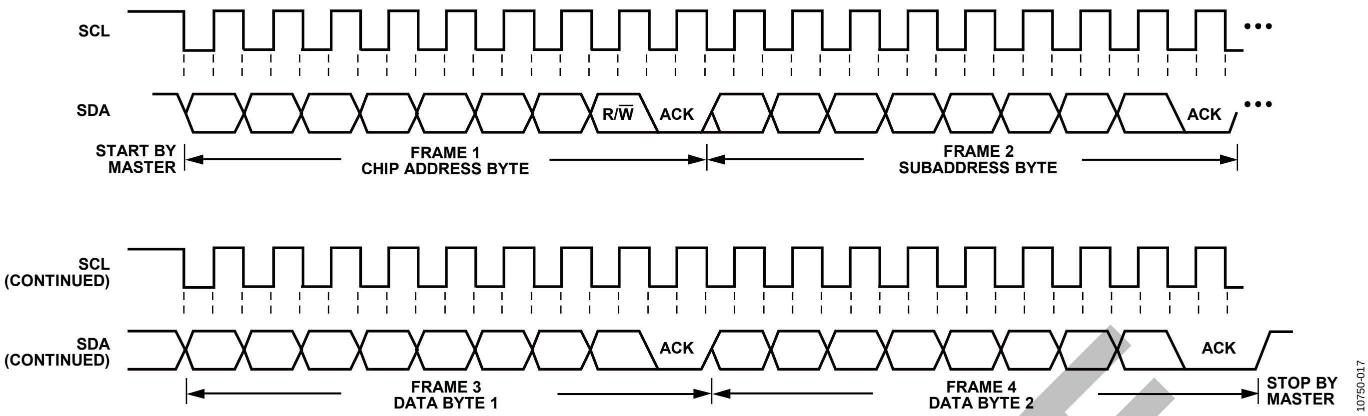

Figure 32. I²C Read/Write Timing

START BIT	CHIP ADDRESS (7 BITS)	R/W̄ = 0	ACK BY SLAVE	SUBADDRESS (8 BITS)	ACK BY SLAVE	DATA BYTE 1 (8 BITS)	STOP BIT

10750-018

Figure 33. Single-Word I²C Write Format

START BIT	CHIP ADDRESS R/W̄ = 0	ACK BY SLAVE	SUBADDRESS	ACK BY SLAVE	DATA-WORD 1	ACK BY SLAVE	DATA-WORD 2	ACK BY SLAVE	• • •	STOP BIT

10750-019

Figure 34. Burst Mode I²C Write Format

START BIT	CHIP ADDRESS R/W̄ = 0	ACK BY SLAVE	SUBADDRESS	ACK BY SLAVE	START BIT	CHIP ADDRESS R/W̄ = 1	ACK BY SLAVE	DATA BYTE 1	ACK BY MASTER	STOP BIT

10750-020

Figure 35. Single-Word I²C Read Format

START BIT	CHIP ADDRESS R/W̄ = 0	ACK BY SLAVE	SUBADDRESS	ACK BY SLAVE	START BIT	CHIP ADDRESS R/W̄ = 1	ACK BY SLAVE	DATA-WORD 1	ACK BY MASTER	• • •	STOP BIT

10750-021

Figure 36. Burst Mode I²C Read Format

REGISTER SUMMARY

Table 15. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	PWR_CTRL	[7:0]	S_RST	RESERVED	NO_BCLK	MCS				SPWDN	0x05	RW
0x01	SYS_CTRL	[7:0]	HPF_EN	AMP_LPM	DAC_LPM	APWDN_EN	EDGE		AMCS	ASR	0x30	RW
0x02	SAI_FMT1	[7:0]	RESERVED	SDATA_FMT		SAI			FS		0x02	RW
0x03	SAI_FMT2	[7:0]	BCLK_GEN	LRCLK_MODE	LRCLK_POL	SAI_MSB	SLOT_WIDTH		BCLK_EDGE	RESERVED	0x00	RW
0x04	CH_SEL	[7:0]	RESERVED				CH_SEL				0x00	RW
0x05	VOL_CTRL	[7:0]	VOL								0x40	RW
0x06	GAIN_CTRL	[7:0]	AMUTE	RESERVED	ANA_GAIN		RESERVED			M_MUTE	0x11	RW
0x07	FAULT_CTRL1	[7:0]	RESERVED	OC	OT	MRCV	MAX_AR		ARCV		0x0C	RW

REGISTER DETAILS

SOFTWARE RESET AND MASTER SOFTWARE POWER-DOWN CONTROL REGISTER

Address: 0x00, Reset: 0x05, Name: PWR_CTRL

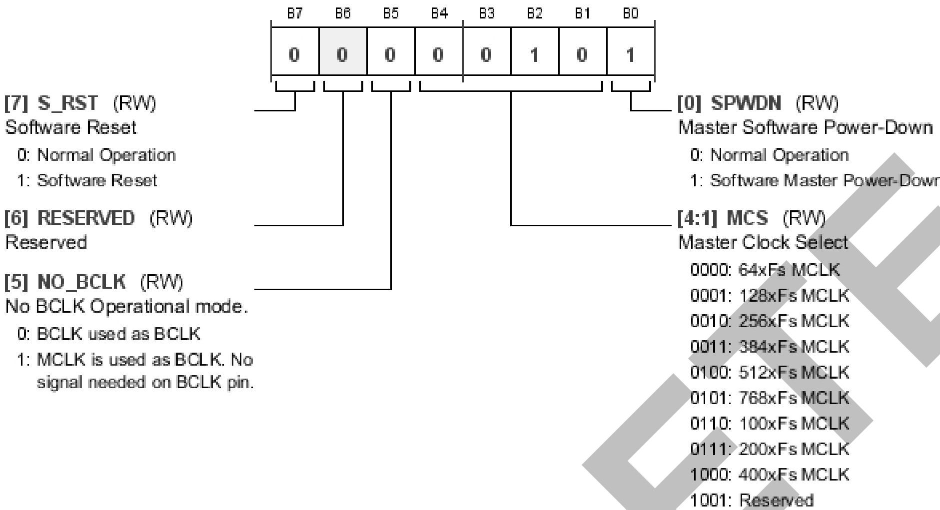

Table 16. Bit Descriptions for PWR_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
7	S_RST		Software reset. The software reset bit resets all internal blocks, including I^2C registers, to their default states.	0x0	RW
		0	Normal operation		
		1	Software reset		
6	RESERVED		Reserved.	0x0	RW
5	NO_BCLK		No BCLK operational mode. MCLK also used as BCLK.	0x0	RW
		0	BCLK used as BCLK		
		1	MCLK used as BCLK. No signal needed on BCLK pin.		
[4:1]	MCS		Master clock select. MCS must be set according to the input MCLK ratio relative to the input sample frequency. Refer to Table 10.	0x2	RW
		0000	$64 \times f_S$ MCLK		
		0001	$128 \times f_S$ MCLK		
		0010	$256 \times f_S$ MCLK		
		0011	$384 \times f_S$ MCLK		
		0100	$512 \times f_S$ MCLK		
		0101	$768 \times f_S$ MCLK		
		0110	$100 \times f_S$ MCLK		
		0111	$200 \times f_S$ MCLK		
		1000	$400 \times f_S$ MCLK		
		1001	Reserved		
0	SPWDN		Master software power-down. Software power-down puts all blocks except the I^2C interface in a low power state.	0x1	RW
		0	Normal operation		
		1	Software master power-down		

EDGE SPEED, POWER, AND CLOCKING CONTROL REGISTER

Address: 0x01, Reset: 0x30, Name: SYS_CTRL

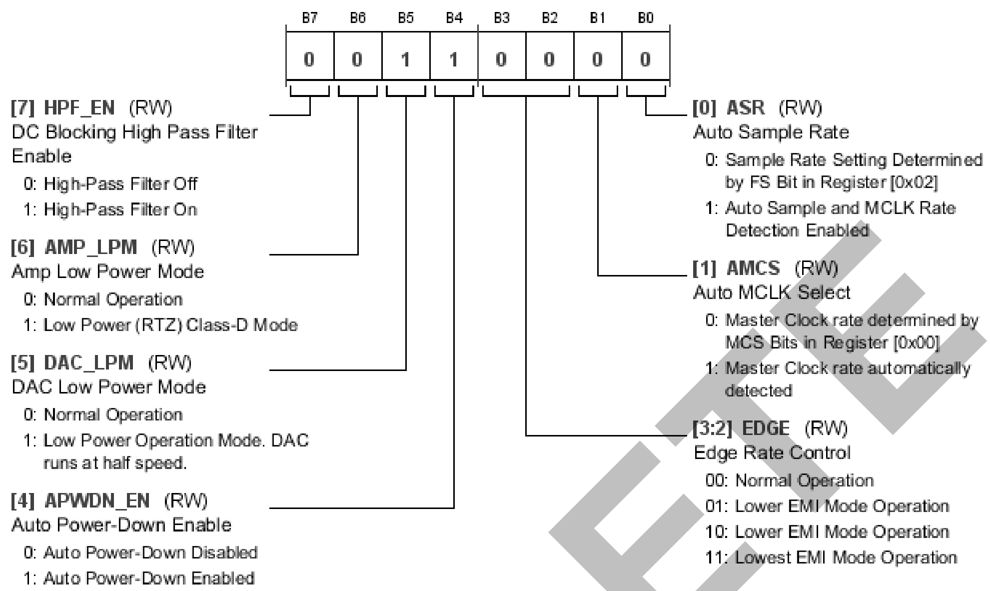

Table 17. Bit Descriptions for SYS_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
7	HPF_EN		DC blocking high-pass filter enable. The SSM2519 contains a selectable high-pass filter. The −3 dB frequency is at 6 Hz with a 48 kHz sample rate. This frequency increases linearly with lower sample rates.	0x0	RW
		0	High-pass filter off		
		1	High-pass filter on		
6	AMP_LPM		Amplifier low power mode.	0x0	RW
		0	Normal operation		
		1	Low power (return to zero) Class-D mode		
5	DAC_LPM		DAC low power mode.	0x1	RW
		0	Normal operation		
		1	Low power operation mode. DAC runs at half speed.		
4	APWDN_EN		Auto power-down enable. Auto power-down automatically puts the IC in a low power state when 2048 consecutive zero input samples have been received.	0x1	RW
		0	Auto power-down disabled		
		1	Auto power-down enabled		
[3:2]	EDGE		Edge rate control. This controls the edge speed of the power stage. The low EMI operation mode reduces the edge speed, lowering EMI and power efficiency.	0x0	RW
		00	Normal operation		
		01	Lower EMI mode operation		
		10	Lower EMI mode operation		
		11	Lowest EMI mode operation		
1	AMCS		Auto MCLK select.	0x0	RW
		0	Master clock rate determined by MCS bits in Register 0x00		
		1	Master clock rate automatically detected		
0	ASR		Autosample rate.	0x0	RW
		0	Sample rate setting determined by FS bit in Register 0x02		
		1	Autosample and MCLK rate detection enabled		

SERIAL AUDIO INTERFACE AND SAMPLE RATE CONTROL REGISTER

Address: 0x02, Reset: 0x02, Name: SAI_FMT1

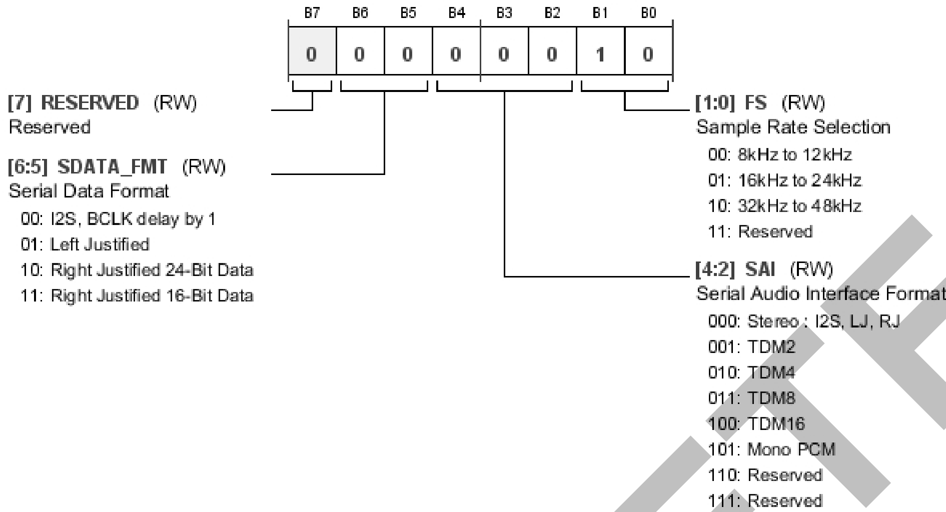

Table 18. Bit Descriptions for SAI_FMT1

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	RW
[6:5]	SDATA_FMT		Serial data format.	0x0	RW
		00	I^2S, BCLK delay by 1		
		01	Left justified		
		10	Right justified 24-bit data		
		11	Right justified 16-bit data		
[4:2]	SAI		Serial audio interface format.	0x0	RW
		000	Stereo: I^2S, LJ, RJ		
		001	TDM2		
		010	TDM4		
		011	TDM8		
		100	TDM16		
		101	Mono PCM		
		110	Reserved		
		111	Reserved		
[1:0]	FS		Sample rate selection.	0x2	RW
		00	8 kHz to 12 kHz		
		01	16 kHz to 24 kHz		
		10	32 kHz to 48 kHz		
		11	Reserved		

SERIAL AUDIO INTERFACE CONTROL REGISTER

Address: 0x03, Reset: 0x00, Name: SAI_FMT2

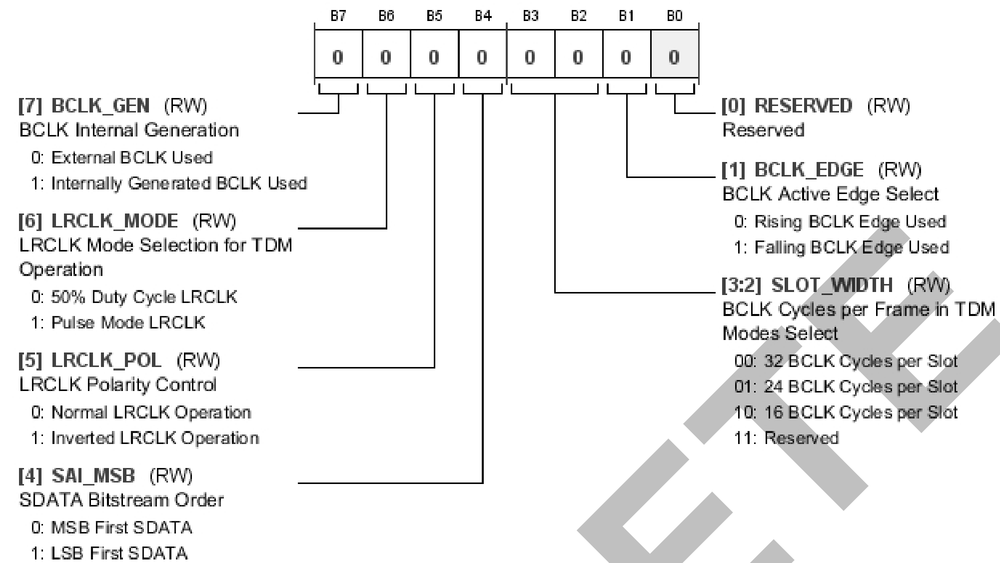

Table 19. Bit Descriptions for SAI_FMT2

Bits	Bit Name	Settings	Description	Reset	Access
7	BCLK_GEN		BCLK internal generation. When BCLK_GEN is enabled, an internally generated BCLK is used. Therefore, routing the BCLK signal to the pin is not required.	0x0	RW
		0	External BCLK used		
		1	Internally generated BCLK used		
6	LRCLK_MODE		LRCLK mode selection for TDM operation.	0x0	RW
		0	50% duty cycle LRCLK		
		1	Pulse mode LRCLK		
5	LRCLK_POL		LRCLK polarity control.	0x0	RW
		0	Normal LRCLK operation		
		1	Inverted LRCLK operation		
4	SAI_MSB		SDATA bit stream order.	0x0	RW
		0	MSB first SDATA		
		1	LSB first SDATA		
[3:2]	SLOT_WIDTH		BCLK cycles per frame in TDM modes select.	0x0	RW
		00	32 BCLK cycles per slot		
		01	24 BCLK cycles per slot		
		10	16 BCLK cycles per slot		
		11	Reserved		
1	BCLK_EDGE		BCLK active edge select.	0x0	RW
		0	Rising BCLK edge used		
		1	Falling BCLK edge used		
0	RESERVED		Reserved.	0x0	RW

CHANNEL MAPPING CONTROL REGISTER

Address: 0x04, Reset: 0x00, Name: CH_SEL

Note that not all the settings of CH_SEL are available in all serial interface modes. For example, in stereo and TDM2 modes, only Setting 0000 (Channel 0) and Setting 0001 (Channel 1) are valid because these modes can only contain two channels. In TDM4, Setting 0000 to Setting 0011 are supported. In TDM8, Setting 0000 to Setting 0111 are supported. In TDM16, Setting 0000 to Setting 1111 are supported.

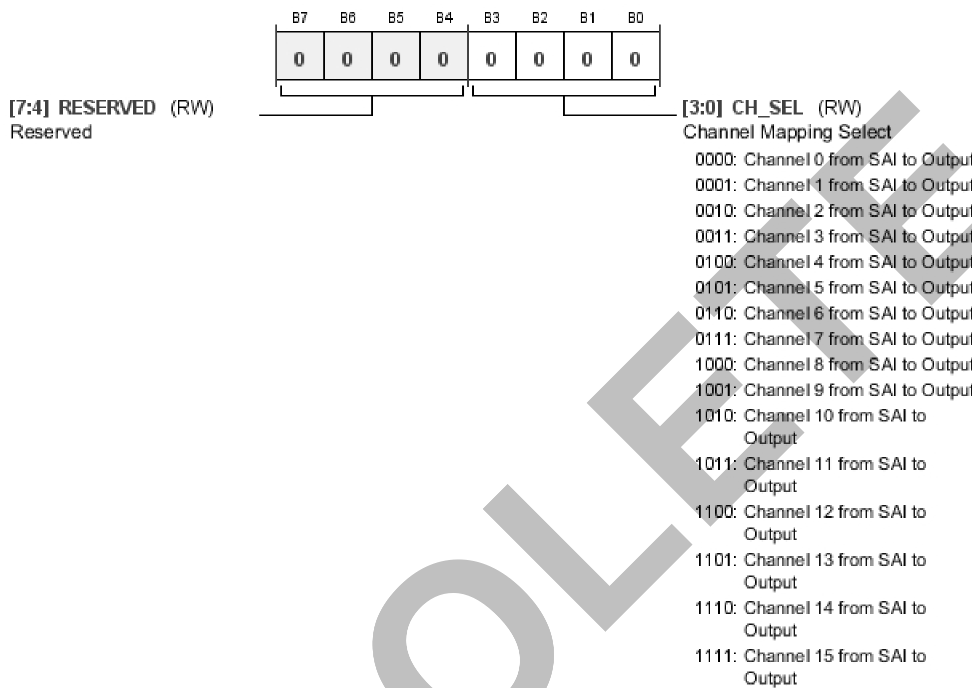

Table 20. Bit Descriptions for CH_SEL

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved.	0x0	RW
[3:0]	CH_SEL		Channel mapping select. Select input SDATA channel to map to left channel output.	0x0	RW
		0000	Channel 0 from SAI to output		
		0001	Channel 1 from SAI to output		
		0010	Channel 2 from SAI to output		
		0011	Channel 3 from SAI to output		
		0100	Channel 4 from SAI to output		
		0101	Channel 5 from SAI to output		
		0110	Channel 6 from SAI to output		
		0111	Channel 7 from SAI to output		
		1000	Channel 8 from SAI to output		
		1001	Channel 9 from SAI to output		
		1010	Channel 10 from SAI to output		
		1011	Channel 11 from SAI to output		
		1100	Channel 12 from SAI to output		
		1101	Channel 13 from SAI to output		
		1110	Channel 14 from SAI to output		
		1111	Channel 15 from SAI to output		

VOLUME CONTROL REGISTER

Address: 0x05, Reset: 0x40, Name: VOL_CTRL

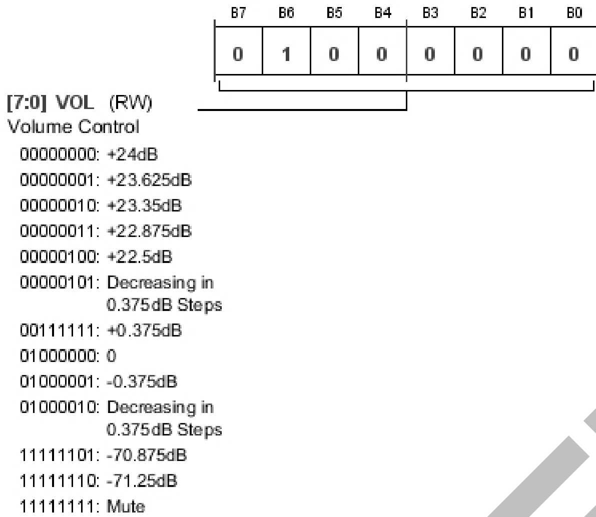

Table 21. Bit Descriptions for VOL_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VOL		Volume control.	0x40	RW
		00000000	+24 dB		
		00000001	+23.625 dB		
		00000010	+23.35 dB		
		00000011	+22.875 dB		
		00000100	+22.5 dB		
		00000101	Decreasing in 0.375 dB steps		
		00111111	+0.375 dB		
		01000000	0		
		01000001	−0.375 dB		
		01000010	Decreasing in 0.375 dB steps		
		11111101	−70.875 dB		
		11111110	−71.25 dB		
		11111111	Mute		

GAIN AND MUTE CONTROL REGISTER

Address: 0x06, Reset: 0x11, Name: GAIN_CTRL

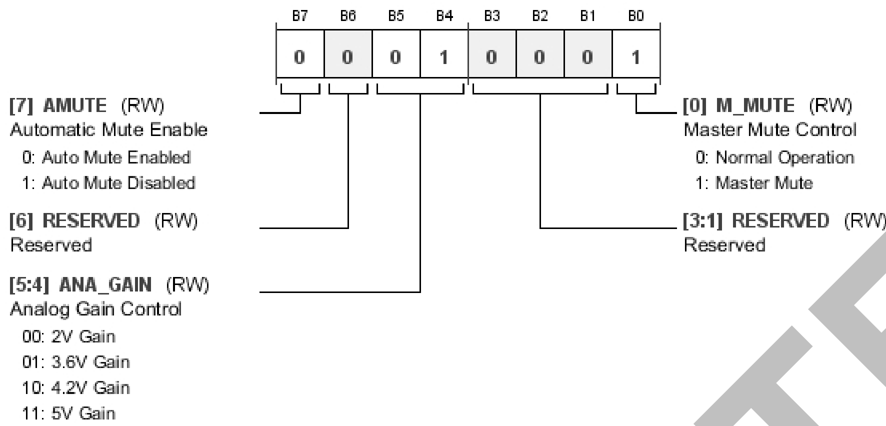

Table 22. Bit Descriptions for GAIN_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
7	AMUTE		Automatic mute enable. When the automatic mute function is enabled, after 2048 consecutive zero input samples have been received, the outputs are automatically muted.	0x0	RW
		0	Automute enabled		
		1	Automute disabled		
6	RESERVED		Reserved.	0x0	RW
[5:4]	ANA_GAIN		Analog gain control. This controls the analog gain of the Class-D modulator. There are two settings optimized for 3.6 V operation from a lithium ion battery and for 5 V operation.	0x1	RW
		00	2 V gain		
		01	3.6 V gain		
		10	4.2 V gain		
		11	5 V gain		
[3:1]	RESERVED		Reserved.	0x0	RW
0	M_MUTE		Master mute control. Setting the master mute control bit soft-mutes both channels.	0x1	RW
		0	Normal operation		
		1	Master mute		

FAULT CONTROL REGISTER

Address: 0x07, Reset: 0x0C, Name: FAULT_CTRL1

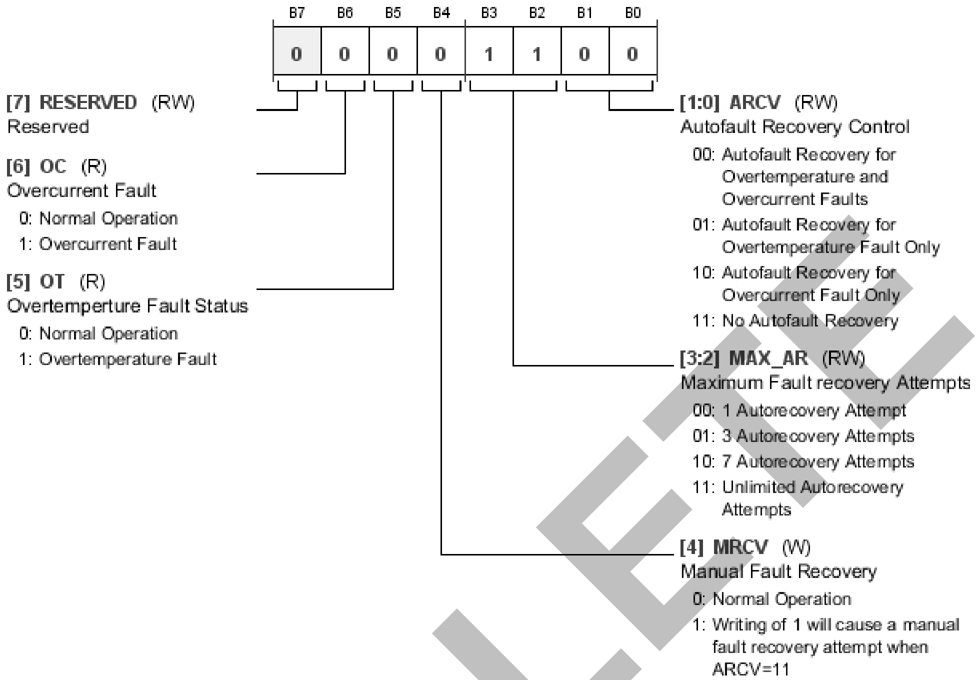

Table 23. Bit Descriptions for FAULT_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved.	0x0	RW
6	OC		Overcurrent fault.	0x0	R
		0	Normal operation		
		1	Overcurrent fault		
5	OT		Overtemperture fault status.	0x0	R
		0	Normal operation		
		1	Overtemperature fault		
4	MRCV		Manual fault recovery.	0x0	W
		0	Normal operation		
		1	Writing Logic 1 causes a manual fault recovery attempt when ARCV = 11		
[3:2]	MAX_AR		Maximum fault recovery attempts. The maximum automatic fault recovery bit determines how many attempts at autorecovery are performed.	0x3	RW
		00	One autorecovery attempt		
		01	Three autorecovery attempts		
		10	Seven autorecovery attempts		
		11	Unlimited autorecovery attempts		
[1:0]	ARCV		Autofault recovery control.	0x0	RW
		00	Autofault recovery for overtemperature and overcurrent faults		
		01	Autofault recovery for overtemperature fault only		
		10	Autofault recovery for overcurrent fault only		
		11	No autofault recovery		

OUTLINE DIMENSIONS

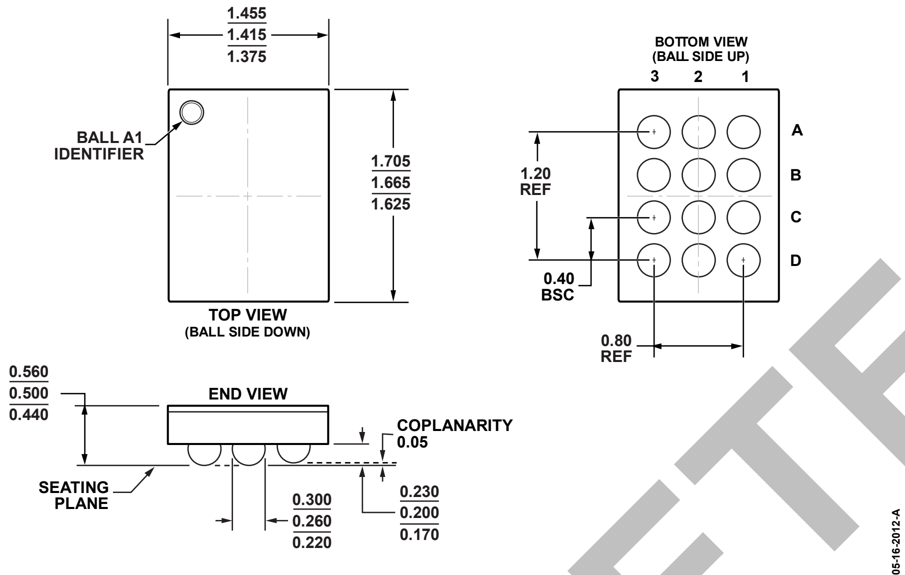

Figure 37. 12-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-12-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
SSM2519ACBZ-R7	−40°C to +85°C	12-Ball Wafer Level Chip Scale Package [WLCSP]	CB-12-6	Y4B
SSM2519ACBZ-RL	−40°C to +85°C	12-Ball Wafer Level Chip Scale Package [WLCSP]	CB-12-6	Y4B
EVAL-SSM2519Z		Evaluation Board		

[1] Z = RoHS Compliant Part.