Data Sheet

ADIN2299

RapID Platform Generation 2 (RPG2) Network Interface

FEATURES

- Configurable industrial protocol support
- PROFINET RT (Class B)
- PROFINET IRT (Class C): coming soon
- EtherNet/IP with DLR
- EtherCAT
- All protocols precertified
- Configurable applications processor interface
- UART: 115,200 bps to 1,000,000 bps
- Ethernet at 10 Mbps or 100 Mbps
- SPI follower: 10 MHz maximum clock
- I^2C, QSPI, and CAN: future option
- Industrial Ethernet interface-compliant to IEEE 802.3, 10Base or 100Base transmit half and full duplex
- Single 3.3 V power supply, 840 mW
- Cycle time down to 1 ms (cycle times vary based on protocol, link type, and application data)
- 194-ball chip-scale package BGA form factor
- RoHS 3 compliant
- –40°C to +85°C industrial temperature range

APPLICATIONS

- Factory and process automation
- Motion control
- Building automation
- Transportation

GENERAL DESCRIPTION

The ADIN2299 is a complete, pretested solution that manages the industrial protocol and network traffic for an applications processor.

The module contains everything needed to participate in a EtherCAT, PROFINET® real-time (RT) and isochronous real time (IRT), EtherNet/IP network, including a communications controller, protocol stack, flash, RAM, follower controller, and physical layer (PHY). An applications processor connects via a universal asynchronous receiver transmitter (UART), serial peripheral interface (SPI), or Ethernet interface.

At the software layer, the applications processor connects to a unified interface so the supported industrial protocols can be used without changing the applications processor software. The ADIN2299 platform was precertified so that the field device can operate in any of the supported industrial Ethernet networks.

PRODUCT HIGHLIGHTS

1. Multiprotocol support
2. Small form factor for embedded applications
3. Low power and low latency
4. Robust network policing ensures passing PROFINET Netload Class 3

Rev. 0

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REVISION HISTORY

4/2022—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

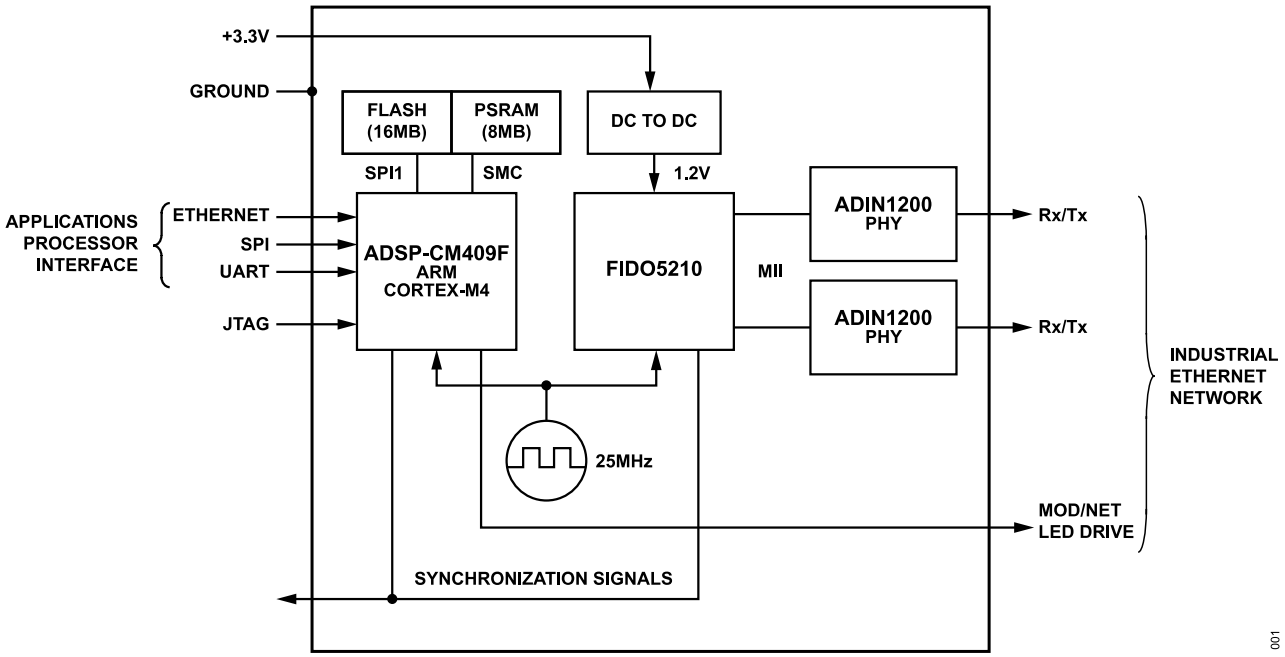

Figure 1.

SPECIFICATIONS

Supply voltage (V_{DD}) = 3.3 V ± 5%, GND = 0 V, all specifications at T_A = –40°C to +85°C, unless otherwise noted.

ELECTRICAL CHARACTERISTICS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER CONSUMPTION					
Supply Current 100Base-TX, Static		172		mA	At T_A = 25°C, idle
Power 100Base-TX, Static		568		mW	At T_A = 25°C, idle, not including light emitting diode (LED) sink and source current
Supply Current 100Base-TX, Full Activity[1]		225		mA	At T_A = 25°C, 100% data throughput, full activity
Power 100Base-TX, Full Activity[1]		743		mW	At T_A = 25°C, 100% data throughput, full activity, not including LED sink and source current
DIGITAL INPUTS AND OUTPUTS					
3.3 V Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)					
Input Voltage					
Low (V_{IL})			0.8	V	
High (V_{IH})	2.0			V	
Output Voltage					
Low (V_{OL})			0.4	V	Output low current (I_{OL}) = 2 mA minimum
High (V_{OH})	2.4			V	Output high current (I_{OH}) = 2 mA minimum
LED OUTPUTS					
Output Drive Current	4			mA	Sink current, applies to MOD_LED1, MOD_LED2, NET_LED1, and NET_LED2
	8			mA	Sink current, applies to $\overline{\text{P1\_ACTIVITY}}$, $\overline{\text{P2\_ACTIVITY}}$, $\overline{\text{P1\_LINK\_STATUS}}$, and $\overline{\text{P2\_LINK\_STATUS}}$

[1] Guaranteed by design and characterization.

PROTOCOL SPECIFIC CHARACTERISTICS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
BRIDGE DELAY					Switch and PHY latency included, from simulation
EtherCAT[1]		1		µs	
EtherNet/IP		3		µs	
PROFINET RT		2		µs	
ETHERCAT					
Cyclic Input and Output Data[2]			1440	Bytes	Up to 1440 bytes can be supported
Cycle Time		0.4		ms	8 bytes of output data and 6 bytes of input data used for this test, Ethernet applications processor interface
ETHERNET/IP					
Cyclic Input and Output Data[2]			504	Bytes	More cyclic input and output data up to 1440 bytes can be supported with multiple connections
Packet Interval	2			ms	
Beacon Interval	0.2		1000	ms	
Cycle Time		1		ms	64 bytes of cyclic output data and 64 bytes of cyclic input data used for this test, Ethernet applications processor interface
PROFINET RT					
Cyclic Input and Output Data[2]			1440	Bytes	

SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Cycle Time		1		ms	8 bytes of cyclic input and output data, Ethernet applications processor interface

[1] Guaranteed by design and characterization.

[2] Cycle times vary based on protocol, link type, and application data.

TIMING CHARACTERISTICS

10 Mbps and 100 Mbps Ethernet MAC Interface Timing

Table 3 through Table 5 and Figure 2 through Figure 4 describe the Ethernet MAC applications processor, interface controller, timing specifications. Note that the externally generated Ethernet MAC clock is $f_{REFCLKEXT}$, and the internal system clock is f_{SYSCLK}. To calculate the externally generated Ethernet MAC clock timing and the internal system clock timing, use the following equations:

$$t_{REFCLKEXT} = 1/f_{REFCLKEXT}$$

$$t_{SYSCLK} = 1/f_{SYSCLK}$$

Table 3. 10 Mbps and 100 Mbps Ethernet MAC Reduced Media Independent Interface (RMII) Receive Signal Timing

Parameter		Min	Max	Unit
$f_{REFCLKEXT}$	ETH0_REFCLK Frequency		50	MHz
t_{REFCLK}	ETH0_REFCLK Period[1]	$t_{REFCLKEXT}$ – 1%		ns
$t_{REFCLKW}$	ETH0_REFCLK Width[1]	$t_{REFCLKEXT}$ × 35%	$t_{REFCLKEXT}$ × 65%	ns
$t_{REFCLKIS}$	Receive Input Valid to RMII ETH0_REFCLK Rising Edge (Data In Setup)	4		ns
$t_{REFCLKIH}$	RMII ETH0_REFCLK Rising Edge to Receive Input Invalid (Data In Hold)	2.0		ns

[1] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty-cycle variation or jitter.

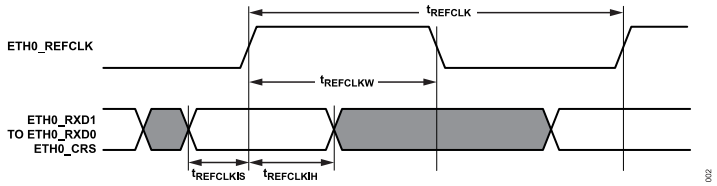

Figure 2. RMII Receive Timing

Table 4. 10 Mbps and 100 Mbps Ethernet MAC RMII Transmit Signal Timing

Parameter		Min	Max	Unit
$t_{REFCLKOV}$	RMII ETH0_REFCLK Rising Edge to Transmit Output Valid (Data Out Valid)		14	ns
$t_{REFCLKOH}$	RMII ETH0_REFCLK Rising Edge to Transmit Output Valid (Data Out Hold)	2		ns

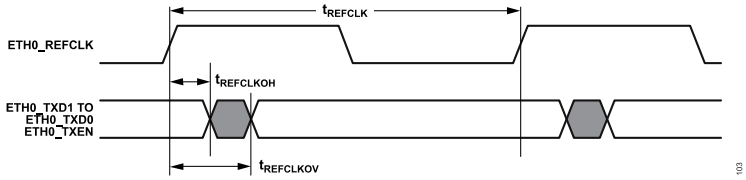

Figure 3. RMII Transmit Timing

SPECIFICATIONS

Table 5. 10 Mbps and 100 Mbps Ethernet MAC Management Interface Timing

Parameter		Min	Max	Unit
f_{SYSCLK}	Internal System Clock		100	MHz
t_{MDIOS}	ETH0_MDIO Input Valid to ETH0_MDC Rising Edge (Setup)	14		ns
t_{MDIOH}	ETH0_MDC Rising Edge to ETH0_MDIO Input Invalid (Hold)	0		ns
t_{MDCOV}	ETH0_MDC Falling Edge to ETH0_MDIO Output Valid		t_{SYSCLK} + 5	
t_{MDCOH}	ETH0_MDC Falling Edge to ETH0_MDIO Output Invalid (Hold)	t_{SYSCLK} – 5		ns

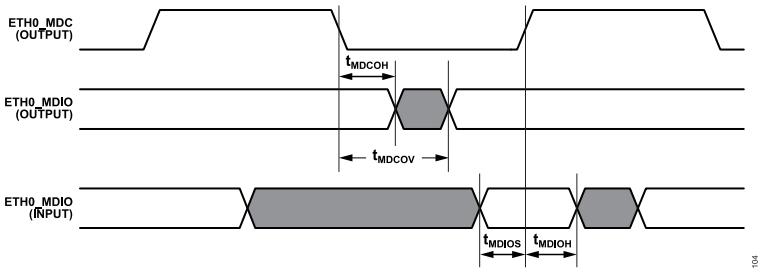

Figure 4. Ethernet 10 Mbps and 100 Mbps MAC Management Interface Timing

SPECIFICATIONS

SPI Follower Interface Timing

Table 6 and Figure 5 describe the SPI port follower timing specifications. Note that, in SPI follower mode, the SPI clock is supplied externally ($f_{SPICLKEXT}$). To calculate the timing for the external SPI clock, use the following equation:

$t_{SPICLKEXT} = 1/f_{SPICLKEXT}$

Table 6. SPI Port Follower Timing

Parameter		Min	Max	Unit
$f_{SPICLKEXT}$	SPI0_CLK Frequency		10	MHz
t_{SPICHS}	SPI0_CLK High Period	0.5 × $t_{SPICLKEXT}$ − 1		ns
t_{SPICLS}	SPI0_CLK Low Period	0.5 × $t_{SPICLKEXT}$−1		ns
t_{SPICLK}	SPI0_CLK Period	$t_{SPICLKEXT}$−1		ns
t_{HDS}	Last SPI0_CLK Edge to $\overline{\text{SPI0\_SEL3\_SS}}$ Not Asserted	5		ns
t_{SPITDS}	Sequential Transfer Delay	t_{SPICLK} − 1		ns
t_{SDSCI}	$\overline{\text{SPI0\_SEL3\_SS}}$ Assertion to First SPI_CLK Edge	10.5		ns
t_{SSPID}	Data Input Valid to SPI0_CLK Edge (Data Input Setup)	2		ns
t_{HSPID}	SPI0_CLK Sampling Edge to Data Input Invalid	1.6		ns
t_{DSOE}	$\overline{\text{SPI0\_SEL3\_SS}}$ Assertion to Data Out Active	0	14	ns
t_{DSDHI}	$\overline{\text{SPI0\_SEL3\_SS}}$ Deassertion to Data High Impedance	0	12.5	ns
t_{DDSPID}	SPI0_CLK Edge to Data Out Valid (Data Out Delay)		14	ns
t_{HDSPID}	SPI0_CLK Edge to Data Out Invalid (Data Out Hold)	0		ns

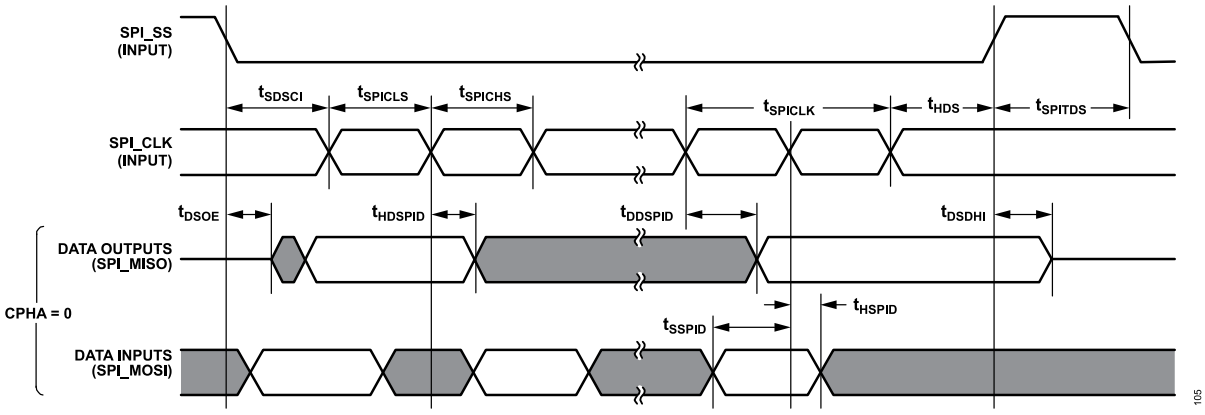

Figure 5. SPI Follower Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
VDD to GND	−0.3 V to +3.6 V
Power Dissipation	840 mW
Temperature	
T_A Range, Industrial	–40°C to +85°C
Storage Range	–65°C to +150°C
Junction (T_J Maximum)	125°C
Lead, Soldering	JEDEC industry-standard, J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the ADIN2299

Table 8. ADIN2299, 194-Ball CSP_BGA

ESD Model	Withstand Threshold (V)	Class
HBM	2500	2
FICDM	2000	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

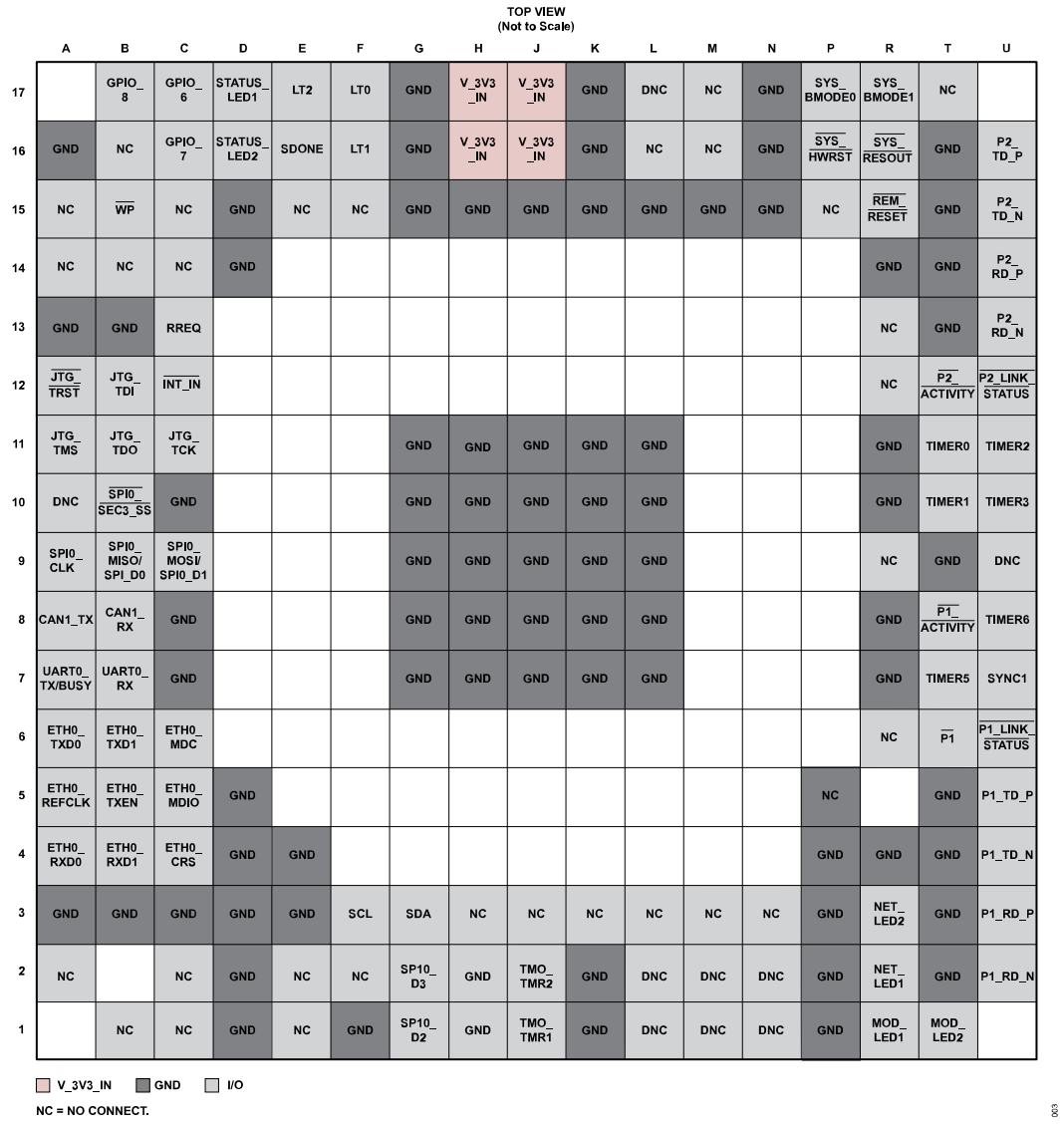

Figure 6. Ball Configuration

Table 9. Ball Function Descriptions

Ball No.	Mnemonic	Direction	Description
A2, A14, A15, B1, B14, B16, C1, C2, C14, C15, E1, E2, E15, F2, F15, H3, J3, K3, L3, L16, M3, M16, M17, N3, P5, P15, R6, R9, R12, R13, T17	NC	Not applicable	No Connect.
A3, A13, A16, B3, B13, C3, C7, C8, C10, D1, D2, D3, D4, D5, D14, D15, E3, E4, F1, G7, G8, G9, G10, G11, G15, G16, G17, H1, H2, H7, H8, H9, H10, H11, H15, J7, J8, J9, J10, J11, J15, K1, K2, K7, K8, K9, K10, K11, K15, K16, K17, L7, L8, L9, L10, L11, L15,	GND	Not applicable	Ground.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 9. Ball Function Descriptions

Ball No.	Mnemonic	Direction	Description
M15, N15, N16, N17, P1, P2, P3, P4, P15, R4, R7, R8, R10, R11, R14, T2, T3, T4, T5, T9, T13, T14, T15, T16			
A4	ETH0_RXD0	Input	Ethernet MAC 0 (EMAC0) Receive Data 0. Receive data bus.
A5	ETH0_REFCLK	Input	EMAC0 Reference Clock. Externally supplied Ethernet clock.
A6	ETH0_TXD0	Output	EMAC0 Transmit Data 0. Transmit data bus.
A7	UART0_TX/BUSY	Output	UART0 Transmit Output When UART Selected as the Applications Processor Interface (UART0_TX). Busy Signal When SPI Selected (BUSY). This signal indicates to the application side that the communication side is busy. Connect a 3 kΩ pull-down resistor to the BUSY pin.
A8	CAN1_TX	Output	This ball can be left floating. It is reserved for the following future option: CAN Applications Processor Interface Transmit (CAN1_TX).
A9	SPI0_CLK	Input	SPI0 Clock Input.
A10	DNC	Not applicable	Do Not Connect. The DNC pin is internally connected and must remain floating.
A11	JTG_TMS	Input	JTAG Mode Select. JTAG test access port mode select.
A12	$\overline{\text{JTG\_TRST}}$	Input	JTAG Reset. JTAG test access port reset.
B4	ETH0_RXD1	Input	EMAC0 Receive Data 1. Receive data bus.
B5	ETH0_TXEN	Output	EMAC0 Transmit Enable. When asserted, this ball indicates that the transmit data is valid.
B6	ETH0_TXD1	Output	EMAC0 Transmit Data 1. Transmit data bus.
B7	UART0_RX	Input	UART0 Receive. Receive input.
B8	CAN1_RX	Input	This ball can be left floating. It is reserved for the following future option: CAN Applications Processor Interface Receive (CAN1_RX).
B9	SPI0_MISO/SPI_D0	Input and output	SPI0 Leader In, Follower Out (SPI0_MISO). When QSPI™ is selected, this ball has the SPI0_D0 function, which is the Data 0 line for the QSPI.
B10	$\overline{\text{SPI0\_SEL3\_SS}}$	Input	SPI0 Follower Select Input.
B11	JTG_TDO	Output	JTAG Serial Data Out. JTAG test access port data output.
B12	JTG_TDI	Input	JTAG Serial Data In. JTAG test access port data input.
B15	$\overline{\text{WP}}$	Input	Write Protect SPI Flash. The $\overline{\text{WP}}$ ball is pulled high internally to the module, and it is recommended to leave this pin floating.
B17	GPIO_8	Output	General-Purpose Input and Output 8. Connect a 10 kΩ pull-up resistor to the GPIO_8 ball.
C4	ETH0_CRS	Input	EMAC0 Carrier Sense. Multiplexed on alternate clock cycles. Carrier Sense (CRS): Asserted by the PHY when either the transmit or receive medium is not idle. Deasserted when both are idle. Receive Divider (RXDV): Asserted by the PHY when the data on Receive Data Line 1 (RXD0) is valid.
C5	ETH0_MDIO	Input and output	EMAC0 Management Channel Serial Data. Bidirectional data bus for PHY control.
C6	ETH0_MDC	Output	EMAC0 Management Channel Clock. Clocks the MDC input of the PHY.
C9	SPI0_MOSI/SPI0_D1	Input and output	SPI0 Leader Out, Follower In (SPI0_MOSI). When QSPI is selected, this ball has the SPI0_D1 function, which is the Data 1 line for the QSPI.
C11	JTG_TCK	Input	JTAG Clock. JTAG test access port clock.
C12	$\overline{\text{INT\_IN}}$	Input	Interrupt Input to Applications Processor. Connect a 4.7 kΩ pull-up resistor to the $\overline{\text{INT\_IN}}$ ball.
C13	RREQ	Output	Interrupt Output to Applications Processor. Signal goes high to notify the application side that a message is ready to be read. Connect a 3 kΩ pull-down resistor to the RREQ ball.
C16	GPIO_7	Output	General-Purpose Input and Output 7.
C17	GPIO_6	Input and output	General-Purpose Input and Output 6.
D16	STATUS_LED2	Input and output	The STATUS_LED2 ball goes low to activate the red LED of the optional dual-color STATUS signal LED.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 9. Ball Function Descriptions

Ball No.	Mnemonic	Direction	Description
D17	STATUS_LED1	Output	The STATUS_LED1 ball goes low to activate the green LED of the optional dual-color STATUS signal LED.
E16	SDONE	Output	Communication Start Up Done. Connect a 4.7 kΩ pull-down resistor to the SDONE ball.
E17	LT2	Input and output	Applications Processor Interface Selection: Link Type 2 (see Table 11).
F3	SCL	Input and output	I^2C Serial Clock. Clock output when leader and clock input when follower. Compatible with I^2C bus standard. Requires external pull-up.
F16	LT1	Input and output	Applications Processor Interface Selection: Link Type 1 (see Table 11).
F17	LT0	Input and output	Applications processor interface Selection: Link Type 0 (see Table 11).
G1	SPI0_D2	Input and output	When QSPI is selected, this ball has SPI0_D2 function, which is the Data 2 line for the QSPI.
G2	SPI0_D3	Input and output	When QSPI is selected, this ball has SPI0_D3 function, which is the Data 3 line for the QSPI.
G3	SDA	Input and output	I^2C Serial Data. Receives or transmits data. Compatible with I^2C bus standard. Requires external pull-up.
H16, H17, J16, J17	V_3V3_IN	Not applicable	3.3 V Power Supply.
J1	TMO_TMR1	Input and output	General-Purpose Timer Input and Output.
J2	TMO_TMR2	Input and output	General-Purpose Timer Input and Output.
L1, L2, L17, M1, M2, N1, N2, U9	DNC	Not applicable	Do Not Connect. This ball is internally connected and must remain floating.
P16	$\overline{\text{SYS\_HWRST}}$	Input	Processor Hardware Reset Control. Resets the device when asserted. Connect a 10 kΩ pull-up resistor to this ball.
P17	SYS_BMODE0	Input	Boot Mode Control 0. The SYS_BMODE0 ball is pulled high internally to the module.
R1	MOD_LED1	Output	The MOD_LED1 ball goes low to activate the green LED of the dual-color LED1.
R2	NET_LED1	Output	The NET_LED1 ball goes low to activate the green LED of the dual-color LED2.
R3	NET_LED2	Output	The NET_LED2 ball goes low to activate the red LED of the dual-color LED2.
R15	$\overline{\text{REM\_RESET}}$	Output	Reset Output from the fido5200 on the module.
R16	$\overline{\text{SYS\_RESOUT}}$	Output	Processor Reset Output. Indicates that the device is in the reset state. Connect a 1 kΩ pull-down resistor to this ball.
R17	SYS_BMODE1	Input	Boot Mode Control 1. The SYS_BMODE1 ball is pulled low internally to the module.
T1	MOD_LED2	Output	The MOD_LED2 ball goes low to activate the red LED of the dual-color LED1.
T6	$\overline{\text{P1\_ACTIVITY}}$	Output	Port 1 Activity LED Output Driver.
T7	TIMER5	Output	Internal Precision Timer 5 Synchronization Output.
T8	SYNC2	Output	REM Switch Synchronization Signal. This signal can be connected to the applications processor for use in isochronous control applications.
T10	TIMER1	Input and output	Internal Precision Timer 1 Synchronization Signal.
T11	TIMER0	Input and output	Internal Precision Timer 0 Synchronization Signal.
T12	$\overline{\text{P2\_ACTIVITY}}$	Output	Port 2 Activity LED Output Driver.
U2	P1_RD_N	Input and output	Physical Receive or Transmit Signal (Negative Differential) for Port 1.
U3	P1_RD_P	Input and output	Physical Receive or Transmit Signal (Positive Differential) for Port 1.
U4	P1_TD_N	Input and output	Physical Transmit or Receive Signal (Negative Differential) for Port 2.
U5	P1_TD_P	Input and output	Physical Transmit or Receive Signal (Positive Differential) for Port 2.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 9. Ball Function Descriptions

Ball No.	Mnemonic	Direction	Description
U6	$\overline{\text{P1\_LINK\_STATUS}}$	Input	Port 1 Link Status from PHY.
U7	SYNC1	Output	REM Switch Synchronization Signal. This signal can be connected to the applications processor for use in isochronous control applications.
U8	TIMER6	Output	Internal Precision Timer 6 Synchronization Output.
U10	TIMER3	Input and output	Internal Precision Timer 3 Synchronization Signal.
U11	TIMER2	Input and output	Internal Precision Timer 2 Synchronization Signal.
U12	$\overline{\text{P2\_LINK\_STATUS}}$	Output	Port 2 Link Status from PHY.
U13	P2_RD_N	Input and output	Physical Receive or Transmit Signal (Negative Differential) for Port 2.
U14	P2_RD_P	Input and output	Physical Receive or Transmit Signal (Positive Differential) for Port 2.
U15	P2_TD_N	Input and output	Physical Transmit or Receive Signal (Negative Differential) for Port 2.
U16	P2_TD_P	Input and output	Physical Transmit or Receive Signal (Positive Differential) for Port 2.

THEORY OF OPERATION

The main use case for the ADIN2299 is to provide multiprotocol, industrial Ethernet connectivity to field devices that require the robust, deterministic Ethernet capability supported by mainstream industrial protocols.

Figure 7 shows the ADIN2299 system block diagram. The communications controller is the ADSP-CM409F within the module, while the application processor is the applications processor. The applications processor communicates with the communications controller on the ADIN2299 module via the Unified Interface common language. The timing for the interfaces of the applications processor of the ADIN2299 module are detailed in the Timing Characteristics section. The Unified Interface is described in the Unified Interface Control Document User Guide.

As shown in the typical application circuit shown in Figure 16, the user is responsible for connecting the following to the ADIN2299 module:

- 3.3 V power and ground for the ADIN2299 module.
- An industrial Ethernet connection: magnetics and RJ-45 connections to the industrial network from the PHY outputs.
- An applications processor interface: via SPI, UART, or Ethernet.
- Industrial Ethernet LEDs (module (MOD) and network (NET)).

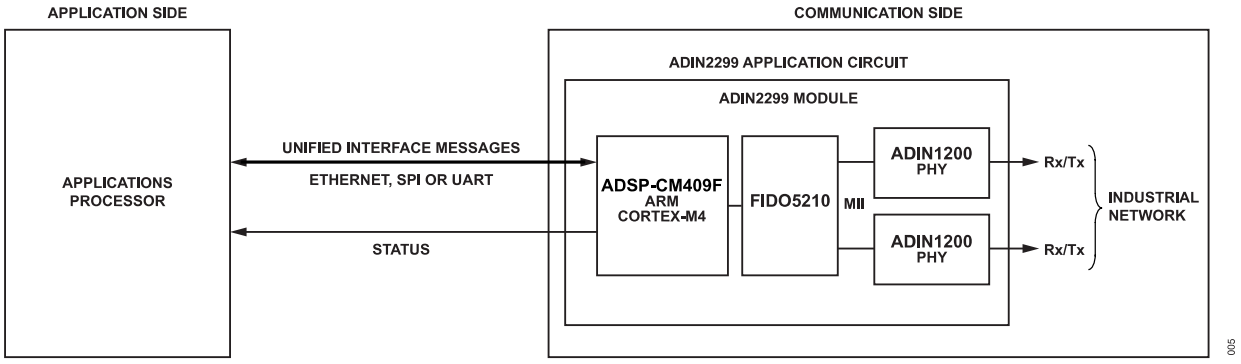

Figure 7. System Block Diagram

THEORY OF OPERATION

INDUSTRIAL ETHERNET CONNECTION

The ADIN2299 application circuit shown in Figure 16 includes magnetics and a connector with link status and activity LEDs for each Ethernet port.

The ADIN2299 module provides two PHYs to connect to the industrial Ethernet network.

See Table 10 for the ADIN2299 connections to the RJ-45 and Ethernet connectors on the user board as also shown in Figure 16.

Table 10. ADIN2299 Connections to the RJ-45 and Ethernet Connectors

Ball No.	Mnemonic
U2	P1_RD_N
U3	P1_RD_P
U4	P1_TD_N
U5	P1_TD_P
U13	P2_RD_N
U14	P2_RD_P
U15	P2_TD_N
U16	P2_TD_P

APPLICATIONS PROCESSOR INTERFACE

The applications processor interface is selected via the LT0 to LT2 balls as shown in Table 11. Keep LT2, LT1, and LT0 at ground when the communication interface is selected by the board configuration file. An option is available to override the pin configuration via the Link Configuration File. See the RPG2 Hardware Design Integration Guide for more details on the Link Configuration File.

For the communication protocol and information regarding how to interface the application processor to the ADSP-CM409F on the ADIN2299, see the RPG2 Unified Interface User Guide.

Table 11. Unified Interface Link Type Selection

LT2	LT1	LT0	Unified Interface Link Type
0	0	0	Ethernet
0	0	1	Reserved
0	1	0	SPI
0	1	1	Reserved
1	0	0	UART0
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

UART Applications Processor Interface

If the UART interface is selected, connect the applications processor interface to the ADIN2299 module as shown in Figure 8 using the balls indicated in Table 12. The UART is configured for 115,200 bps to 1,000,000 bps with 8 data bits, no parity, one start bit, and one stop bit.

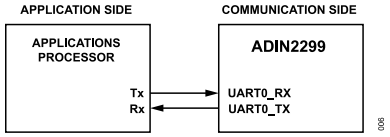

Figure 8. UART Applications Processor Interface

Table 12. UART Applications Processor Interface Balls

Mnemonic	Direction	Description
UART0_TX	Output	UART0 transmit output
UART0_RX	Input	UART0 receive input

SPI Applications Processor Interface

If the SPI is selected, connect the applications processor interface to the ADIN2299 module as shown in Figure 12 using the balls indicated in Table 14. The SPI follower connection supports a 10 MHz maximum clock rate with the clock phase bit (CPHA) = 0, so that data is captured on the leading edge, and the clock polarity bit (CPOL) = 0 with the leading clock edge rising, and this timing is described in the SPI Follower Interface Timing section. The Unified Interface protocol is described in the Unified Interface Control Document User Guide.

It is critical when a user is using the SPI that the user understands the following regarding the BUSY and RREQ signals:

- For the BUSY signal, the following is applicable:
  - A falling edge on BUSY indicates that transaction processing is complete, and that the SPI follower is ready for the next transaction.
  - Figure 11 shows the multitransaction read operation sequence in detail.
  - BUSY is only used to pace the rate at which SPI transactions occur. BUSY is not raised or lowered for other purposes.
  - BUSY always goes inactive after a SPI transaction, and there are no cases in which BUSY goes high and stays high.
  - If a SPI transaction initiates while BUSY is high, undefined behavior may result.
  - Due to underlying hardware and software constraints and considerations, some jitter on BUSY is expected.
  - BUSY becomes active (high) no sooner than 1.14 µs after $\overline{\text{SPI0\_SEL3\_SS}}$ goes inactive (high). BUSY stays active (high) for at least 3.3 µs.
- For the RREQ signal, the following is applicable:
  - A rising edge of this signal requires the SPI leader to acknowledge the read request with a short SPI transaction before the data can be read. After the read request is acknowledged, the SPI follower drops RREQ to indicate that the data is ready to be read.
  - The general recommendation is to configure the SPI leader to interrupt on a rising edge of this signal. However, RREQ can also be polled, if using interrupts is not possible or desired.

THEORY OF OPERATION

- RREQ is only related to read operations. RREQ is not related to write operations in any form. RREQ may go active (high) anytime, including during a write operation.

See Figure 9 for a sample SPI transaction.

For the busy signal, there are some values that can be expected regarding the timing of these signals (see Table 13).

The data detailed in Table 13 was gathered empirically and other factors, such as the application processor code and environment, can influence these numbers.

An example of a write transaction and a read transaction with actual data is shown in Figure 10 and Figure 11, respectively. The transaction is an NI_Discover message with the UI_EchoReq and UI_EchoRes message, which is detailed in the code for the ni-api-srv found in the NI-Example-App workspace in the Developer Portal.

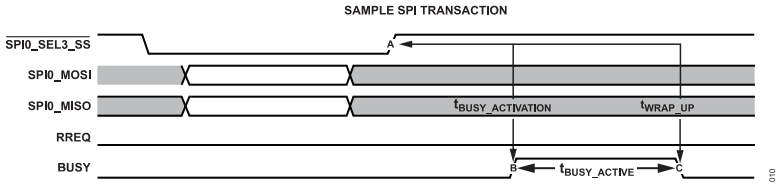

Figure 9. Sample SPI Transaction

Table 13. SPI Timing Requirements

Parameter	Minimum (µs)	Maximum (µs)
BUSY Activation Time, $t_{BUSY\_ACTIVATION}$	1.14	27.04
BUSY Active Time, t_{BUSY_ACTIVE}	3.34	33.04
Wrap-Up Time, t_{WRAP_UP}	4.48	36.16

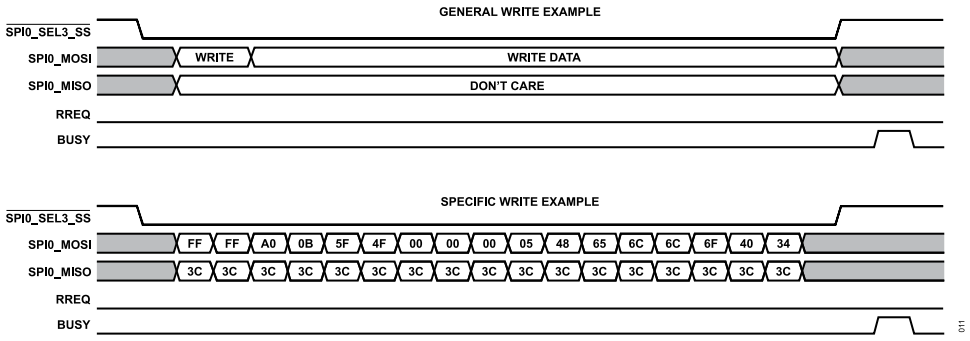

Figure 10. General and Specific SPI Write Example

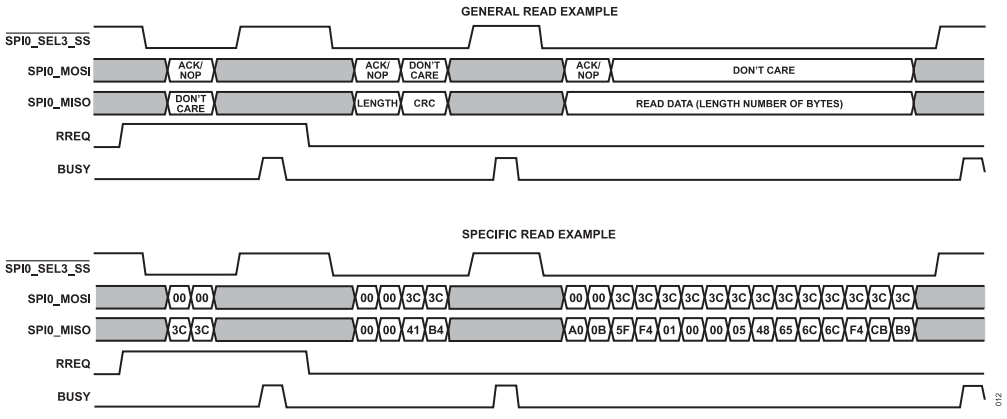

Figure 11. General and Specific SPI Read Example

THEORY OF OPERATION

There is also an error recovery mechanism in the SPI. In the event the SPI leader detects something wrong with the SPI link, it may flush the link to reset low level SPI communication. A flush is initiated by issuing a SPI transaction the length of 0 byte or 1 byte. If a transaction with a length of 1 is issued, the byte value placed on MOSI is ignored by the SPI follower. Similarly, the value on MISO can be ignored. If a flush is initiated between any two read or write operations, nothing notable happens. If a flush is initiated during a read operation, the following notable actions are taken.

If the RREQ signal is high and no read request acknowledge transaction has been sent, the following occurs:

- RREQ goes low.
- A flush at this point concludes the read operation, and the SPI leader must not attempt to retrieve the data status header or message data.
- The data status header and message data that the SPI follower prepared for transmission is discarded.
- The SPI follower does not attempt to retransmit flushed messages.
- SPI transactions can operate normally from this point.

If the RREQ signal is high and a read request acknowledge transaction has been sent, the following occurs:

- RREQ goes low.
- A flush at this point concludes the read operation, and the SPI leader must not attempt to retrieve the data status header or message data.
- The data status header and message data that the SPI follower prepared for transmission is discarded.
- The SPI follower does not attempt to retransmit flushed messages.
- SPI transactions can operate normally from this point.

If RREQ is inactive, the following occurs:

- The data status header and message data that the SPI follower prepared for transmission is discarded.
- The SPI follower does not attempt to retransmit flushed messages.
- SPI transactions can operate normally from this point.

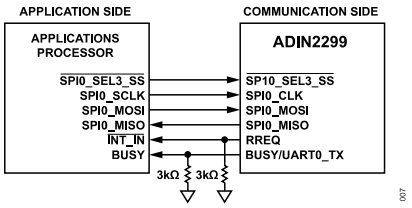

Figure 12. SPI Applications Processor Interface

Table 14. SPI Applications Processor Interface Balls

Mnemonic	Direction	Description
SPI0_SEL3_SS	Input	SPI0 Follower Select Input.
SPI0_CLK	Input	SPI0 Clock Input.
SPI0_MOSI	Input	SPI0 Leader Out, Follower In.
SPI0_MISO	Output	SPI0 Leader In, Follower Out.
RREQ	Output	RREQ is a signal that notifies the application side that a message is ready to be read.
BUSY	Output	Busy Signal. This signal indicates to the application side that the communication side is busy.

Ethernet Applications Processor Interface Selection

Figure 13 shows the Ethernet applications processor interface direct connection through the RMII.

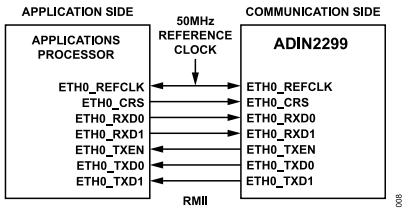

Figure 13. Direct Connection Through RMII

Figure 14 shows the Ethernet applications processor interface indirect connection.

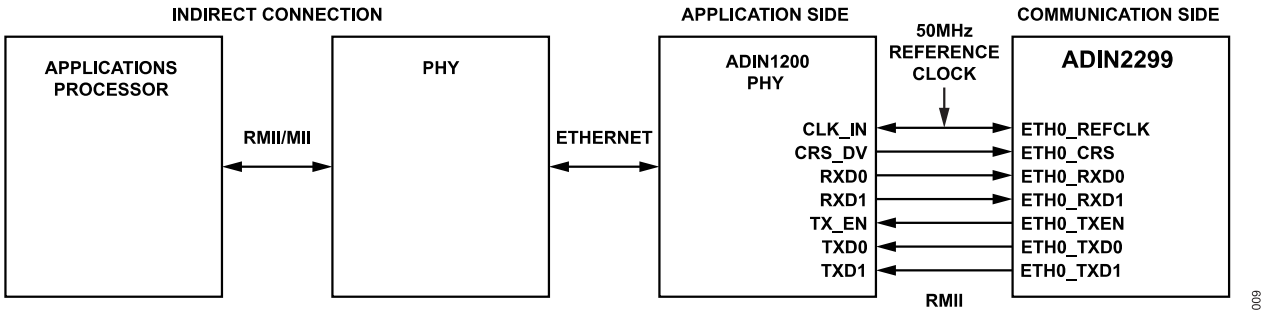

Figure 14. Indirect Connection

THEORY OF OPERATION

Table 15. Ethernet Applications Interface Signals

Mnemonic	Direction	Description
ETH0_REFCLK	Input	EMAC0 Reference Clock. Externally supplied Ethernet clock.
ETH0_CRS	Input	EMAC0 Carrier Sense. Multiplexed on alternate clock cycles.
	Input	CRS: asserted by the PHY when either the transmit or receive medium is not idle. Deasserted when both are idle.
	Input	RXDV: asserted by the PHY when the data on RXD0 is valid.
ETH0_RXD0	Input	EMAC0 Receive Data 0. Receive data bus.
ETH0_RXD1	Input	EMAC0 Receive Data 1. Receive data bus.
ETH0_TXEN	Input and output	EMAC0 Transmit Enable. When asserted, ETH0_TXEN indicates that the data on TXD0 is valid.
ETH0_TXD0	Output	EMAC0 Transmit Data 0. Transmit data bus.
ETH0_TXD1	Output	EMAC0 Transmit Data 1. Transmit data bus.

THEORY OF OPERATION

INDUSTRIAL ETHERNET MOD AND NET LEDS

LED behavior is specified by each protocol. The functionality of the MOD and NET LEDs, shown as LED1 and LED2 in Table 16 vary depending on the industrial Ethernet protocol selected. This functionality is described in the RPG2 Hardware Design Integration Guide.

PROGRAMMING

The secure methods of updating the module are through the following:

- The industrial Ethernet ports via a webserver interface described in the RPG2 Web Server User Guide.
- A JTAG connection, which is described further in the RPG2 Programming Guide.

If the ADIN2299 schematic is implemented directly on the customer board as a reference design instead of purchasing a module, the only option for programming is through a JTAG connection using the Segger toolchain. Note that a serial wire debug connection is not supported. See the RPG2 Programming Guide for more information.

APPLICATION CIRCUIT SUPPORT CIRCUITRY

Table 16 lists the required external components in the ADIN2299 application circuit, as shown in Figure 16.

Table 16. External Components

		Recommended Component		
Component	**Value**	**Manufacturer**	**Manufacturer Part Number[1]**	**Notes/Comments**
Capacitors				
Decoupling for 3.3 V	47 µF	User specified	User specified	It is recommended to decouple each voltage rail with 47 µF, 0.1 µF, and 4.7 µF capacitors. These are at a 20% tolerance.
	0.1 µF	User specified	User specified	
	4.7 µF	User specified	User specified	
LEDs				
LED1 and LED2		Kingbright	KPBA-3010ESGC	Dual color, green and red.
Transient Voltage Suppressor (TVS) Diodes		Littelfuse	SP0504SHTG	Each device incorporates multiple 5.5 V clamping, 8.5 V reverse standoff diodes to provide electrostatic discharge (ESD) protection. One TVS device is required per Ethernet port, and two are required per ADIN2299 application circuit.
Resistors				
	470 Ω			LED current limit.
Other Components				
Ferrite Bead		Murata	BLM15EG121SN1D	1.5 A, 120 Ω at 100 MHz.
MagJack		Wurth	7499010121A	RJ-45 connector with integrated magnetics and LEDs.
Reset Supervisor		Analog Devices	AMD708SARZ	2.9 V power monitoring reset supervisor chip.

[1] Use the recommended components or ones that are similar.

THEORY OF OPERATION

REFLOW PROFILE

When soldering the ADIN2299 module to a PCB, there are specifics regarding the reflow temperature profile that must be followed to ensure that the module is correctly soldered onto the PCB (see Figure 15 and Table 17).

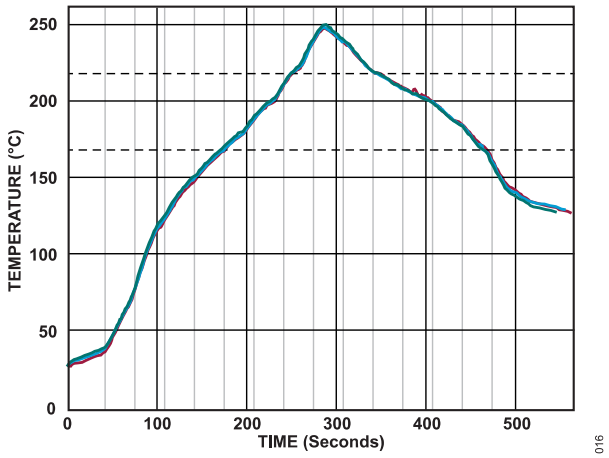

Figure 15. High Peak Reflow Temperature Profile (SMT Process)

Table 17. High Peak Reflow Temperature Profile Specifications

Item	Temperature Change	Profile Data(seconds)
Ramp Rate (°C/sec)	30°C to approximately 150°C	0.86
Soak Time (sec) at 170°C to Approximately 220°C	70°C to approximately 100°C	77.07
Dwell Time (sec) at More Than 220°C	60°C to approximately 90°C	84.82
Peak Temperature (°C)	245°C to approximately 255°C	247.69
Cooling Rate (°C/sec)	Peak to approximately 150°C	0.50

TYPICAL APPLICATION CIRCUIT

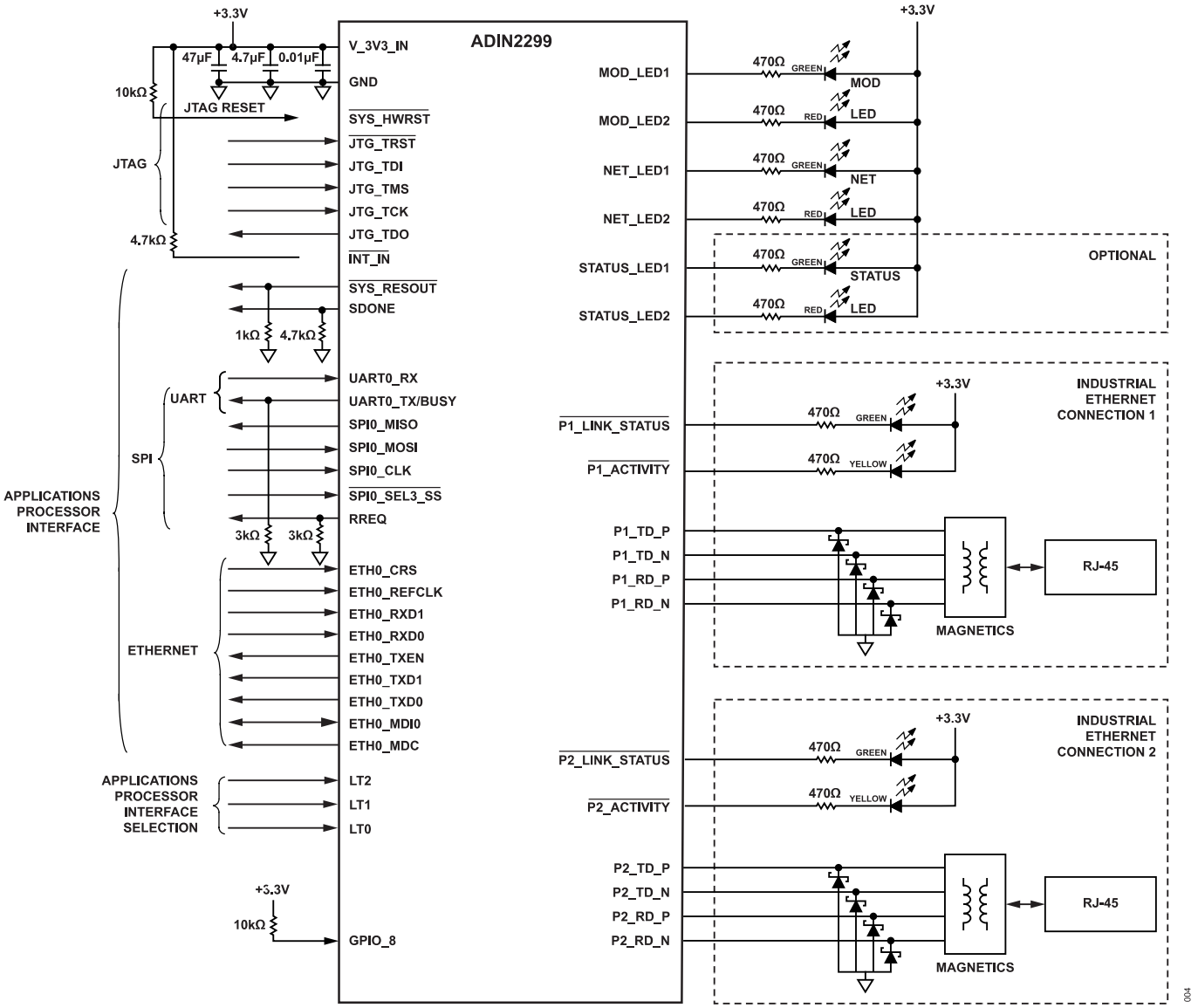

Figure 16.

OUTLINE DIMENSIONS

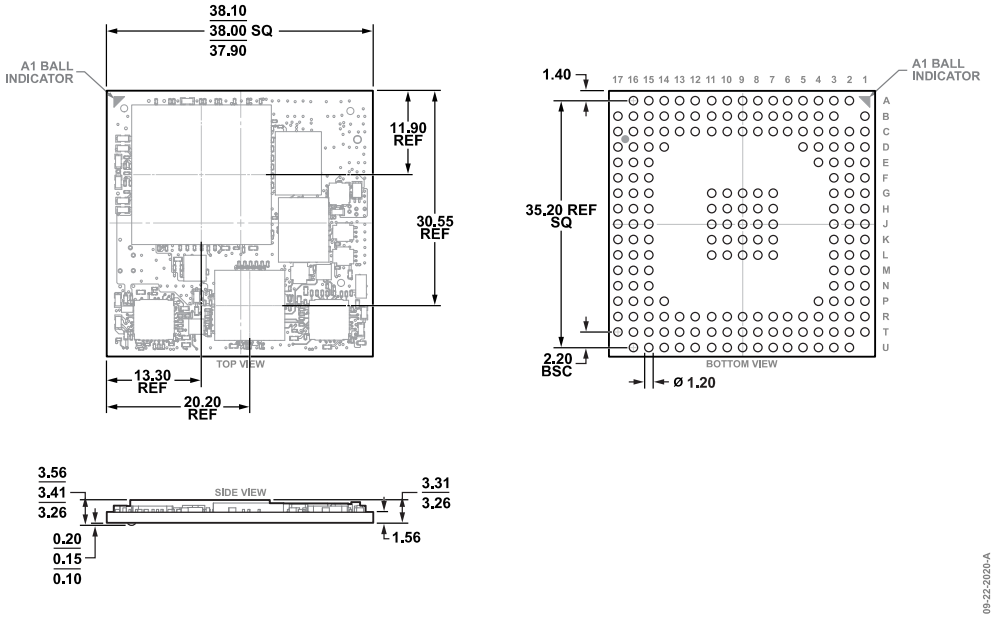

Figure 17. 194-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-194-1)
Dimensions Shown in Millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADIN2299BBCZ	–40°C to +85°C	194-Ball Chip-Scale Package, Ball Grid Array [CSP_BGA]	BC-194-1
ADIN2299BBCZ-RL	–40°C to +85°C	194-Ball Chip-Scale Package, Ball Grid Array [CSP_BGA]	BC-194-1

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Package Description
EV-RPG2-ENZ	Evaluation Board for EtherNet/IP
EV-RPG2-ECZ	Evaluation Board for EtherCAT
EV-RPG2-PNZ	Evaluation Board for PROFINET

[1] Z = RoHS Compliant Part.

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