Real-Time Ethernet Multiprotocol (REM) Switch

Data Sheet

fido5100/fido5200

FEATURES

144-lead CSP_BGA RoHS compliant package
−40°C to +105°C industrial temperature range rating
3.3 V input/output buffers
IEEE 802.3, 10 Mbps/100 Mbps, half and full duplex, IPv6 and IPv4 communication
2 independent Ethernet ports: 1 MII and 1 RMII interface per port
Support for all industrial protocols
    PROFINET Class B and Class C with fast startup (Version 2.3)
    EtherNet/IP with QuickConnect, CIP Sync, and CIP Motion
    Modbus TCP
    EtherCAT
    Ethernet POWERLINK
Host interface transfer rate: 32 bits per 28 ns
    Supports EtherCAT cycle times down to 12.5 μs and PROFINET cycle times down to 31.25 μs
PI Net Load Class III capable
DLR (supervisor and node, announce and beacon based), MRPD, HSR, PRP, shared device, controller redundancy
IEEE 1588 Version 2 support: ordinary clock; both peer to peer and end to end transparent clocks, raw frames, and UDP
8 independent timer signals synchronized with an internal precision timer
    4 independently programmable timer signals for timer capture events or timer output events
    4 timer signals create programmable periodic waveforms synchronized to the internal precision timer
    DCP, LLDP, DHCP, RSTP, VLAN, IGMP snooping support
    Forwarding table with aging and learning
   **Drive LEDs for link activity**

APPLICATIONS

Industrial automation
    Process control
    Managed Ethernet switch

FUNCTIONAL BLOCK DIAGRAM
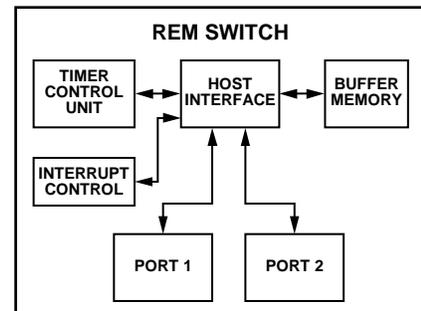
Figure 1.

GENERAL DESCRIPTION

The fido5100 and fido5200 (REM switch) are programmable IEEE 802.3 10 Mbps/100 Mbps Ethernet Internet Protocol Version 6 (IPv6) and Internet Protocol Version 4 (IPv4) switches that support virtually any Layer 2 or Layer 3 protocol. The switches are personalized to support the desired protocol by firmware that is downloaded from a host processor.

The firmware is contained in the real-time Ethernet multiprotocol (REM) switch driver and is downloaded at power-up. The REM switch can be ready for network data operation in less than 4 ms to support fast startup and quick connect type network functionality. The REM switch devices have the same signal assignments as defined in this data sheet.

The fido5100 supports the following protocols: PROFINET real time (RT) and isochronous real time (IRT), EtherNet/IP with and without device level ring (DLR), Modbus TCP, and POWERLINK.

The fido5200 supports the following protocols: EtherCAT and all protocols defined for the fido5100.

The REM switch is intended for use with a host processor. Network operation is handled using the functions and services provided in the REM switch driver. The host processor can implement any protocol stack by integrating it with the REM switch driver. An example application is shown in Figure 11.

The REM switches are available in a 144-ball chip scale package ball grid array (CSP_BGA) package.

Note that throughout this data sheet, multifunction pins, such as A02/ALE, are referred to either by the entire pin name or by a single function of the pin, for example, ALE, when only that function is relevant.

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REVISION HISTORY

SPECIFICATIONS
REM SWITCH CHARACTERISTICS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OPERATING CONDITIONS					
Core Voltage	1.08	1.2	1.32	V	
Core Current			48	mA	At T_A = 85°C
Input/Output (I/O) Buffers	2.97	3.3	3.63	V	3.3 V power supply
I/O Current			0.035	mA	At T_A = 85°C
PLL Analog Voltage Regulator Power Supply	1.08	1.2	1.32	V	
DC Input Voltage	−0.5		+3.8	V	
Output Voltage	−0.5		+3.8	V	
Operating Junction Temperature (Industrial)	−40		+125	°C	
DC CHARACTERISTICS (I/O STANDARD)					
3.3 V LVCMOS					
VCC+3V3	2.97	3.3	3.63	V	Voltage level applied to the VCC+3V3 signal
Input Voltage					
Low (V_{IL})	−0.3		+0.8	V	
High (V_{IH})	2.0		3.6	V	
Output Voltage					
Low (V_{OL})			0.4	V	
High (V_{OH})	2.4			V	
Output Current					
Low (I_{OL})	8.2	13.0	16.1	mA	
High (I_{OH})	9.2	19.2	30.7	mA	
LEAKAGE CURRENT					
Input Pin	−10		+10	µA	Input voltage (V_{IN}) = 0 V to 3.3 V maximum
Tristated I/O Pin	−10		+10	µA	Output voltage (V_{OUT}) = 0 V to 3.3 V maximum
HOST INTERFACE TRANSFER RATE[1]		32		Bits	Per 28 ns

[1] Supports EtherCAT cycle times down to 12.5 µs and PROFINET cycle times down to 31.25 µs.

TIMING SPECIFICATIONS—NONMULTIPLEXED ADDRESS DATA BUS

Table 2. Nonmultiplexed Address Data Bus—Read and Write Cycle Timing[1, 2, 3]

Parameter	Min	Typ	Max	Unit	Description
t_{AS}	2			ps	Address setup time
t_{AH}	370			ps	Address hold time
t_{CDV}			20	ns	$\overline{CS}$ to data valid time
t_{ODV}			20	ns	Output enable to data valid time
t_{OEL}	20			ns	Output enable low time
t_{CSH}	8			ns	$\overline{CS}$ high time
t_{CSL}	20			ns	$\overline{CS}$ low time
t_{EOE}	0			ns	$\overline{CS}$ to output enable time
t_{COE}	0			ns	Output enable high to $\overline{CS}$ high
t_{DO}	150			ps	Output enable to data drive time
t_{DHZ}			110	ps	Output disable to high-Z time
t_{CHZ}			110	ps	$\overline{CS}$ high to high-Z time
t_{WES}	0			ns	$\overline{CS}$ to write enable
t_{WEWC}	16			ns	Write enable to write complete
t_{WECS}	0			ns	Write enable high to $\overline{CS}$ high
t_{DS}	30			ps	Data setup to $\overline{WE}$ high
t_{DH}	30			ps	Input data hold after $\overline{WE}$ high

[1] The MBS pin determines whether the host interfaced has multiplexed or separate address and data lines. When MBS = 0, the interface is nonmultiplexed.

[2] $\overline{OE}$ can be taken low before $\overline{CS}$. Therefore, t_{EOE} can be a negative value. In this case, a board designer must closely monitor t_{DO} and t_{CDV} to avoid bus contention and ensure proper data transfer.

[3] The read bus cycle terminates when either $\overline{CS}$ or $\overline{OE}$ is taken high. Therefore, a negative value for t_{COE} is acceptable in some circumstances.

Timing Diagrams, Nonmultiplexed REM Switch
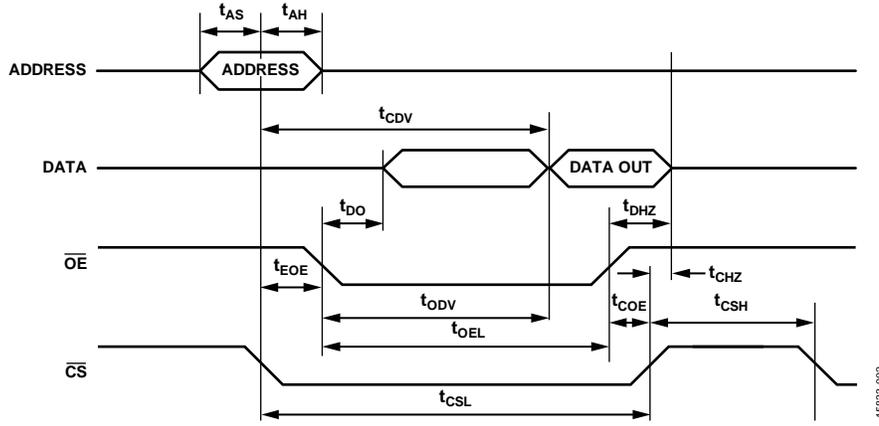
Figure 2. REM Switch Nonmultiplexed Address and Data Bus Read Timing, MBS = 0
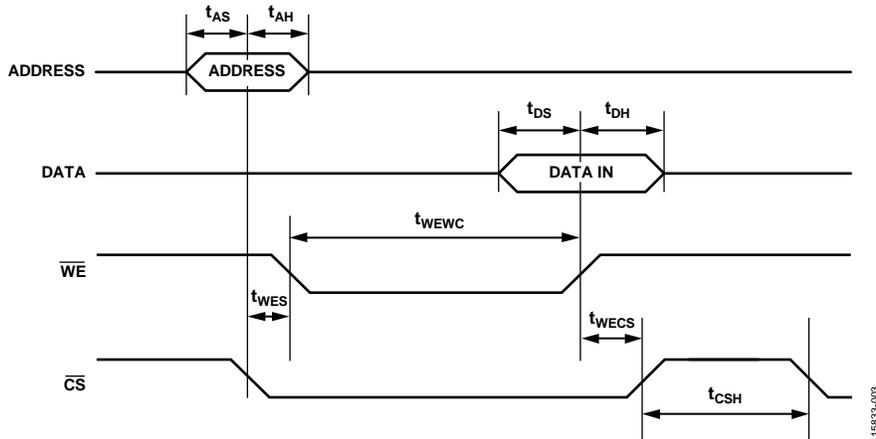
Figure 3. REM Switch Nonmultiplexed Address and Data Bus Write Timing, MBS = 0

TIMING SPECIFICATIONS—MULTIPLEXED ADDRESS DATA BUS

Table 3. Multiplexed Address Data Bus—Read and Write Cycle Timing[1]

Parameter	Min	Typ	Max	Unit	Description
t_{ALEH}	8			ns	ALE high time
t_{ALEL}	16			ns	ALE low time
t_{AS}	170			ps	Address setup time
t_{AH}	170			ps	Address hold time
t_{CDV}			20	ns	ALE to valid data
t_{ALOE}	2			ns	ALE to output enable
t_{ODV}			20	ns	Output enable to data valid
t_{DHZ}			150	ps	Output disable to high-Z time
t_{CHZ}			150	ps	$\overline{CS}$ high to high-Z time
t_{CLLL}	0			ns	$\overline{CS}$ low to ALE low
t_{CSH}	8			ns	$\overline{CS}$ high time
t_{EOE}	2			ns	$\overline{CS}$ to output enable
t_{DO}	2		110	ps	Output enable to output drive time
t_{COE}	0			ns	Output disable to $\overline{CS}$ high
t_{WES}	0			ns	$\overline{CS}$ to write enable
t_{WEWC}	16			ns	Write enable to write complete
t_{WECS}	0			ns	Write enable high to $\overline{CS}$ high
t_{WHLH}	0			ns	$\overline{WE}$ high to next ALE high
t_{DS}	60			ps	Data setup to $\overline{WE}$ high
t_{DH}	60			ps	Input data hold after $\overline{WE}$ high

[1] The MBS pin determines whether the host interfaced has multiplexed or separate address and data lines. When MBS = 1, the interface is multiplexed.

Timing Diagrams, Multiplexed REM Switch
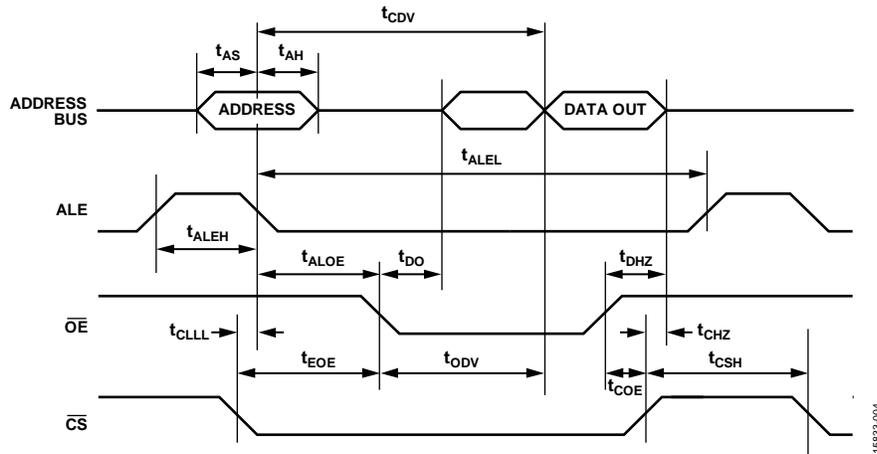
Figure 4. REM Switch Multiplexed Address and Data Bus Read Timing, MBS = 1
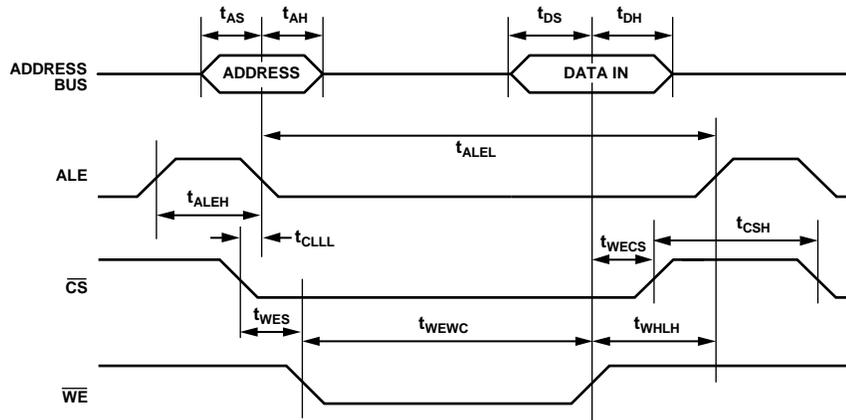
Figure 5. REM Switch Multiplexed Address and Data Bus Write Timing, MBS = 1

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Power Supply	
Core Voltage and Periphery Circuitry	1.08 V to 1.32 V
I/O (VCC+3V3)	2.97 V to 3.63 V
PLL Analog	1.08 V to 1.32 V
DC Input Voltage	−0.5 V to +3.8 V
Operating Temperature Range	
Junction	−40°C to +125°C
Ambient	−40°C to +85°C
Storage Temperature (No Bias) Range	−65°C to +150°C
Electrostatic Discharge (ESD) Voltage, Human Body Model	−2000 V to +2000 V
Lead Temperature (Soldering)	J-STD-020C[1]
Power Dissipation	172.6 mW

[1] Compliant with JEDEC Standard J-STD-020C and restriction of hazardous substances (RoHS), Directive 2002/95/EU.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

REM SWITCH
TOP VIEW
(Not to Scale)

	1	2	3	4	5	6	7	8	9	10	11	12
A	D02/AD02	D04/AD04	D07	D11	D15	D18	D19	D22	D25	D27	D30	D31
B	D01	D03/AD03	D06	D10	D14	D17	D20	D23	D26	D29	$\overline{OE}$	$\overline{WE}$
C	A04/UNUSED	D00	D05/A05	D09	D13	D16	D21	D24	D28	INT2	INT1	INT0
D	A02/ALE	A03/UNUSED	A05/UNUSED	D08	D12	VCC+1V2	GND	VCC+3V3	GND	TIMER7	TIMER6	$\overline{CS}$
E	$\overline{RESET}$	LE	SIZE_32	GND	VCC+1V2	GND	VCC+1V2	GND	VCC+3V3	TIMER5	TIMER4	TIMER3
F	GND	MBS	GND	VCC+3V3	GND	VCC+1V2	GND	GND	GND	TIMER2	TIMER1	TIMER0
G	XTAL0	XTAL1	VCC+1V2A	GND	VCC+1V2	GND	GND	VCC+1V2	GND	RMII_CLK	CLKOUT	$\overline{P2\_ACTIVITY}$
H	GND	VCC+3V3	GND	VCC+3V3	GND	VCC+1V2	GND	GND	VCC+3V3	P2_CRS	P2_COL	$\overline{P2\_LINK\_STATUS}$
J	P1_TXEN	P1_TXCLK	NC	GND	VCC+3V3	GND	VCC+1V2	NC	NC	NC	P2_RXDV	P2_RXCLK
K	P1_TXD0	NC	NC	NC	NC	P1_RXDV	$\overline{P1\_LINK\_STATUS}$	P2_TXD1	NC	P2_RXD0	NC	NC
L	P1_TXD1	P1_TXD2	P1_RXD0	P1_RXD3	NC	P1_CRS	$\overline{P1\_ACTIVITY}$	P2_TXD0	P2_TXD3	NC	P2_RXD2	NC
M	P1_TXD3	NC	P1_RXD1	P1_RXD2	NC	P1_RXCLK	P1_COL	P2_TXEN	P2_TXD2	P2_TXCLK	P2_RXD1	P2_RXD3

■ VCC+1V2	■ VCC+3V3	■ VCC+1V2	■ GND	☐ I/O

Figure 6. Pin Configuration

15833-006

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Direction[1]	Description
A1	D02/AD02	I/O	Data Bus Bit 02 Nonmultiplexed/Data Bus Bit 02 Multiplexed. This is a multifunction pin.
			When MBS = 0, Pin A1 (D02) is Data Bus Bit 02 to and from the REM switch for the nonmultiplexed address data bus.
			When MBS = 1, Pin A1 (AD02) is for the multiplexed address data bus, Bit 02 of the address (LSB), and Bit 02 of the data.
A2	D04/AD04	I/O	Data Bus Bit 04 Nonmultiplexed/Data Bus Bit 04 Multiplexed. This is a multifunction pin.
			When MBS = 0, Pin A2 (D04) is Data Bus Bit 04 to and from the REM switch for the nonmultiplexed address data bus.
			When MBS = 1, Pin A2 (AD04) is for the multiplexed address data bus, Bit 04 of the address, Bit 04 of the data.
A3	D07	I/O	Data Bus Bit 07. Pin A3 is Data Bus Bit 07 to and from the REM switch.
A4	D11	I/O	Data Bus Bit 11. Pin A4 is Data Bus Bit 11 to and from the REM switch.
A5	D15	I/O	Data Bus Bit 15. Pin A5 is Data Bus Bit 15 to and from the REM switch.
A6	D18	I/O	Data Bus Bit 18. Pin A6 is Data Bus Bit 18 to and from the REM switch.
A7	D19	I/O	Data Bus Bit 19. Pin A7 is Data Bus Bit 19 to and from the REM switch.
A8	D22	I/O	Data Bus Bit 22. Pin A8 is Data Bus Bit 22 to and from the REM switch.
A9	D25	I/O	Data Bus Bit 25. Pin A9 is Data Bus Bit 25 to and from the REM switch.
A10	D27	I/O	Data Bus Bit 27. Pin A10 is Data Bus Bit 27 to and from the REM switch.
A11	D30	I/O	Data Bus Bit 30. Pin A11 is Data Bus Bit 30 to and from the REM switch.
A12	D31	I/O	Data Bus Bit 31. Pin A12 is Data Bus Bit 31 to and from the REM switch.
B1	D01	I/O	Data Bus Bit 01. Pin B1 is Data Bus Bit 01 to and from the REM switch.
B2	D03/AD03	I/O	Data Bus Bit 03 Nonmultiplexed/Data Bus Bit 03 Multiplexed. This is a multifunction pin.
			When MBS = 0, Pin B2 (D03) is Data Bus Bit 03 to and from the REM switch for the nonmultiplexed address data bus.
			When MBS = 1, Pin B2 (AD03) is for the multiplexed address data bus, Bit 03 of the address, Bit 03 of the data.
B3	D06	I/O	Data Bus Bit 06. Pin B3 is Data Bus Bit 06 to and from the REM switch.
B4	D10	I/O	Data Bus Bit 10. Pin B4 is Data Bus Bit 10 to and from the REM switch.
B5	D14	I/O	Data Bus Bit 14. Pin B5 is Data Bus Bit 14 to and from the REM switch.
B6	D17	I/O	Data Bus Bit 17. Pin B6 is Data Bus Bit 17 to and from the REM switch.
B7	D20	I/O	Data Bus Bit 20. Pin B7 is Data Bus Bit 20 to and from the REM switch.
B8	D23	I/O	Data Bus Bit 23. Pin B8 is Data Bus Bit 23 to and from the REM switch.
B9	D26	I/O	Data Bus Bit 26. Pin B9 is Data Bus Bit 26 to and from the REM switch.
B10	D29	I/O	Data Bus Bit 29. Pin B10 is Data Bus Bit 29 to and from the REM switch.
B11	$\overline{OE}$	I	Output Enable. Setting Pin B11 low allows the REM switch to drive data lines.
B12	$\overline{WE}$	I	Write Enable. Setting Pin B12 low enables a write; setting Pin B12 high enables a read.
C1	A04/UNUSED	I	Address Line 04/Multiplexed Address Bus (UNUSED). This is a multifunction pin.
			Pin C1 is Address Line 04 when MBS = 0 for the nonmultiplexed address data bus. When MBS = 1, Pin C1 is Bit 04 of the address bus. Line A04 is sampled on the falling edge of $\overline{CS}$ (Pin D12).
			Pin C1 is unused when MBS = 1 for the multiplexed address data bus.
C2	D00	I/O	Data Bus Bit 00. C2 is Data Bus Bit 00 to and from the REM switch.
C3	D05/A05	I/O	Data Bus Bit 05 Nonmultiplexed/Data Bus Bit 05 Multiplexed. This is a multifunction pin.
			When MBS = 0, Pin C3 (D05) is Data Bus Bit 05 to and from the REM switch for the nonmultiplexed address data bus.
			When MBS = 1, Pin C3 (A05) is for the multiplexed address data bus, Bit 05 of the address, Bit 05 of the data.
C4	D09	I/O	Data Bus Bit 09. Pin C4 is Data Bus Bit 09 to and from the REM switch.
C5	D13	I/O	Data Bus Bit 13. Pin C5 is Data Bus Bit 13 to and from the REM switch.
C6	D16	I/O	Data Bus Bit 16. Pin C6 is Data Bus Bit 16 to and from the REM switch.

Pin No.	Mnemonic	Direction[1]	Description
C7	D21	I/O	Data Bus Bit 21. Pin C7 is Data Bus Bit 21 to and from the REM switch.
C8	D24	I/O	Data Bus Bit 24. Pin C8 is Data Bus Bit 24 to and from the REM switch.
C9	D28	I/O	Data Bus Bit 28. Pin C9 is Data Bus Bit 28 to and from the REM switch.
C10	INT2	O	Interrupt 2 Output to Host Processor. Pin C10 can be configured to respond to one or more internal events.
C11	INT1	O	Interrupt 1 Output to Host Processor. Pin C11 can be configured to respond to one or more internal events.
C12	INT0	O	Interrupt 0 Output to Host Processor. Pin C12 can be configured to respond to one or more internal events.
D1	A02/ALE	I	Address Line 02/Address Latch Enable. This is a multifunction pin.
		N/A	Pin D1 is Address Line 02 when MBS = 0 for the nonmultiplexed address data bus. When MBS = 0, Pin D1 is Bit 02 of the address bus. Line A02 is sampled on the falling edge of $\overline{CS}$ (Pin D12). The addresses are 32-bit aligned/addressable.
			When MBS = 1, this pin is the address latch enable pin.
D2	A03/UNUSED	I	Address Line 03/Multiplexed Address Bus. This is a multifunction pin.
			Pin D2 is Address Line 03 when MBS = 0 for the nonmultiplexed address data bus. When MBS = 0, Pin D2 is Bit 03 of the address bus. Line A03 is sampled on the falling edge of $\overline{CS}$ (Pin D12). The addresses are 32-bit aligned/addressable.
			Pin D2 is unused when MBS = 1 for the multiplexed address data bus.
D3	A05/UNUSED	I	Address Line 05/Multiplexed Address Bus. This is a multifunction pin.
			Pin D3 is Address Line 05 when MBS = 0 for the nonmultiplexed address data bus. When MBS = 0, Pin D3 is Bit 05 of the address bus. Line A05 is sampled on the falling edge of $\overline{CS}$ (Pin D12). The addresses are 32-bit aligned/addressable.
			Pin D3 is unused when MBS = 1 for the multiplexed address data bus.
D4	D08	I/O	Data Bus Bit 08. Pin D4 is Data Bus Bit 08 to and from the REM switch.
D5	D12	I/O	Data Bus Bit 12. Pin D5 is Data Bus Bit 12 to and from the REM switch.
D6, E5, E7, F6, G5, G8, H6, J7	VCC+1V2	N/A	1.2 V Power Supply.
D7, D9, E4, E6, E8, F1, F3, F5, F7, F8, F9, G4, G6, G7, G9, H1, H3, H5, H7, H8, J4, J6	GND	N/A	Ground.
D8, E9, F4, H2, H4, H9, J5	VCC+3V3	N/A	3.3 V Power Supply.
D10	TIMER7	O	Internal Precision Timer Clock 7 Synchronized. Pin D10 is a programmable output.
D11	TIMER6	O	Internal Precision Timer Clock 6 Synchronized. Pin D11 is a programmable output.
D12	$\overline{CS}$	I	Address Bus Chip Select. The address bus is sampled on the falling edge of $\overline{CS}$. A rising edge on $\overline{CS}$ terminates the current read or write cycle.
E1	$\overline{RESET}$	I	Reset. When Pin E1 is asserted low, all internal registers initialize and bus configuration pins enable for sampling.
E2	LE	I	System Endianness. When Pin E2 is set high, the data format is little endian. When Pin E2 is set low, the data format is big endian. The value is captured on the rising edge of $\overline{RESET}$.
E3	SIZE_32	I	Data Bus Size. The data bus size is 32 bits when Pin E3 is set high and 16 bits when Pin E3 is set low. The value is captured on the rising edge of $\overline{RESET}$.
E10	TIMER5	O	Internal Precision Timer Clock 5 Synchronized. Pin E10 is a programmable output.
E11	TIMER4	O	Internal Precision Timer Clock 4 Synchronized. Pin E11 is a programmable output.
E12	TIMER3	I/O	Internal Precision Timer 3 Clock Synchronized. Pin E12 is a programmable output or input.
F2	MBS	I	Multiplex Bus Select. When Pin F2 is set high, the host interface bus operates as a multiplexed bus. The host interface operates as a nonmultiplexed bus when Pin F2 is set low. The value is captured on the rising edge of Pin E1, $\overline{RESET}$.
F10	TIMER2	I/O	Internal Precision Timer Clock 2 Synchronized. Pin F10 is a programmable output or input.

Pin No.	Mnemonic	Direction[1]	Description
F11	TIMER1	I/O	Internal Precision Timer Clock 1 Synchronized. Pin F11 is a programmable output or input.
F12	TIMER0	I/O	Internal Precision Timer Clock 0 Synchronized. Pin F12 is a programmable output or input.
G1	XTAL0		Clock Input. This pin has a frequency of 25 MHz.
G2	XTAL1		Output Pair for XTAL0. Pin G2 is required for use with a crystal clock source.
G3	VCC+1V2A		Analog 1.2 V Power Supply. This pin must be isolated from VCC+1V2.
G10	RMII_CLK	O	50 MHz Reduced Media Independent Interface (RMII) Transmit and Receive Clock Reference for Port 1 and Port 2.
G11	CLKOUT	O	Output Clock. Pin G11 has the same frequency as XTAL0 (25 MHz).
G12	P2_ACTIVITY	O	Port 2 Activity LED Output Driver. The LED turns on when G12 is asserted low.
H10	P2_CRS	I	Port 2 Carrier Sense. When H10 is asserted high, a carrier has been sensed on Port 2.
H11	P2_COL	I	Port 2 Media Independent Interface (MII) Collision. Pin H11 asserting high indicates a collision on Port 2.
H12	P2_LINK_STATUS	I	Port 2 Link Status from Physical Layer (PHY). When H12 is asserted low, the link on Port is active.
J1	P1_TXEN	O	Port 1 MII Transmit Enable. Setting Pin J1 high enables transmission on Port 1.
J2	P1_TXCLK	I	Port 1 MII Transmit Clock from PHY.
J3, J8, J9, J10, K2, K3, K4, K5, K9, K11, K12, L5, L10, L12, M2, M5	NC	N/A	No Connection.
J11	P2_RXDV	I	Port 2 Received Data Valid. Data from the Port 2 PHY is valid when J11 is asserted high (used as CRS/RXDV in RMII mode).
J12	P2_RXCLK	I	Port 2 MII Receive Clock from PHY.
K1	P1_TXD0	O	Transmit Data Output Bit 0 for Port 1 MII and RMII.
K6	P1_RXDV	I	Port I MII Received Data Valid. Asserting Pin K6 high indicates that data from the Port 1 PHY is valid (used as CRS/RXDV in RMII mode).
K7	P1_LINK_STATUS	I	Port 1 Link Status from PHY. Asserting Pin K7 low activates the Port 1 link.
K8	P2_TXD1	O	Transmit Data Output Bit 1 for Port 2 MII and RMII.
K10	P2_RXD0	I	Receive Data Input Bit 0 for Port 2 MII and RMII.
L1	P1_TXD1	I	Transmit Data Output Bit 1 for Port 1 MII and RMII.
L2	P1_TXD2	O	Transmit Data Output Bit 2 for Port 1 MII.
L3	P1_RXD0	I	Receive Data Input Bit 0 for Port 1 MII and RMII.
L4	P1_RXD3	I	Receive Data Input Bit 3 for Port 1 MII.
L6	P1_CRS	I	Port 1 Carrier Sense. When L6 is asserted high, a carrier has been sensed on Port 1.
L7	P1_ACTIVITY	O	Port 1 Activity LED Output Driver. The LED turns on when Pin L7 is asserted low.
L8	P2_TXD0	O	Transmit Data Output Bit 0 for Port 2 MII and RMII.
L9	P2_TXD3	O	Transmit Data Output Bit 3 for Port 2 MII.
L11	P2_RXD2	I	Receive Data Input Bit 2 for Port 2 MII.
M1	P1_TXD3	O	Transmit Data Output Bit 3 for Port 1 MII.
M3	P1_RXD1	I	Receive Data Input Bit 1 for Port 1 MII AND RMII.
M4	P1_RXD2	I	Receive Data Input Bit 2 for Port 1 MII.
M6	P1_RXCLK	I	Port I MII Receive Clock from PHY.
M7	P1_COL	I	Port 1 MII Collision. Asserting Pin M7 high indicates a collision on Port 1.
M8	P2_TXEN	O	Port 2 MII Transmit Enable. Setting Pin M8 to high enables the Port 2 transmit.
M9	P2_TXD2	O	Transmit Data Output Bit 2 for Port 2 MII.
M10	P2_TXCLK	I	Port 2 MII Transmit Clock from PHY.
M11	P2_RXD1	I	Receive Data Input Bit 1 for Port 2 MII and RMII.
M12	P2_RXD3	I	Receive Data Input Bit 3 for Port 2 MII.

[1] I is input, I/O is input/output, O is output, and N/A is not applicable.

THEORY OF OPERATION

DEVICE INTERFACES

Oscillator

The oscillator clock source is routed to an internal phase-locked loop (PLL) to create the following clock sources:

- 25 MHz for the CLKOUT reference clock
- 50 MHz for the RMII reference clock

An oscillator used as a clock source requires a tighter tolerance.
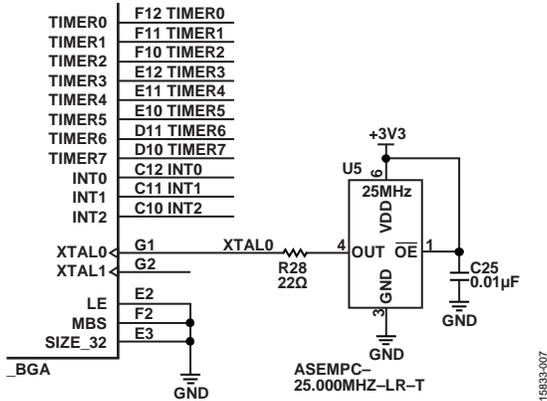
Figure 7. Oscillator Clock Source Circuit

Crystal

When using the REM switch with a crystal, use an oscillator pad configuration, as shown Figure 8.
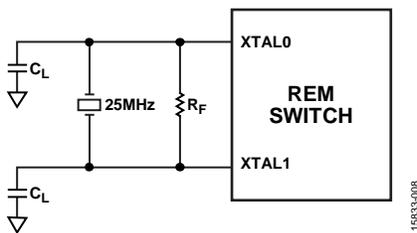
Figure 8. Crystal Clock Source Circuit

The values presented in the following list are typical for operation when using a 25 MHz crystal:

- ESR = 40 Ω
- C_L = 8 pF
- R_F = 1 MΩ

Reset Timing

The timing requirement for $\overline{\text{RESET}}$ is a minimum active low time of 16 ns.

INTERNAL PRECISION TIMER

The REM switch includes an internal precision timer (IPT). The IPT maintains a system time that has a resolution of 1 ns. Use the IPT to trigger timer output events or capture input event times on the TIMER0, TIMER1, TIMER2, and TIMER3 pins, or to create a complex pulse pattern on the TIMER4, TIMER5, TIMER6, and TIMER7 pins.

TIMER0 to TIMER3 Inputs/Outputs

TIMER0 to TIMER3 inputs/outputs can be configured to either time stamp an input event or time trigger an output event. When configured to time stamp an input event, the value of the IPT is captured in a 64-bit register when the associated timer signal transitions from low to high. User software reads this register and uses the value to time stamp an associated event. For example, when the TIMER0 signal transitions from low to high, the value of the IPT is stored in the Timer 0, 64-bit register (consult the *REM Switch Software Driver User Guide*, available at www.analog.com/en/products/industrial-ethernet.html for more details). The same is true when configuring TIMER1, TIMER2, or TIMER3 to time stamp input events. User software uses the generated time stamp to associate the time stored in the 64-bit register with a particular event.

When configured to time trigger an output event, the timer signal toggles when the IPT reaches the value stored in the Timer x, 64-bit register. The process of time triggering an output event is as follows using the Timer 0 register in the example:

1. The host processor software stores a value in the Timer 0, 64-bit register.
2. The IPT reaches that value stored in the Timer 0, 64-bit register.
3. The TIMER0 pin toggles from high to low or low to high (depending on its state when the 64-bit register was loaded).

The same process is followed when the TIMER1, TIMER2, and TIMER3 pins are configured to time trigger output events.

TIMER4 to TIMER7 Outputs

TIMER4 to TIMER7 outputs are configured to output independent, IPT clock synchronized, programmable, pulse-width modulated signals. Each of these timers has a resolution of 16 ns. Each timer can have its own pulse-width modulation program that allows an arbitrary number of rising and falling edges, depending on the protocols that repeat on a programmable interval. The software drivers for the REM switch provide the capability to define the rising and falling edges for each TIMERx output.

HOST INTERFACE

Multiplex Bus Select

The host interface supports a separate address bus and data bus or a multiplexed address and data bus. The selection between the two types of busses is provided by the MBS signal (Pin F2), which is sampled on the rising edge of $\overline{\text{RESET}}$. See Table 5 for pin function descriptions for the MBS and $\overline{\text{RESET}}$ signals.

Data Bus Width

The host interface supports either a 16-bit or 32-bit wide data bus. The data bus width is determined by the SIZE_32 (Pin E3) signal that is sampled on the rising edge of $\overline{RESET}$. See Table 5 for pin function descriptions for the SIZE_32 and $\overline{RESET}$ signals.

Endianness

The host interface presents data on the data bus in either big endian or little endian format. The endianness of the data is determined by the $\overline{LE}$ signal (Pin E2), which is sampled on the rising edge of the $\overline{RESET}$ signal. See Table 5 for pin function descriptions for the $\overline{LE}$ and $\overline{RESET}$ signals.

The REM switch data bus is defined as follows:

- D0 = LSB
- D15 = MSB for 16-bit bus
- D31 = MSB for 32-bit bus

For all control/status register accesses, there is no difference in operation based on the setting of the LE pin. The data representation in a host processor register must match the data that is transferred over the bus.

All control/status registers are 16-bits wide. If using a 32-bit bus, transfer the data in the following order: D15 to D0 (D31 to D16 are ignored when using a 32-bit bus). For example, the REM switch driver reads the device number register early in the

initialization process. In the case of the number, 0x00003300, the value read from this register must be transferred across the bus, as shown in Table 6. When evaluated in the software on the host processor, the value of these 32 bits results in 0x00003300.

For queue accesses, the REM switch treats all data as byte arrays. Consider the following example of a stream of bytes received over an Ethernet cable into a REM switch port and then transferred to the host. The packet data in network order is as follows: 0x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x08, 0x09, 0x0A, 0x0B, 0x0C, 0x0D, 0x0E, 0x0F.

The data is read differently depending on the setting, as follows:

- Big endian 16-bit host interface: 0x0001, 0x0203, 0x0405, 0x0607, 0x0809, 0x0A0B, 0x0C0D, 0x0E0F.
- Big endian 32-bit host interface: 0x00010203, 0x04050607, 0x08090A0B, 0x0C0D0E0F.
- Little endian 16-bit host interface: 0x0100, 0x0302, 0x0504, 0x0706, 0x0908, 0x0B0A, 0x0D0C, 0x0F0E.
- Little endian 32-bit host interface: 0x03020100, 0x07060504, 0x0B0A0908, 0x0F0E0D0C.

Consult the *REM Switch Software Driver User Guide*, available at www.analog.com/en/products/industrial-ethernet.html for more details on how to handle endianness in an application of a device.

Table 6. Control/Status Registers Bit Map

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0

Table 7. Big Endian 16-Bit Data Bus Bit Map, 0x0E0F Hexadecimal

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	1

Table 8. Big Endian 32-Bit Data Bus Bit Map, 0x0C0D0E0F Hexadecimal

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	1
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	1

Table 9. Little Endian 16-Bit Data Bus Bit Map, 0x0E0F Hexadecimal

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	0

Table 10. Little Endian 32-Bit Data Bus Bit Map, 0x0F0E0D0C Hexadecimal

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	1	1	0	1	0	0	0	0	1	1	0	0

Address/Data Bus Operation

The host interface address/data bus connects to the address/ data bus of the CPU. There are four bits of data for the address bus and either 16 bits or 32 bits of data for the data bus. Each REM switch address is 32-bit aligned, meaning that the addresses increment by four bytes (A05 to A02). Regardless of whether the data bus is 16 bits wide or 32 bits wide, the least significant address bit supplied to the REM switch is always the same.

In addition, all accesses to indirect registers return the register data in the lower 16 bits only (even if the interface is 32 bits wide). For wider registers, such as a 64-bit timer, use a repeated set of reads or writes to access the full content of the register.

Nonmultiplexed Address Data Bus

MBS = 0 selects the nonmultiplexed address data bus configuration. The read and write cycle timings are defined in Figure 2 and Figure 3. See Table 2 for the read and write cycle timing parameters.

Multiplexed Address Data Bus

MBS = 1 selects the multiplexed address data bus configuration. The read and write cycle timings are defined in Figure 4 and Figure 5. See Table 3 for the read and write cycle timing parameters.

Register and Data Access

Four bits of address provide direct access to 16 registers. A read cycle or a write cycle obtains or sets the data in these registers. To access additional registers, use the host indirect address register. The direct address register definitions are provided in Table 11.

The REM switch software driver provides the necessary application programming interface (API) functions to access these registers and manage all aspects of the switch for a specific protocol. Ethernet packets are received and transmitted directly through the Queue 0, Queue 1, Queue 2, and Queue 3 read and write registers, depending on the protocol.

Ethernet protocol control and switch management are performed by the software driver API through the host read/write queue data registers and the host direct/indirect registers (refer to the *REM Switch Driver User Guide*, available at www.analog.com/en/products/industrial-ethernet.html, for more information about these registers). Interrupt management is performed by the software driver API using the three interrupt lines in conjunction with the queue status register, timer status register, universal input/output controller (UIC) interrupt status register, and the composite interrupt status register.

Table 11. Direct Address Register Definitions

Register Name	Width	Address[5:0]	Read/Write[1]	Reset Value[2]
Queue 0 Read	16/32	0x00	R	0x00000000
Queue 0 Write	16/32	0x00	W	N/A
Queue 1 Read	16/32	0x04	R	0x00000000
Queue 1 Write	16/32	0x04	W	N/A
Queue 2 Read	16/32	0x08	R	0x00000000
Queue 2 Write	16/32	0x08	W	N/A
Queue 3 Read	16/32	0x0C	R	0x00000000
Queue 3 Write	16/32	0x0C	W	N/A
Reserved	N/A	0x10 to 0x14		N/A
Host Read Queue 0 Data	16/32	0x18	R	0x00000000
Host Read Queue 0 Data Head	16/32	0x18	W	0x00000000
Host Read Queue 1 Data	16/32	0x1C	R	0x00000000
Host Read Queue 1 Data Head	16/32	0x1C	W	N/A
Queue Status Register	16	0x20	R/W	0x00000F00
Timer Status Register	16	0x24	R/W	0x00000000
UIC Interrupt Status	16	0x28	R/W	0x0000
Composite Interrupt Status	16	0x2C	R	0x0000
Host Indirect Address	16	0x30	R/W	0x0000
Host Indirect Read Data	16	0x34	R	N/A
Host Indirect Write Data	16	0x34	W	N/A
Host Write Queue 0 Completion	16	0x38	R	0x0000
Host Write Queue 1 Completion	16	0x3C	R	0x0000

[1] R means read only, W means write only, and R/W means read/write.
[2] N/A means not applicable.

Interrupts

Three interrupt lines are outputs from the REM switch; these three lines are labeled INT0, INT1, and INT2. Each of these interrupt lines must be mapped according to the interrupt inputs of the host processor. To ensure the best protocol performance, give INT2 the highest priority in the processor priority scheme, and do not disable it.

The interrupt lines are mapped to the events defined by the queue status register, timer status register, UIC interrupt status register, and composite interrupt status register for each protocol. It is the responsibility of the software driver API to provide the appropriate interrupt service routine for the mapped event. Refer to the *REM Switch Driver User Guide*, available at www.analog.com/en/products/industrial-ethernet.html, for technical details on handling REM switch interrupts for a specific industrial Ethernet protocol.

When an interrupt event defined in the appropriate status registers occurs, the associated REM switch interrupt output line becomes active (Logic 1) and remains active until the register is cleared. If multiple events are mapped to the same REM switch interrupt output, and more than one becomes active, the associated interrupt line remains in the active (Logic 1) state until all active interrupt source registers are cleared.

Note that although the interrupts, INT0, INT1, and INT2, are labeled as priorities of low, medium, and high, there is not any inherent priority on the lines themselves, and they can be mapped accordingly.

ETHERNET INTERFACE

There are two Ethernet ports on the REM switch. Each port is capable of configuration to support RMII or MII. Each port also has an input for link status from the PHY and an output for a link activity LED.

Connections

The pins associated specifically with the RMII and MII interfaces are listed in Table 12; their full descriptions are defined in Table 5.

The RMII interface is a seven-signal interface for each port (see Figure 9). This interface uses a 50 MHz reference clock (RMII_CLK) provided by the REM switch to the PHY.

The MII interface is a 14-signal interface for each port (see Figure 10). The REM switch provides the base clock to the PHYs using the synchronized 25 MHz CLKOUT signal. The PHYs then provide a receive and transmit clock (RX_CLK and TX_CLK) for each port.

Link Status and Activity

The $\overline{Px\_LINK\_STATUS}$ signal is an input to the REM switch from the selected PHY, configured so that the $\overline{Px\_LINK\_STATUS}$ signal is asserted continuously (not blinking) and determines the link up or link down state.

The $\overline{Px\_ACTIVITY}$ signal is an output from the REM switch and is typically used to drive an LED to indicate a link is valid.
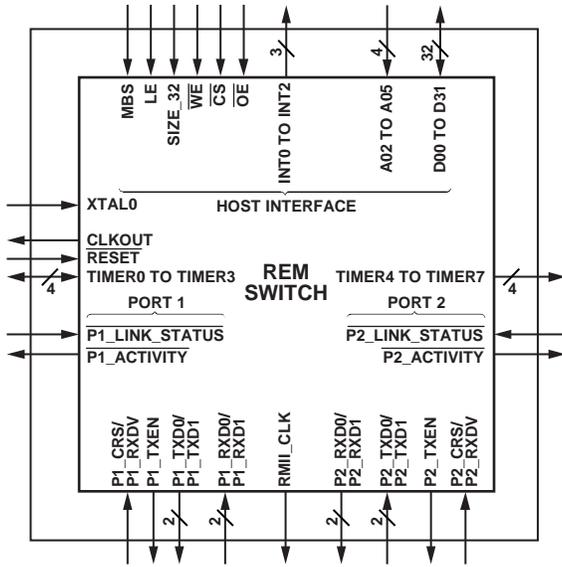
Figure 9. REM Switch Configured for RMII Interface
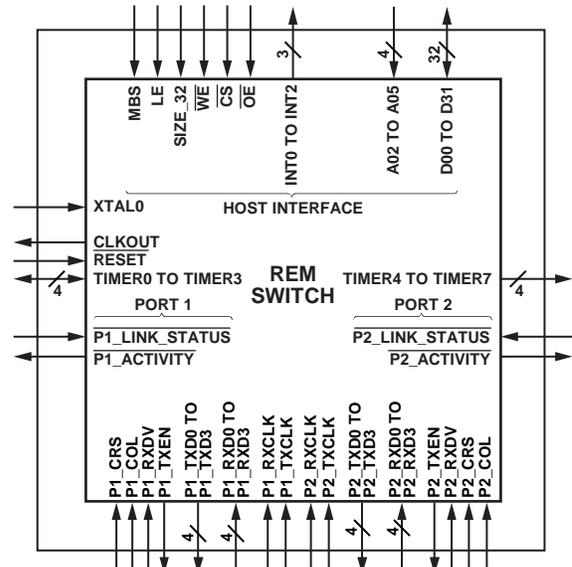
Figure 10. REM Switch Configured for MII Interface

Table 12. Brief Descriptions for MII and RMII Pins

Pin No.	Mnemonic	Brief Description
G10	RMII_CLK	50 MHz RMII Transmit and Receive Clock for Port 1 and Port 2.
G11	CLKOUT	Output Clock.
G12	P2_ACTIVITY	Port 2 Activity LED Output Driver.
H10	P2_CRS	Port 2 Carrier Sense.
H11	P2_COL	Port 2 MII Collision.
H12	P2_LINK_STATUS	Port 2 Link Status from PHY.
J1	P1_TXEN	Port 1 MII Transmit Enable.
J2	P1_TXCLK	Port 1 MII Transmit Clock from PHY.
J11	P2_RXDV	Port 2 Received Data Valid.
J12	P2_RXCLK	Port 2 MII Receive Clock from PHY.
K1	P1_TXD0	Transmit Data Output Bit 0 for Port 1 MII, RMII.
K6	P1_RXDV	Port I MII Received Data Valid.
K7	P1_LINK_STATUS	Port 1 Link Status from PHY.
K8	P2_TXD1	Transmit Data Output Bit 1 for Port 2 MII, RMII.
K10	P2_RXD0	Receive Data Input Bit 0 for Port 2 MII, RMII.
L1	P1_TXD1	Transmit Data Output Bit 1 for Port 1 MII, RMII.
L2	P1_TXD2	Transmit Data Output Bit 2 for Port 1 MII.
L3	P1_RXD0	Receive Data Input Bit 0 for Port 1 MII, RMII.
L4	P1_RXD3	Receive Data Input Bit 3 for Port 1 MII.
L6	P1_CRS	Port 1 MII Carrier Sense.
L7	P1_ACTIVITY	Port 1 Activity LED Output Driver.
L8	P2_TXD0	Transmit Data Output Bit 0 for Port 2 MII, RMII.
L9	P2_TXD3	Transmit Data Output Bit 3 for Port 2 MII.
L11	P2_RXD2	Receive Data Input Bit 2 for Port 2 MII.
M1	P1_TXD3	Transmit Data Output Bit 3 for Port 1 MII.
M3	P1_RXD1	Receive Data Input Bit 1 for Port 1 MII, RMII.
M4	P1_RXD2	Receive Data Input Bit 2 for Port 1 MII.
M6	P1_RXCLK	Port 1 Receive Clock from PHY.
M7	P1_COL	Port 1 MII Collision.
M8	P2_TXEN	Port 2 MII Transmit Enable.
M9	P2_TXD2	Transmit Data Output Bit 2 for Port 2 MII.
M10	P2_TXCLK	Port 2 MII Transmit Clock from PHY.
M11	P2_RXD1	Receive Data Input Bit 1 for Port 2 MII, RMII.
M12	P2_RXD3	Receive Data Input Bit 3 for Port 2 MII.

APPLICATIONS INFORMATION
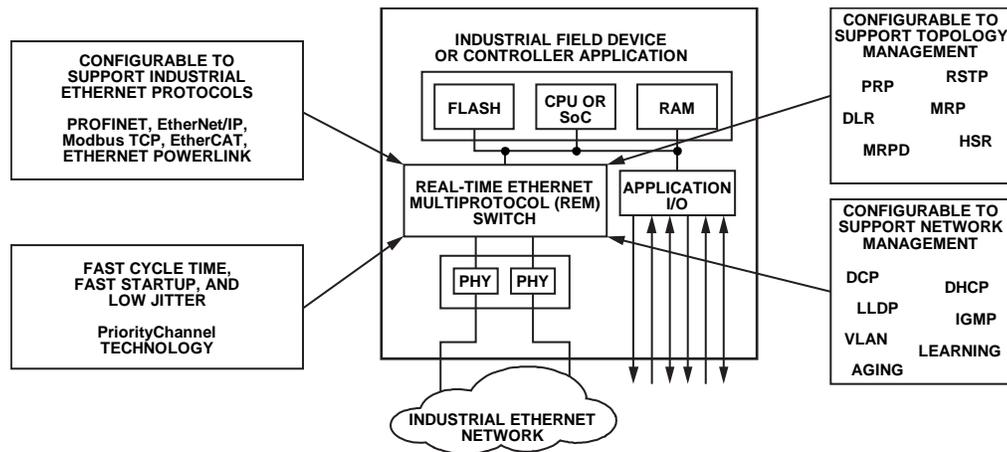
Figure 11. Application for the REM Switch

REM SWITCH HARDWARE

The basic REM switch hardware is identified as the fido5100 or fido5200. For example, the fido5100 supports the following protocols:

- PROFINET RT and IRT, Class B and Class C with fast startup (Version 2.3)
- EtherNet/IP with and without DLR (supervisor and node, announce based and beacon based), QuickConnect, CIP Sync, and CIP Motion
- Modbus TCP
- POWERLINK

The fido5200 supports the following protocols:

- EtherCAT
- All protocols defined for the fido5100

The REM switches are PI Net Load Class III capable, and support media redundancy for planned duplication (MRPD), high availability seamless redundancy (HSR), and parallel redundancy protocol (PRP). They also support IEEE 1588 Version 2 for ordinary clock (both peer to peer and end to end transparent clocks), raw frames, and user datagram protocol (UDP), as well as discovery configuration protocol (DCP), link layer discovery protocol (LLDP), dynamic host configuration protocol (DHCP), rapid spanning tree protocol (RSTP), virtual local area network (VLAN), and Internet group management protocol (IGMP) snooping support.

REM Switch Drivers

The REM switch driver for each protocol is provided as portable C code. The *REM Switch Software Driver User Guide* describes the driver for each protocol and its integration into a host processor. Visit www.analog.com/en/products/industrial-ethernet.html to download the user guide.

BOARD LAYOUT

The following guidelines provide best practice for board layout with the REM switch:

- Use individual polygons for the power planes for each of the three supplies. Allow at least 0.2 mm of isolation between the power planes.
- Isolate clock signals from the other traces and make them as short as possible.
- A minimum clearance around the REM switch of 3 mm is required to facilitate heat dissipation.

DESIGN CONSIDERATIONS

Power

The REM switch require 1.2 V and 3.3 V power supplies. Each power level requires its own power plane on the PCB.

The REM switch uses 3.3 V LVCMOS logic levels for its I/O. This I/O requires a 3.3 V (±10%) power supply circuit. Ideally, this circuit uses a low noise switching power supply. The REM switch use a 1.2 V (±10%) supply for the core of the chip. The core power supply requires its own power plane on the PCB. Additional best practices include

- Use one 0.1 µF bypass capacitor for every 1.2 V power pin.
- Use a power supply IC rated to supply at least 100 mA.
- Supply 3.3 V power from its own layer on the PCB to the 3.3 V power input pins on the REM switch.
- Use one 0.1 µF bypass capacitor for every 3.3 V power pin.
- For the 1.2 V analog supply, the signal must be isolated using a 120 Ω, 500 mA ferrite bead and 10 µF, 1 µF, and 0.1 µF filtering capacitors.

Reset

The $\overline{\text{RESET}}$ signal is typically driven by the host microprocessor that is paired with the REM switch. $\overline{\text{RESET}}$ is an active low signal; therefore, pull $\overline{\text{RESET}}$ high as power becomes valid.

Physical Layer (PHY)

The REM switch is designed intentionally without PHYs because of the different requirements on PHY performance. EtherCAT and PROFINET IRT have much tighter latency and jitter requirements than standard Ethernet.

Clocking

Most PHYs allow the user to clock the PHY with a crystal oscillator or a separate clock source when using an MII interface. It is a requirement for EtherCAT designs (and recommended for other designs) to use the CLKOUT signal from the REM switch as the clock source for the PHYs. This approach minimizes jitter as much as possible.

CLKOUT from the REM switch is a 25 MHz clock signal generated from the 25 MHz input clock to the REM switch using the internal PLL of the REM switch. The PHY uses the 25 MHz CLKOUT signal to generate the MII receive (Rx) and transmit (Tx) clock inputs (P1_RXCLK, P1_TXCLK, P2_RXCLK, and P2_TXCLK pins) to the REM switch.

For RMII, the REM switch generates the required 50 MHz clock for the RMII interface. The clock is generated from the 25 MHz input clock to the REM switch using the internal PLL of the REM switch.

As with all clock signals, take care when routing these signals to minimize noise and loading effects.

Management Data Input/Output (MDIO)

All PHYs require configuration and can provide some type of status information in return. Each PHY is different, but most PHYs use a management data input/output (MDIO) interface to communicate this configuration and status. The REM switch does not provide separate communication to the PHYs. The host processor paired with the REM switch is required to provide this PHY communication.

Contact Analog Devices, Inc., technical support regarding questions about PHY settings or the MDIO interface.

fido5100/fido5200

OUTLINE DIMENSIONS

COMPLIANT WITH JEDEC STANDARDS MO-275-EEAB-1

Figure 12. 144-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-144-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
FIDO5100BBCZ	−40°C to +85°C	144-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-144-12
FIDO5100CBCZ	−40°C to +105°C	144-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-144-12
FIDO5110BBCZ	−40°C to +85°C	144-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-144-12
FIDO5110CBCZ	−40°C to +105°C	144-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-144-12
FIDO5200BBCZ	−40°C to +85°C	144-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-144-12
FIDO5200CBCZ	−40°C to +105°C	144-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-144-12
FIDO5210BBCZ	−40°C to +85°C	144-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-144-12
FIDO5210CBCZ	−40°C to +105°C	144-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-144-12
RAPID-NIEK-V0004		Evaluation Kit	

[1] Z = RoHS Compliant Part.

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