GaAs, Nonreflective, SP4T Switch 100 MHz to 4 GHz

Enhanced Product

HMC241ATCPZ-EP

FEATURES

- Broadband frequency range: 100 MHz to 4 GHz
- Nonreflective 50 Ω design
- Low insertion loss: 0.7 dB at 2 GHz
- High isolation: 43 dB at 2 GHz
- High input linearity at 250 MHz to 4 GHz
  - 1 dB compression (P1dB): 29 dBm typical
  - Third order intercept (IP3): 47 dBm typical
- High power handling
  - 28.5 dBm through path
  - 25 dBm terminated path
- Single positive supply: 3 V to 5 V
- Integrated 2 to 4 line decoder
- 16-lead, 3 mm × 3 mm LFCSP package
- ESD rating: 250 V (Class 1A)

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range (−55°C to +125°C)
- Controlled manufacturing baseline
- One assembly/test site
- Product change notification
- Qualification data available on request

APPLICATIONS

- Cellular/4 G infrastructure
- Wireless infrastructure
- Automotive telematics
- Mobile radios
- Test equipment

FUNCTIONAL BLOCK DIAGRAM

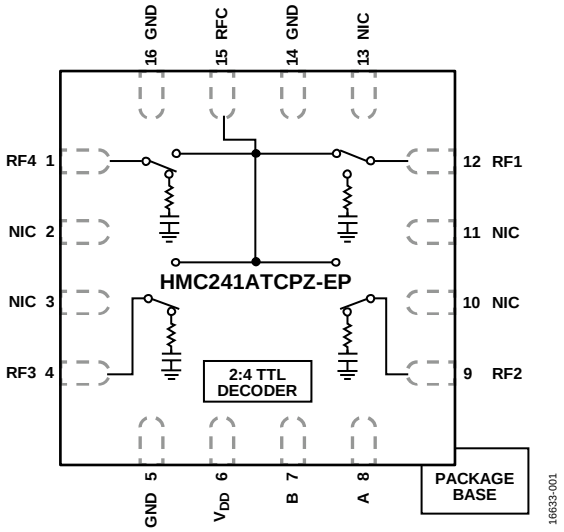

Figure 1.

GENERAL DESCRIPTION

The HMC241ATCPZ-EP is a general-purpose, nonreflective, 100 MHz to 4 GHz single-pole, four-throw (SP4T) switch manufactured using a gallium arsenide (GaAs) process. This switch offers high isolation of 43 dB typical at 2 GHz, low insertion loss of 0.7 dB at 2 GHz, and on-chip termination of the isolated ports.

The on-chip circuitry allows the HMC241ATCPZ-EP to operate at a single, positive supply voltage range of 3 V to 5 V. This switch requires two positive logic control voltages. The HMC241ATCPZ-EP includes an on-chip, binary two to four line decoder that provides logic control from two logic input lines to select one of the four radio frequency (RF) lines.

The HMC241ATCPZ-EP is available in a 3 mm × 3 mm, 16-lead LFCSP package. Additional application and technical information can be found in the HMC241ALP3E data sheet.

Rev. 0

Document Feedback

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Technical Support
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REVISION HISTORY

3/2018—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 3 V or 5 V, V_{CTRL} = 0 V or V_{DD}, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.1		4	GHz
INSERTION LOSS						
Between RFC and RF1 to RF4 (On)		100 MHz to 1 GHz		0.6	0.9	dB
		1 GHz to 2 GHz		0.7	1.0	dB
		2 GHz to 2.5 GHz		0.9	1.2	dB
		2.5 GHz to 4 GHz		1.2	1.5	dB
ISOLATION						
Between RFC and RF1 to RF4 (Off)		100 MHz to 1 GHz	40	45		dB
		1 GHz to 2 GHz	38	43		dB
		2 GHz to 2.5 GHz	35	41		dB
		2.5 GHz to 4 GHz	25	32		dB
RETURN LOSS						
RFC and RF1 to RF4 (On)		100 MHz to 2.5 GHz		18		dB
		2.5 GHz to 4 GHz		12		dB
RF1 to RF4 (Off)		100 MHz to 4 GHz		12		dB
SWITCHING		250 MHz to 4 GHz				
Rise and Fall Time	t_{RISE}, t_{FALL}	10 % to 90 % of RF output		30		ns
On and Off Time	t_{ON}, t_{OFF}	50 % V_{CTL} to 90 % of RF output		100		ns
INPUT LINEARITY[1]		250 MHz to 4 GHz				
1 dB Power Compression	P1dB	V_{DD} = 3 V		24		dBm
		V_{DD} = 5 V	23	29		dBm
Third-Order Intercept	IP3	10 dBm per tone, 1 MHz spacing				
		V_{DD} = 3 V		50		dBm
		V_{DD} = 5 V		47		dBm
SUPPLY		V_{DD} pin				
Voltage	V_{DD}		3		5	V
Current	I_{DD}			2.5	5	mA
DIGITAL CONTROL INPUTS		CTRLA and CTRLB pins				
Voltage	V_{CTL}					
Low	V_{INL}	V_{DD} = 3 V	0		0.8	V
		V_{DD} = 5 V	0		0.8	V
High	V_{INH}	V_{DD} = 3 V	2		3	V
		V_{DD} = 5 V	2		5	V
Current						
Low	I_{INL}			0.2		µA
High	I_{INH}			40		µA
OPERATING TEMPERATURE			−55		+125	°C

[1] Input linearity performance degrades at frequencies less than 250 MHz.

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.

Table 2.

Parameter	Rating
Positive Supply Voltage (V_{DD})	7 V
Digital Control Input Voltage	−0.5 V to V_{DD} +1 V
RF Input Power (See Figure 2)	
(f = 100 MHz to 4 GHz, T_{CASE} = 85°C)	
V_{DD} = 3 V	
Through Path	23.5 dBm
Terminated Path	20 dBm
Hot Switching	17.5 dBm
V_{DD} = 5 V	
Through Path	28.5 dBm
Terminated Path	23.5 dBm
Hot Switching	22.5 dBm
Junction Temperature, T_J	150°C
Storage Temperature Range	−65°C to +150°C
Reflow Temperature (MSL3 Rating)[1]	260°C
Junction to Case Thermal Resistance, θ_{JC}	
Through Path	144°C/W
Terminated Path	300°C/W
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	250 V (Class 1A)

[1] See the Ordering Guide section.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

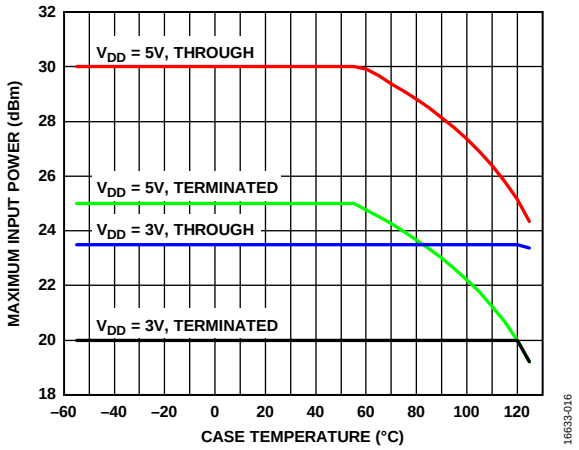

Figure 2. Maximum Input Power vs. Case Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

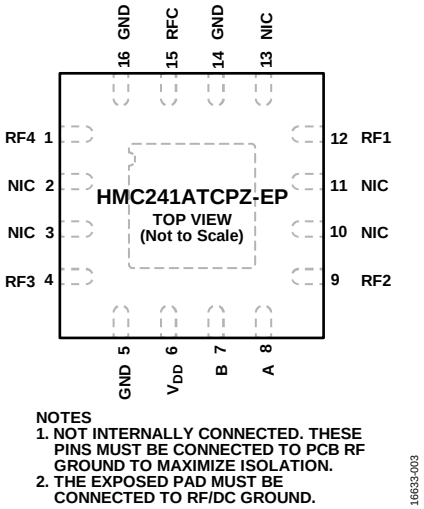

Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RF4	RF Port 4. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
2, 3, 10, 11, 13	NIC	Not Internally Connected. These pins must be connected to the printed circuit board (PCB) RF ground to maximize isolation.
4	RF3	RF Port 3. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
5, 14, 16	GND	Ground. The package bottom has an exposed metal pad that must connect to the PCB RF/dc ground.
6	V_{DD}	Supply Voltage.
7	B	Logic Control Input B. See Figure 5 for the control input interface schematic. See the recommended input control voltages range in Table 1 and the control voltage truth table (Table 4).
8	A	Logic Control Input A. See Figure 5 for the control input interface schematic. See the recommended input control voltages range in Table 1 and the control voltage truth table (Table 4).
9	RF2	RF Port 2. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
12	RF1	RF Port 1. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
15	RFC	RF Common Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
	EPAD	Exposed Pad. The exposed pad must be connected to RF/dc ground.

Table 4. Control Voltage Truth Table

Digital Control Input		RF Paths			
CTRLA	CTRLB	RFC to RF1	RFC to RF2	RFC to RF3	RFC to RF4
Low	Low	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
High	Low	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
Low	High	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
High	High	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)

INTERFACE SCHEMATICS

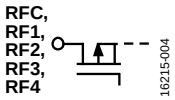

Figure 4. RFC to RF4 Interface Schematic

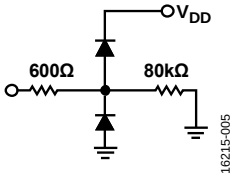

Figure 5. CTRLA and CTRLB Interface Schematic

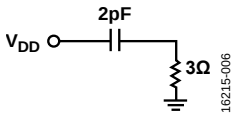

Figure 6. Supply Voltage Schematic

TYPICAL PERFORMANCE CHARCTERISTICS

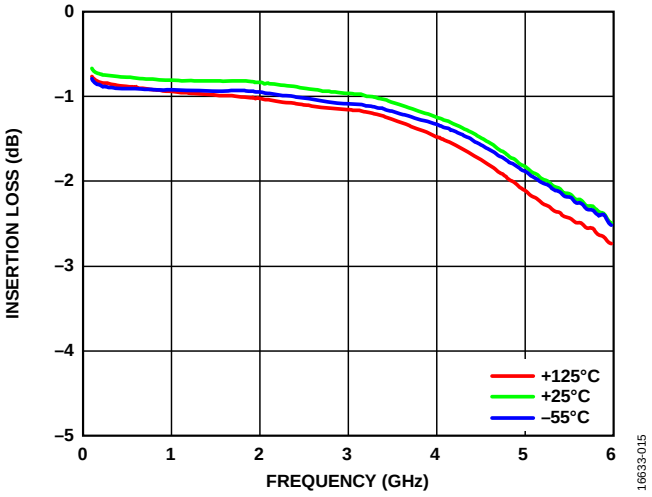

Figure 7. Insertion Loss Between RFC and RF1 vs. Frequency at Various Temperatures

OUTLINE DIMENSIONS

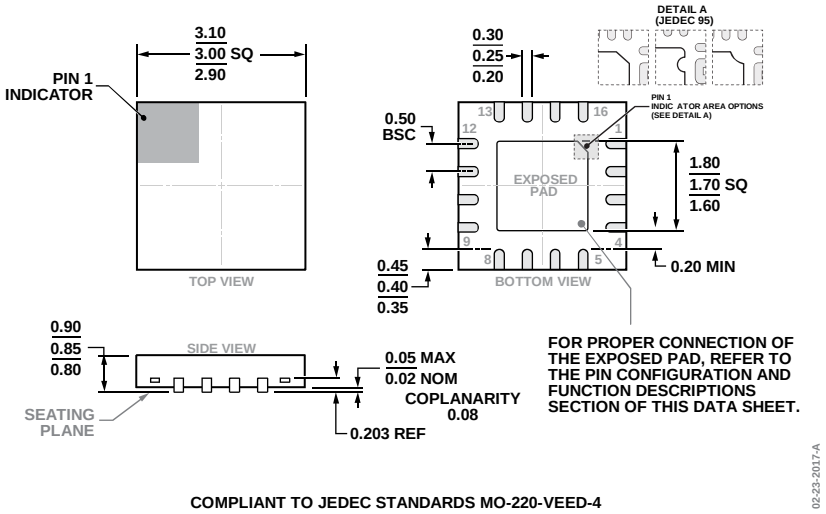

Figure 8. 16-Terminal Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.85 mm Package Height
(CP-16-51)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description	Package Option
HMC241ATCPZ-EP-PT	−55°C to +125°C	MSL3	16-Terminal Lead Frame Chip Scale Package [LFCSP]	CP-16-51
HMC241ATCPZ-EP-R7	−55°C to +125°C	MSL3	16-Terminal Lead Frame Chip Scale Package [LFCSP]	CP-16-51

[1] All models are RoHS compliant.
[2] See the Absolute Maximum Ratings section.

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