



InGaP HBT GAIN BLOCK MMIC AMPLIFIER, DC - 4.5 GHz

Typical Applications

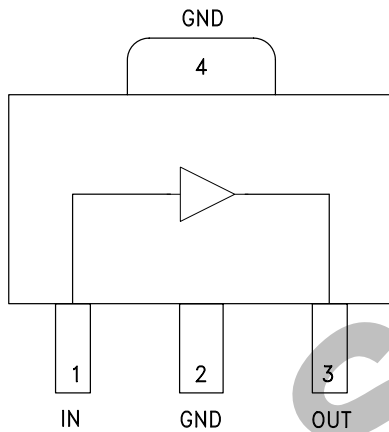
The HMC475ST89 / HMC475ST89E is an ideal RF/IF gain block & LO or PA driver:

- Cellular / PCS / 3G
- Fixed Wireless & WLAN
- CATV, Cable Modem & DBS
- Microwave Radio & Test Equipment
- IF and RF Applications

Features

- P1dB Output Power: +22 dBm
- Gain: 21.5 dB
- Output IP3: +35 dBm
- Cascadable 50 Ohm I/Os
- Single Supply: +8V to +12V
- Industry Standard SOT89 Package

Functional Diagram



General Description

The HMC475ST89(E) is a InGaP Heterojunction Bipolar Transistor (HBT) Gain Block MMIC SMT amplifier covering DC to 4.5 GHz. Packaged in an industry standard SOT89, the amplifier can be used as a cascadable 50 Ohm RF/IF gain stage as well as a LO or PA driver with up to +25 dBm output power. The HMC475ST89(E) offers 21.5 dB of gain and +35 dBm output IP3 at 850 MHz while requiring only 110 mA from a single positive supply. The Darlington topology results in reduced sensitivity to normal process variations and excellent gain stability over temperature while requiring a minimal number of external bias components.

Electrical Specifications, $V_s = 8.0$ V, $R_{bias} = 9.1$ Ohm, $T_A = +25^\circ$ C

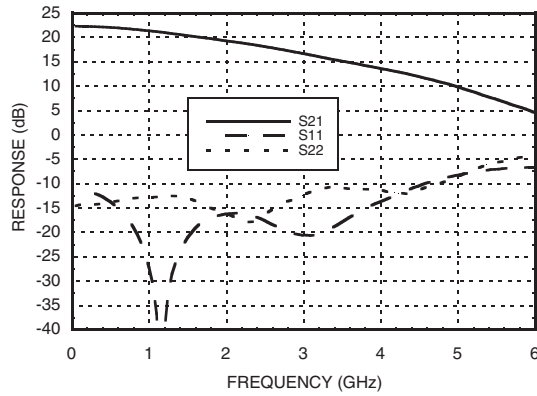
| Parameter | Min. | Typ. | Max. | Units | |
|---|---------------|------|-------|-------|--------|
| Gain | DC - 1.0 GHz | 19.5 | 21.5 | dB | |
| | 1.0 - 2.0 GHz | 17.5 | 19.5 | dB | |
| | 2.0 - 3.0 GHz | 14.5 | 16.5 | dB | |
| | 3.0 - 4.0 GHz | 11.5 | 13.5 | dB | |
| | 4.0 - 4.5 GHz | 9 | 12 | dB | |
| Gain Variation Over Temperature | DC - 4.5 GHz | | 0.008 | 0.012 | dB/ °C |
| Input Return Loss | DC - 1.0 GHz | | 11 | | dB |
| | 1.0 - 2.0 GHz | | 14 | | dB |
| | 2.0 - 4.5 GHz | | 14 | | dB |
| Output Return Loss | DC - 1.0 GHz | | 13 | | dB |
| | 1.0 - 4.5 GHz | | 10 | | dB |
| Reverse Isolation | DC - 4.5 GHz | | 25 | | dB |
| Output Power for 1 dB Compression (P1dB) | DC - 1.0 GHz | 19.0 | 22.0 | | dBm |
| | 1.0 - 2.0 GHz | 18.0 | 21.0 | | dBm |
| | 2.0 - 3.0 GHz | 17.5 | 19.5 | | dBm |
| | 3.0 - 4.0 GHz | 13.0 | 16.0 | | dBm |
| | 4.0 - 4.5 GHz | 11.0 | 14.0 | | dBm |
| Output Third Order Intercept (IP3) (Pout= 0 dBm per tone, 1 MHz spacing) | DC - 2.5 GHz | | 35 | | dBm |
| | 2.5 - 4.5 GHz | | 30 | | dBm |
| Noise Figure | DC - 3.0 GHz | | 3.5 | | dB |
| | 3.0 - 4.5 GHz | | 3.8 | | dB |
| Supply Current (Icq) | | | 110 | 135 | mA |

Note: Data taken with broadband bias tee on device output.

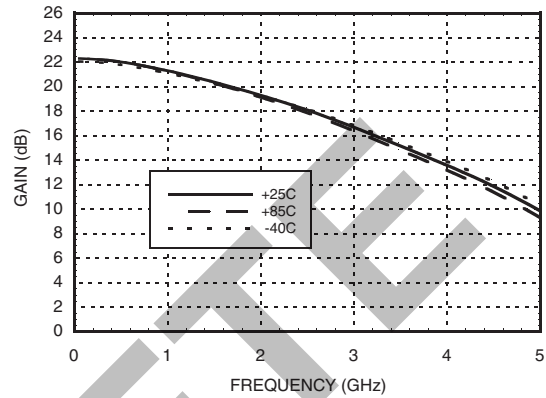


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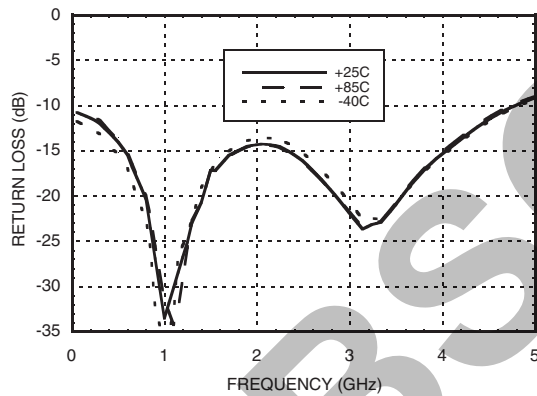
Broadband Gain & Return Loss



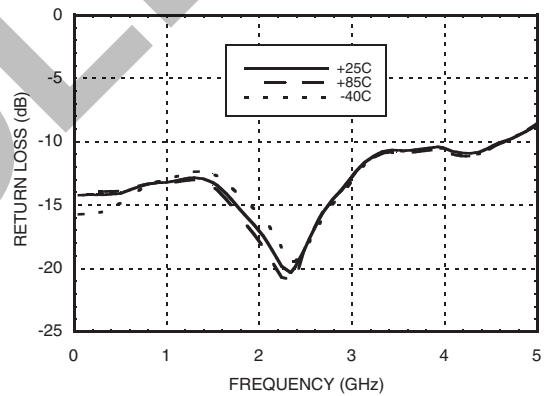
Gain vs. Temperature



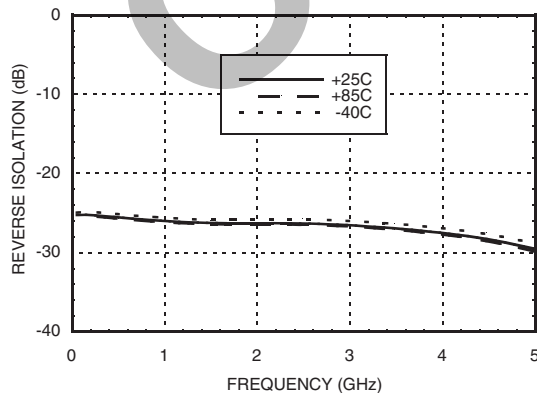
Input Return Loss vs. Temperature



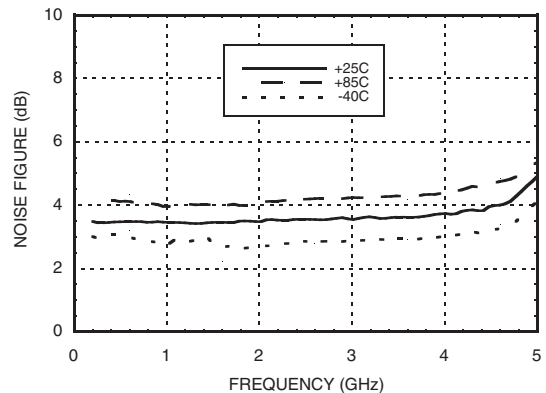
Output Return Loss vs. Temperature



Reverse Isolation vs. Temperature



Noise Figure vs. Temperature



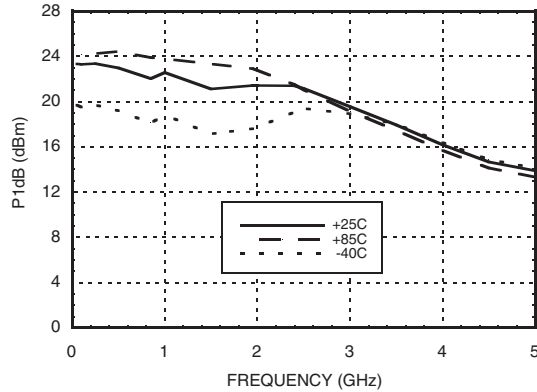
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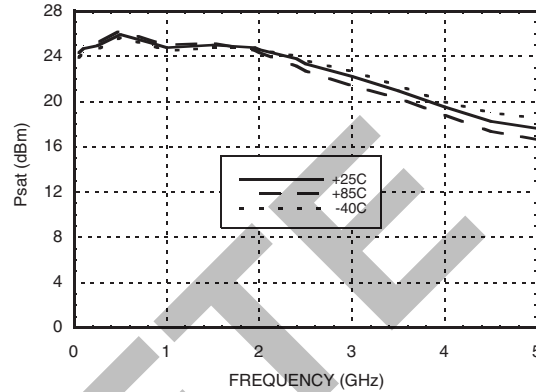


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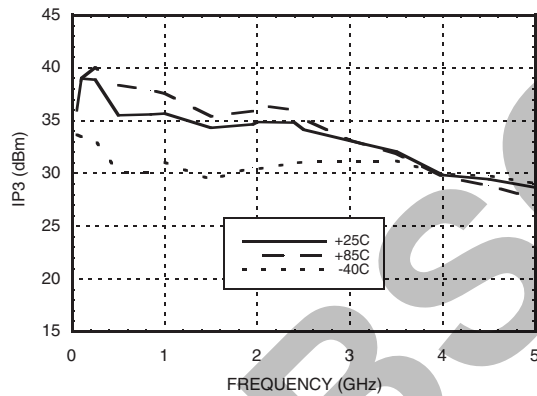
P1dB vs. Temperature



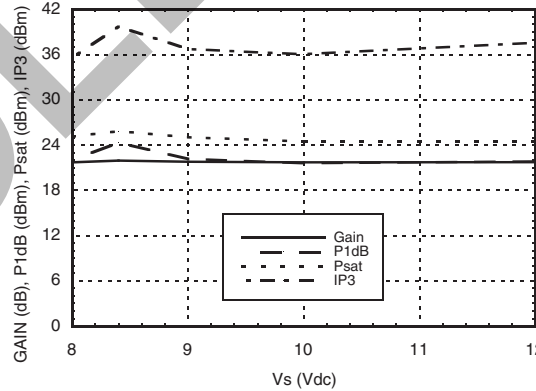
Psat vs. Temperature



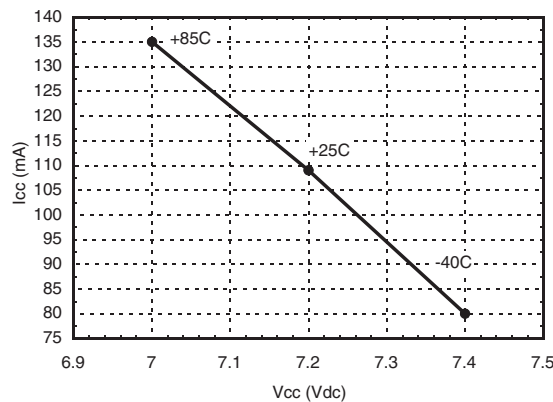
Output IP3 vs. Temperature



**Gain, Power & OIP3 vs. Supply Voltage
for Constant Icc= 110 mA @ 850 MHz**



**Vcc vs. Icc Over Temperature for
Fixed Vs= 8V, RBIAS= 9.1 Ohms**



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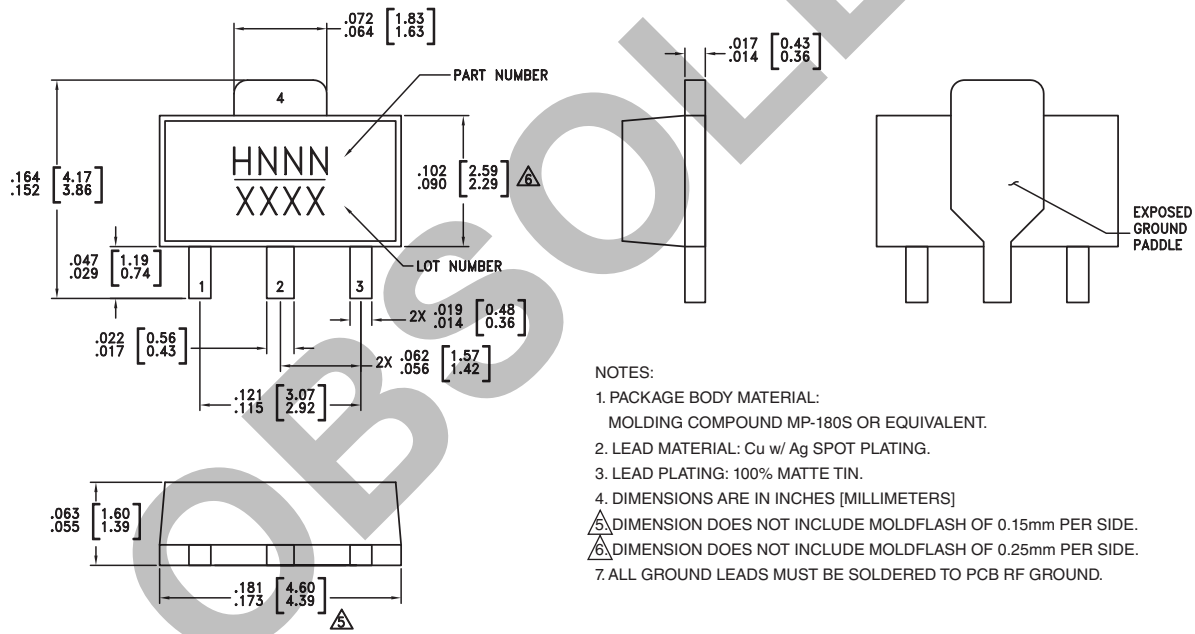
Absolute Maximum Ratings

| | |
|--|----------------|
| Collector Bias Voltage (Vcc) | +8.0 Vdc |
| RF Input Power (RFIN)(Vcc = +7.2 Vdc) | +17 dBm |
| Junction Temperature | 150 °C |
| Continuous Pdiss (T = 85 °C) (derate 16.86 mW/°C above 85 °C) | 1.09 W |
| Thermal Resistance (junction to lead) | 59.3 °C/W |
| Storage Temperature | -65 to +150 °C |
| Operating Temperature | -40 to +85 °C |



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



Package Information

| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking ^[3] |
|-------------|--|---------------|---------------------|--------------------------------|
| HMC475ST89 | Low Stress Injection Molded Plastic | Sn/Pb Solder | MSL1 ^[1] | H475 XXXX |
| HMC475ST89E | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1 ^[2] | H475 XXXX |

[1] Max peak reflow temperature of 235 °C

[2] Max peak reflow temperature of 260 °C

[3] 4-Digit lot number XXXX

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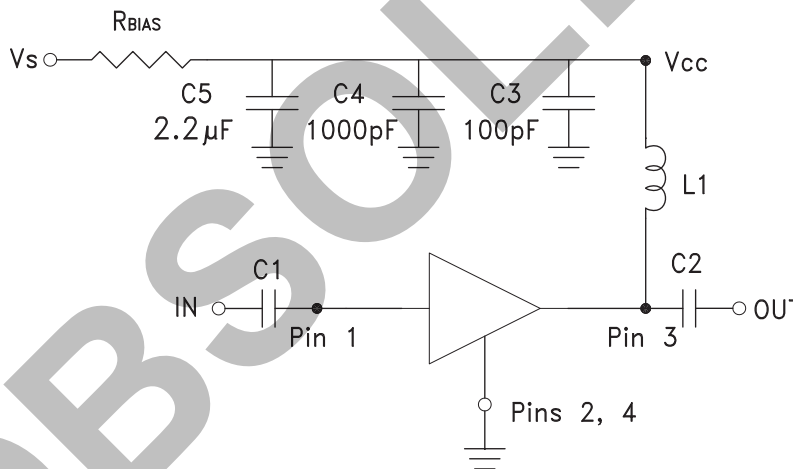
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Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|------------|----------|---|---------------------|
| 1 | IN | This pin is DC coupled. An off chip DC blocking capacitor is required. | |
| 3 | OUT | RF output and DC Bias (Vcc) for the output stage. | |
| 2, 4 | GND | These pins and package bottom must be connected to RF/DC ground. | |

Application Circuit



Recommended Bias Resistor Values for $I_{cc} = 110 \text{ mA}$, $R_{bias} = (V_s - V_{cc}) / I_{cc}$

| Supply Voltage (Vs) | 8V | 9V | 10V | 12V |
|---------------------|--------------|-------------|-------------|-------------|
| RBIAS VALUE | 9.1 Ω | 18 Ω | 27 Ω | 43 Ω |
| RBIAS POWER RATING | ¼ W | ½ W | ½ W | 1 W |

Note:

- External blocking capacitors are required on RFIN and RFOUT.
- RBIAS provides DC bias stability over temperature.

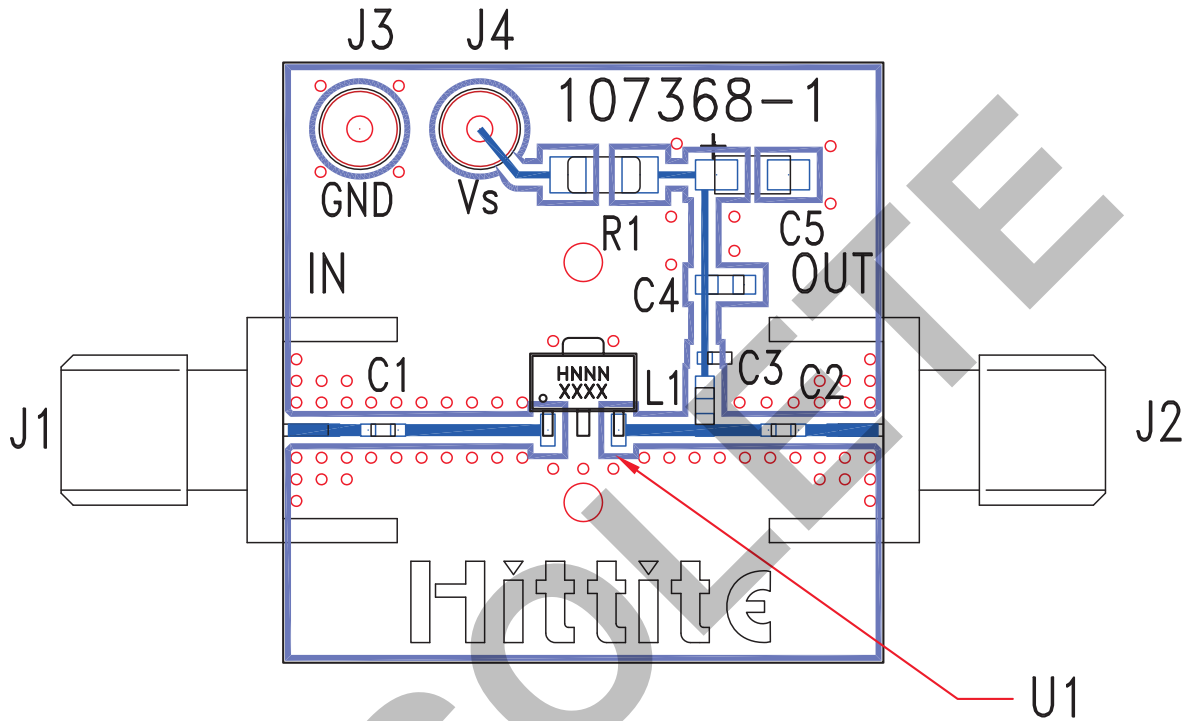
Recommended Component Values for Key Application Frequencies

| Component | Frequency (MHz) | | | | | | |
|-----------|--------------------|--------|--------|--------|--------|--------|--------|
| | 50 | 900 | 1900 | 2200 | 2400 | 3500 | 4500 |
| L1 | 270 nH | 56 nH | 18 nH | 18 nH | 15 nH | 8.2 nH | 6.8 nH |
| C1, C2 | 0.01 μF | 100 pF | 100 pF | 100 pF | 100 pF | 100 pF | 100 pF |



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Evaluation PCB



List of Materials for Evaluation PCB 116092 [1]

| Item | Description |
|---------|---------------------------------|
| J1 - J2 | PCB Mount SMA Connector |
| J3 - J4 | DC Pin |
| C1, C2 | Capacitor, 0402 Pkg. |
| C3 | 100 pF Capacitor, 0402 Pkg. |
| C4 | 1000 pF Capacitor, 0603 Pkg. |
| C5 | 2.2 μ F Capacitor, Tantalum |
| R1 | Resistor, 1206 Pkg. |
| L1 | Inductor, 0603 Pkg. |
| U1 | HMC475ST89 / HMC475ST89E |
| PCB [2] | 107368 Evaluation PCB |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and package bottom should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.

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