## FEATURES

Broadband frequency range: 0.1 GHz to 20 GHz
Nonreflective $\mathbf{5 0 \Omega}$ design

High isolation: $\mathbf{4 0} \mathbf{d B}$ up $\mathbf{2 0 ~ G H z}$
High input linearity at $\mathbf{2 5 0} \mathbf{~ M H z}$ to 20 GHz
P1dB: 24 dBm typical, $\mathrm{V}_{\text {ss }}=-5 \mathrm{~V}$
IP3: 41 dBm typical
High power handling, $\mathrm{V}_{\mathrm{ss}}=-5 \mathrm{~V}$
26.5 dBm through path

23 dBm terminated path
Integrated 2 to 4 line decoder
24-lead, $4 \mathrm{~mm} \times 4 \mathrm{~mm}$ LFCSP
ESD sensitivity, HBM: 250 V (Class 1A)

## ENHANCED PRODUCT FEATURES

## Supports defense and aerospace applications (AQEC standard) <br> Military temperature range: $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ <br> Controlled manufacturing baseline <br> One assembly/test site <br> One fabrication site <br> Enhanced product change notification <br> Qualification data available on request

## APPLICATIONS

## Test instrumentation

Microwave radios and very small aperture terminals (VSATs)
Military radios, radars, and electronic counter measures (ECMs)
Broadband telecommunications systems

## GENERAL DESCRIPTION

The HMC641ATCPZ-EP is a general-purpose, nonreflective, single-pole, four-throw (SP4T) switch manufactured using a gallium arsenide (GaAs) process. This switch offers high isolation, low insertion loss, and on-chip termination of the isolated ports.

The switch operates with a negative supply voltage range of -5 V to -3 V and requires two negative logic control voltages.

## FUNCTIONAL BLOCK DIAGRAM

HMC641ATCPZ-EP


Figure 1.

The HMC641ATCPZ includes an on-chip, binary 2 to 4 line decoder that provides logic control from two logic input lines.

The HMC641ATCPZ comes in a 24 -lead, $4 \mathrm{~mm} \times 4 \mathrm{~mm}$ LFCSP and operates from 0.1 GHz to 20 GHz .
Additional application and technical information can be found in the HMC641ALP4E data sheet.

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## REVISION HISTORY

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8/2017—Revision 0: Initial Version
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## Enhanced Product

## SPECIFICATIONS

$\mathrm{V}_{\text {SS }}=-3 \mathrm{~V}$ or -5 V , control voltage $\left(\mathrm{V}_{\text {CTRL }}\right)=0 \mathrm{~V}$ or $\mathrm{V}_{\text {SS }}$, case temperature $\left(\mathrm{T}_{\text {CASE }}\right)=25^{\circ} \mathrm{C}$, and $50 \Omega$ system, unless otherwise noted.
Table 1.

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| FREQUENCY RANGE | f |  | 0.1 |  | 20 | GHz |
| INSERTION LOSS <br> Between RFC and RF1 to RF4 (On) |  | 0.1 GHz to 12 GHz <br> 12 GHz to 20 GHz |  | $\begin{aligned} & 2.0 \\ & 3.0 \end{aligned}$ |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \end{aligned}$ |
| ISOLATION <br> Between RFC and RF1 to RF4 (Off) |  | 0.1 GHz to 12 GHz <br> 12 GHz to 20 GHz |  | $\begin{aligned} & 42 \\ & 40 \end{aligned}$ |  | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \end{aligned}$ |
| RETURN LOSS <br> RFC and RF1 to RF4 (On) <br> RF1 to RF4 (Off) |  | 0.1 GHz to 12 GHz <br> 12 GHz to 20 GHz <br> 0.1 GHz to 20 GHz |  | $\begin{aligned} & 18 \\ & 17 \\ & 13 \end{aligned}$ |  | dB <br> dB <br> dB |
| SWITCHING Rise Time and Fall Time On Time and Off Time | $\mathrm{t}_{\text {RISE, }} \mathrm{t}_{\text {fall }}$ <br> ton, toff | $10 \%$ to $90 \%$ of radio frequency (RF) output $50 \% \mathrm{~V}_{\text {ctRL }}$ to $90 \%$ of RF output |  | $\begin{aligned} & 30 \\ & 100 \end{aligned}$ |  | $\begin{aligned} & \mathrm{ns} \\ & \mathrm{~ns} \end{aligned}$ |
| INPUT LINEARITY ${ }^{1}$ <br> 1 dB Power Compression <br> Third-Order Intercept | P1dB <br> IP3 | $\begin{aligned} & 250 \mathrm{MHz} \text { to } 20 \mathrm{GHz} \\ & \mathrm{~V}_{\mathrm{ss}}=-5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{ss}}=-3 \mathrm{~V} \end{aligned}$ <br> 10 dBm per tone, 1 MHz spacing $\begin{aligned} & \mathrm{V}_{\mathrm{ss}}=-5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{ss}}=-3 \mathrm{~V} \end{aligned}$ | 20 | $\begin{aligned} & 24 \\ & 22 \\ & 41 \\ & 41 \end{aligned}$ |  | dBm <br> dBm <br> dBm <br> dBm |
| SUPPLY <br> Voltage Current | $\begin{aligned} & \mathrm{V}_{\mathrm{ss}} \\ & \mathrm{I} s \mathrm{ss} \end{aligned}$ | $\mathrm{V}_{\text {ss }} \mathrm{pin}$ | -5 |  | $\begin{aligned} & -3 \\ & 5 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~mA} \end{aligned}$ |
|  | $V_{\text {Ctrl }}$ <br> $\mathrm{V}_{\mathrm{INL}}$ <br> $\mathrm{V}_{\text {INH }}$ <br> $I_{\text {ctrl }}$ <br> IINL <br> Inn | CTRLA and CTRLB pins $\begin{aligned} & \mathrm{V}_{\mathrm{ss}}=-5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{ss}}=-3 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{ss}}=-5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{ss}}=-3 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & -3 \\ & -1 \\ & -5 \\ & -3 \end{aligned}$ | $\begin{aligned} & 30 \\ & 0.5 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & -4.2 \\ & -2.2 \end{aligned}$ | $\begin{aligned} & \mathrm{V} \\ & \mathrm{~V} \\ & \mathrm{~V} \\ & \mathrm{~V} \\ & \mu \mathrm{~A} \\ & \mu \mathrm{~A} \end{aligned}$ |

[^1]
## ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.
Table 2.

| Parameter | Rating |
| :---: | :---: |
| Negative Supply Voltage (Vss) | -7V |
| Digital Control Input Voltage | $\mathrm{V}_{5 s}-0.5 \mathrm{~V}$ to +1 V |
| RF Input Power ${ }^{1}$ ( $\mathrm{f}=250 \mathrm{MHz}$ to 20 GHz , $\left.\mathrm{T}_{\text {CASE }}=85^{\circ} \mathrm{C}\right)$ |  |
| $\mathrm{V}_{\text {SS }}=-5 \mathrm{~V}$ |  |
| Through Path | 26.5 dBm |
| Terminated Path | 23 dBm |
| Hot Switching | 20 dBm |
| $\mathrm{V}_{\text {SS }}=-3 \mathrm{~V}$ |  |
| Through Path | 21 dBm |
| Terminated Path | 20 dBm |
| Hot Switching | 17 dBm |
| Temperature |  |
| Junction, $\mathrm{T}_{\text {J }}$ | $150^{\circ} \mathrm{C}$ |
| Case, Case $^{\text {a }}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| Storage | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Reflow (MSL3 Rating) ${ }^{2}$ | $260^{\circ} \mathrm{C}$ |
| Junction to Case Thermal Resistance, $\theta_{\text {J }}$ |  |
| Through Path | $201^{\circ} \mathrm{C} / \mathrm{W}$ |
| Terminated Path | $321^{\circ} \mathrm{C} / \mathrm{W}$ |
| Electrostatic Discharge (ESD) Sensitivity Human Body Model (HBM) | 250 V (Class 1A) |

${ }^{1}$ For power derating at frequencies less than 250 MHz , see Figure 2, and for the maximum input power vs. the case temperature, see Figure 3.
${ }^{2}$ See the Ordering Guide section.
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## POWER DERATING CURVES

Figure 2 shows power derating vs. frequency at $<250 \mathrm{MHz}$, and Figure 3 shows the maximum power dissipation vs. the case temperature.


Figure 2. Power Derating at Frequencies Less than 250 MHz


Figure 3. Maximum Input Power vs. Case Temperature ( $T_{\text {CASE }}$ )

## ESD CAUTION

 ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

|  |  |  |
| :---: | :---: | :---: |
|  | O |  |
| NIC | 1) ,------------18 | NIC |
| GND | 2) HMC641ATCPZ-EP ${ }^{17}$ | GND |
| RFC | 3) $\mathrm{HMC641ATCPZ-EP}{ }_{16}$ | CTRLA |
| GND | 4) (Not to Scale) 15 | CTRLB |
| NIC | 5) 14 | $\mathrm{V}_{\text {SS }}$ |
| NIC | 6) ------------13 | NIC |
|  |  |  |
|  |  |  |

NOTES

1. NIC = NOT INTERNALLY CONNECTED. THE PINS ARE NOT CONNECTED INTERNALLY; HOWEVER, ALL DATA SHOWN IN THIS DATA SHEET IS MEASURED WITH THESE PINS CONNECTED TO RF/DC GROUND
2. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO THE RF/DC GROUND OF THE PCB.

Figure 4. Pin Configuration
Table 3. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
| :---: | :---: | :---: |
| 1,5,6,13, 18 | NIC | Not Internally Connected. The pins are not connected internally; however, all data shown in this data sheet is measured with these pins connected to RF/dc ground externally. |
| $\begin{aligned} & 2,4,7,9,10,12,17 \\ & 19,21,22,24 \end{aligned}$ | GND | Ground. These pins must be connected to the RF/dc ground of the printed circuit board (PCB). |
| 3 | RFC | RF Common Port. This pin is dc-coupled and matched to $50 \Omega$. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc . See Figure 5 for the interface schematic. |
| 8 | RF4 | RF4 Port. This pin is dc-coupled and matched to $50 \Omega$. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc . See Figure 5 for the interface schematic. |
| 11 | RF3 | RF3 Port. This pin is dc-coupled and matched to $50 \Omega$. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc . See Figure 5 for the interface schematic. |
| 14 | Vss | Negative Supply Voltage Pin. See Figure 6 for the interface schematic. |
| 15 | CTRLB | Control Input 2 Pin. See Table 4 for the control voltage truth table. See Figure 6 for the interface schematic. |
| 16 | CTRLA | Control Input 1 Pin. See Table 4 for the control voltage truth table. See Figure 6 for the interface schematic. |
| 20 | RF2 | RF2 Port. This pin is dc-coupled and matched to $50 \Omega$. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc . See Figure 5 for the interface schematic. |
| 23 | RF1 | RF1 Port. This pin is dc-coupled and matched to $50 \Omega$. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc . See Figure 5 for the interface schematic. |
|  | EPAD | Exposed Pad. The exposed pad must be connected to the RF/dc ground of the PCB. |

## INTERFACE SCHEMATICS



Figure 5. RFC to RF4 Interface Schematic


Figure 6. CTRLA, CTRLB, and Vss Interface Schematic

## TRUTH TABLE

Table 4. Control Voltage Truth Table

| Digital Control Input |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- |
| RF Paths |  |  |  |  |  |
| CTRLA | CTRLB | RFC to RF1 | RFC to RF2 | RFC to RF3 | RFC to RF4 |
| High | High | Insertion loss (on) | Isolation (off) | Isolation (off) | Isolation (off) |
| Low | High | Isolation (off) | Insertion loss (on) | Isolation (off) | Isolation (off) |
| High | Low | Isolation (off) | Isolation (off) | Insertion loss (on) | Isolation (off) |
| Low | Low | Isolation (off) | Isolation (off) | Isolation (off) | Insertion loss (on) |

## TYPICAL PERFORMANCE CHARCTERISTICS



Figure 7. Insertion Loss Between RFC and RF1 vs. Frequency for Various Temperatures

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-8.
Figure 8. 24-Lead Lead Frame Chip Scale Package [LFCSP]
$4 \mathrm{~mm} \times 4 \mathrm{~mm}$ Body and 0.85 mm Package Height (CP-24-22)
Dimensions shown in millimeters

## ORDERING GUIDE

| Model $^{1}$ | Temperature Range | MSL <br> Rating <br>  | Package Description | Package <br> Option |
| :--- | :--- | :--- | :--- | :--- |
| HMC641ATCPZ-EP-PT | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | MSL3 | 24-Lead Lead Frame Chip Scale Package [LFCSP] | CP-24-22 |
| HMC641ATCPZ-EP-RL7 | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | MSL3 | 24-Lead Lead Frame Chip Scale Package [LFCSP] | CP-24-22 |

${ }^{1} Z=$ RoHS Compliant Part.
${ }^{2}$ See the Absolute Maximum Ratings section.

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[^1]:    ${ }^{1}$ Input linearity performance degrades at frequencies less than 250 MHz .

