BiCMOS MMIC 5-BIT DIGITAL VARIABLE GAIN AMPLIFIER, 30 - 400 MHz

Typical Applications

The HMC680LP4(E) is ideal for:

- Cellular/3G Infrastructure
- WiBro / WiMAX / 4G
- Microwave Radio & VSAT
- Test Equipment and Sensors
- IF & RF Applications

Features

TTL/CMOS compatible parallel or latched parallel control interface

High Output IP3: +40 dBm (At all gain settings)

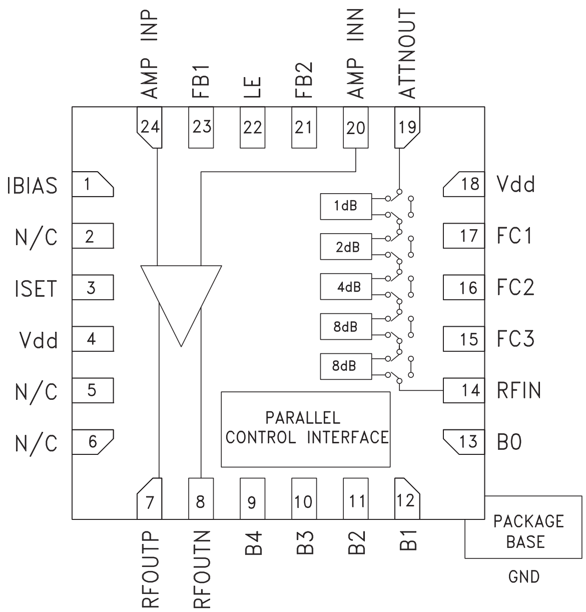
Low Noise Figure: 5 dB

Wide Gain Control Range: 23 dB

24 Lead 4x4 mm SMT Package: 16 mm²

Excellent State & Step Accuracy (±0.05 dB)

Functional Diagram



General Description

The HMC680LP4(E) is a digitally controlled variable gain amplifier which operates from 30 to 400 MHz, and can be programmed to provide -4 dB to +19 dB of gain, in 1 dB steps. The HMC680LP4(E) delivers noise figure of 5 dB in its maximum gain state, with output IP3 of up to +40 dBm in any state. This high linearity DVGA also provides a differential RF output which can be used to interface directly with SAW filters in Tx and Rx applications, and with digital to analog converters in Rx chains. The HMC680LP4(E) is housed in a RoHS compliant 4x4 mm QFN leadless package, and is CMOS/ TTL compatible.

Electrical Specifications, T_A = +25° C, 50 Ohm System, Vdd = +5V

Parameter	Min.	Typ.	Max.	Units
Frequency Range		30 - 400		MHz
Gain (Maximum Gain State)	17	19		dB
Gain Control Range		23		dB
Input Return Loss		12		dB
Output Return Loss		13		dB
Gain Accuracy: (Referenced to Maximum Gain State) All Gain States		± (0.15 + 3% of Gain Setting) Max.		dB
Output Power for 1dB Compression	23	25		dBm
Output Third Order Intercept Point (Two-Tone Output Power= +5 dBm Each Tone) [1]		40		dBm
Output Second Order Intercept Point (Two-Tone Output Power= +5 dBm Each Tone) [1]		65		dBm
Harmonics 2nd Order 3rd Order		70 75		dBc dBc
Step Accuracy (Referenced to Maximum Gain State)		±0.2		dB
Noise Figure (max gain state)		5		dB
Switching Characteristics tRise, tFall (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)		11 13		ns ns
Control Supply Current Idd		4	5	mA
Amp Supply Current (RFOUTP)		122	135	mA
Amp Supply Current (RFOUTN)		122	135	mA

[1] Test frequency 50 MHz

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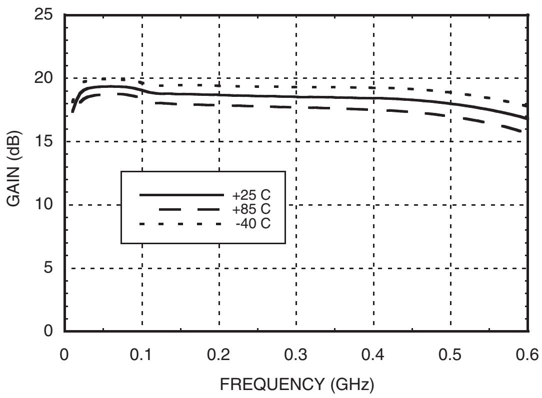
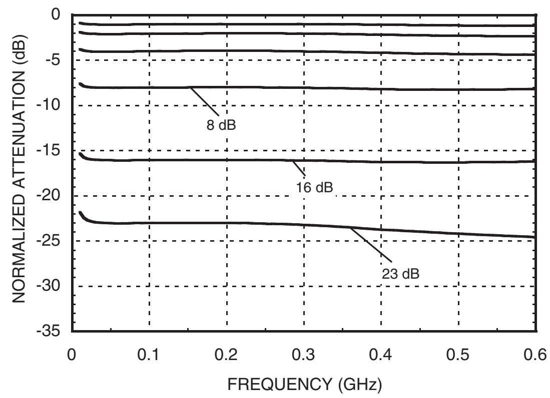
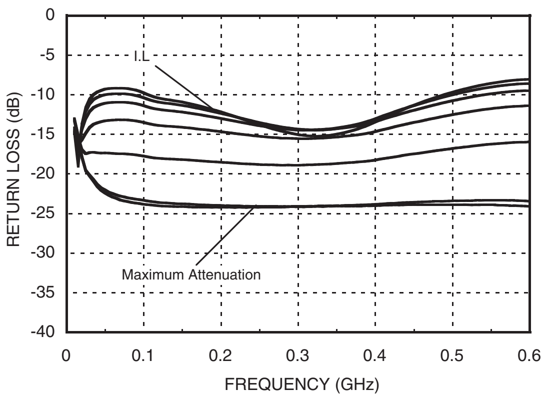
Maximum Gain vs. Frequency



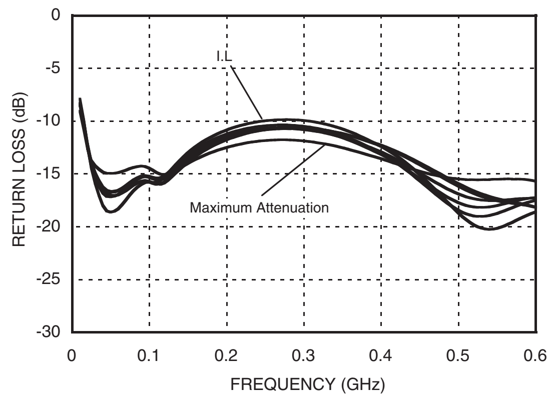
Normalized Attenuation
(Only Major States are Shown)



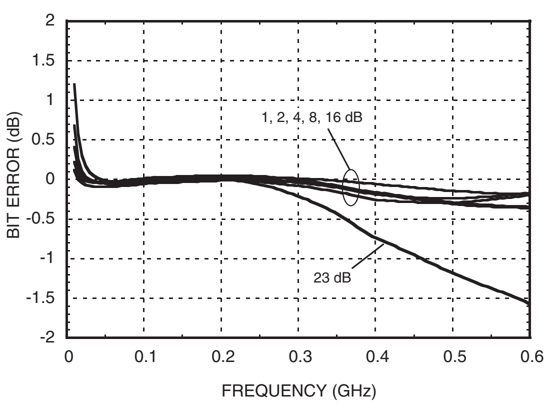
Input Return Loss
(Only Major States are Shown)



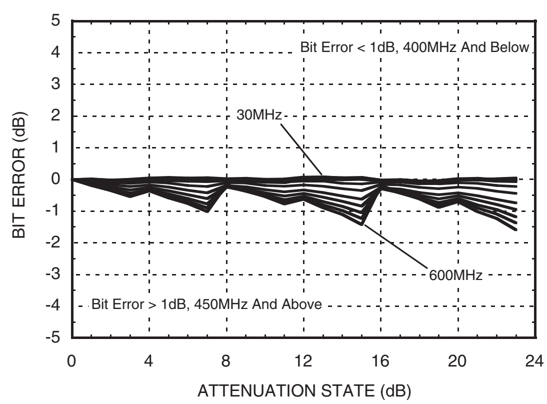
Output Return Loss
(Only Major States are Shown)



Bit Error vs. Frequency
(Only Major States are Shown)



Bit Error vs. Attenuation State



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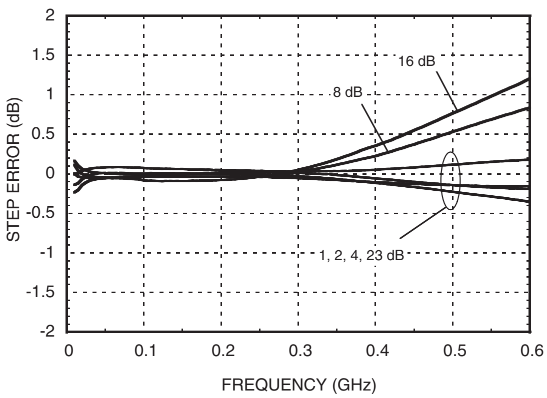
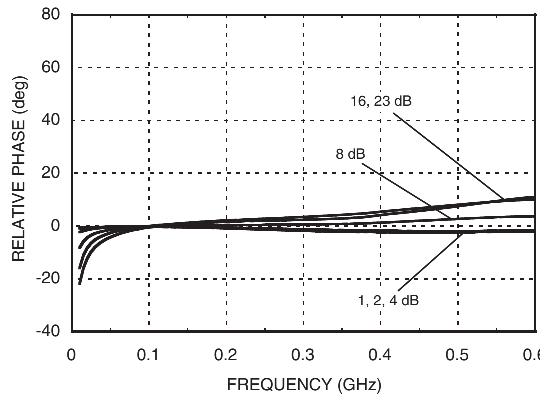
Step Accuracy vs. Frequency



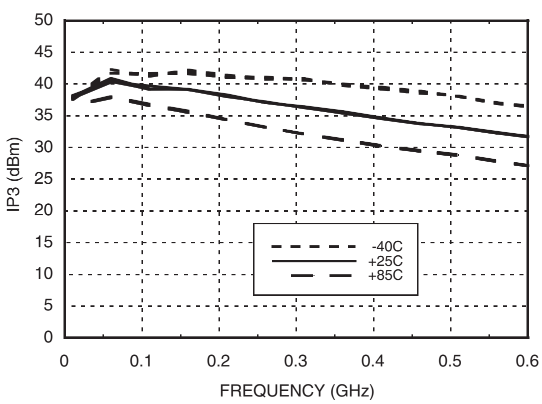
Relative Phase vs. Frequency

(Only Major States are Shown)

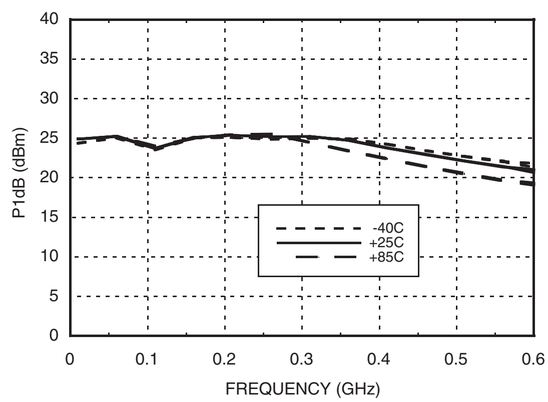


Output IP3 vs. Temperature

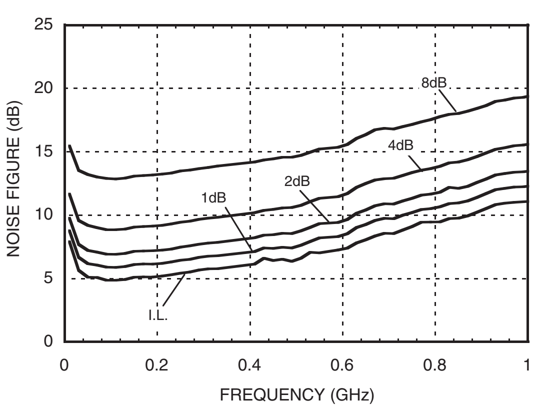
(+5 dBm Output Power Per Tone)



Output P1dB vs. Temperature

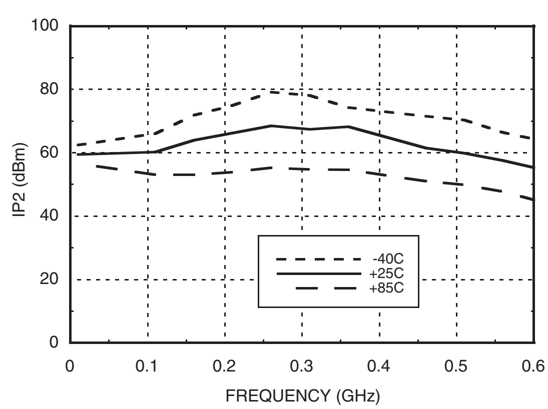


Noise Figure vs. Attenuation State



Output IP2 vs. Temperature

(+5 dBm Output Power Per Tone)



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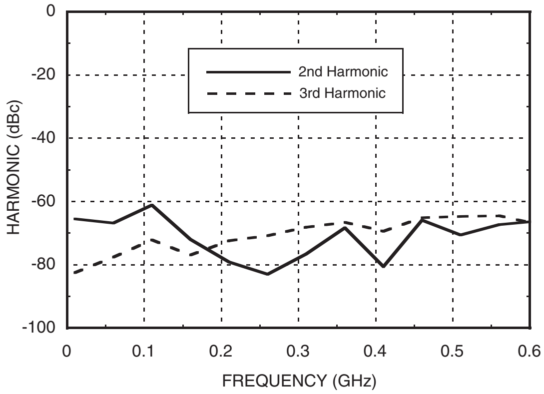
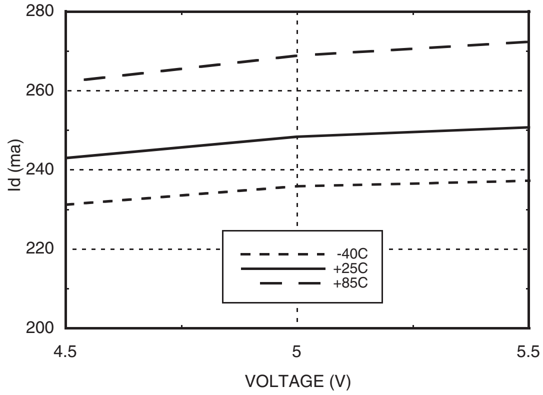
Harmonics vs. Frequency



Supply Current vs. Temperature



Absolute Maximum Ratings

RF Input Power	20 dBm
RF Output Power	22 dBm
Digital Inputs (B0-B4, Latch Enable)	-0.5 to Vdd +0.5V
Bias Voltage (Vdd)	5.6 V
Channel Temperature	125 °C
Continuous Pdiss (T = 85 °C) (derate 42 mW/°C above 85 °C)	1.7 W
Thermal Resistance (channel to ground paddle)	24 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Truth Table

ATTENUATION (dB)	B4[1]	B3[1]	B2	B1	B0
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	X	0	0	0
17	1	X	0	0	1
18	1	X	0	1	0
19	1	X	0	1	1
20	1	X	1	0	0
21	1	X	1	0	1
22	1	X	1	1	0
23	1	X	1	1	1

[1] Enabling B4 disables B3, the minimum attenuation is 16 dB

Amp Bias Voltage

Vdd $_{RF}$ (V)	Idd (Typ.) (mA)
5V	244

Control Voltage Table

State	Vdd = +3V	Vdd = +5V
Low	0 to 0.5V @ <1 µA	0 to 0.8V @ <1 µA
High	2 to 3V @ <1 µA	2 to 5V @ <1 µA

Control Interface:

The gain of HMC680LP4(E) is controlled by adjusting the state of the attenuator. The attenuator has a 5-bit parallel CMOS/TTL compatible interface. State of the attenuator can be set with respect to the truth table above.

Power on sequence:

The ideal power up sequence is: GND, Vdd, Digital inputs, RF inputs. Relative order of the digital inputs is not important as long as they are powered after VDD/GND.

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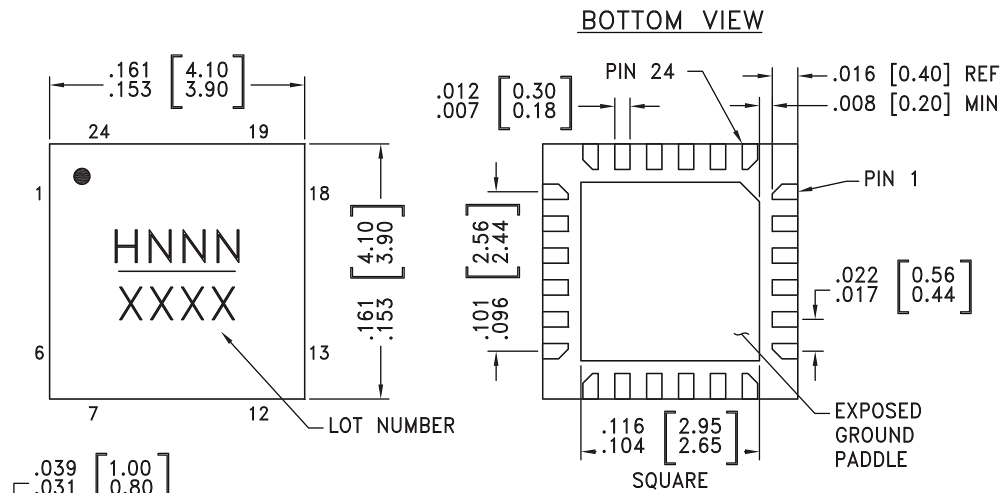
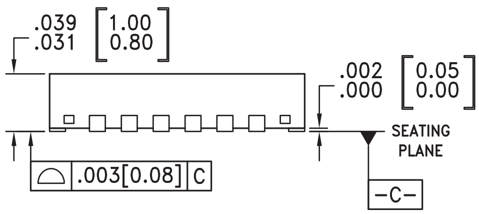
Outline Drawing





NOTES:
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC680LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H680 XXXX
HMC680LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H680 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

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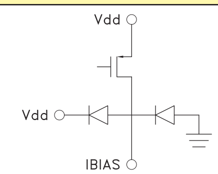
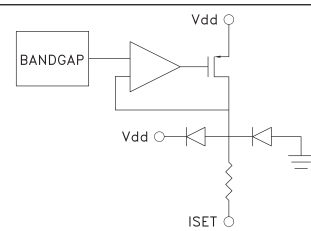
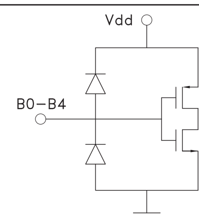
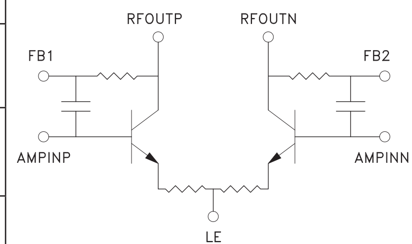
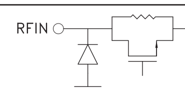
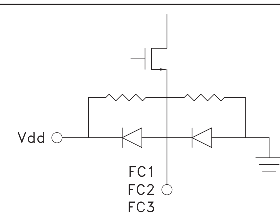
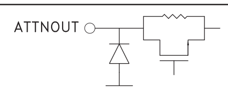
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	IBIAS	Bias current to amplifier. External inductors required.	
2, 5, 6, Package Bottom	N/C, GND	These pins and package bottom must be connected to RF/DC ground.	
3	ISET	External bias resistor to adjust the current of the amplifier.	
4, 18	Vdd	Power Supply	
9, 10, 11, 12, 13	B4 - B0	Control inputs to digital attenuator. See Truth Table & Control Voltage Table.	
7, 8	RFOUTP, RFOUTN	Balanced amplifier outputs. External components required	
20, 24	AMPINN, AMPINP	Balanced Amplifier inputs. External components required.	
21, 23	FB2, FB1	Feedback capacitance for the amplifier.	
22	LE	Common mode emitter inductor. The LE Pin requires high quality (less than 200mOhms resistance) inductor to ground. An inductance of 100nH is recommended.	
14	RFIN	RF input to digital attenuator. DC blocking capacitor required.	
15, 16, 17	FC3 - FC1	External capacitors to ground are required. Place these capacitors close to the package.	
19	ATTNOUT	RF output to digital attenuator. DC blocking capacitor required.	

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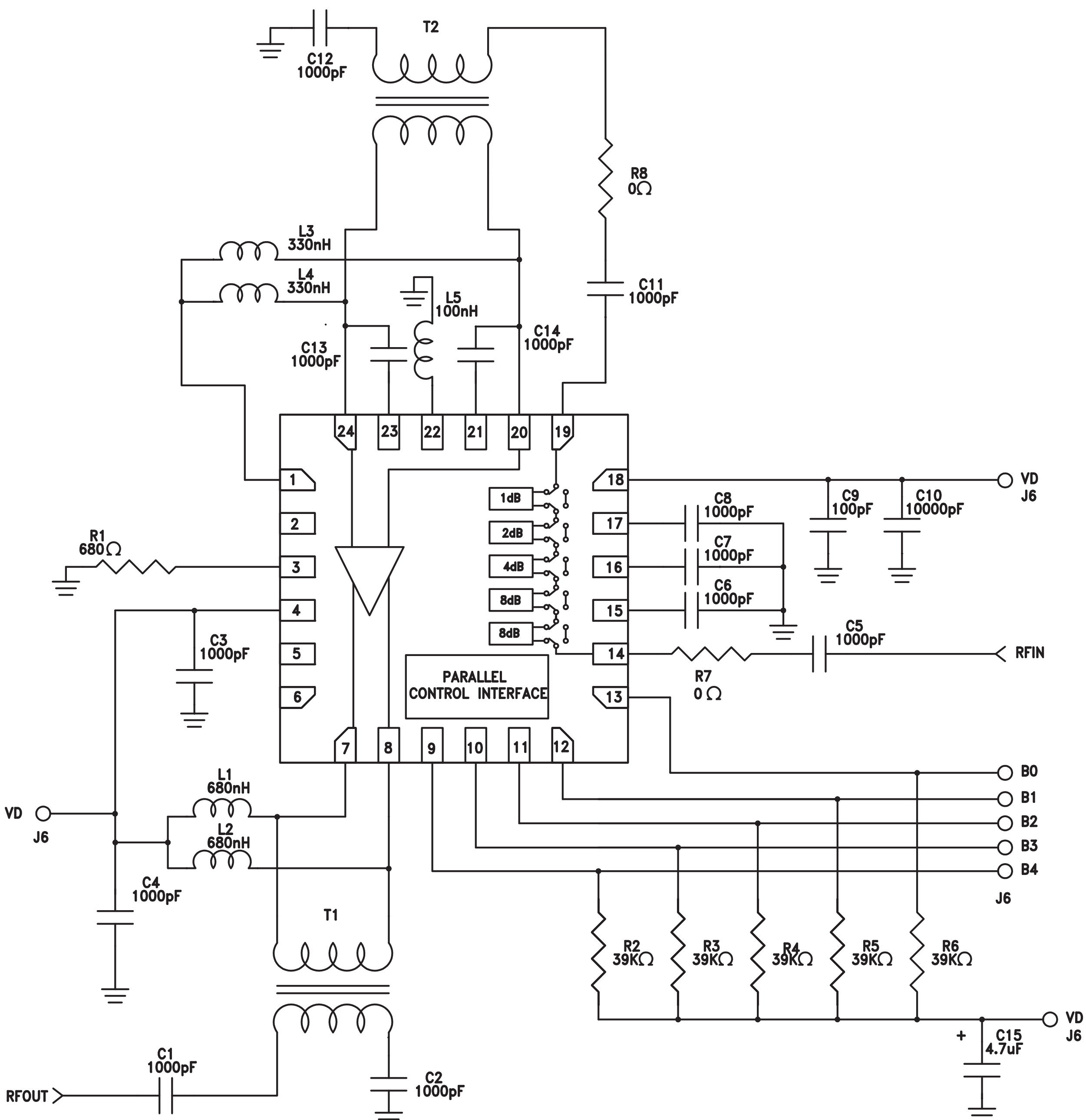
Application Circuit



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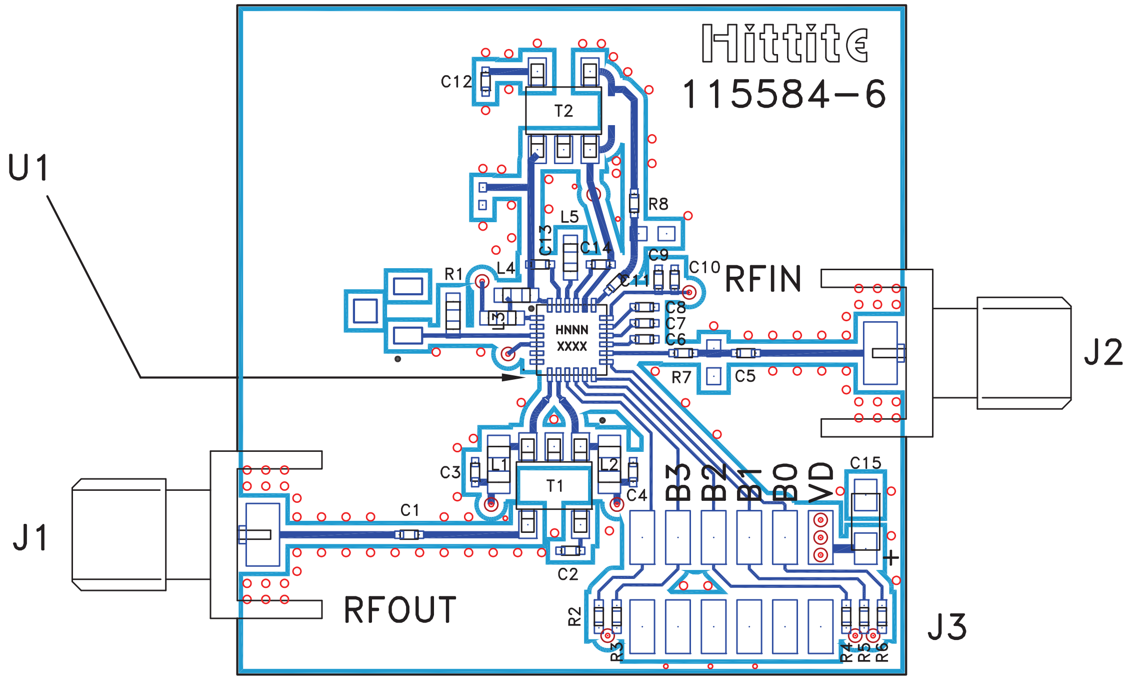
Evaluation PCB



List of Materials for Evaluation PCB 115585 [1]

Item	Description
J1 - J2	PCB Mount SMA Connector
J3	12 Pin DC Connector
C1 - C8, C11 - C14	1000 pF Capacitor, 0402 Pkg.
C9	100 pF Capacitor, 0402 Pkg.
C10	10k pF Capacitor, 0402 Pkg.
C15	4.7 μF Tantalum Capacitor, Case A Size
L1, L2	680 nH Inductor, 0805 Pkg.
L3, L4	330 nH Inductor, 0603 Pkg.
L5	100 nH Inductor, 0603 Pkg.
R1	680 Ohm Resistor, 0603 Pkg.
R2 - R6	39 kOhm Resistor, 0402 Pkg.
R7, R8	0 Ohm Resistor, 0402 Pkg.
T1, T2	1:1 RF Transformer, MA/COM SMT Balun (ETC1-1-13)
U1	HMC680LP4(E) Variable Gain Amplifier
PCB [2]	115584 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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