



## 13 Gbps, NRZ-to-RZ CONVERTER +3.3V SUPPLY

### Typical Applications

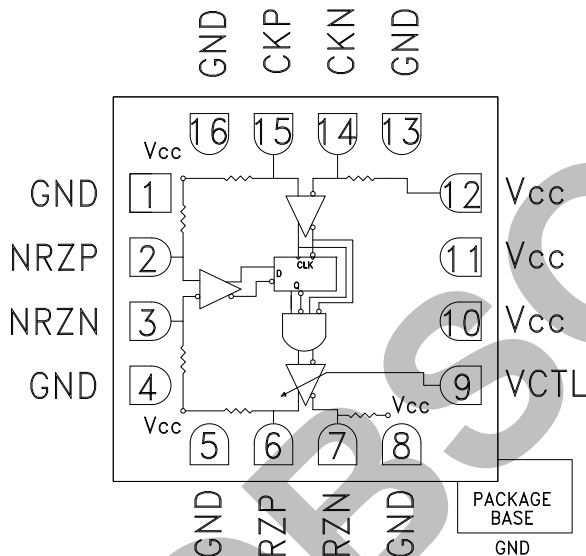
The HMC706LC3C is ideal for:

- NRZ-to-RZ data type conversion
- SONET OC-192 applications and equipment
- Mach-Zehnder optical modulator drivers
- Broadband test & measurement

### Features

- Supports high data rates: up to 13 Gbps
- Differential & single-ended operation
- Fast rise and fall times: 15/13 ps
- Low power consumption: 594 mW typ.
- Programmable differential output voltage swing: 300 mV - 1200 mV
- Propagation delay: 275 ps
- Single supply: +3.3V
- 16 lead ceramic 3 x 3 mm SMT package: 9 mm<sup>2</sup>

### Functional Diagram



### General Description

The HMC706LC3C is a NRZ-to-RZ converter designed to support data transmission rates of up to 13 Gbps, and clock frequencies as high as 13 GHz. During normal operation, RZ data is transferred to the outputs on the positive edge of the clock. Reversing the clock inputs allows for negative-edge triggered applications. All input signals to the HMC706LC3C are terminated with 50  $\Omega$  to Vcc on-chip, and may be either AC or DC coupled.

The differential outputs of the HMC706LC3C may be either AC or DC coupled. Outputs can be connected directly to a 50  $\Omega$  Vcc terminated system, while DC blocking capacitors may be used if the terminating system is 50  $\Omega$  to a non-Vcc DC voltage. The 50  $\Omega$  termination resistors are bypassed on chip from Vcc to ground. The HMC706LC3C operates from a single +3.3V DC supply and is available in a ceramic RoHS compliant 3 x 3 mm SMT package.

### Electrical Specifications, $T_A = +25^\circ\text{C}$ , $V_{CC} = +3.3\text{V}$

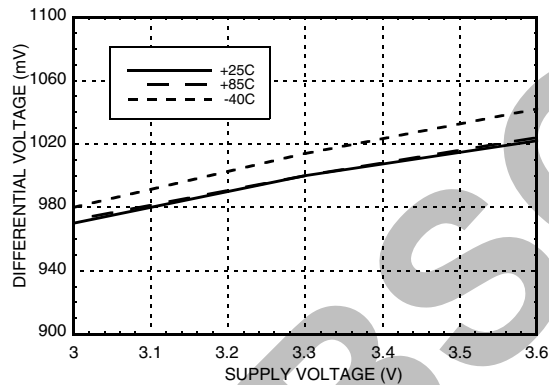
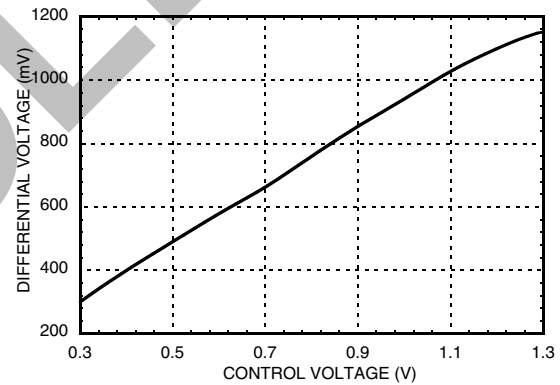
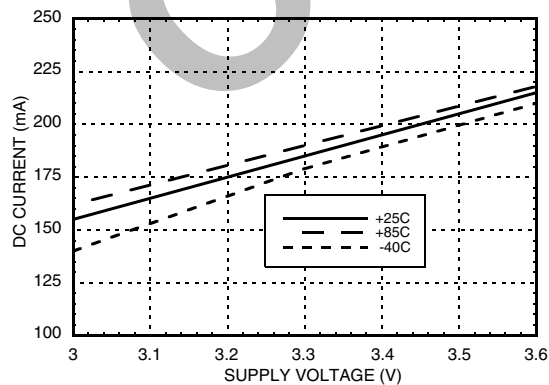
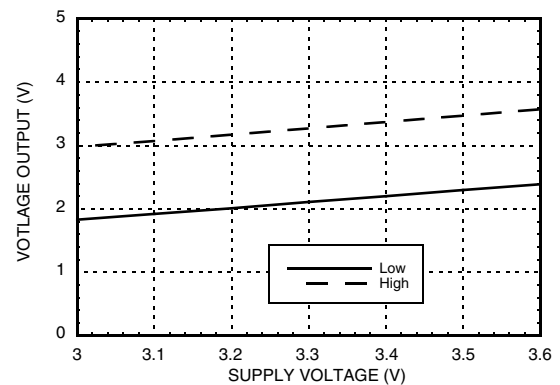
Parameter	Conditions	Min.	Typ.	Max	Units
Power supply voltage		3.0	3.3	3.6	V
Power supply current			180		mA
Maximum data rate			13		Gbps
Maximum clock rate			13		GHz
Input high voltage		$V_{CC} - 0.5$		$V_{CC} + 0.5$	V
Input low voltage		$V_{CC} - 1.1$		$V_{CC}$	V
Input return loss	Frequency < 13 GHz		12		dB
Input amplitude	Single-ended, peak-to-peak	50		1200	mVp-p
	Differential, peak-to-peak	100		2000	mVp-p
Adjustable output amplitude	Single-Ended, peak-to-peak	150		600	mVp-p
	Differential, peak-to-peak	300		1200	mVp-p
Output high voltage			3.28		V


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**Electrical Specifications, (continued)**

Parameter	Conditions	Min.	Typ.	Max	Units
Output low voltage			2.76		V
Output rise/fall time	Differential, 20% - 80%		15/13		ps
Output return loss	Frequency <13 GHz		13.5		dB
Random jitter, jr	rms <sup>[1]</sup>			0.2	ps rms
Deterministic jitter, jd	peak-to-peak, 2 <sup>31</sup> -1 PRBS input <sup>[2]</sup>		2		ps, p-p
Propagation delay clock to data, td			275		ps
Clock phase margin	13 GHz		270		deg

[1] Measured at 12.5 Gbps continuous 1010.... input pattern.

[2] Deterministic jitter calculated by simultaneously measuring the edge by edge variation of the output data stream with respect to the input clock.

**Differential Output  
Voltage vs. Supply Voltage<sup>[1]</sup>**

**Differential Output  
Voltage vs. Control Voltage**

**DC Current vs. Supply Voltage<sup>[1]</sup>**

**Output Low Voltage, Output High  
Voltage vs. Supply Voltage<sup>[1] [2]</sup>**


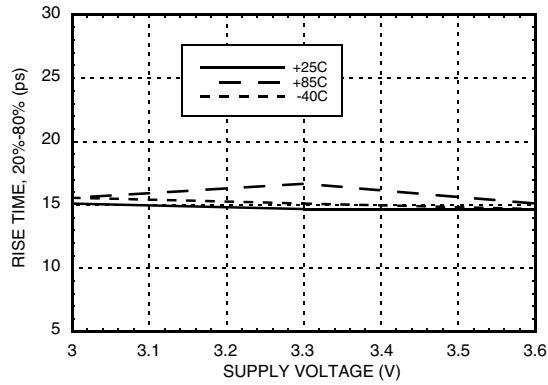
[1] Vctl = 1.1V

[2] Frequency = 13 GHz

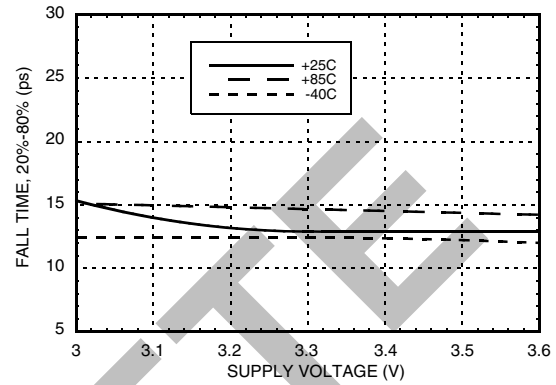


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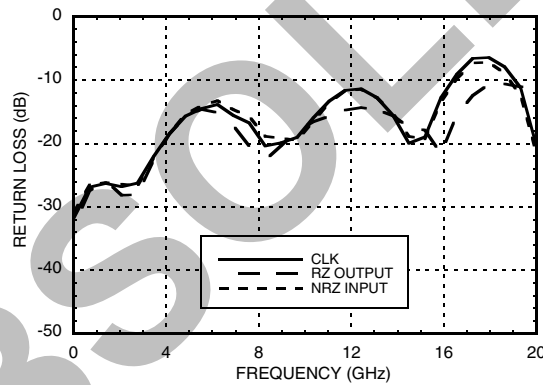
**Rise Time vs. Supply Voltage** <sup>[1] [2]</sup>



**Fall Time vs. Supply Voltage** <sup>[1] [2]</sup>



**Return Loss**



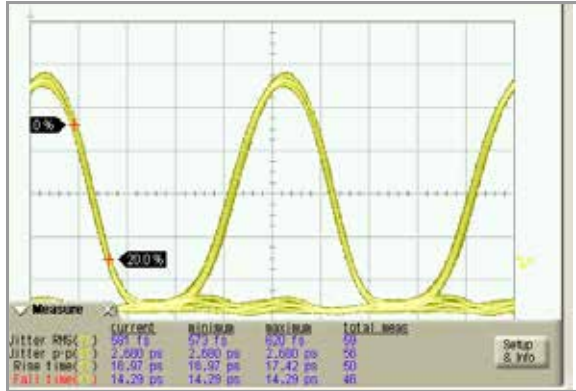
[1] Vctl = 1.1V

[2] Data Rate = 13 Gbps



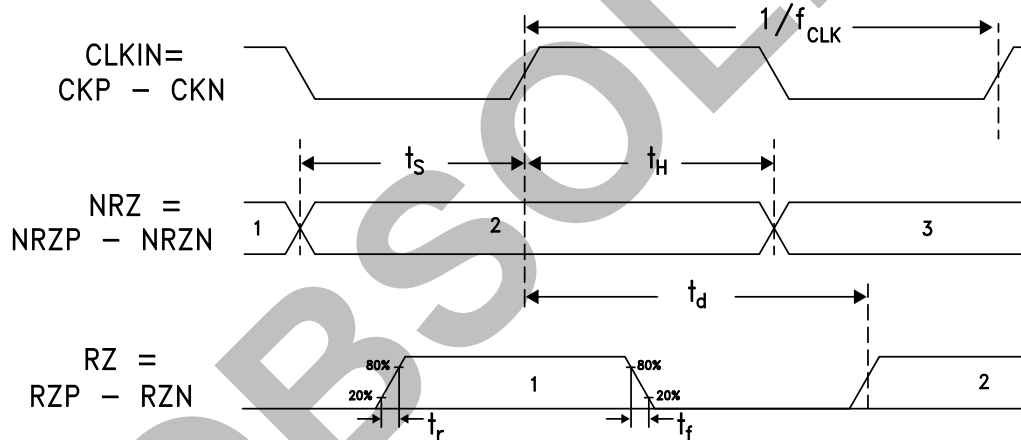
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**Eye Diagram [1]**



[1] Test Conditions:  
 Eye diagram data presented on an Infinium DCA 86100A  
 Rate = 10.0 GB/s  
 Pseudo random code = 2<sup>31</sup> - 1  
 Vin = 400 mVp-p differential

**Timing Diagram**



$t_s$  = Set up time  
 $t_h$  = Hold time  
 $t_d$  = Propagation delay

$$t_c = \frac{1}{f_{CLK}}$$

$$t_{SH} = t_s + t_h$$

$$CPM = \text{Clock phase margin} = 360^\circ \frac{t_c - t_{SH}}{t_c}$$

**Truth Table**

Input		Outputs
D	C	Q
L	L -> H	L
H	L -> H	H
X	H -> L	L

Notes:  
 D = DP - DN  
 C = CP - CN  
 Q = QP - QN

H - Negative voltage level  
 L - Positive voltage level

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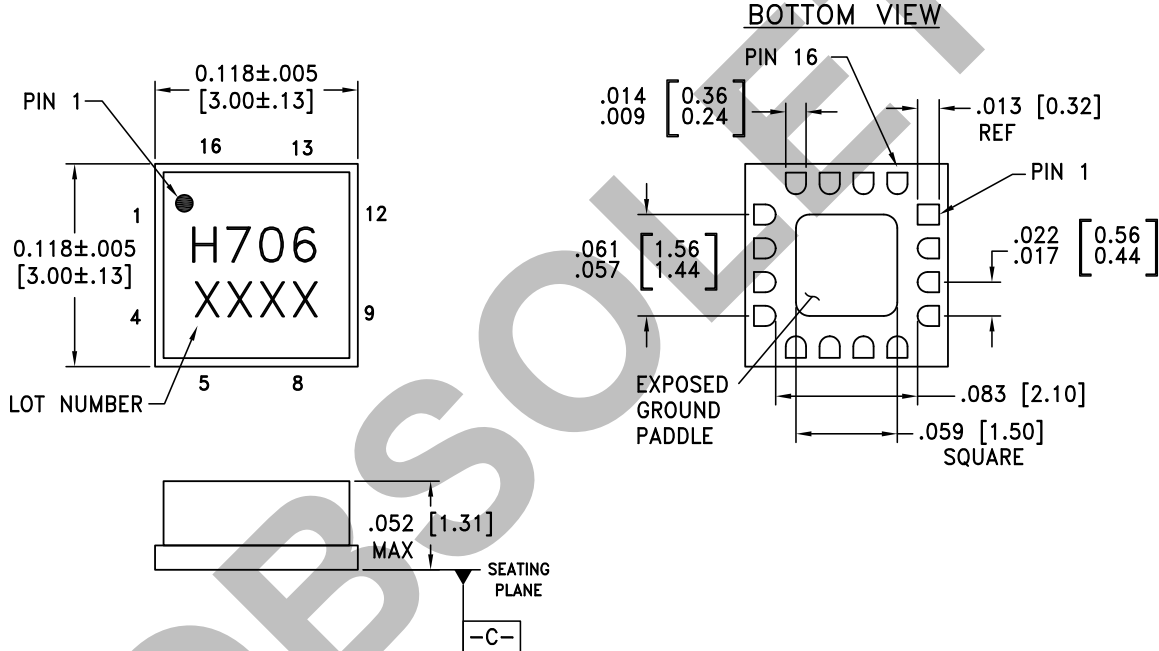
### Absolute Maximum Ratings

Power supply voltage (Vcc)	-0.5V to +3.6V
Input signals	Vcc - 2V to Vcc + 0.5V
Output signals	Vcc -1.5V to Vcc +1.0V
Storage temperature	-65 °C to +150 °C
Operating temperature	-40 °C to +85 °C
ESD sensitivity level (HBM)	Class 0 (>100V)



ELECTROSTATIC SENSITIVE DEVICE  
OBSERVE HANDLING PRECAUTIONS

### Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:  
30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05 mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. GROUND PADDLE MUST BE SOLDERED TO GND.

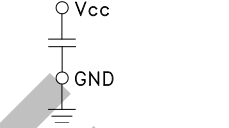
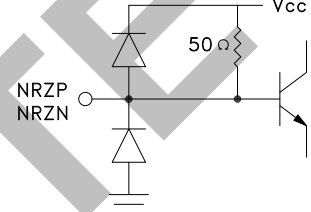
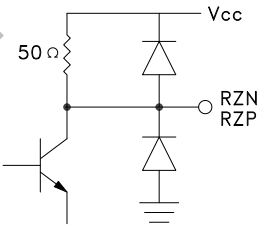
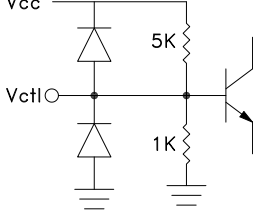
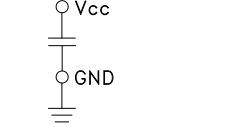
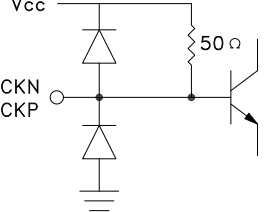
### Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking <sup>[2]</sup>
HMC706LC3C	Alumina, white	Gold over nickel	MSL3 <sup>[1]</sup>	H706 XXXX

[1] Max peak reflow temperature of 260 °C

[2] 4-digit lot number XXXX


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**Pin Descriptions**

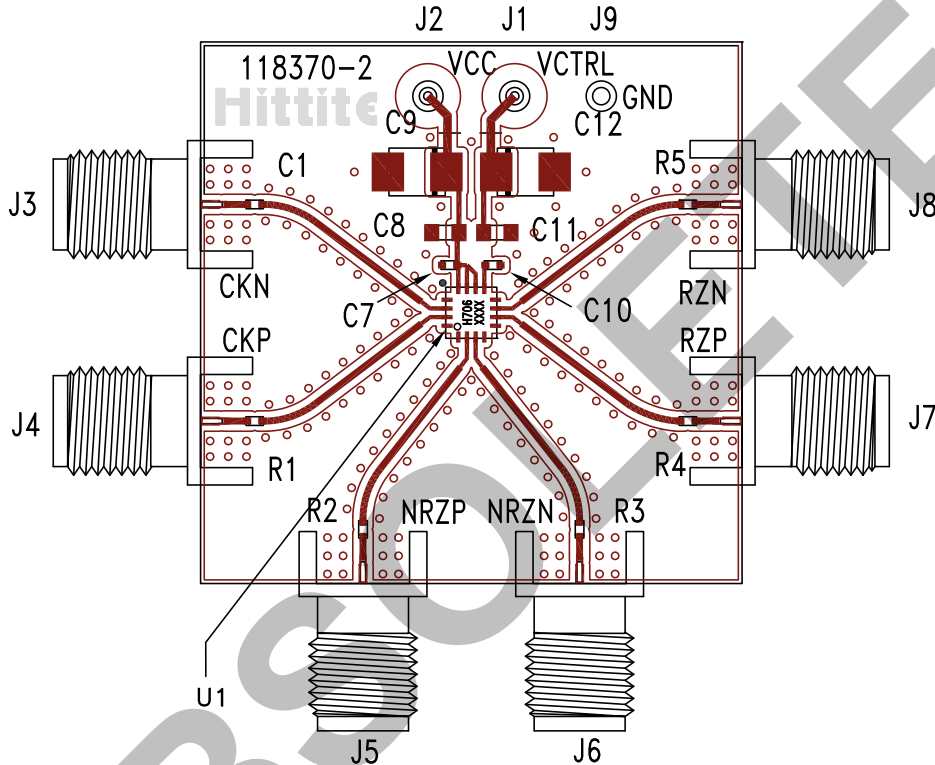
Pin Number	Function	Description	Interface Schematic
1, 4, 5, 8, 13, 16 Ground paddle	GND	Signal & supply ground	
2, 3	NRZP, NRZN	NRZ data inputs	
6, 7	RZP, RZN	RZ data outputs	
9	Vctl	Output level control	
10 - 12	Vcc	Positive supply	
14, 15	CKN, CKP	Clock inputs	



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**Evaluation PCB**

NOTE: ORIENTATION OF PIN 1



**List of Materials for Evaluation PCB 118372 [1]**

Item	Description
J1, J2, J9	DC pin
J3 - J8	K connector
C1	10 pF capacitor, 0402 pkg.
C7	1 nF capacitor, 0402 pkg.
C8, C11	100 nF capacitor, 0603 pkg.
C9, C12	4.7 μF Case A, Tantalum
C10	100 pF capacitor, 0402 pkg.
R1 - R5	0 Ω resistor, 0402 pkg.
U1	HMC706LC3C High speed logic, NRZ to RZ converter
PCB [2]	118370 evaluation board

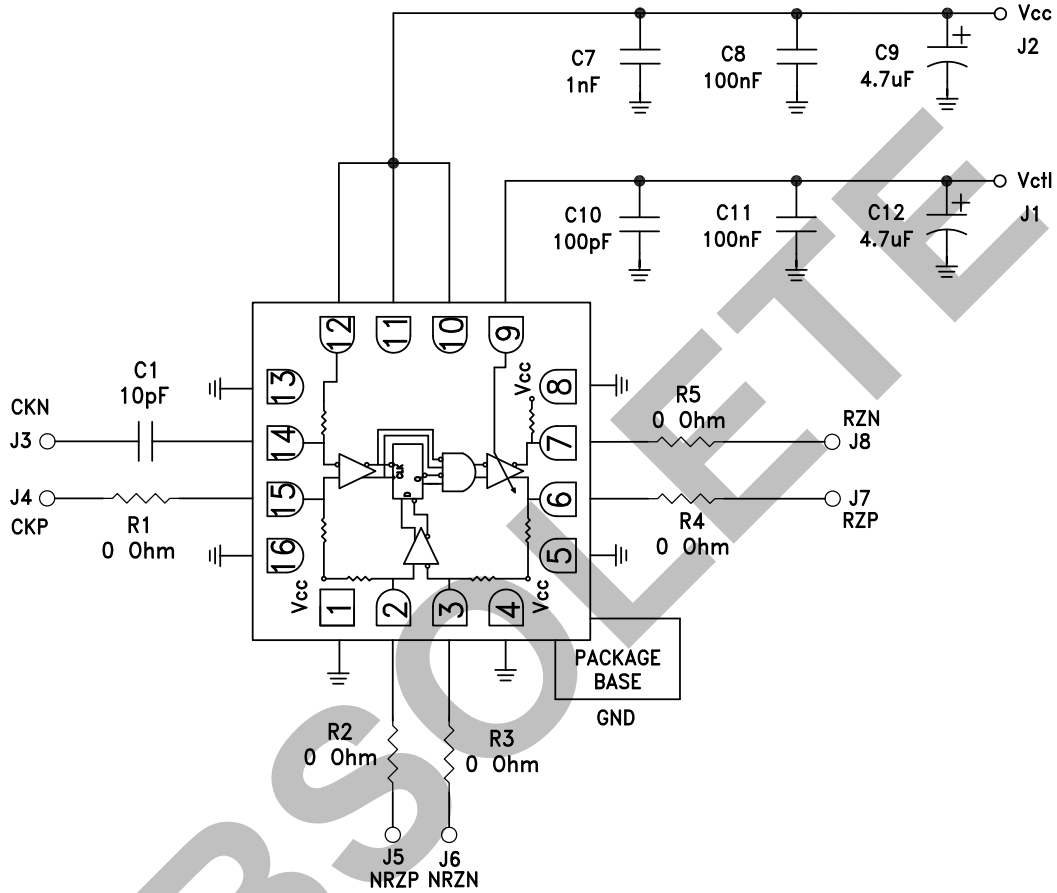
[1] Reference this number when ordering complete evaluation PCB  
 [2] Circuit board material: Arlon 25FR, FR4

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ω impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed package base should be connected to ground. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.



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**Application Circuit**



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