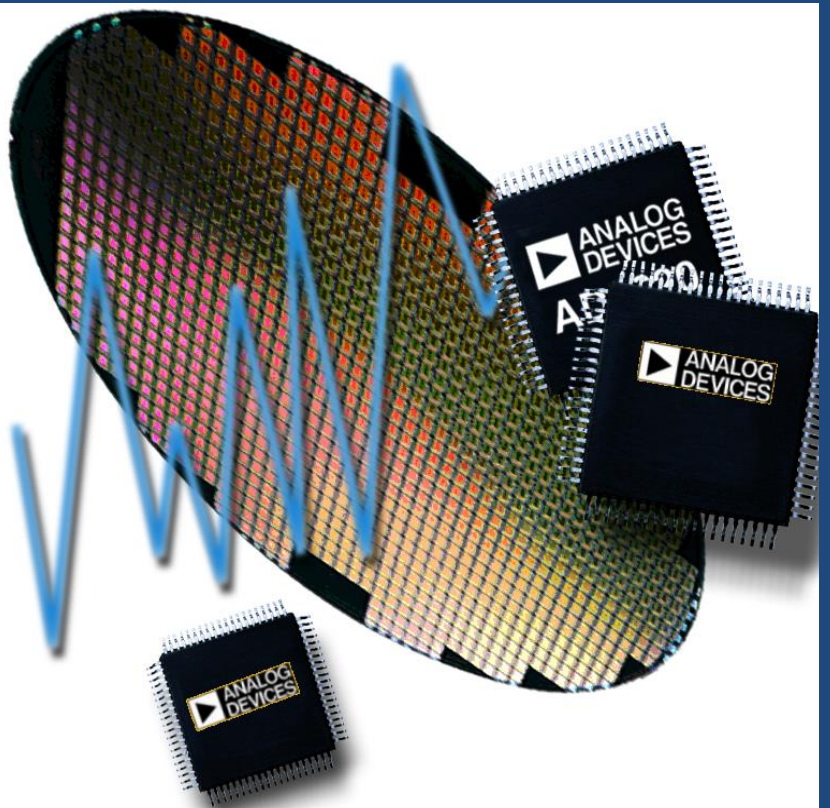


# Analog Devices Welcomes Hittite Microwave Corporation

NO CONTENT ON THE ATTACHED DOCUMENT HAS CHANGED





# ***Reliability Report***

<b>Report Title:</b>	<b>Qualification Test Report</b>
<b>Report Type:</b>	<b>See Attached</b>
<b>Date:</b>	<b>See Attached</b>

# Process FIT Rate Report

**QTR: 2014- 00061**

**Rev: 01**

**Wafer Process: BiCMOS-D**

HMC6545

HMC6590

HMC7590

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## Introduction

The testing performed for this report is designed to accelerate the predominant failure mode, electro-migration (EM), for the devices under test. The devices are stressed at high temperature and DC biased to simulate a lifetime of use at typical operating temperatures. Using the Arrhenius equation, the acceleration factor (AF) is calculated for the stress testing based on the stress temperature and the typical use operating temperature.

This report is intended to summarize all of the High Temperature Operating Life Test (HTOL) data for the BiCMOS-D process. The FIT/MTTF data contained in this report includes all the stress testing performed on this process to date and will be updated periodically as additional data becomes available. Data sheets for the tested devices can be found at [www.hittite.com](http://www.hittite.com).

## Glossary of Terms & Definitions:

1. **HTOL:** High Temperature Operating Life. This test is used to determine the effects of bias conditions and temperature on semiconductor devices over time. It simulates the devices' operating condition in an accelerated way, through high temperature and/or bias voltage, and is primarily for device qualification and reliability monitoring. This test was performed in accordance with JEDEC JESD22-A108.
2. **Operating Junction Temp ( $T_{oj}$ ):** Temperature of the die active circuitry during typical operation.
3. **Stress Junction Temp ( $T_{sj}$ ):** Temperature of the die active circuitry during stress testing.

## Qualification Sample Selection:

All qualification devices used were manufactured and tested on standard production processes and met pre-stress acceptance test requirements.

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## Summary of Qualification Tests:

### HMC6545 (QTR2012-00514)

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Initial Electrical	80	80	Complete	
HTOL, 1072 hours	80	80	Complete	
Post HTOL Electrical Test	80	80	Pass	

## BiCMOS-D Failure Rate Estimate

Based on the HTOL test results, a failure rate estimation was determined using the following parameters:

With device ambient case temp,  $T_c = 60^\circ\text{C}$

HMC6545 (QTR2012-00514)

Operating Junction Temp ( $T_{oj}$ ) =  $80^\circ\text{C}$  ( $353^\circ\text{K}$ )

Stress Junction Temp ( $T_{sj}$ ) =  $193^\circ\text{C}$  ( $466^\circ\text{K}$ )

Device hours:

HMC6545 (QTR2012-00514) =  $(80 \times 1072\text{hrs}) = 85,760$  hours

For BiCMOS-D MMIC, Activation Energy =  $0.7$  eV

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$$AF = \exp \left[ \left( \frac{E_A}{k} \right) \cdot \left( \left( \frac{1}{T_{USE}} \right) - \left( \frac{1}{T_{STRESS}} \right) \right) \right]$$

Acceleration Factor (AF):

HMC6545 (QTR2012-00514) Acceleration Factor =  $\exp[0.7/8.6 \cdot e^{-5(1/353-1/466)}] = 322.7$

Equivalent hours = Device hours x Acceleration Factor

Equivalent hours =  $(85,760 \times 322.7) = 2.77 \times 10^7$  hours

Since there were no failures and we used a time terminated test,  $F=0$ , and  $R = 2F+2 = 2$

The failure rate was calculated using Chi Square Statistic:

$\lambda_{CL} = \frac{\chi^2_{\%CL, 2f+2} \cdot 10^9}{2 \cdot t \cdot SS \cdot AF}$  at 60% and 90% Confidence Level (CL), with 0 units out of spec and a 60°C package backside temp;

## Failure Rate

$\lambda_{60} = [(\chi^2)_{60,2}] / (2 \times 2.10 \times 10^8) = 1.8 / 5.54 \times 10^7 = 3.31 \times 10^{-8}$  failures/hour or 33.1 FIT or MTTF =  $3.02 \times 10^7$  hours

$\lambda_{90} = [(\chi^2)_{90,2}] / (2 \times 2.10 \times 10^8) = 4.6 / 5.54 \times 10^7 = 8.33 \times 10^{-8}$  failures/hour or 83.3 FIT or MTTF =  $1.20 \times 10^7$  hours

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