71 GHz to 86 GHz, E-Band Low Noise Amplifier

Data Sheet **HMC8325**

FEATURES

Gain: 21 dB typical
Noise figure: 3.6 dB typical
Output power for 1 dB compression: 13 dBm typical
Input third-order intercept at maximum gain: 1 dBm typical
Output third-order intercept at maximum gain: 22 dBm typical
Saturated output power: 17 dBm typical
Input return loss: 15 dB typical
Output return loss: 17 dB typical
Die size: 2.844 mm × 0.999 mm × 0.05 mm

APPLICATIONS

E-band communication systems
High capacity wireless backhauls
Test and measurement

GENERAL DESCRIPTION

The HMC8325 is an integrated E-band gallium arsenide (GaAs), monolithic microwave integrated circuit (MMIC), low noise amplifier (LNA) chip that operates from 71 GHz to 86 GHz. The HMC8325 provides 21 dB of gain, 13 dBm of output P1dB, 22 dBm of OIP3, and 17 dBm of P_{SAT} while requiring only 50 mA from a 3 V power supply. The HMC8325 exhibits excellent linearity and is optimized for E-band communications and high capacity, wireless backhaul radio systems. All data is taken with the chip in a 50 Ω test fixture connected via a 3 mil wide × 0.5 mil thick × 7 mil long ribbon on each port.

FUNCTIONAL BLOCK DIAGRAM

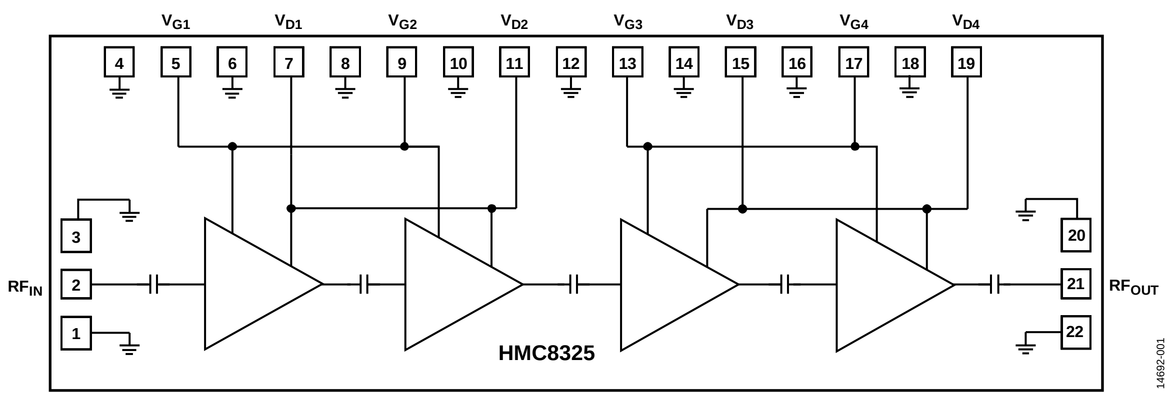

Figure 1.

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Technical Support **www.analog.com**

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REVISION HISTORY

2/2017—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_{Dx} (V_{D1} and V_{D2} to V_{D3} and V_{D4}) = 3 V, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
OPERATING CONDITIONS				
Radio Frequency (RF) Range	71		86	GHz
PERFORMANCE				
Gain	19.5	21		dB
Gain Variation over Temperature		0.02		dB/°C
Output Power for 1 dB Compression (P1dB)		13		dBm
Saturated Output Power (P_{SAT})		17		dBm
Input Third-Order Intercept (IIP3) at Maximum Gain[1]		1		dBm
Output Third-Order Intercept (OIP3) at Maximum Gain[1]		22		dBm
Noise Figure		3.6	4.5	dB
Return Loss				
Input		15		dB
Output		17		dB
POWER SUPPLY				
Total Drain Current (I_{Dx})[2]		50		mA

[1] Data taken at power output (P_{OUT}) = 5 dBm/tone, 1 MHz spacing.
[2] Adjust V_{G1} and V_{G2} to V_{G3} and V_{G4} from −2 V to 0 V to achieve a total drain current (I_{Dx}) = 50 mA.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Drain Bias Voltage (V_{D1} to V_{D4})	4.5 V
Gate Bias Voltage (V_{G1} to V_{G4})	−3 V to 0 V
Maximum Junction Temperature (to Maintain 1 Million Hours Mean Time to Failure (MTTF))	175°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +85°C
ESD Sensitivity, Human Body Model (HBM)	Class 0 (150 V)

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 3. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
C-22-1[2]	225	°C/W

[1] Based on ABLEBOND® 84-1LMIT as die attach epoxy.
[2] Test Condition: Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with four thermal vias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

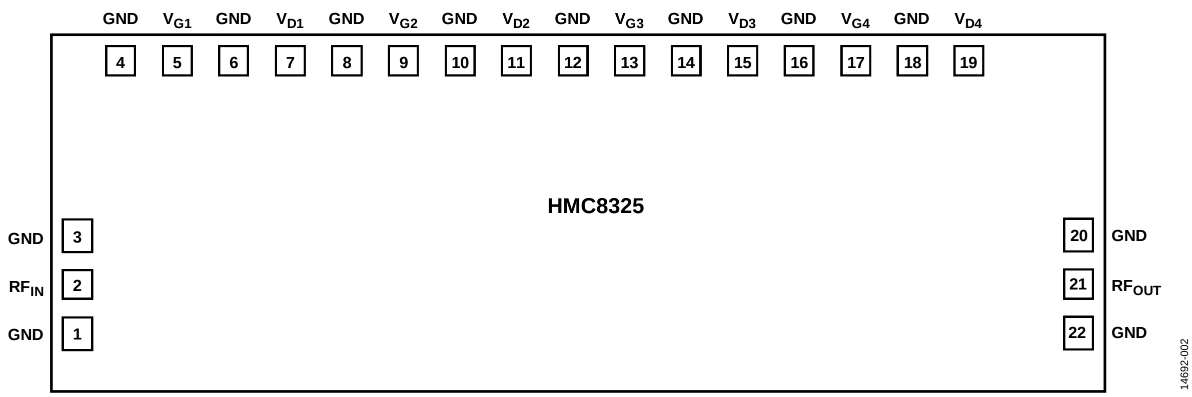

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pad No.	Mnemonic	Description
1, 3, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22	GND	Ground Connection.
2	RF_{IN}	RF Input. AC couple RF_{IN} and match it to 50 Ω.
5, 9, 13, 17	V_{G1} to V_{G4}	Gate Bias Voltage for the Low Noise Amplifier.
7, 11, 15, 19	V_{D1} to V_{D4}	Drain Bias Voltage for the Low Noise Amplifier.
21	RF_{OUT}	RF Output. AC couple RF_{OUT} and match it to 50 Ω.
Die Bottom	GND	Ground. Die bottom must be connected to the RF/dc ground.

INTERFACE SCHEMATICS

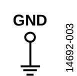

Figure 3. GND Interface Schematic

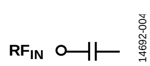

Figure 4. RF_{IN} Interface Schematic

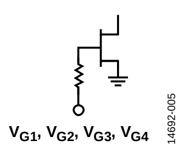

Figure 5. V_{G1} to V_{G4} Interface Schematic

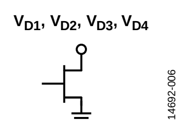

Figure 6. V_{D1} to V_{D4} Interface Schematic

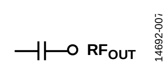

Figure 7. RF_{OUT} Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

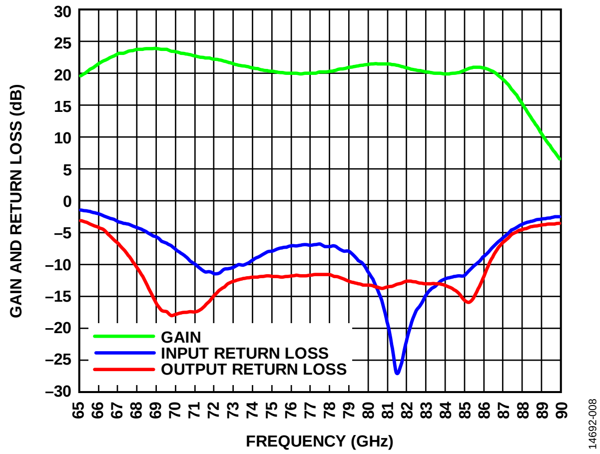

Figure 8. Gain and Return Loss vs. Frequency, V_{Dx} = 3 V, I_{Dx} = 57 mA

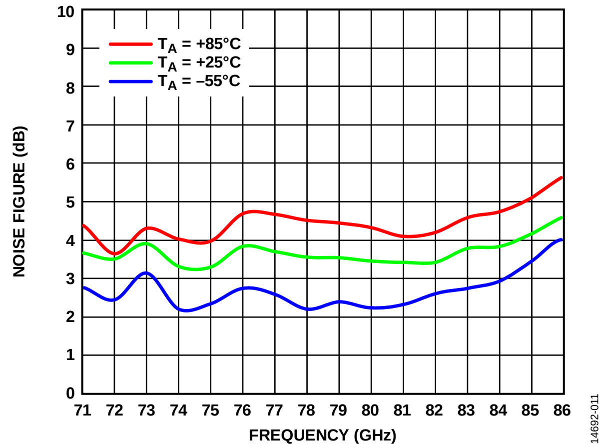

Figure 11. Noise Figure vs. Frequency over Temperature, V_{Dx} = 3 V, I_{Dx} = 50 mA

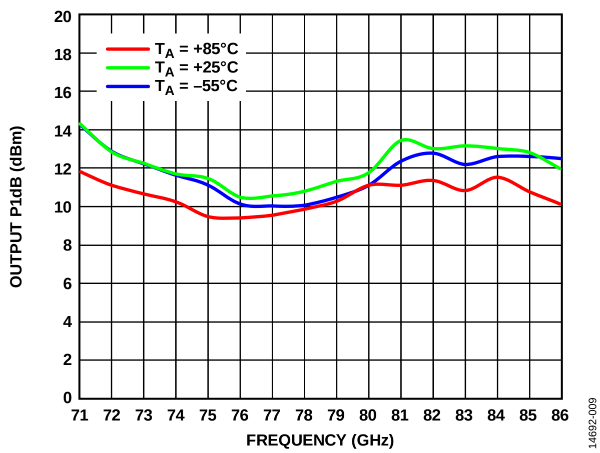

Figure 9. Output P1dB vs. Frequency over Temperature, V_{Dx} = 3 V, I_{Dx} = 50 mA

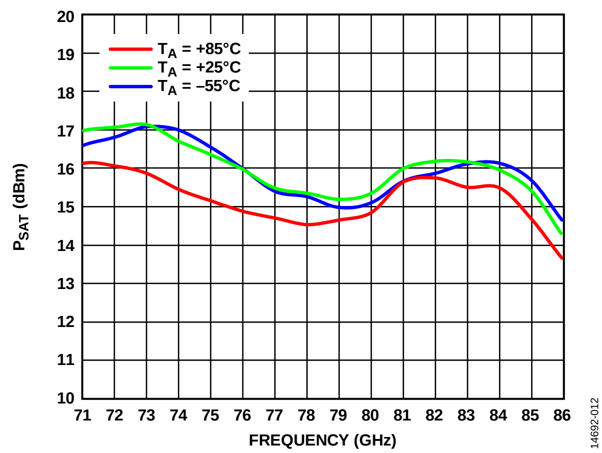

Figure 12. Saturated Output Power (P_{SAT}) vs. Frequency over Temperature, V_{Dx} = 3 V, I_{Dx} = 50 mA

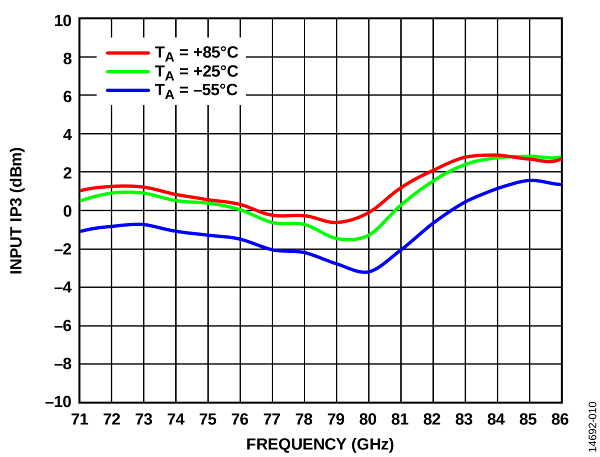

Figure 10. Input Third-Order Intercept (IP3) vs. Frequency over Temperatures, P_{OUT} = 5 dBm/Tone, V_{Dx} = 3 V, I_{Dx} = 50 mA

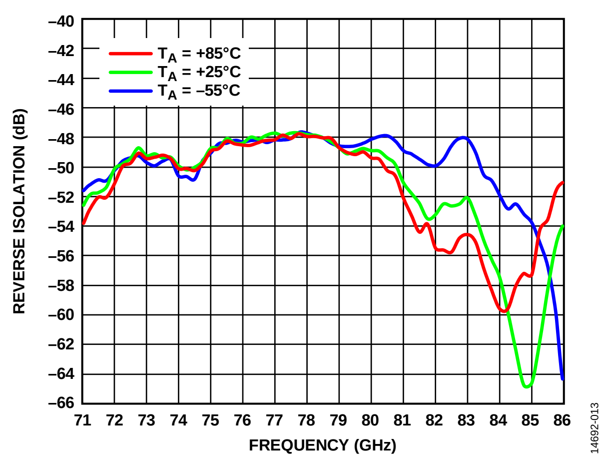

Figure 13. Reverse Isolation vs. Frequency over Temperature, V_{Dx} = 3 V, I_{Dx} = 57 mA

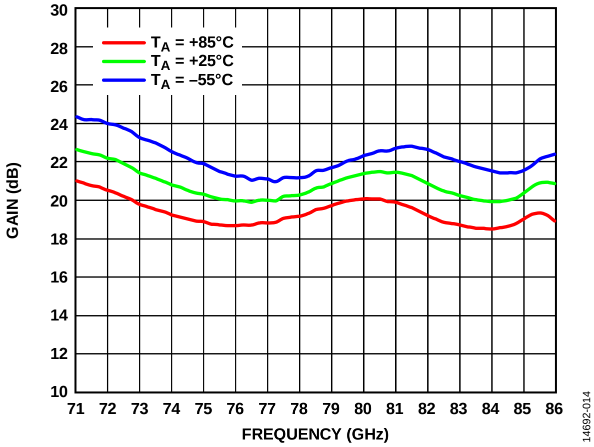

Figure 14. Gain vs. Frequency over Temperature, V_{Dx} = 3 V, I_{Dx} = 57 mA

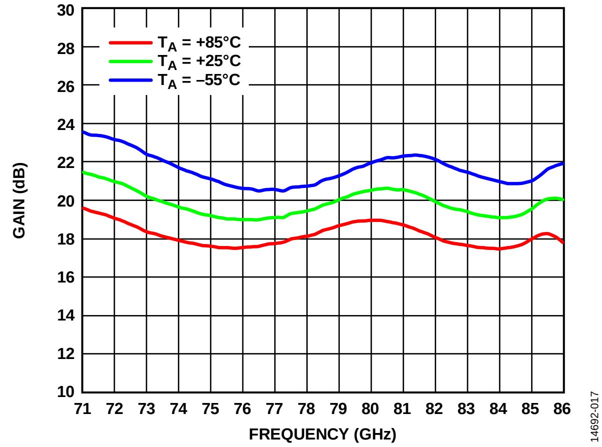

Figure 17. Gain vs. Frequency over Temperature, V_{Dx} = 4 V, I_{Dx} = 57 mA

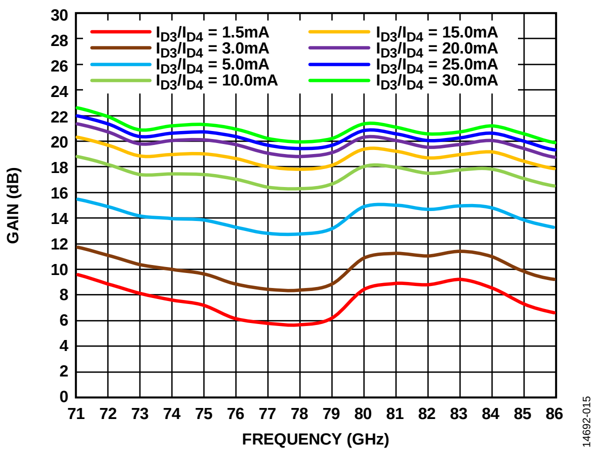

Figure 15. Gain vs. Frequency over Drain Current, V_{Dx} = 3 V, V_{G1} and V_{G2} Fixed at 20 mA, V_{G3} and V_{G4} Swept

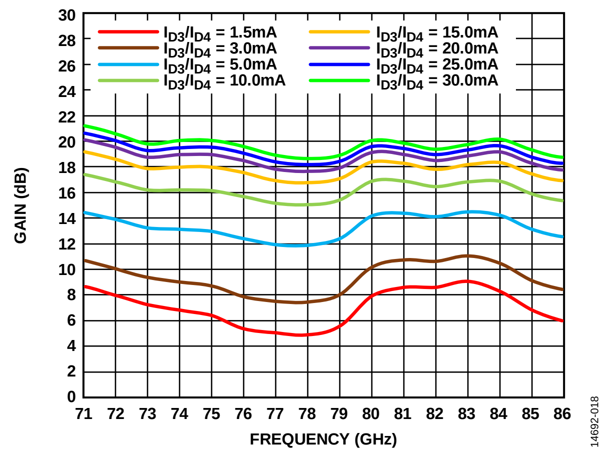

Figure 18. Gain vs. Frequency over Drain Current, V_{Dx} = 4 V, V_{G1} and V_{G2} Fixed at 20 mA, V_{G3} and V_{G4} Swept

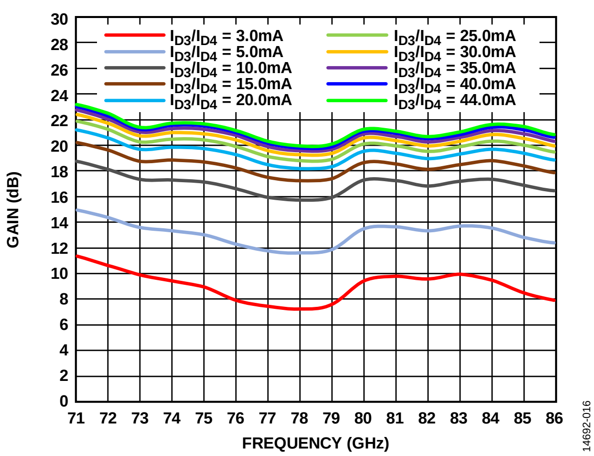

Figure 16. Gain vs. Frequency over Drain Current, V_{D1} and V_{D2} = 2 V, V_{D3} and V_{D4} = 4 V

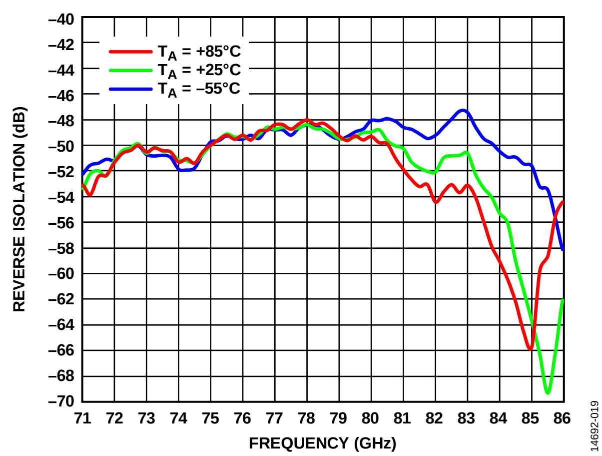

Figure 19. Reverse Isolation vs. Frequency over Temperature, V_{Dx} = 4 V, I_{Dx} = 57 mA

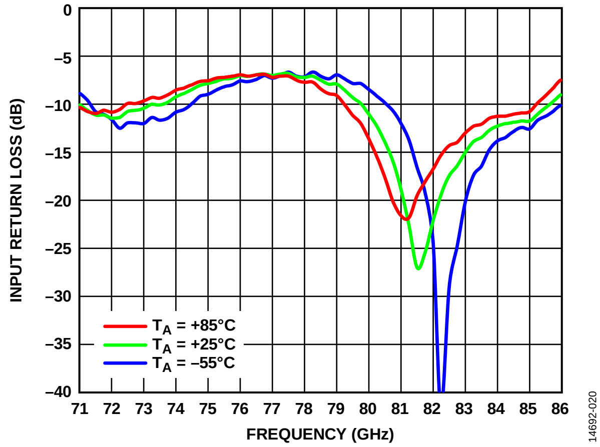

Figure 20. Input Return Loss vs. Frequency over Temperature, V_{Dx} = 3 V, I_{Dx} = 57 mA

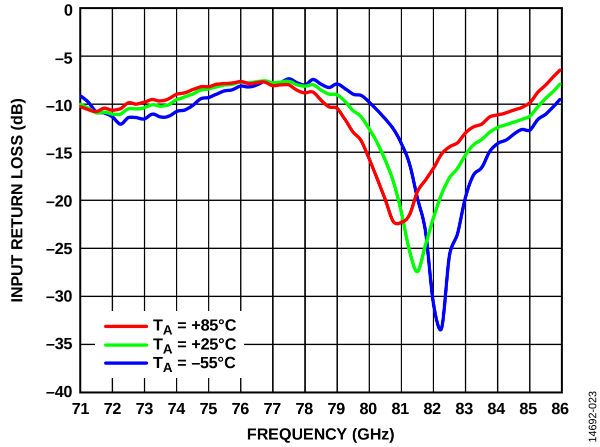

Figure 23. Input Return Loss vs. Frequency over Temperature, V_{Dx} = 4 V, I_{Dx} = 57 mA

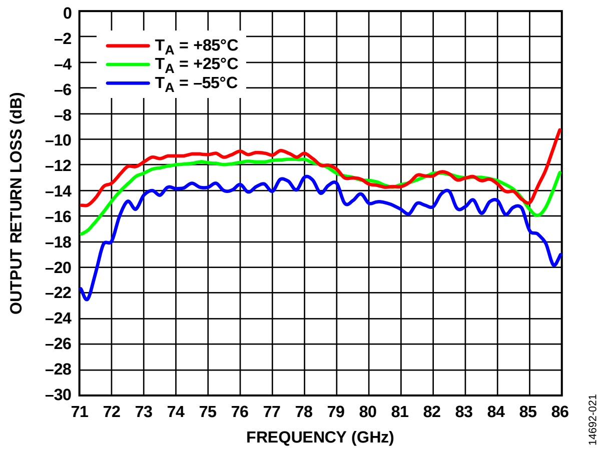

Figure 21. Output Return Loss vs. Frequency over Temperature, V_{Dx} = 3 V, I_{Dx} = 57 mA

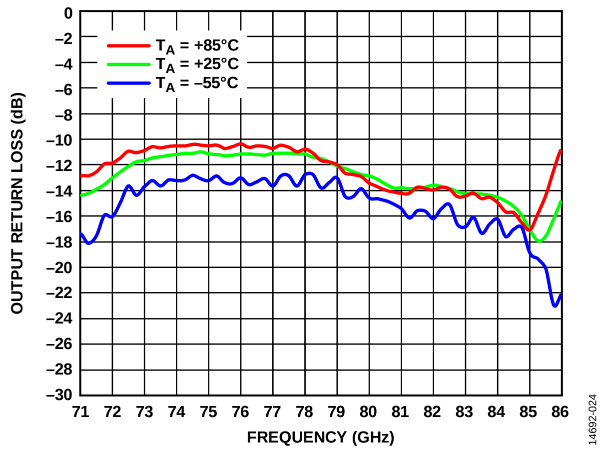

Figure 24. Output Return Loss vs. Frequency over Temperature, V_{Dx} = 4 V, I_{Dx} = 57 mA

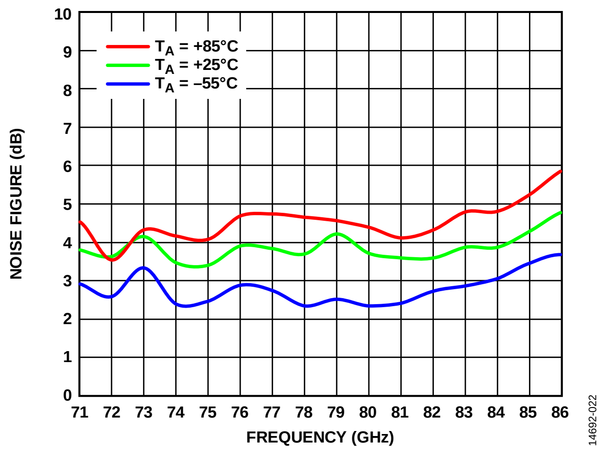

Figure 22. Noise Figure vs. Frequency over Temperature, V_{Dx} = 4 V, I_{Dx} = 50 mA

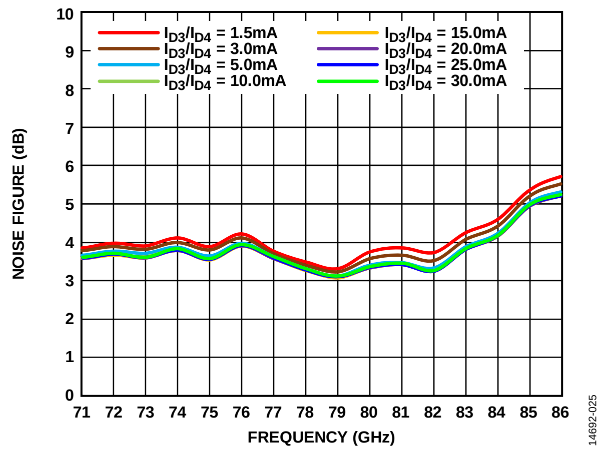

Figure 25. Noise Figure vs. Frequency over Drain Current, V_{Dx} = 3 V, V_{G1} and V_{G2} Fixed at 20 mA, V_{G3} and V_{G4} Swept

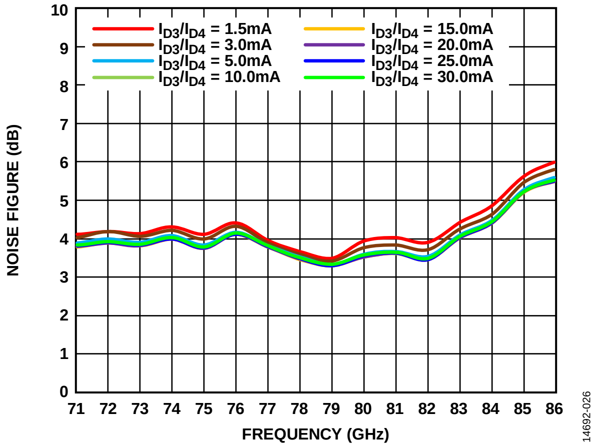

Figure 26. Noise Figure vs. Frequency over Drain Current, V_{Dx} = 4 V, V_{G1} and V_{G2} Fixed at 20 mA, V_{G3} and V_{G4} Swept

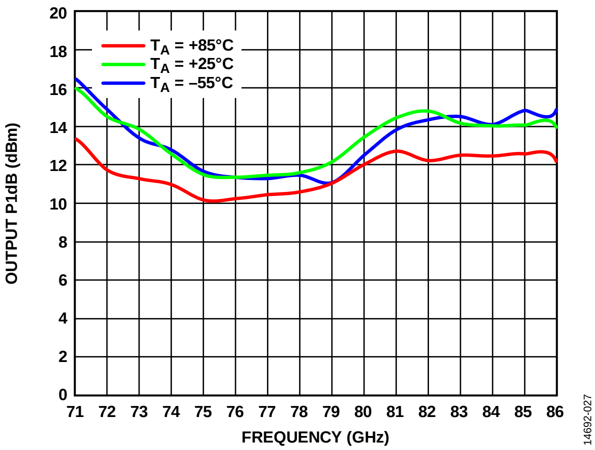

Figure 27. Output P1dB vs. Frequency over Temperature, V_{Dx} = 4 V, I_{Dx} = 50 mA

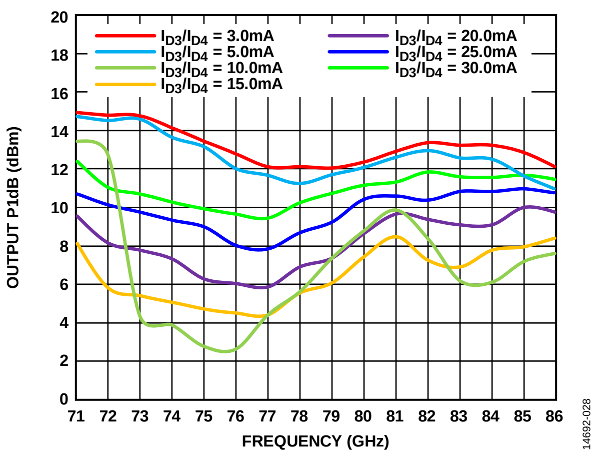

Figure 28. Output P1dB vs. Frequency over Drain Current, V_{Dx} = 3 V, V_{G1} and V_{G2} Fixed at 20 mA, V_{G3} and V_{G4} Swept

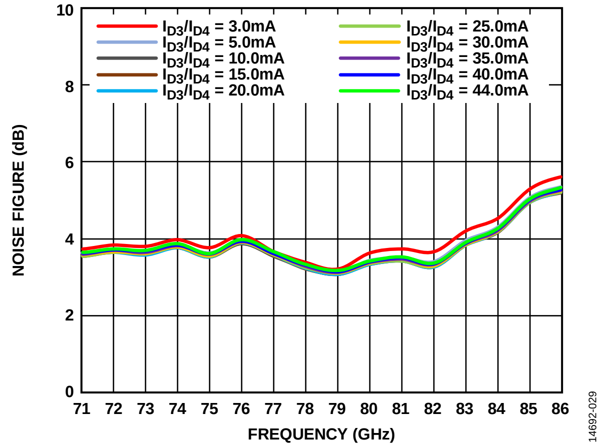

Figure 29. Noise Figure vs. Frequency over Drain Current, V_{D1} and V_{D2} = 2 V, V_{D3} and V_{D4} = 4 V

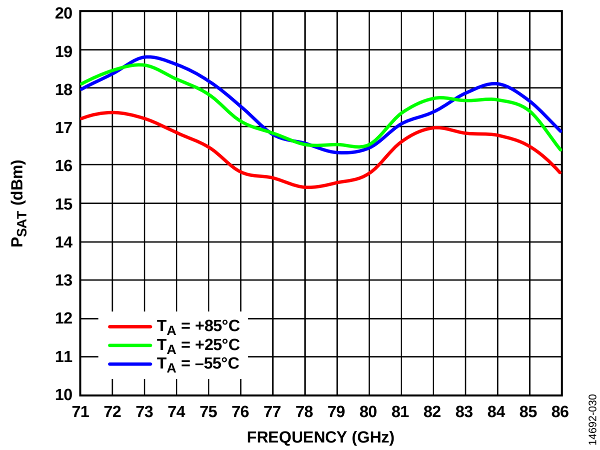

Figure 30. Saturated Output Power (P_{SAT}) vs. Frequency over Temperature, V_{Dx} = 4 V, I_{Dx} = 50 mA

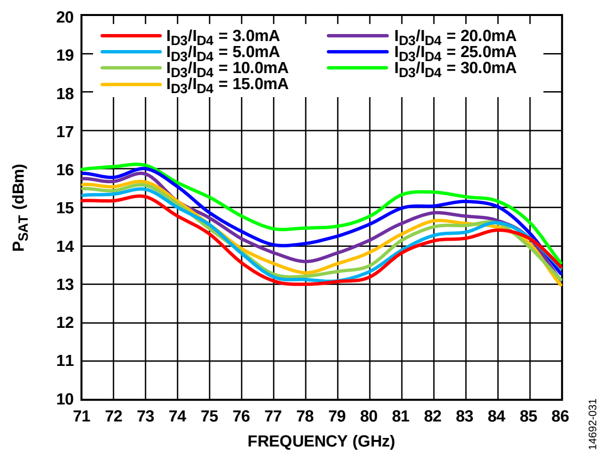

Figure 31. Saturated Output Power (P_{SAT}) vs. Frequency over Drain Current, V_{Dx} = 3 V, V_{G1} and V_{G2} Fixed at 20 mA, V_{G3} and V_{G4} Swept

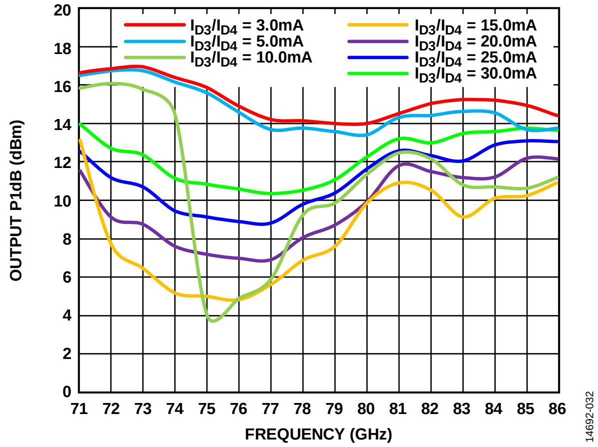

Figure 32. Output P1dB vs. Frequency over Drain Current, V_{Dx} = 4 V, V_{G1} and V_{G2} Fixed at 20 mA, V_{G3} and V_{G4} Swept

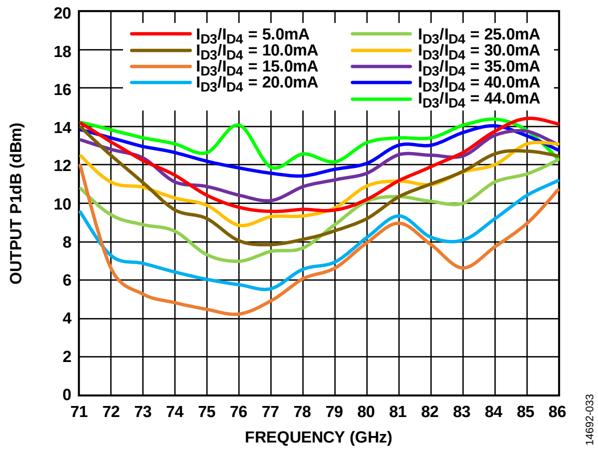

Figure 33. Output P1dB vs. Frequency over Drain Current, V_{D1} and V_{D2} = 2 V, V_{D3} and V_{D4} = 4 V

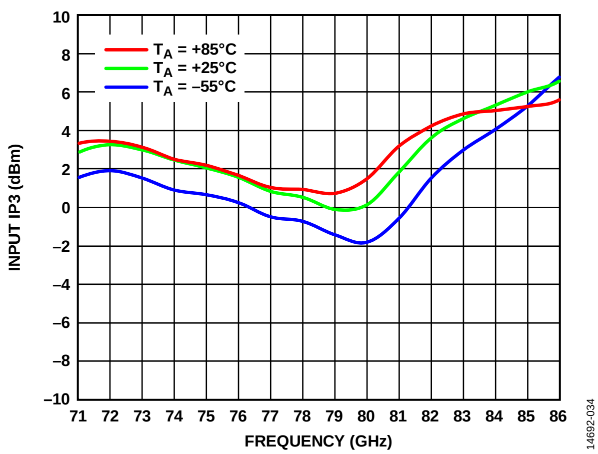

Figure 34. Input Third-Order Intercept (IP3) vs. Frequency over Temperature, V_{Dx} = 4 V, I_{Dx} = 50 mA

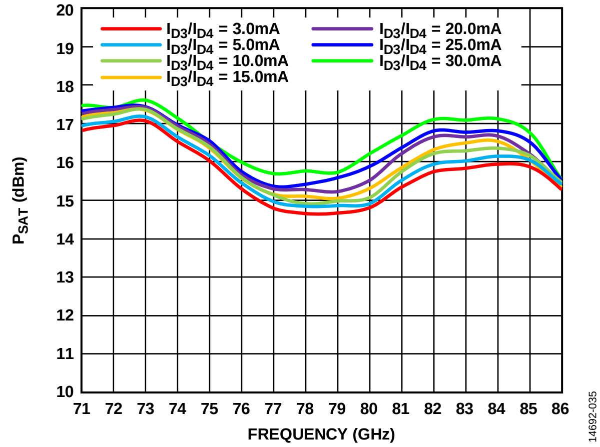

Figure 35. Saturated Output Power (P_{SAT}) vs. Frequency over Drain Current, V_{Dx} = 4 V, V_{G1} and V_{G2} Fixed at 20 mA, V_{G3} and V_{G4} Swept

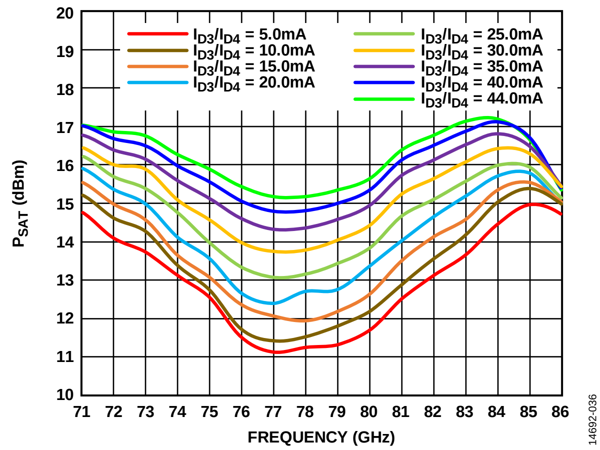

Figure 36. Saturated Output Power (P_{SAT}) vs. Frequency over Drain Current, V_{D1} and V_{D2} = 2 V, V_{D3} and V_{D4} = 4 V

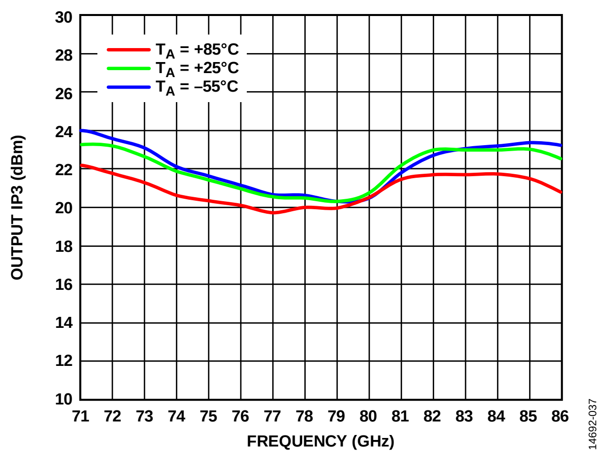

Figure 37. Output Third-Order Intercept (IP3) vs. Frequency over Temperature, V_{Dx} = 4 V, I_{Dx} = 50 mA

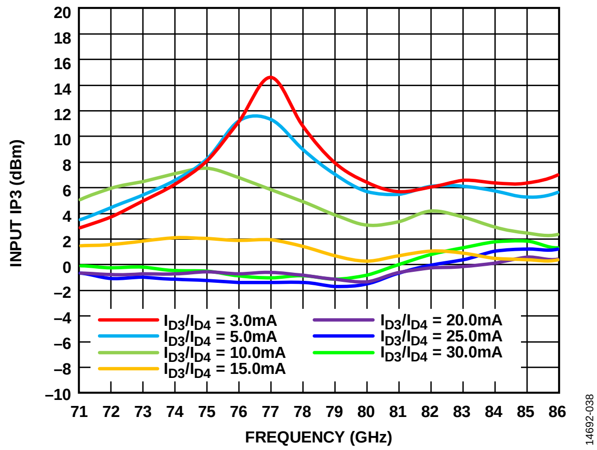

Figure 38. Input Third-Order Intercept (IP3) vs. Frequency over Drain Current, V_{Dx} = 3 V, V_{G1} and V_{G2} Fixed at 20 mA, V_{G3} and V_{G4} Swept

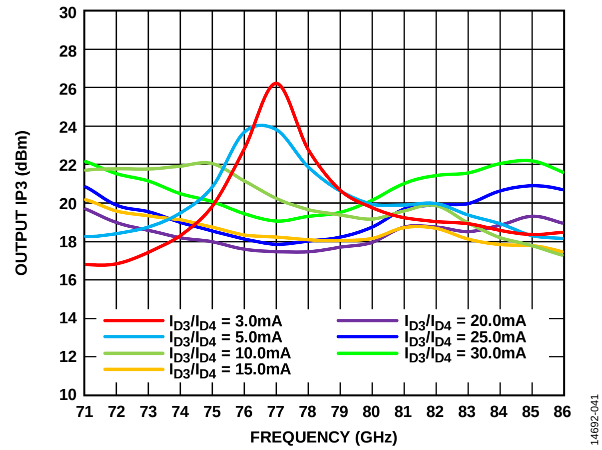

Figure 41. Output Third-Order Intercept (IP3) vs. Frequency over Drain Current, V_{Dx} = 3 V, V_{G1} and V_{G2} Fixed at 20 mA, V_{G3} and V_{G4} Swept

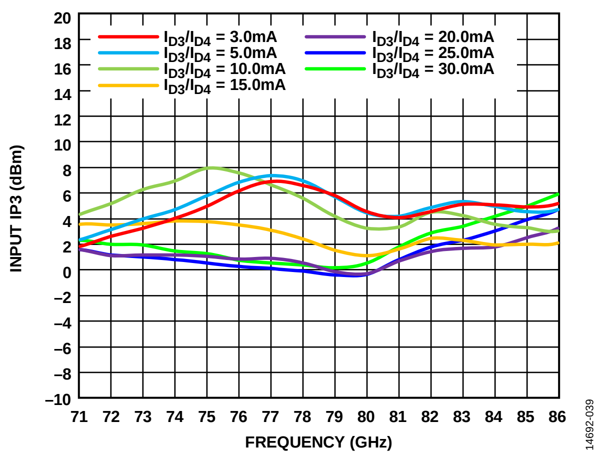

Figure 39. Input Third-Order Intercept (IP3) vs. Frequency over Drain Current, V_{Dx} = 4 V, V_{G1} and V_{G2} Fixed at 20 mA, V_{G3} and V_{G4} Swept

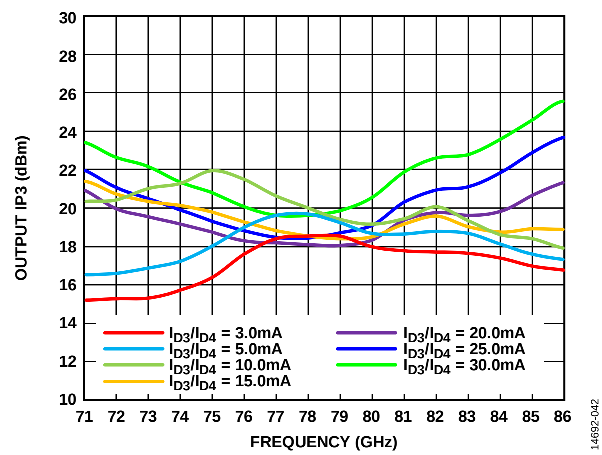

Figure 42. Output Third-Order Intercept (IP3) vs. Frequency over Drain Current, V_{Dx} = 4 V, V_{G1} and V_{G2} Fixed at 20 mA, V_{G3} and V_{G4} Swept

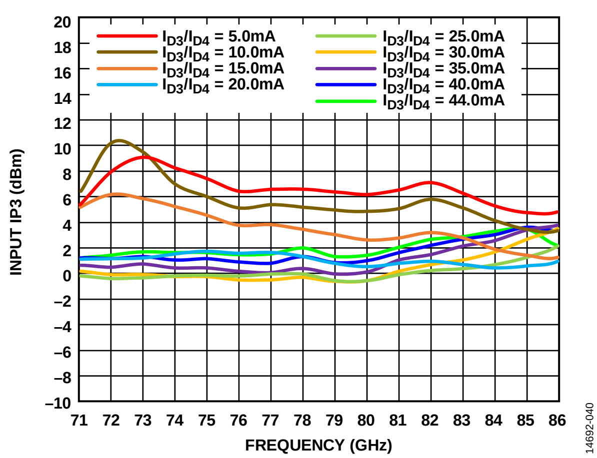

Figure 40. Input Third-Order Intercept (IP3) vs. Frequency over Drain Current, V_{D1} and V_{D2} = 2 V, V_{D3} and V_{D4} = 4 V

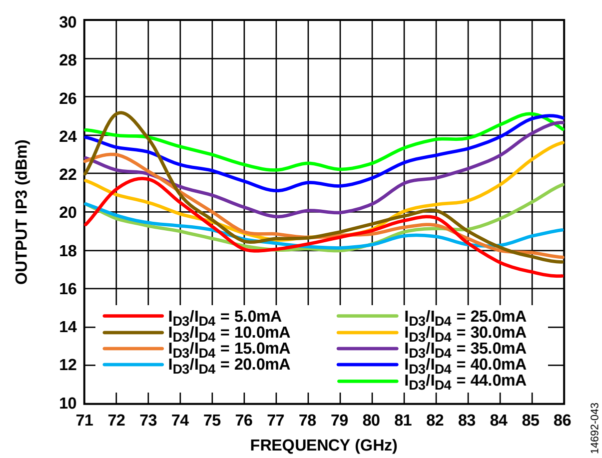

Figure 43. Output Third-Order Intercept (IP3) vs. Frequency over Drain Current, V_{D1} and V_{D2} = 2 V, V_{D3} and V_{D4} = 4 V

THEORY OF OPERATION

The circuit architecture of the HMC8325 low noise amplifier is shown in Figure 44. The HMC8325 uses four cascaded gain stages to form an amplifier with a combined gain of 21 dB (typical), a noise figure of 3.6 dB (typical), and 1 dBm (typical) input IP3 across the 71 GHz to 86 GHz frequency range. Stage 1 and Stage 2 can be biased separately from Stage 3 and Stage 4. Operating at $V_{D1} = V_{D2} = 2$ V and $V_{D3} = V_{D4} = 4$ V improves gain and noise figure compared to $V_{D1} = V_{D2} = V_{D3} = V_{D4} = 4$ V.

The input IP3 is slightly lower for the $V_{D1} = V_{D2} = 2$ V and $V_{D3} = V_{D4} = 4$ V case. A compromise bias voltage between the gain noise figure vs. the input IP3 is $V_{D1} = V_{D2} = V_{D3} = V_{D4} = 3$ V. Gain control can be achieved by down biasing Stage 3 and Stage 4. By lowering the drain current of I_{D3} and I_{D4}, a 12 dB reduction in gain can be achieved with a small degradation in the noise figure. Refer to Figure 45 for further details on biasing arrangements for the different stages.

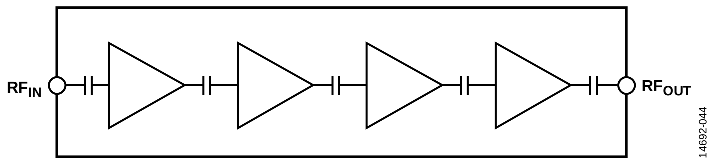

Figure 44. Circuit Architecture

APPLICATION INFORMATION

The typical application circuit shown in Figure 45 shows the HMC8325 chip with all of its required bypassing components. Bypass all supply connections with adequate bypassing capacitors is recommended. Use single-layer chip capacitors with a very high, self-resonant frequency close to the HMC8325 chip. Typically, 120 pF chip capacitors are recommended, followed by 0.01 µF and 4.7 µF surface-mount capacitors. Supply lines can be combined into single drain and single gate bias sources to minimize external component count and simplify power supply routing. The recommended single power supply source is 3 V (V_{Dx} = V_{D1}/V_{D2} and V_{D3}/V_{D4} = 3 V). Alternatively, 2 V and 4 V power supply sources can be used for V_{D1}/V_{D2} and V_{D3}/V_{D4}, respectively.

The HMC8325 uses several amplifier stages. All stages use depletion mode, pseudomorphic high electron mobility transfer (pHEMT) transistors. Therefore, follow the following recommended bias sequence during power-up of the devices to ensure that damage does not occur.

1. Apply −2 V bias to V_{Gx} (V_{G1} and V_{G2} to V_{G3} and V_{G4}).
2. Apply 3 V bias to V_{Dx} (V_{D1} and V_{D2} to V_{D3} and V_{D4}).
3. Adjust V_{G1}/V_{G2} to V_{G3}/V_{G4} between −2 V and 0 V to achieve a total drain current (I_{Dx}) of 50 mA.
4. Apply the RF input signal.

The recommended bias sequence during power-down of the device is as follows:

1. Turn off the RF input signal.
2. Turn off the V_{Dx} (V_{D1} and V_{D2} to V_{D3} and V_{D4}) voltage supply or set it to 0 V.
3. Turn off the V_{Gx} (V_{G1} and V_{G2} to V_{G3} and V_{G4}) voltage supply.

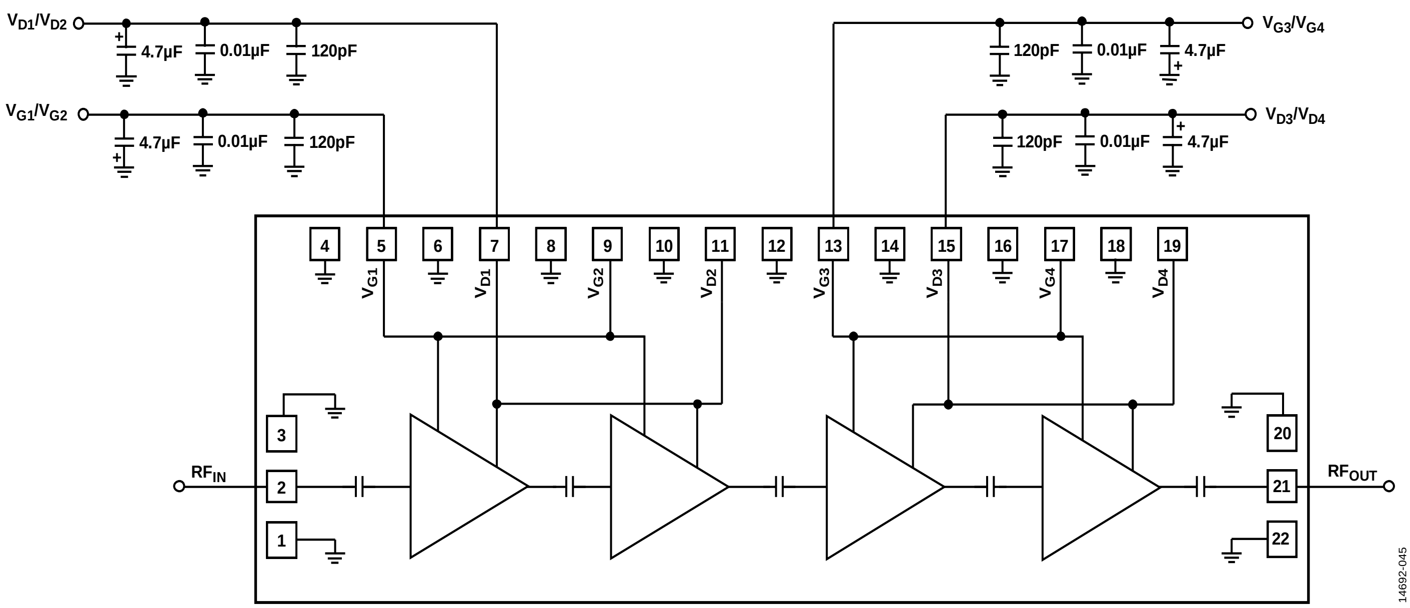

Figure 45. Typical Application Circuit (Two Power Supply Source Configuration)

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GAAS MMICS

Attach the die directly to the ground plane eutectically or with conductive epoxy.

To bring RF to and from the chip, use 50 Ω microstrip transmission lines on 0.127 mm (0.005”) thick, alumina thin film substrates (see Figure 46).

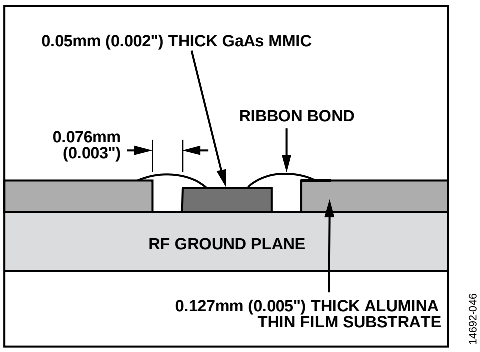

Figure 46. Routing RF Signals

To minimize bond wire length, place microstrip substrates as close to the die as possible. Typical die to substrate spacing is 0.076 mm to 0.152 mm (0.003” to 0.006”).

HANDLING PRECAUTIONS

To avoid permanent damage, adhere to the following storage, cleanliness, static sensitivity, transient, and general handling precautions.

Storage

All bare die ship in either waffle or gel-based ESD protective containers, sealed in an ESD protective bag. After opening the sealed ESD protective bag, all die must be stored in a dry nitrogen environment.

Cleanliness

Handle the chips in a clean environment. Never use liquid cleaning systems to clean the chip.

Static Sensitivity

Follow ESD precautions to protect against ESD strikes.

Transients

Suppress instrument and bias supply transients while bias is applied. To minimize inductive pickup, use shielded signal and bias cables.

General Handling

Handle the chip on the edges only using a vacuum collet or with a sharp pair of bent tweezers. Because the surface of the chip has fragile air bridges, never touch the surface of the chip with a vacuum collet, tweezers, or fingers.

MOUNTING

The chip is back metallized and can be die mounted with gold/tin (AuSn) eutectic preforms or with electrically conductive epoxy. The mounting surface must be clean and flat.

Eutectic Die Attach

It is best to use an 80% gold/20% tin preform with a work surface temperature of 255°C and a tool temperature of 265°C. When hot 90% nitrogen/10% hydrogen gas is applied, maintain a tool tip temperature of 290°C. Do not expose the chip to a temperature greater than 320°C for more than 20 sec. No more than 3 sec of scrubbing is required for attachment.

Epoxy Die Attach

The ABLEBOND 84-1LMIT is recommended for die attachment. Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after placing it into position. Cure the epoxy per the schedule provided by the manufacturer.

WIRE BONDING

RF bonds made with 3 mil (0.0762 mm) × 0.5 mil (0.0127 mm) gold ribbon are recommended. Thermosonically bond these bonds with a force of 40 grams to 60 grams. DC bonds of 1 mil (0.0254 mm) diameter, thermosonically bonded, are recommended. Create ball bonds with a force of 40 grams to 50 grams and wedge bonds with a force of 18 grams to 22 grams. Create all bonds with a nominal stage temperature of 150°C. Apply a minimum amount of ultrasonic energy to achieve reliable bonds. Keep all bonds as short as possible, less than 12 mil (0.31 mm).

ASSEMBLY DIAGRAM

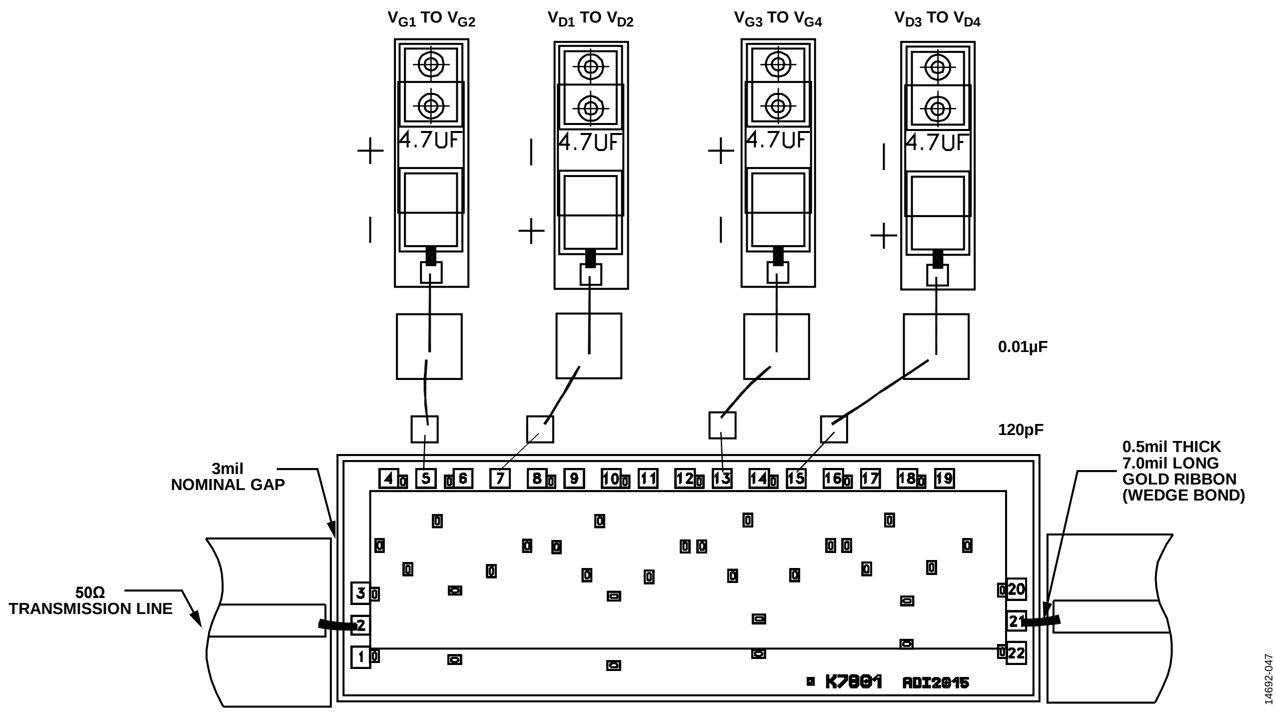

Figure 47. Assembly Diagram

OUTLINE DIMENSIONS

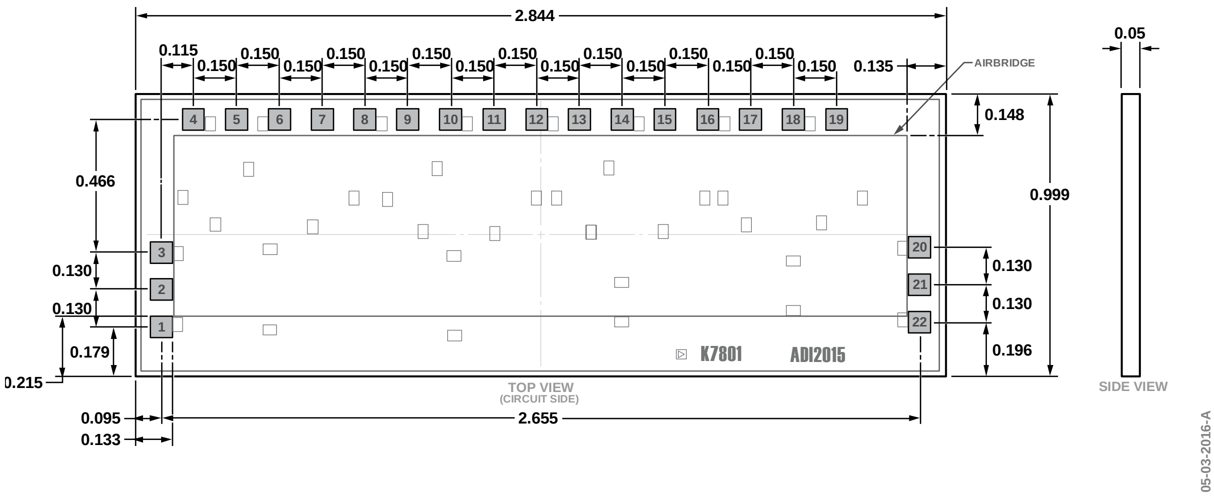

Figure 48. 22-Pad Bare Die [CHIP]
(C-22-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
HMC8325	−55°C to +85°C	22-Pad Bare Die [CHIP]	C-22-1
HMC8325-SX	−55°C to +85°C	22-Pad Bare Die [CHIP]	C-22-1

[1] The HMC8325-SX is two pairs of the die in a gel pack for the sample orders.
[2] This is a waffle pack option; contact Analog Devices, Inc., for additional packaging options.