

FEATURES

- Propagation delay: 88 ps**
- Propagation delay at 50 mV overdrive: 20 ps**
- Minimum detectable pulse width: 60 ps**
- Differential latch control**
- Power dissipation: 240 mW**
- 16-terminal 2.9 mm × 2.9 mm LCC package**

APPLICATIONS

- Automatic test equipment (ATE)**
- High speed instrumentation**
- Clock and data restoration**
- Semiconductor test systems**
- Threshold detection in electronic warfare systems**

GENERAL DESCRIPTION

The [HMC974LC3C](#) is a silicon germanium (SiGe) monolithic, ultra fast window comparator that features reduced swing positive emitter-coupled logic (RSPECL) output drivers that are level latched. Three output ports detect whether an analog input signal is above, below, or between two reference levels supplied at the input (see Figure 2).

FUNCTIONAL BLOCK DIAGRAM

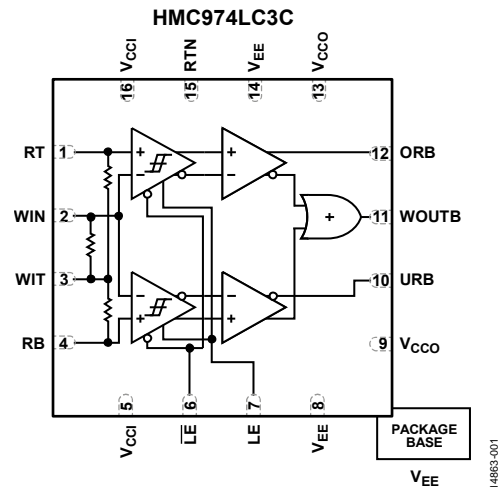


Figure 1.

The outputs are single-ended negative logic. Incorporating two proven comparators at the input provides good dc and dynamic matching and reduces the input capacitance. The reduced swing output stages are designed to directly drive 400 mV into 50 Ω terminated to a voltage ($V_{\text{TERM}} = V_{\text{CC0}} - 2 \text{ V}$).

The [HMC974LC3C](#) features high speed latches that can either be enabled to latch the output data or left in the track mode to implement a tracking window comparator.

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REVISION HISTORY

4/2018—Rev. D to Rev. E

Changes to WOUTB Parameter, Unit Column, Table 1 and URB and ORB Parameter, Unit Column, Table 1	3
Changes to Ordering Guide	12

6/2017—Rev. C to Rev. D

Changes to Table 1.....	3
Added Maximum Peak Reflow Temperature Parameter, Table 2	5
Updated Outline Dimensions	12
Changes to Ordering Guide	12

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

3/2017—v04.0616 to Rev. C

Updated Format.....	Universal
Changes to General Description	1
Changes to Table 1.....	3
Added Negative Supply (V_{EE} to GND) Parameter, Table 2	5
Changes to Table 3.....	5
Added Theory of Operation Section, Power Sequencing Section, and Table 4.....	9
Added Applications Information Section	
Changes to Evaluation Board Section and Table 5	10
Updated Outline Dimensions.....	12
Changes to Ordering Guide	12

SPECIFICATIONS

$T_A = 25^\circ\text{C}$, $V_{EE} = -3\text{ V}$, $V_{CCI} = 3.3\text{ V}$, $V_{CCO} = 2\text{ V}$, $V_{TERM} = 0\text{ V}$, $V_{CM} = 0\text{ V}$, $V_{OD} = 50\text{ mV}$. V_{OD} is the input overdrive voltage, for example, $V_{WIN} - V_{RT} = V_{OD}$ or $V_{WIN} - V_{RB} = V_{OD}$.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC INPUT CHARACTERISTICS					
Offset Voltage	-10	±4	+10	mV	WIT pin termination open Measured between the WIN pin voltage and the RT pin voltage or RB pin voltage
Bias Current	-30	+20	+30	µA	
Differential Voltage	-2		+2	V	
Input Impedance					
WIN Pin to WIT Pin		50		Ω	
RT Pin to WIT Pin		50		Ω	
RB Pin to WIT Pin		50		Ω	
Common-Mode Input Voltage Range	-1.5		+1.5	V	WIT to GND
Input Capacitance			1	pF	
LATCH ENABLE CHARACTERISTICS					
LE and $\overline{\text{LE}}$					If not driven, the device is unlatched
Input Low Voltage (V_{IL})			1.6	V	
Input High Voltage (V_{IH})	2.2			V	
LE and $\overline{\text{LE}}$ Impedance		7.8		kΩ	
DC OUTPUT CHARACTERISTICS					
Output Voltage					
High Level, V_{OH} (50 Ω to 0 V)		1.06		V	
Low Level, V_{OL} (50 Ω to 0 V)		0.73		V	
Output Voltage Swing					
WOUTB	300	360	420	mV	
URB and ORB	320	380	440	mV	
AC PERFORMANCE					
Propagation Delay Dispersion vs. V_{OD}		20		ps	For $V_{OD} > 50\text{ mV}$
Rise Time (ORB, WOUTB, URB), t_R		25.3		ps	20% to 80%
Fall Time (ORB, WOUTB, URB), t_F		21.9		ps	80% to 20%
Minimum Detectable Pulse Width		60		ps	$V_{CM} = 0\text{ V}$; ±100 mV overdrive voltage
Equivalent Input Bandwidth ¹		11		GHz	
Input to Output Delay, t_{PD}		88		ps	
Latch to Output Delay, t_{PD}		83		ps	
Maximum Input Slew Rate		5		V/ns	
Noise (Referred to Input)		6		nV/√(Hz)	
Random Jitter (rms)		0.2		ps rms	At 5 Gbps with ±100 mV overdrive
Deterministic Jitter (Peak to Peak)		2		ps	At 5 Gbps with ±100 mV overdrive
POWER SUPPLIES (INCLUDING LOAD)					
Positive Supply Voltage Input Stage (V_{CCI})	3.135	3.3	3.465	V	
Positive Supply Voltage Output Stage (V_{CCO})	1.8	3.3	3.465	V	
Negative Power Supply (V_{EE})	-3.15	-3.0	-2.85	V	
Positive Supply Current Input Stage (I_{CCI})	10	15	20	mA	
Positive Supply Current Output Stage (I_{CCO})	60	70	80	mA	
Negative Current (I_{EE})	21	31	41	mA	
Power Dissipation (P_D)		240		mW	

¹ Equivalent input bandwidth is calculated with the following formula: $B_{WEQ} = 0.22/\sqrt{(TR_{COMP}^2 - TR_{IN}^2)}$, where B_{WEQ} is the equivalent bandwidth formula, TR_{IN} is the 20% to 80% transition time of a quasi Gaussian signal applied to the comparator input, and TR_{COMP} is the effective transition time digitized by the comparator.

TIMING DIAGRAM

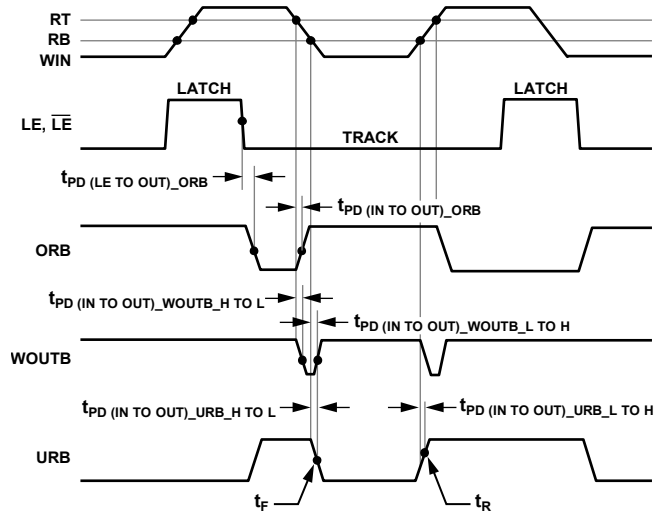


Figure 2. Timing Diagram

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ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Input Supply Voltage (V_{CCI} to GND)	-0.5 V to +4 V
Output Supply Voltage (V_{CCO} to GND)	-0.5 V to +4 V
Positive Supply Differential ($V_{CCI} - V_{CCO}$)	-0.5 V to +3 V
Negative Supply (V_{EE} to GND)	-3.3 V to +0.5 V
Input Voltage	-2 V to +2 V
Differential Input Voltage	-2 V to +2 V
Output Current	40 mA
Junction Temperature	125°C
Continuous Power Dissipation ($T = 85^\circ\text{C}$; Derate 20.4 mW/°C Above 85°C)	0.816 W
Thermal Resistance (θ_{JC})	49°C/W
Maximum Peak Reflow Temperature ¹	
Moisture Sensitivity Level 1 (MSL1) and Moisture Sensitivity Level 3 (MSL3)	260°C
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C
Electrostatic Discharge (ESD) Sensitivity Human Body Model	Class 1B

¹ See the Ordering Guide section.

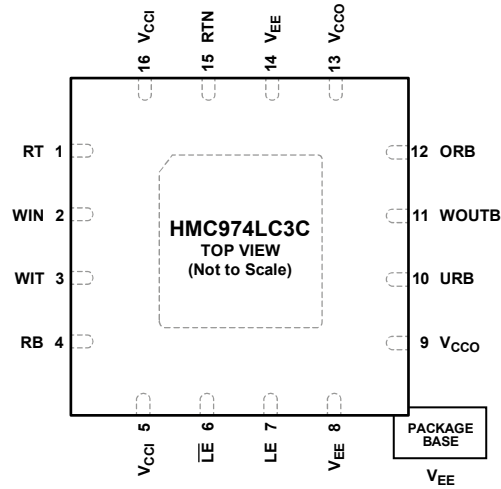
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
 1. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO VEE.

Figure 3. Pin Configuration

14883-003

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RT	Termination Resistor for Reference Top.
2	WIN	Analog Input Window.
3	WIT	Common Mode Window for Termination Resistors.
4	RB	Termination Resistor Return for Reference Bottom.
5, 16	VCCI	Positive Supply Voltage Input Stage.
6	\overline{LE}	Inverting Latch Enable Input.
7	LE	Noninverting Latch Enable Input.
8, 14	VEE	Negative Power Supply
9, 13	VCCO	Positive Supply Voltage Output Stage.
10	URB	Underrange Output. URB is asserted low when the analog input voltage is below the RB pin voltage.
11	WOUTB	Window Output. WOUTB is asserted low when the analog input voltage is between the RB pin voltage and the RT pin voltage.
12	ORB	Ovrerange output. ORB is asserted low when the analog input voltage range is above the RT pin voltage.
15	RTN	ESD Protection Return.
	EPAD	Exposed Pad. The exposed pad must be connected to VEE.

INTERFACE SCHEMATICS

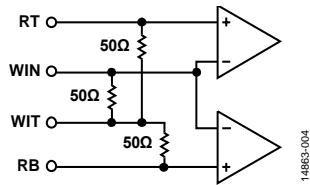


Figure 4. Interface Schematic for RT, RB, WIN, and WIT

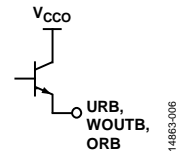


Figure 6. Interface Schematic for URB, WOUTB, and ORB

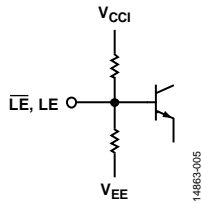


Figure 5. Interface Schematic for LE and LE-bar

TYPICAL PERFORMANCE CHARACTERISTICS

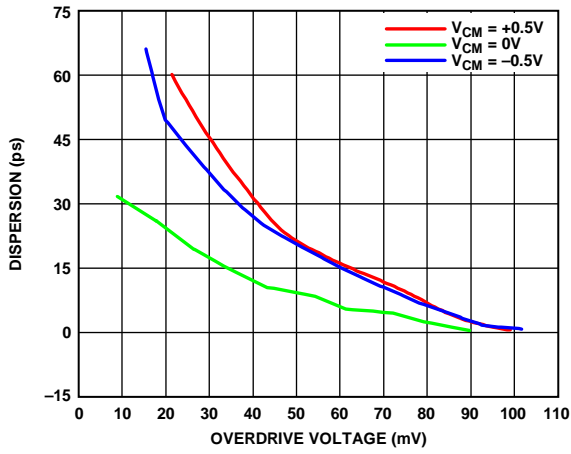


Figure 7. Dispersion vs. Overdrive Voltage

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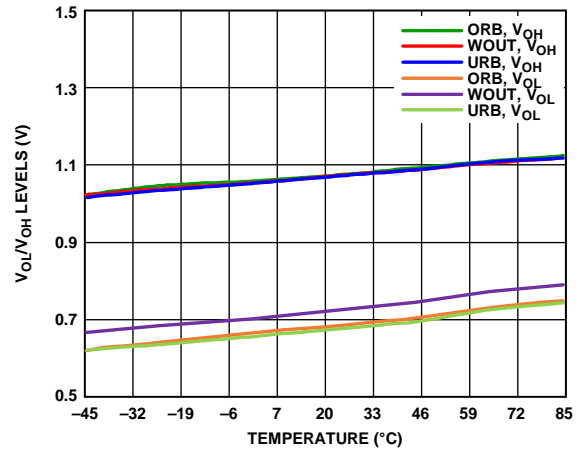


Figure 10. V_{OL}/V_{OH} Levels vs. Temperature

14863-010

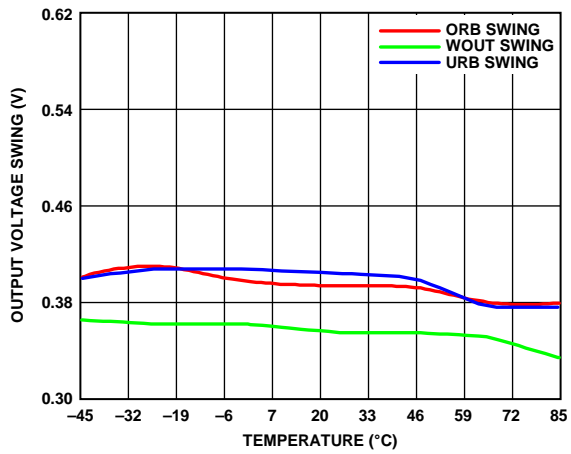


Figure 8. Output Voltage Swing vs. Temperature

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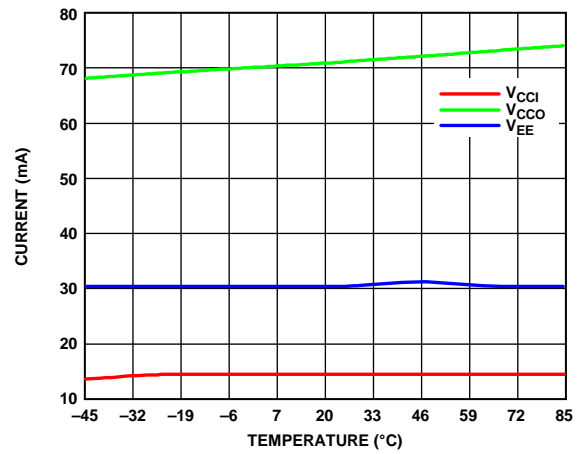


Figure 11. Power Supply Currents

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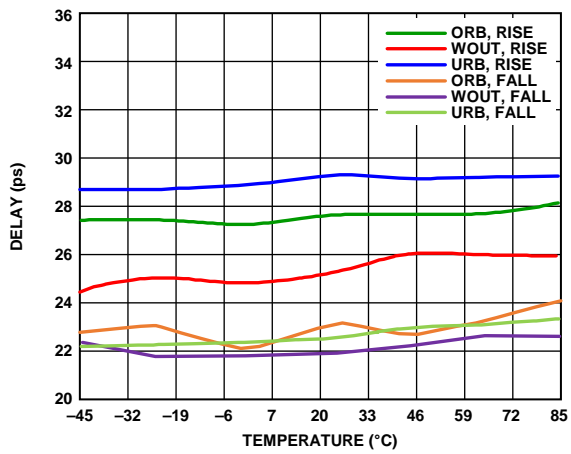


Figure 9. Output Rise and Fall Time

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THEORY OF OPERATION

The HMC974LC3C is a window comparator where the range of the window is defined with RT as the top of the voltage window range and RB as the bottom of the voltage window range. The comparator has two modes of operation: track mode and latch mode. While in track mode, the comparator determines three things:

1. If the signal is below the window voltage value, RT, and above the window voltage value, RB, represented by the WOUTB output.
2. If the signal is above the window voltage value RT, which is represented by the ORB output.
3. If the signal is below the window voltage value RB, which is represented by the URB output.

A typical 5 Gbps output eye is shown in Figure 12 with specific details outlined in Table 4.

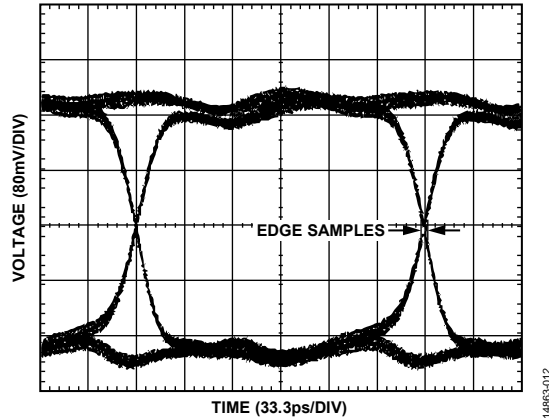


Figure 12. Eye Diagram at 5 Gbps

Table 4. Eye Diagram Details

Parameter	Value
Bit Rate	5 Gbps
Pattern Length	$2^{15} - 1$
Deterministic Jitter (Peak-to-Peak)	2.15 ps
Vertical Scale	80 mV/div
Time Scale	33.3 ps/div

POWER SEQUENCING

Use the following supplies sequentially to power up the device:

1. V_{EE}
2. V_{CCI} and V_{CCO} (if $V_{CCO} = V_{CCI}$)
3. V_{CCO} (if different than ground)

The power-down sequence is the reverse of the previous sequence:

1. V_{CCO} (if different than ground)
2. V_{CCI} and V_{CCO} (if $V_{CCO} = V_{CCI}$)
3. V_{EE}

Apply power to the HMC974LC3C before applying the input signals (WIN and WIT) and remove the input signals (WIN and WIT) prior to powering it down.

APPLICATIONS INFORMATION

EVALUATION BOARD

The [HMC974LC3C](#) evaluation printed circuit board (PCB) must use RF circuit design techniques. Signal lines must have 50 Ω impedance while the package ground leads must connect directly to the ground plane of the PCB. The exposed metal package base must connect to V_{EE}. Ensure the top and bottom ground planes connect together with via holes. The evaluation PCB shown in Figure 13 is available from Analog Devices, Inc., upon request.

Figure 14 shows the [EVAL-HMC974LC3C](#) schematic. Figure 15 shows the typical application circuit.

Table 5. Bill of Materials

Reference Designator	Description
J1	Eight-position vertical header
J2 to J7	K connector, SRI
J8	Terminal strip, single row, 3-pin
JP1, JP2	Two position vertical header
C1 to C3, C5, C6, C8 to C10, C15	100 pF capacitor, 0402
C4, C7, C11	330 pF capacitor, 0402
C12 to C14	4.7 μF tantalum capacitor
TP1 to TP4	DC pin
U1	HMC974LC3C window comparator
PCB	EVAL-HMC974LC3C evaluation board, circuit board material is either Rogers 4350 or Arlon 25FR

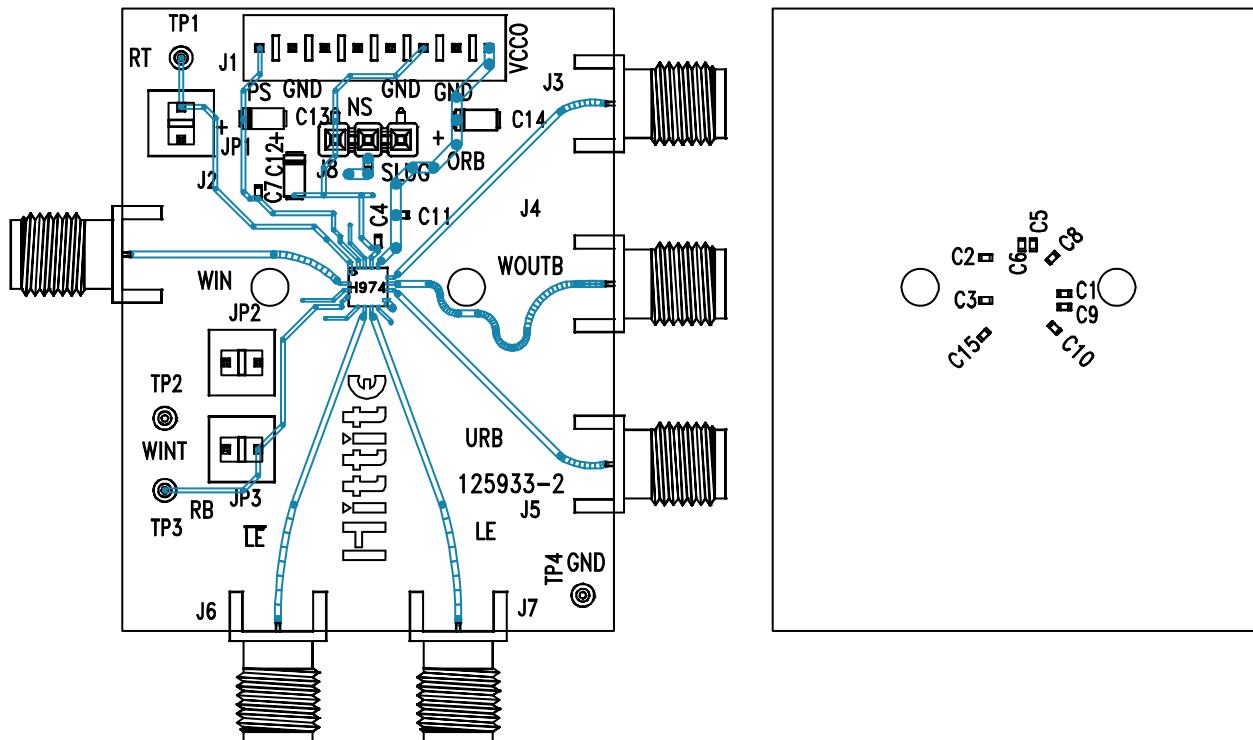


Figure 13. Evaluation Printed Circuit Board

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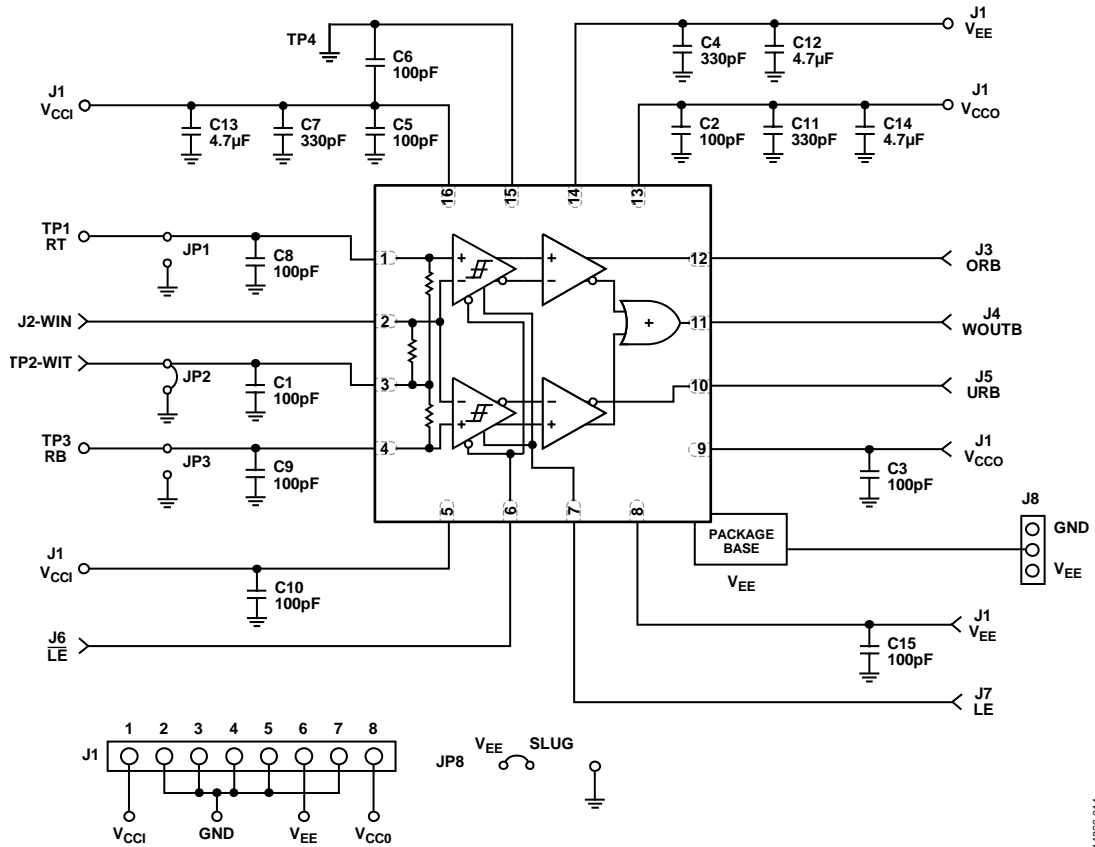


Figure 14. Evaluation Board Schematic

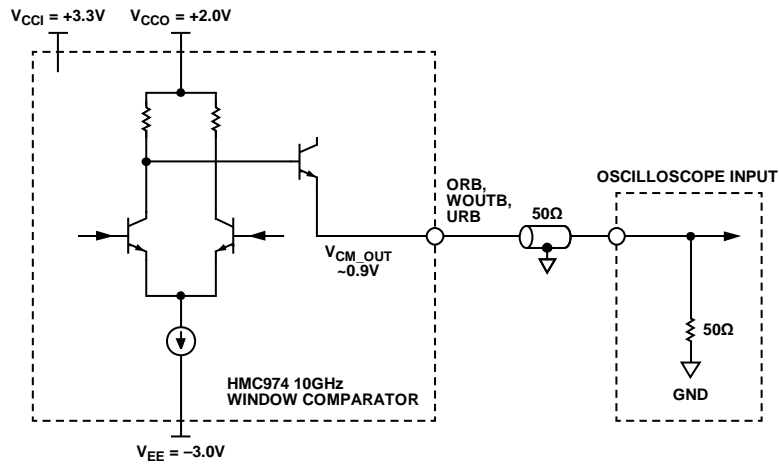


Figure 15. Typical Application Circuit

OUTLINE DIMENSIONS

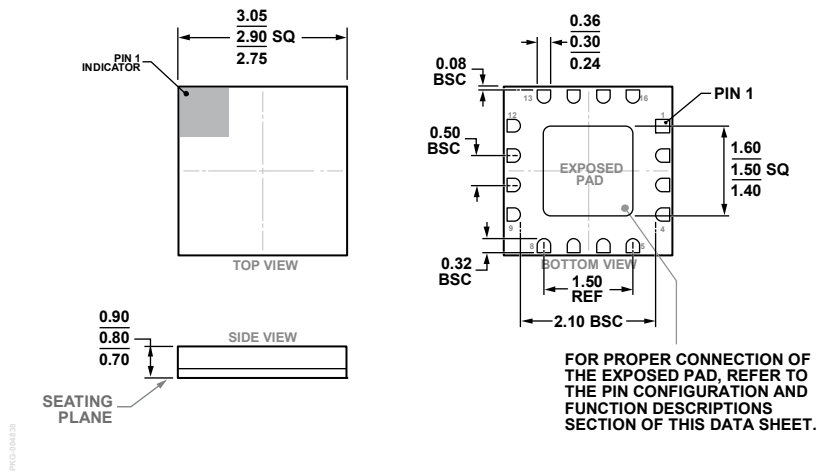


Figure 16. 16-Terminal Ceramic Leadless Chip Carrier [LCC] (E-16-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	MSL Rating ²	Package Description ³	Package Option
HMC974LC3C	-40°C to +85°C	MSL3	16-Terminal Ceramic Leadless Chip Carrier [LCC]	E-16-1
HMC974LC3CTR	-40°C to +85°C	MSL3	16-Terminal Ceramic Leadless Chip Carrier [LCC]	E-16-1
HMC974LC3CTR-R5	-40°C to +85°C	MSL3	16-Terminal Ceramic Leadless Chip Carrier [LCC]	E-16-1
129538-HMC974LC3C			Evaluation Board	

¹ The HMC974LC3C, the HMC974LC3CTR, and the HMC974LC3CTR-R5 are RoHS Compliant Parts.

² See the Absolute Maximum Ratings section.

³ Alumina and white package body material with a gold over nickel lead finish.

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[AZV331KSTR-G1](#) [LTC1841IS8#PBF](#) [LTC1440CN8#PBF](#) [LTC1542CS8#PBF](#) [LTC1445CS#PBF](#) [TL331VSN4T3G](#) [LT6700IDCB-](#)
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