High Speed ADC USB FIFO Evaluation Kit

HSC-ADC-EVALB

FEATURES

Buffer memory board for capturing digital data used with high speed ADC evaluation boards to simplify evaluation
32 kB FIFO depth at 133 MSPS (upgradable)
Measures performance with ADC Analyzer™
Real-time FFT and time domain analysis
Analyze SNR, SINAD, SFDR, and harmonics
Simple USB port interface (2.0)
Supporting ADCs with serial port interfaces (SPI)
On-board regulator circuit, no power supply required
6 V, 2 A switching power supply included
Compatible with Windows 98 (2nd ed.), Windows 2000, Windows ME, and Windows XP

EQUIPMENT NEEDED

Analog signal source and antialiasing filter
Low jitter clock source
High speed ADC evaluation board and ADC data sheet
PC running Windows 98 (2nd ed.), Windows 2000, Windows ME, or Windows XP
Latest version of ADC Analyzer
USB 2.0 (USB 1.1-compatible) port recommended

PRODUCT DESCRIPTION

The high speed ADC FIFO evaluation kit includes the latest version of ADC Analyzer and a buffer memory board to capture blocks of digital data from the Analog Devices, Inc., high speed analog-to-digital converter (ADC) evaluation boards. The FIFO board is connected to the PC through a USB port and is used with ADC Analyzer to quickly evaluate the performance of high speed ADCs. Users can view an FFT for a specific analog input and encode rate to analyze SNR, SINAD, SFDR, and harmonic information.

The evaluation kit is easy to set up. Additional equipment needed includes an Analog Devices high speed ADC evaluation board, a signal source, and a clock source. Once the kit is connected and powered, the evaluation is enabled instantly on the PC.

The HSC-ADC-EVALB-DCZ can be used with single and multi-channel ADCs and converters with demultiplexed digital outputs.

PRODUCT HIGHLIGHTS

1. Easy to Set Up. Connect the included power supply and signal sources to the two evaluation boards. Then connect to the PC and instantly evaluate the performance.

FUNCTIONAL BLOCK DIAGRAM

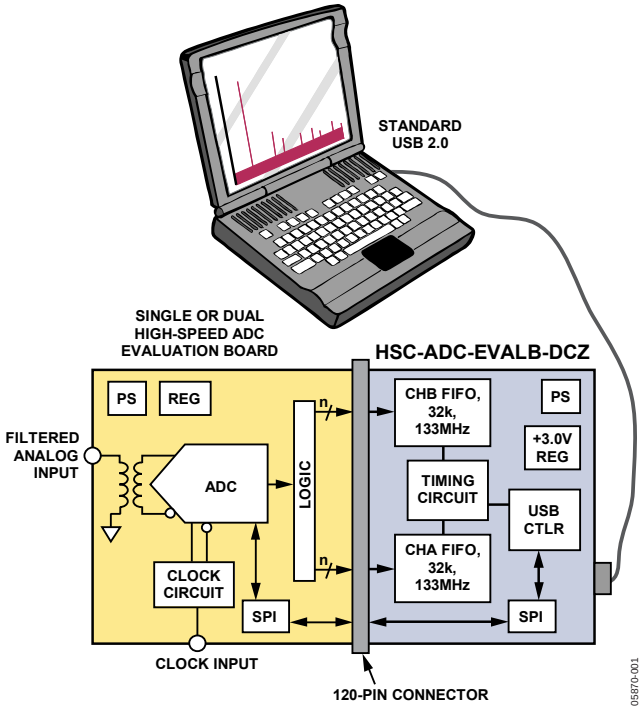

Figure 1.

2. ADIsimADC™. ADC Analyzer supports virtual ADC evaluation using Analog Devices proprietary behavioral modeling technology. This allows rapid comparison between multiple ADCs, with or without hardware evaluation boards. For more information, see the AN-737 Application Note at www.analog.com/ADIsimADC.
3. USB Port Connection to PC. The PC interface is a USB 2.0 (1.1-compatible) connection. A USB cable is provided in the kit.
4. FIFO of 32 kB. The FIFO stores data from the ADC for processing. A pin-compatible FIFO family is used for easy upgrading.
5. Up to 133 MSPS Encode Rate on Each Channel. Single-channel ADCs with encode rates of up to 133 MSPS can be used with the FIFO board. Multichannel and demultiplexed output ADCs can also be used with the FIFO board with clock rates up to 266 MSPS.
6. Supports ADC with Serial Port Interface (SPI). Some ADCs include a feature set that can be changed via the SPI. The FIFO supports these features through the existing USB connection to the computer without requiring additional cabling.

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REVISION HISTORY

7/07—Rev. 0 to Rev. A

Deleted HSC-ADC-EVALB-SC ..... Universal
Changes to Table 1 8
Added the Connecting to the HSC-ADC-AD922xFFA or HSC-ADC-AD9283FFA Adapter Boards Section 8
Changes to the Connecting to the HSC-ADC-DEMUX Adapter Board Section 8
Added the Connecting ADC Evaluation Boards with Double Row Connectors Section 8
Added Figure 4 and Figure 5 8
Added Figure 7 12
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2/06—Revision 0: Initial Version

QUICK START GUIDE: FIFO EVALUATION BOARD

REQUIREMENTS

- FIFO evaluation board, ADC Analyzer, and USB cable
- High speed ADC evaluation board and ADC data sheet
- Power supply for ADC evaluation board
- Analog signal source and appropriate filtering
- Low jitter clock source applicable for specific ADC evaluation, typically <1 ps rms
- PC running Windows® 98 (2nd ed.), Windows 2000, Windows ME, or Windows XP
- PC with a USB 2.0 (USB 1.1-compatible) port recommended

QUICK START STEPS

Note that you need administrative rights for the Windows operating systems during the entire easy start procedure. It is recommended to complete all steps before reverting to a normal user mode.

1. Install ADC Analyzer from the CD provided in the FIFO evaluation kit or download the latest version from the Web. For the latest software updates, check the Analog Devices website at www.analog.com/hsc-FIFO.
2. Connect the FIFO evaluation board to the ADC evaluation board. If an adapter is required, insert the adapter between the ADC evaluation board and the FIFO board. Connect the evaluation board to the bottom two rows of the 120-pin connector, closest to the installed IDT FIFO chip. If using an ADC with a SPI interface, remove the two 4-pin corner keys so that the third row can be connected.
3. Connect the provided USB cable to the FIFO evaluation board and to an available USB port on the computer.
4. Refer to Table 4 to make necessary jumper changes. Most evaluation boards can be used with the default settings.
5. After verification of the first four steps, connect the appropriate power supplies to the ADC evaluation boards. The FIFO evaluation board is supplied with a wall-mountable switching power supply that provides a 6 V, 2 A maximum output. Connect the supply end to the rated 100 V ac to 240 V ac wall outlet at 47 Hz to 63 Hz. The other end is a 2.1 mm inner diameter jack that connects to the PCB at J301. Refer to the instructions included in the ADC data sheet (at www.analog.com) for more information about the ADC evaluation board's power supply and other requirements.
6. Once the cable is connected to both the computer and the FIFO board and power is supplied, the USB drivers start to install. To complete the total installation of the FIFO drivers, you need to complete the new hardware sequence two times.

   The first time, the **Found New Hardware Wizard** opens with the text message **This wizard helps you install software for…Pre-FIFO 4.1.** Click the recommended install, and go to the next screen. A hardware installation warning window displays. Click **Continue Anyway**. The next window that opens finishes the pre-FIFO 4.1 installation. Click **Finish**.

   The **Found New Hardware Wizard** dialog box opens for the second time, but with the text message **This wizard helps you install software for…Analog Devices FIFO 4.1** displayed. Click the recommended install, and go to the next screen. Again, a hardware installation warning window displays. Click **Continue Anyway**. Then click **Finish** on the next two windows. This completes the installation.
7. (Optional) Verify in the device manager that Analog Devices FIFO 4.1 is listed under the USB hardware.
8. Apply power to the evaluation board and check the voltage levels at the board level.
9. Connect the appropriate analog input (which should be filtered with a band-pass filter) and low jitter clock signal. Make sure that the evaluation boards are powered on before connecting the analog input and clock.
10. Start ADC Analyzer.
11. Choose an existing configuration file for the ADC evaluation board or create a new one.
12. Click **Time Data** (the leftmost button under the menus) in ADC Analyzer. A reconstruction of the analog input is displayed. If the expected signal does not appear, or if there is only a flat red line, refer to the ADC Analyzer data sheet at www.analog.com/hsc-FIFO for more information.

QUICK START GUIDE: VIRTUAL EVALUATION USING ADIsimADC

REQUIREMENTS

- Complete installation of ADC Analyzer, Version 4.8.2 or later.
- Download ADIsimADC product model files for the desired converter. (Models are not installed with the software, but they can be downloaded from the ADIsimADC Virtual Evaluation Board website at no charge.)

Note that no hardware is required to virtually evaluate an ADC using ADIsimADC. However, if you wish to compare these results to those using a real evaluation board, you can easily switch between the two, as outlined in the following Quick Start Steps section.

QUICK START STEPS

1. Visit www.analog.com/ADIsimADC and download the ADC model files of interest to a local drive. The default location is c:\program files\adc_analyzer\models.
2. Start ADC Analyzer (see the *ADC Analyzer User Manual*).
3. From the menu, click **Config** > **Buffer** > **Model** as the buffer memory. In effect, the model functions in place of the ADC and data capture hardware.
4. After selecting the model, click **Model** (located next to the **Stop** button) to select and configure which converter is to be modeled. A dialog box appears in the workspace, where you can select and configure the behavior of the model.
5. In the **ADC Modeling** dialog box, click the **Device** tab and then click **… (Browse)**, which is the button adjacent to the open box in the dialog window. This opens a file browser and displays all of the models found in the default directory: c:\program files\adc_analyzer\models. If no model files are found, follow the on-screen directions or repeat Step 1 to install the available models. If you have saved the models somewhere other than the default location, use the browser to navigate to that location and select the file of interest.
6. From the menu, click **Config** > **FFT**. In the FFT Configuration dialog box, ensure that the **Encode Frequency** is set to a valid rate for the simulated device under test. If set too low or too high, the model will not run.
7. Once a model has been selected, information about the model displays on the **Device** tab of the **ADC Modeling** dialog box. After ensuring that you have selected the correct model, click the **Input** tab. This lets you configure the input to the model. Click either **Sine Wave** or **Two Tone** for the input signal.
8. Click **Time Data** (the leftmost button under the pull-down menus). A reconstruction of the analog input is displayed**.** The model can now be used as a standard evaluation board would be.
9. The model supports additional features not found when testing a standard evaluation board. When using the modeling capabilities, it is possible to sweep either the analog amplitude or the analog frequency. Consult the *ADC Analyzer User Manual* at www.analog.com/hsc-FIFO for more information.

FIFO 4.1 DATA CAPTURE BOARD FEATURES

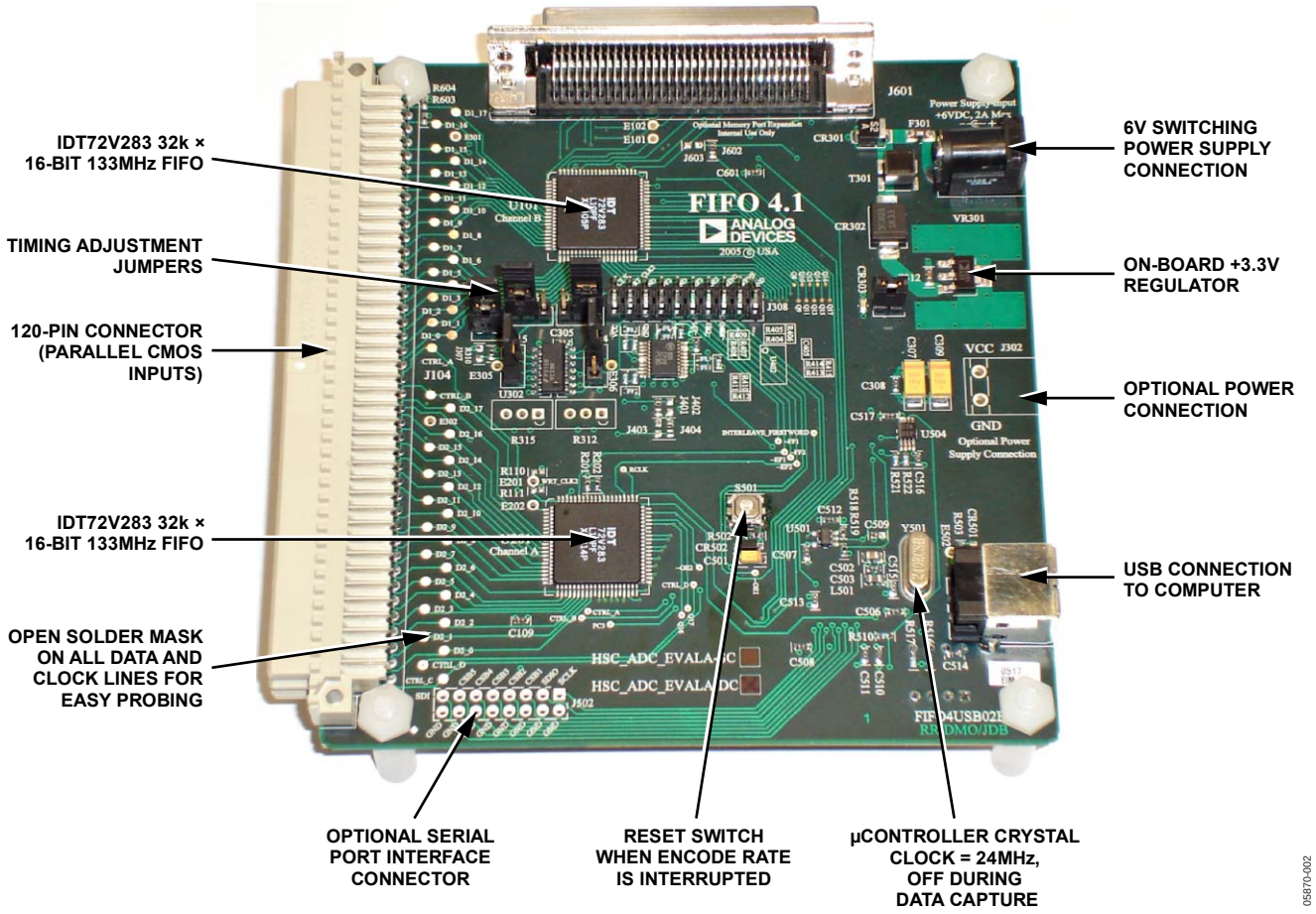


Figure 2. FIFO Components (Top View)

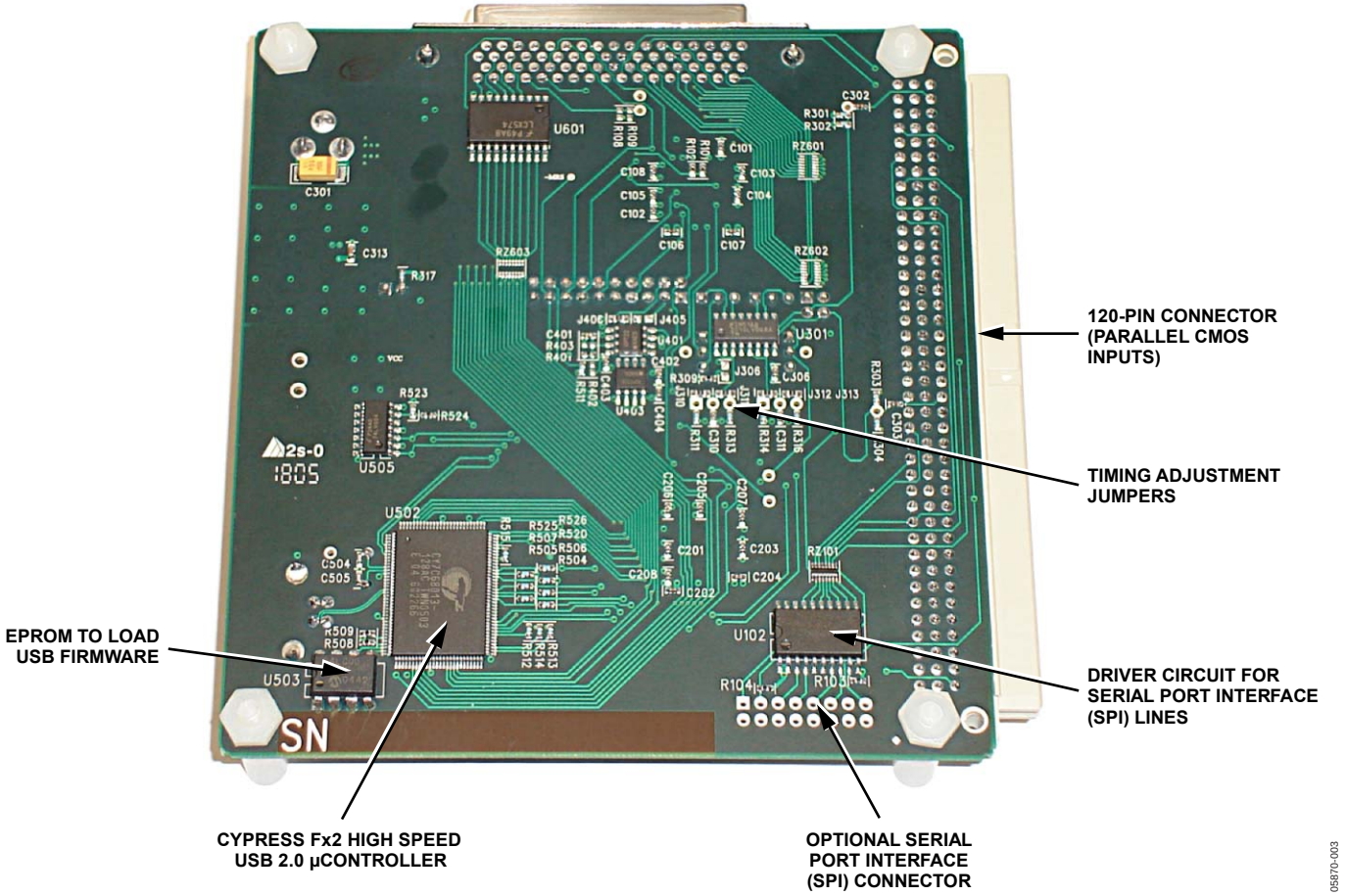


Figure 3. FIFO Components (Bottom View)

FIFO 4.1 SUPPORTED ADC EVALUATION BOARDS

All the evaluation boards that can be used with the high speed ADC FIFO evaluation kit can be found at www.analog.com/fifo. Some evaluation boards may require an adapter between the ADC evaluation board output connector and the FIFO input connector. If an adapter is needed, send an email to highspeed.converters@analog.com indicating the part number of the adapter, the ADC being used, and contact information.

THEORY OF OPERATION

The FIFO evaluation board can be divided into several circuits, each of which plays an important part in acquiring digital data from the ADC and allows the PC to upload and process that data. The evaluation kit is based on the IDT72V283 FIFO chip from Integrated Device Technology, Inc. (IDT). The system can acquire digital data at speeds of up to 133 MSPS and data record lengths of up to 32 kB using the HSC-ADC-EVALB-DCZ, which has two FIFO chips and is available to evaluate single and multi-channel ADCs or demultiplexed data from ADCs sampling faster than 133 MSPS. A USB 2.0 microcontroller communicating with ADC Analyzer allows for easy interfacing to newer computers using the USB 2.0 (USB 1.1-compatible) interface.

The process of filling the FIFO chip or chips and reading the data back requires several steps. First, ADC Analyzer initiates the FIFO chip fill process. The FIFO chips are reset using a master reset signal (MRS). The USB microcontroller is then suspended, which turns off the USB oscillator and ensures that it does not add noise to the ADC input. After the FIFO chips completely fill, the full flags from the FIFO chips send a signal to the USB microcontroller to wake up the microcontroller from suspend. ADC Analyzer waits for approximately 30 ms and then begins the readback process.

During the readback process, the acquisition of data from FIFO 1 (U201) or FIFO 2 (U101) is controlled via Signal OEA and Signal OEB. Because the data outputs of both FIFO chips drive the same 16-bit data bus, the USB microcontroller controls the OEA and OEB signals to read data from the correct FIFO chip. From an application standpoint, ADC Analyzer sends commands to the USB microcontroller to initiate a read from the correct FIFO chip, or from both FIFO chips in dual or demultiplexed mode.

CLOCKING DESCRIPTION

Each channel of the buffer memory requires a clock signal to capture data. These clock signals are normally provided by the ADC evaluation board and are passed along with the data through Connector J104 (Pin 37 for both Channel A and Channel B). If only a single clock is passed for both channels, they can be connected together by Jumper J303.

Jumpers J304 and J305 at the output of the LVDS receiver allow the output clock to be inverted by the LVDS receiver. By default, the clock outputs are inverted by the LVDS receiver.

The single-ended clock signal from each data channel is buffered and converted to a differential CMOS signal by two gates of a low voltage differential signal (LVDS) receiver, U301. This allows the clock source for each channel to be CMOS, TTL, or ECL.

The clock signals are ac-coupled by 0.1 µF capacitors. Potentiometer R312 and Potentiometer R315 allow for fine-tuning the threshold of the LVDS gates. In applications where fine-tuning the threshold is critical, these potentiometers can be replaced with a higher resistance value to increase the adjustment range. Resistors R301, R302, R303, R304, R311, R313, R314, and R316 set the static input to each of the differential gates to a dc voltage of approximately 1.5 V.

At assembly, Solder Jumper J310 to Solder Jumper J313 are set to bypass the potentiometer. For fine adjustment using the potentiometers, the solder jumpers must be removed and R312 and R315 must be populated.

U302, an XOR gate array, is included in the design to let users add gate delays to the clock paths of the FIFO memory chips. They are not required under normal conditions and are bypassed at assembly by Jumper J314 and Jumper J315. Jumper J306 and Jumper J307 allow the clock signals to be inverted through an XOR gate. In the default setting, the clocks are not inverted by the XOR gate.

These clock paths determine the WRT_CLK1 and WRT_CLK2 signals at each FIFO memory chip (U101 and U201). These timing options should let you choose a clock signal that meets the setup time and hold time requirements to capture valid data.

A clock generator can be applied directly to S1 and/or S3. This clock generator should be the same unit that provides the clock for the ADC. These clock paths are ac-coupled so that a sine wave generator can be used. DC bias can be adjusted by R301/R302 and R303/R304.

The DS90LV048A differential line receiver is used to square the clock signal levels applied externally to the FIFO evaluation board. The output of this clock receiver can either directly drive the write clock of the IDT72V283 FIFO(s), or first pass through the XOR gate timing circuitry previously described.

SPI DESCRIPTION

The Cypress IC (U502) supports the HSC SPI standard to allow programming of ADCs that have SPI-accessible register maps. U102 is a buffer that drives the 4-wire SPI (SCLK, SDI, SDO, CSB) through the 120-pin connector (J104) on the third or top row. (Note that CSB1 is the default CSB line used.) J502 is an auxiliary SPI connector that monitors the SPI signals connected directly to the Cypress IC. For more information on this and other functions, consult the user manual titled *Interfacing to High Speed ADCs via SPI* at www.analog.com/hsc-FIFO.

The SPI interface designed on the Cypress IC can communicate with up to five different SPI-enabled devices. The CLK and data lines are common to all SPI devices. The correct device is chosen to communicate by using one of the five active low chip select pins. This functionality is controlled by selecting a SPI channel in the software.

CLOCKING WITH INTERLEAVED DATA

ADCs with very high data rates can exceed the capability of a single buffer memory channel (~133 MSPS). These converters often demultiplex the data into two channels to reduce the rate

required to capture the data. In these applications, ADC Analyzer must interleave the data from both channels to process it as a single channel. The user can configure the software to process the first sample from Channel A, the second from Channel B, and so on, or vice versa. The synchronization circuit included in the buffer memory forces a small delay between the write enable signals (WENA and WENB) being sent to the FIFO memory chips (Pin 1, U101, and U201), ensuring that the data is captured in one FIFO before the other. Jumper J401 and Jumper J402 determine which FIFO receives WENA and which FIFO receives WENB.

CONNECTING TO THE HSC-ADC-FPGA-8Z

ADCs that have serial LVDS outputs require that another board, that is, the HSC-ADC-FPGA-8Z, be connected between the ADC evaluation board and the FIFO data capture card. This board converts the serial data into parallel CMOS so that the FIFO data capture card can accept the data. Refer to the HSC-ADC-FPGA data sheet at www.analog.com/hsc-FIFO for more detailed information on this board.

CONNECTING TO THE HSC-ADC-AD922xFFA OR HSC-ADC-AD9283FFA ADAPTER BOARDS

Older ADC evaluation boards, such as the AD9203, AD9220, AD9226, and AD9283, have different pinouts and therefore require that another board, that is, the HSC-ADC-AD922xFFA or HSC-ADC-AD9283FFA adapter board, be connected between the ADC evaluation board and the FIFO data capture card. This board routes the outputs of the ADC evaluation board to the correct locations on the FIFO board.

When connecting the HSC-ADC-AD922xFFA or HSC-ADC-AD9283FFA adapter board, connect the female connector to the ADC evaluation board, and then connect the male connector to the FIFO board. Next, ensure that the HSC-ADC-AD922xFFA or HSC-ADC-AD9283FFA adapter board connects to the data lines (Row A and Row B) of the FIFO board connector as shown in Figure 4. Email highspeed.converters@analog.com for more detailed information about this board.

CONNECTING TO THE HSC-ADC-DEMUX ADAPTER BOARD

The AD9480 and AD9430 ADCs have parallel LVDS outputs and require another board connected between the ADC evaluation board and the FIFO data capture card. This board converts parallel LVDS to parallel CMOS, using both channels of the FIFO data capture card. Email highspeed.converters@analog.com for more detailed information about this board.

CONNECTING ADC EVALUATION BOARDS WITH DOUBLE ROW CONNECTORS

The HSC-ADC-EVALA-SC/HSC-ADC-EVALA-DC (FIFO 4) was the predecessor to the HSC-ADC-EVALB-DCZ (FIFO 4.1) and had only an 80-pin, double row input connector. The FIFO 4.1 has a 120-pin, triple row input connector to allow connection with newer ADCs that have SPI. Two examples of connecting FIFO 4.1 to an older style ADC evaluation board are shown in Figure 4 and Figure 5.

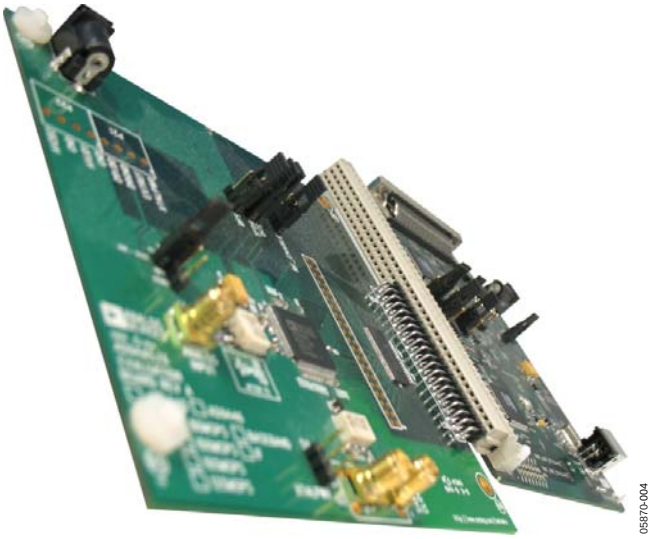


Figure 4. Single-Channel ADC

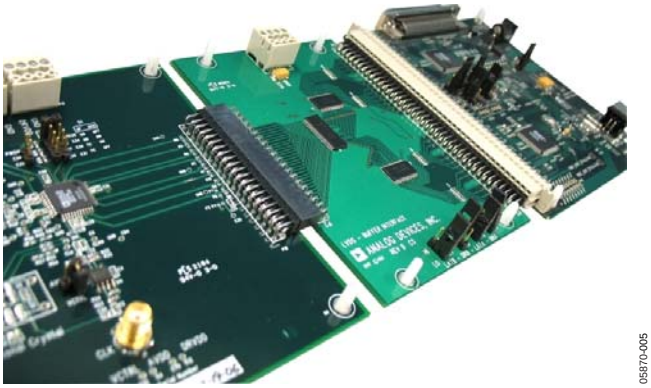


Figure 5. Dual-Channel ADC

UPGRADING FIFO MEMORY

The FIFO evaluation board includes two 32 kB FIFOs that are capable of 133 MHz clock signals. Pin-compatible FIFO upgrades are available from Integrated Device Technology. See Table 1 for the IDT part number matrix.

Table 1. IDT Part Number Matrix[1]

Part Number	FIFO Depth	FIFO Speed
IDT72V283L7-5PF (Default)	32 kB	133 MHz
IDT72V293L7-5PF	64 kB	133 MHz
IDT72V2103L7-5PF	132 kB	133 MHz
IDT72V2113L7-5PF	256 kB	133 MHz
IDT72V283L6PF	32 kB	166 MHz
IDT72V293L6PF	64 kB	166 MHz
IDT72V2103L6PF	132 kB	166 MHz
IDT72V2113L6PF	256 kB	166 MHz

[1] Visit the IDT website for more information.

JUMPERS

Use the information in Table 2 and Table 3 to configure the jumpers. On the FIFO evaluation board, Channel A is associated with the bottom IDT FIFO chip, and Channel B is associated with the top IDT FIFO chip (the one closest to the Analog Devices logo).

Table 2. Jumper Position Descriptions

Position	Description
In	Jumper in place (2-pin header)
Out	Jumper removed (2-pin header)
Position 1 or Position 3	Denotes the position of a 3-pin header. Position 1 is marked on the board.

Table 3. Solder Jumper Position Descriptions

Position	Description
In	Solder pads should be connected with a 0 Ω resistor
Out	Solder pads should not be connected with a 0 Ω resistor

DEFAULT SETTINGS

Table 4 lists the jumper settings to configure the data capture board for use with single-channel, multichannel, and interleaving ADCs. The ADC settings are shown in separate columns, as are the settings for the opposite (top) FIFO, U101, for a single-channel ADC. To align the timing properly, some evaluation boards require modifications to these settings. Refer to the Clocking Description section in the Theory of Operation section for more information.

Another way to easily configure the jumper settings for various configurations is to first consult ADC Analyzer's **Help** menu, selecting **About HSC_ADC_EVALB** from the menu, in order to determine the appropriate configuration setting for your application. Next, click **Setup Default Jumper Wizard** and choose the configuration setting that applies to the application of interest. A picture of the FIFO board is displayed for that application, providing a visual example of the correct jumper settings.

Table 4. Jumper Configurations

Jumper	Single-Channel Settings (Top)[1]	Single-Channel Settings, Default (Bottom)	Demultiplexed Settings	Dual-Channel Settings	Description
J303	In	In	Out	Out	Position 2 to Position 4, ties write clocks together
J304	In	In	In	In	Position 1 to Position 2, POS3: inverts clock out of DS90 (U301)
J305	In	In	In	In	Position 2 to Position 3, POS3: inverts clock out of DS90 (U301)
J306	Out	Out	Out	Out	No invert to encode clock from XOR (U302), 0 Ω resistor
J307	Out	Out	Out	Out	No invert to encode clock from XOR (U302), 0 Ω resistor
J310 to J313	In	In	In	In	All solder jumpers are shorted with 0 Ω resistors, (bypass level shifting to input of DS90)
J314	In	In	In	In	Position 1 to Position 2, one XOR gate timing delay for top FIFO (U101)
J315	In	In	In	In	Position 1 to Position 2, one XOR gate timing delay for bottom FIFO (U201)
J316	In	In	In	In	Power connected using switching power supply
J401	In	In	In	In	Controls if the top FIFO (U101) receives a write enable before or after bottom FIFO, 0 Ω resistor
J402	Out	Out	Out	Out	Controls if the top FIFO (U101) receives a write enable before or after bottom FIFO, 0 Ω resistor
J403	Out	Out	Out	Out	Controls if the bottom FIFO (U201) receives a write enable before or after the top FIFO, 0 Ω resistor
J404	In	In	In	In	Controls if the bottom FIFO (U201) receives a write enable before or after the top FIFO, 0 Ω resistor
J405	Out	Out	In	Out	When this jumper is in, WRT_CLK1 is used to create write enable signals for FIFOs, 0 Ω resistor (significant only for interleave mode)
J406	In	In	In	In	WRT_CLK2 is used to create write enable signals for FIFOs, 0 Ω resistor (significant only for interleave mode)

Jumper	Single-Channel Settings (Top)[1]	Single-Channel Settings, Default (Bottom)	Demultiplexed Settings	Dual-Channel Settings	Description
J503	In	In	In	In	Connect enable empty flag of top FIFO (U101) to USB MCU, 0 Ω resistor
J504	Out	Out	Out	Out	N/A
J505	In	In	In	In	Connect enable full flag of top FIFO (U101) to USB MCU, 0 Ω resistor
J506	Out	Out	Out	Out	N/A
J602	Out	Out	Out	Out	N/A
J603	In	In	In	In	N/A

[1] Some jumpers can be a 0 Ω resistor instead of a physical jumper. This is indicated in Table 4 in the jumper description column.

EVALUATION BOARD

The FIFO provides all of the support circuitry required to accept two channels of an ADC's digital parallel CMOS outputs. Each of the various functions and configurations can be selected by properly connecting various jumpers (see Table 4). When using this in conjunction with an ADC evaluation board, it is critical that the signal sources used for the analog input and clock have very low phase noise (<1 ps rms jitter) to realize the ultimate performance of the converter. Proper filtering of the analog input signal to remove harmonics and lower the integrated or broadband noise at the input is also necessary to achieve the specified noise performance.

See Figure 8 to Figure 18 for complete schematics and layout diagrams.

POWER SUPPLIES

The FIFO board is supplied with a wall-mountable switching power supply that provides a 6 V, 2 A maximum output. Connect the supply to the rated 100 V ac to 240 V ac wall outlet at 47 Hz to 63 Hz. The other end is a 2.1 mm inner diameter jack that connects to the PCB at J301. On the PC board, the 6 V supply is then fused and conditioned before connecting to the low dropout 3.3 V linear regulator that supplies the proper bias to the entire board.

When operating the evaluation board in a nondefault condition, J316 can be removed to disconnect the switching power supply. This enables the user to bias the board independently. Use P302 to connect an independent supply to the board. A 3.3 V supply is needed with at least a 1 A current capability.

CONNECTION AND SETUP

The FIFO board has a 120-pin (three rows of 40 pins each) connector that accepts two 16-bit channels of parallel CMOS inputs (see Figure 6). For those ADC evaluation boards that have only an 80-pin (two rows of 40 pins each) connector, it is pertinent that the lower two rows of the FIFO's triple row connector be connected in order for the data to pass to either FIFO channel correctly. The top, or third row, is used to pass SPI signals across to the adjacent ADC evaluation board that supports this feature.

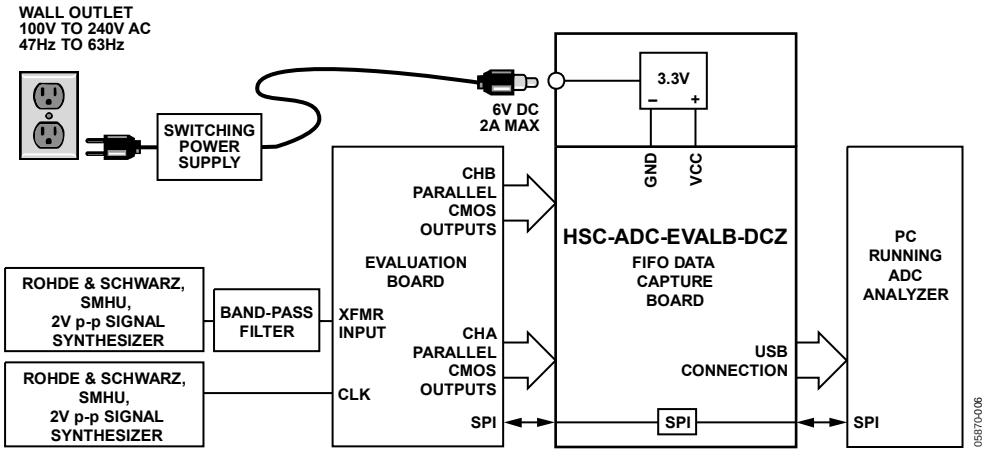


Figure 6. Example Setup Using Quad ADC Evaluation Board and FIFO Data Capture Board

FIFO SCHEMATICS AND PCB LAYOUT

PIN DEFINITIONS/ASSIGNMENTS

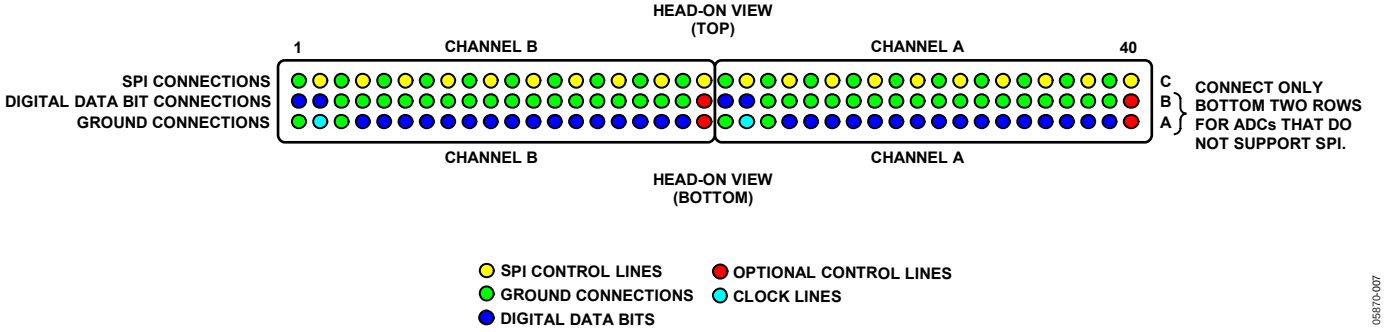


Figure 7. FIFO 4.1 Triple Row, 120-Pin Input Header

SCHEMATICS

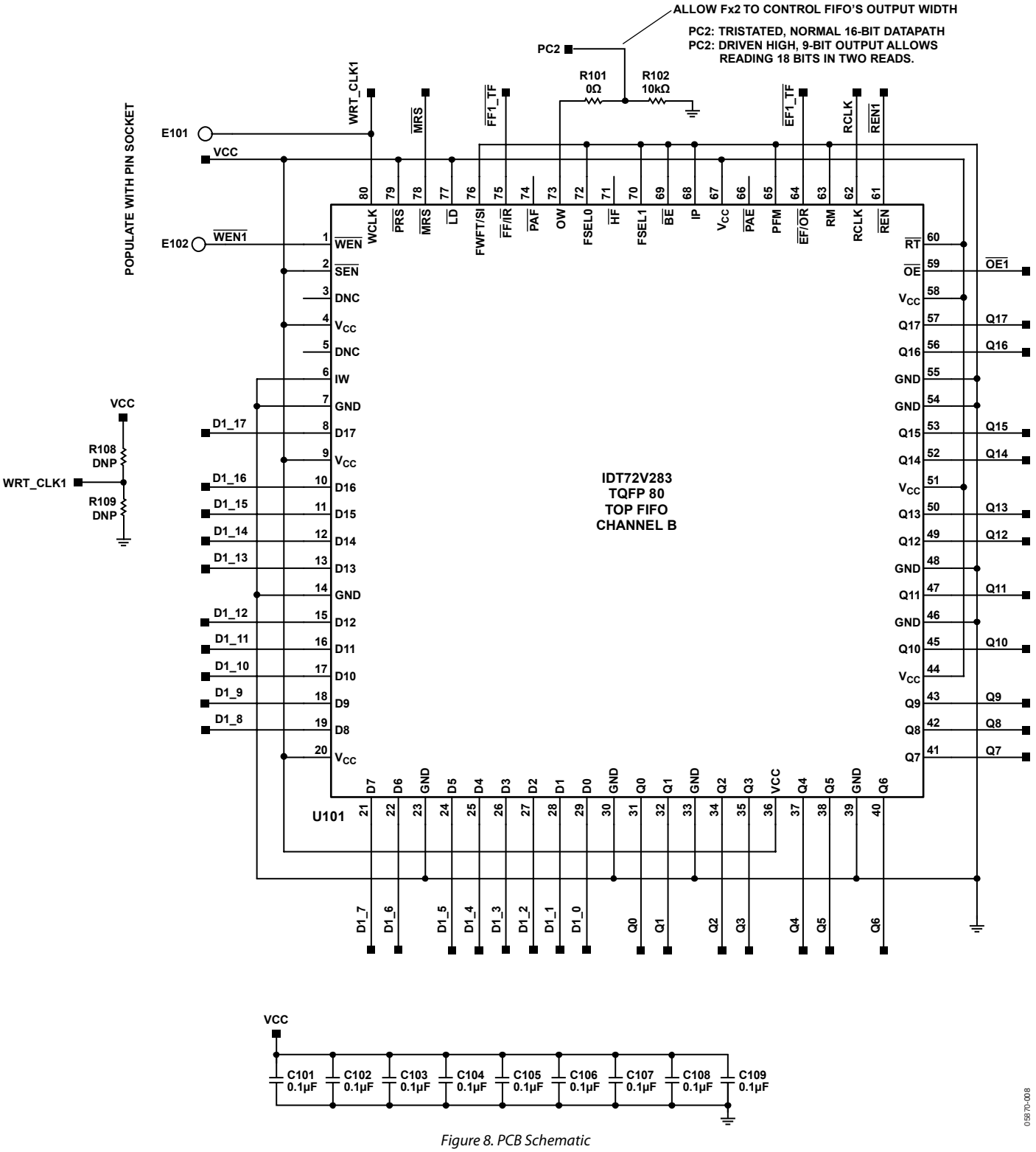


Figure 8. PCB Schematic

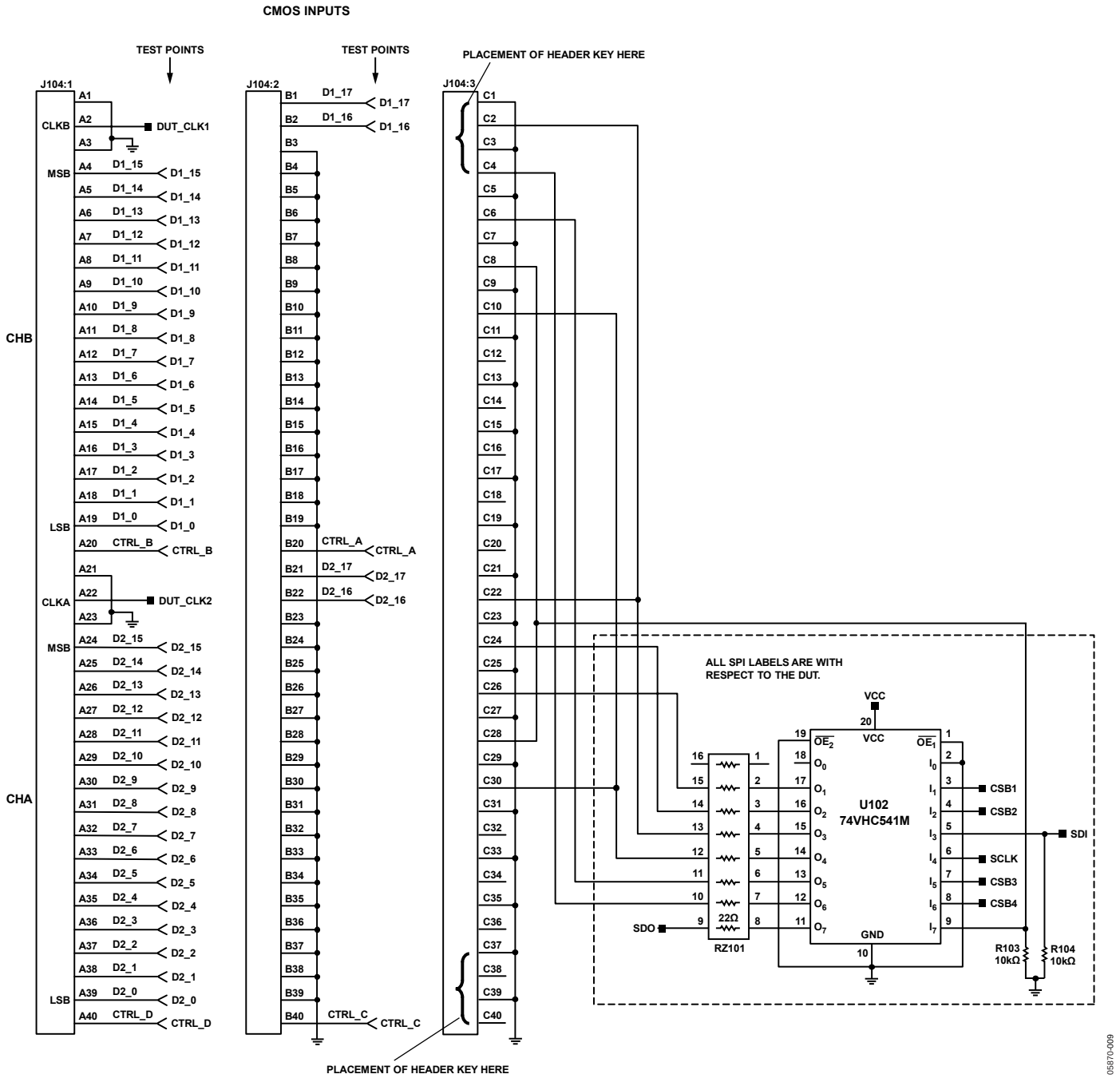


Figure 9. PCB Schematic (Continued)

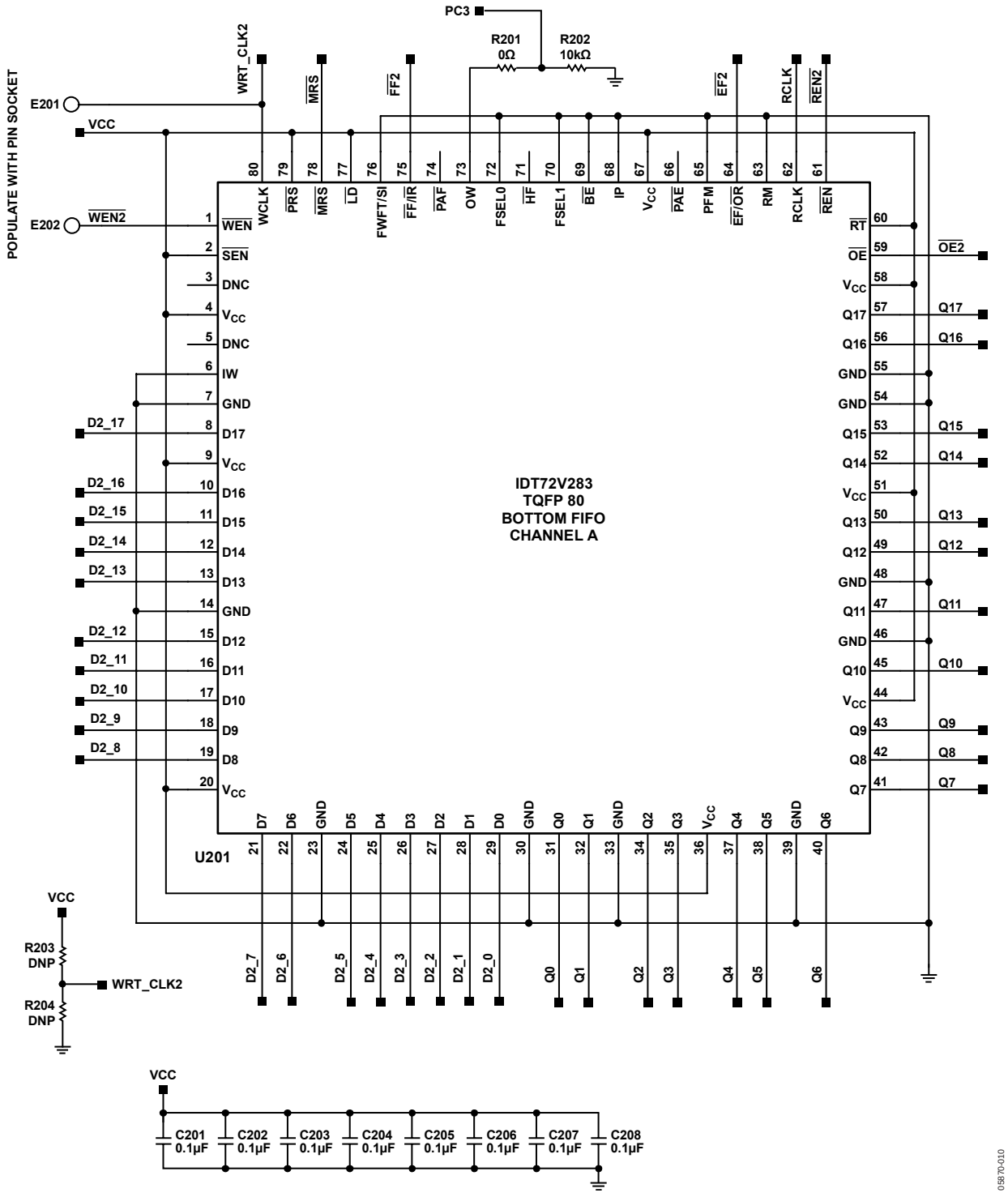


Figure 10. PCB Schematic (Continued)

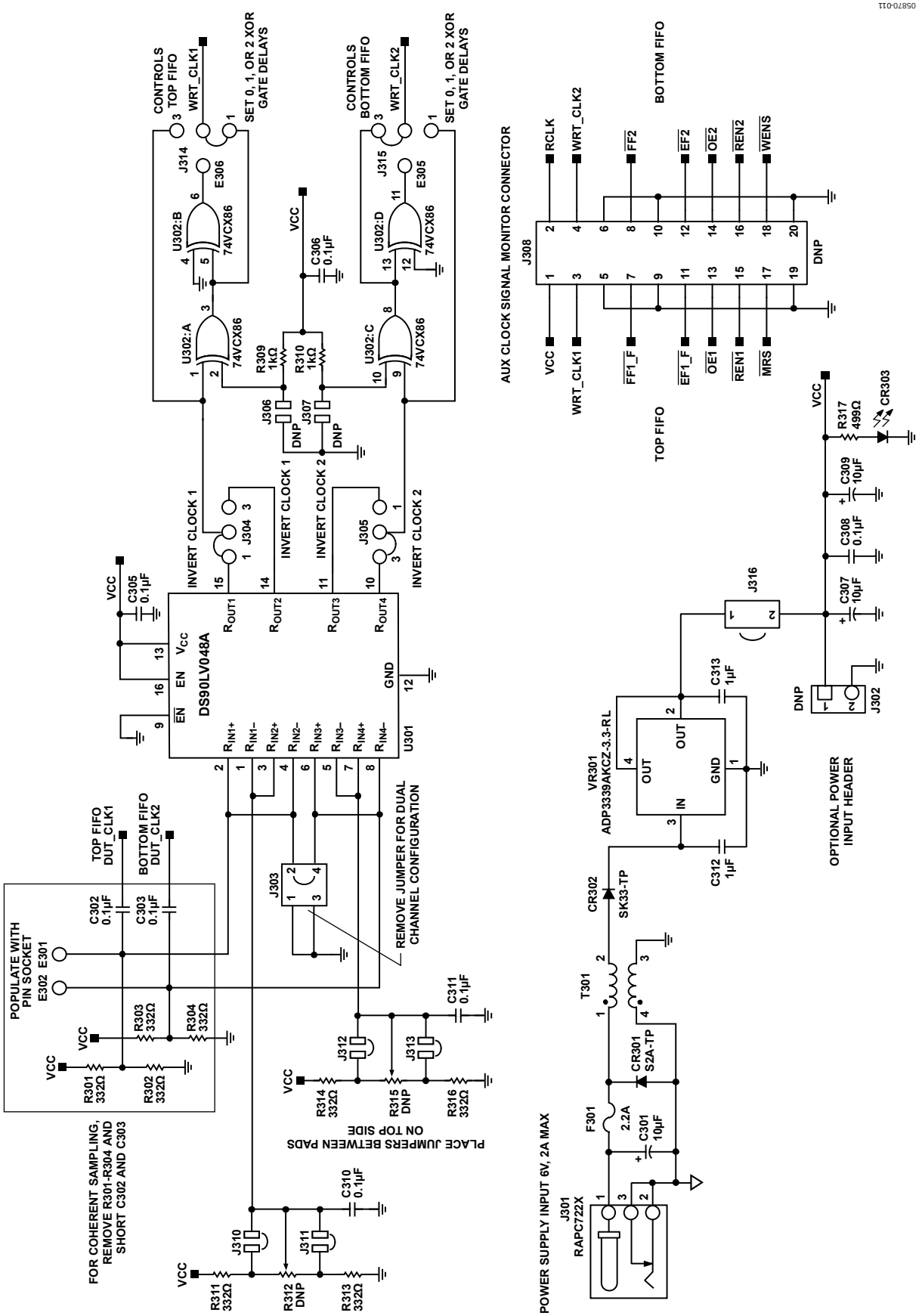


Figure 11. PCB Schematic (Continued)

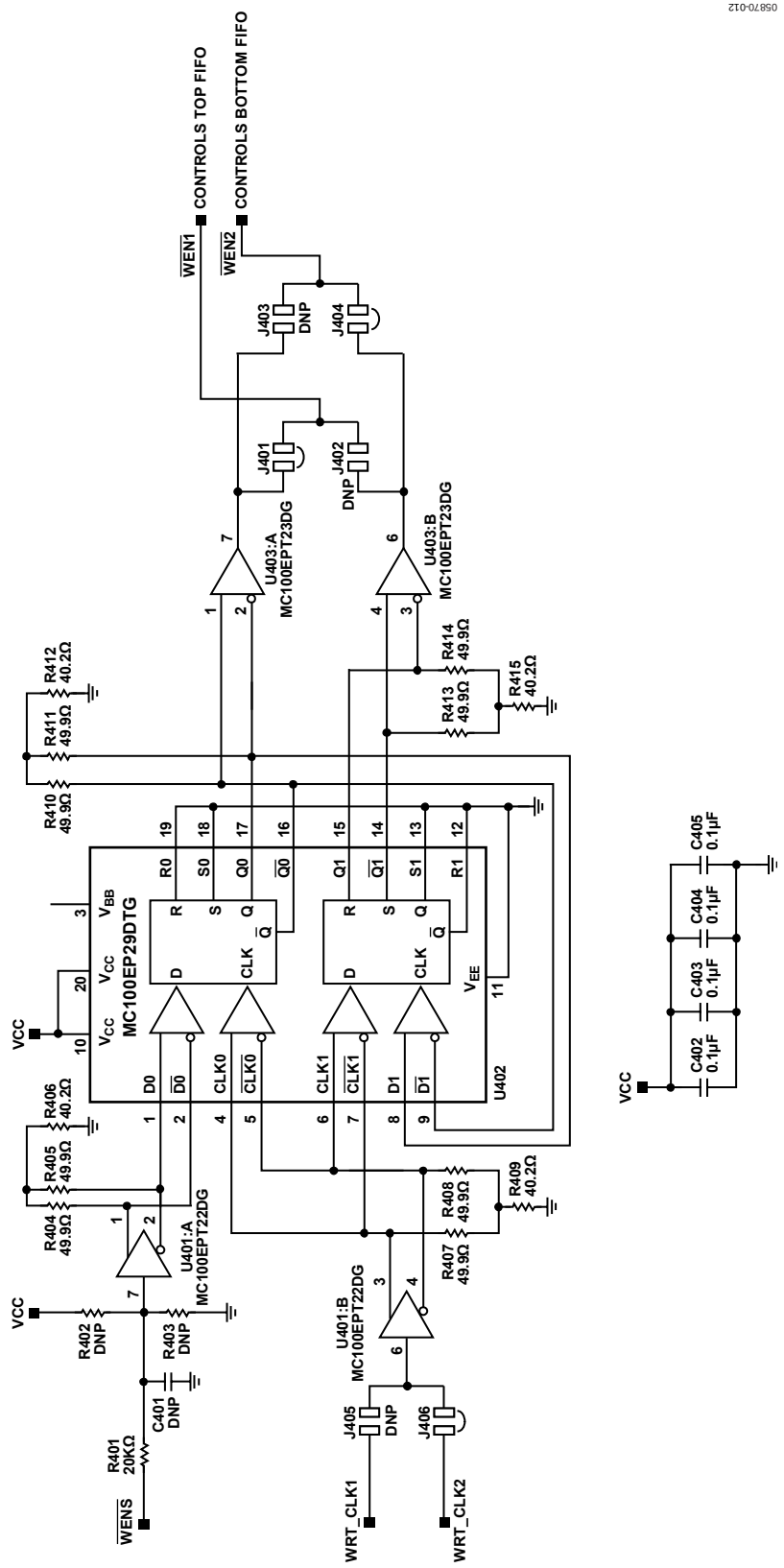


Figure 12. PCB Schematic (Continued)

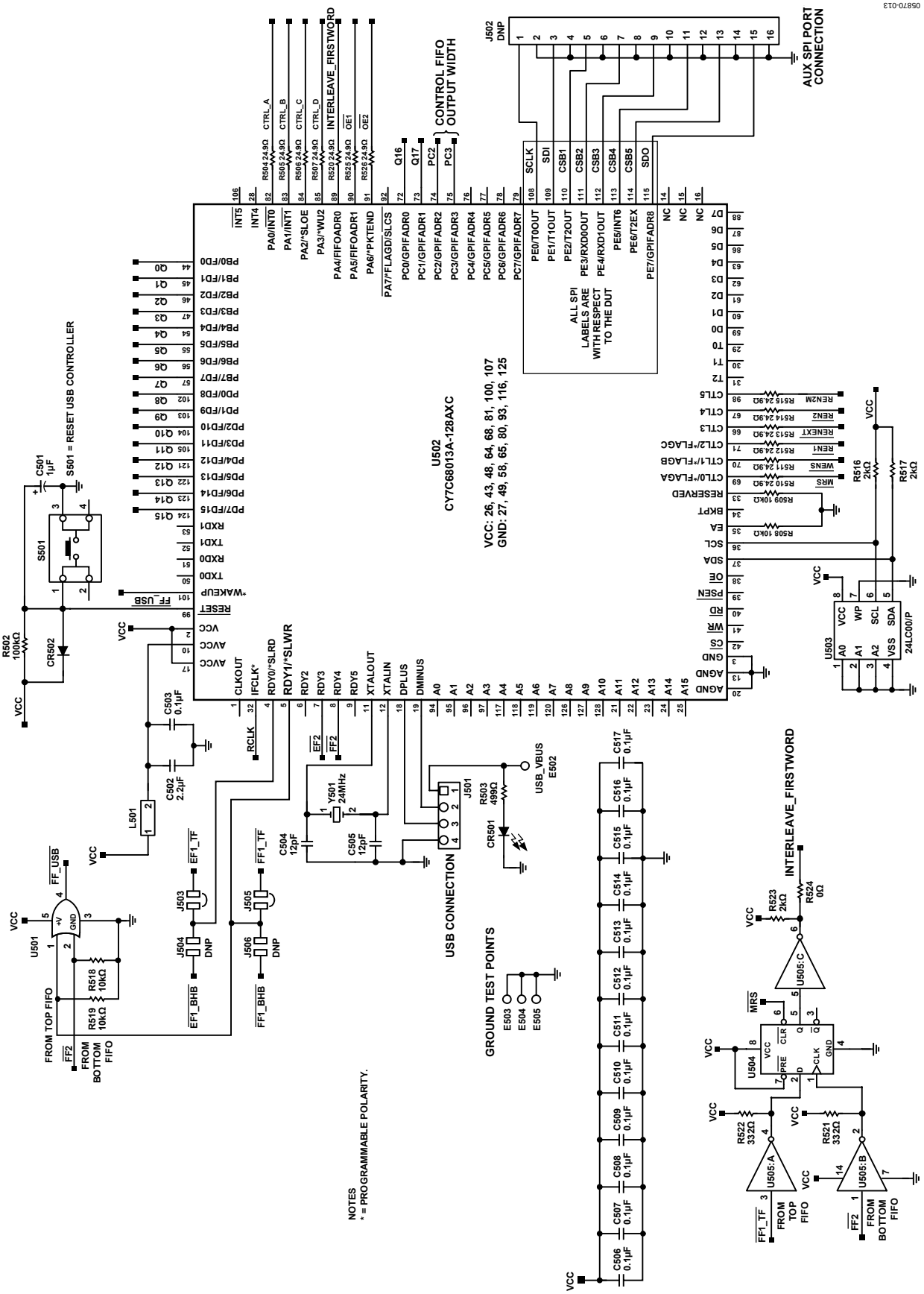


Figure 13. PCB Schematic (Continued)

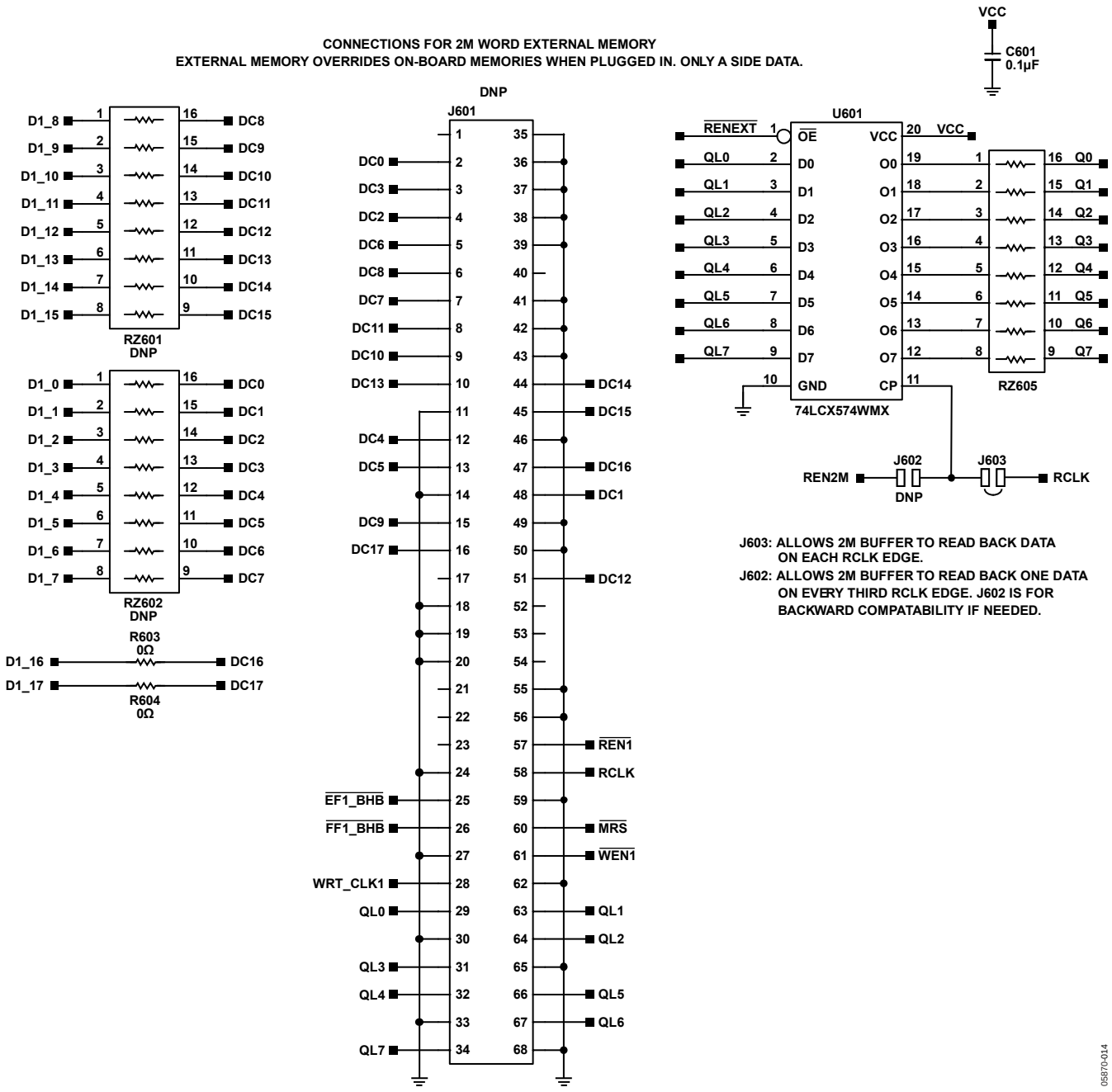


Figure 14. PCB Schematic (Continued)

PCB LAYOUT

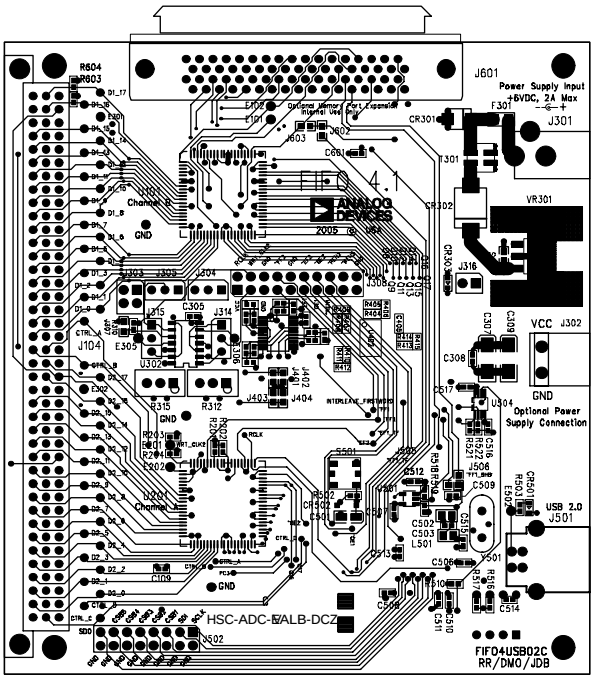


Figure 15. Layer 1—Primary Side

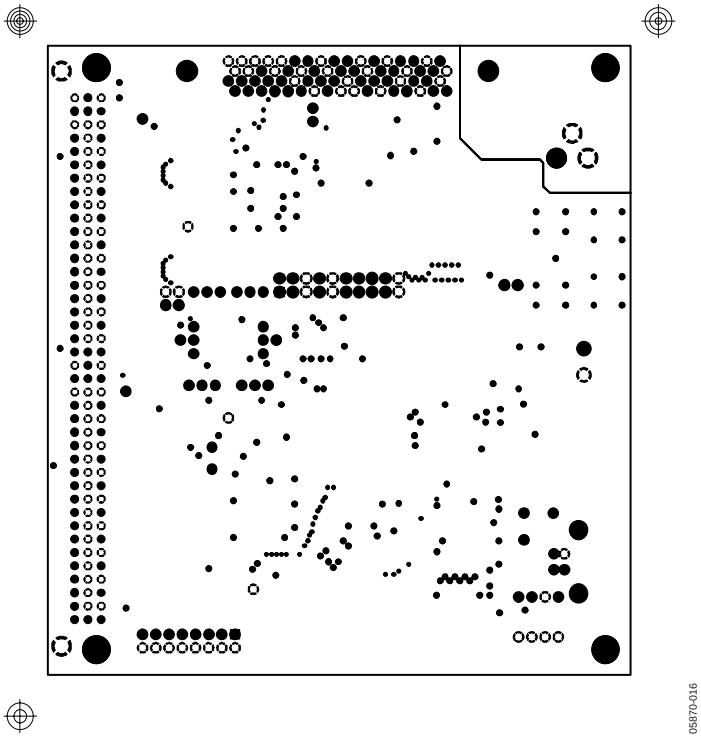
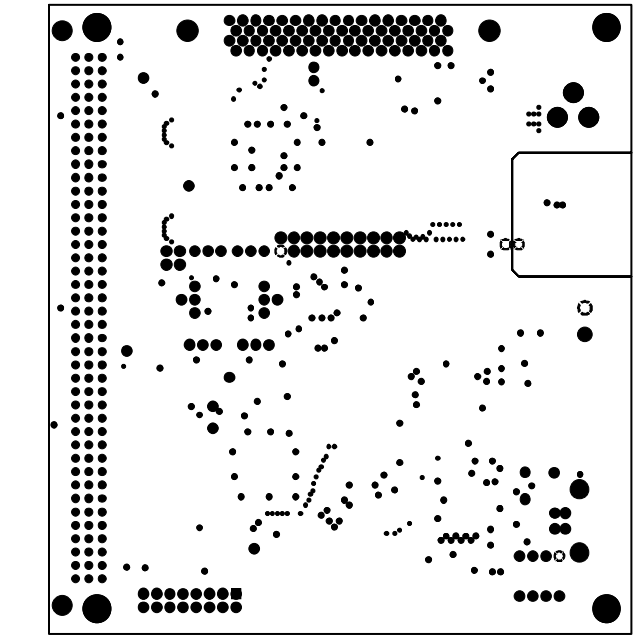
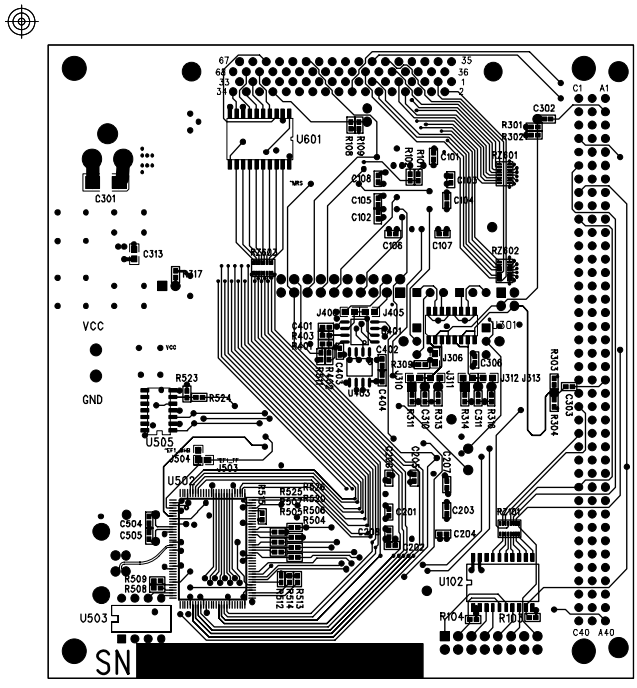


Figure 16. Layer 2—Ground Plane



05870-017

Figure 17. Layer 3—Power Plane



05870-018

Figure 18. Layer 4—Secondary Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 5. HSC-ADC-EVALB-DCZ Bill of Materials[1]

Item	Qty	Reference Designation	Device	Package	Description	Manufacturer	Mfg Part Number
1	42	C101 to C109, C201 to C208, C302, C303, C305, C306, C308, C310, C311, C402 to C405, C503, C506 to C517, C601	Capacitor	402	Ceramic, 0.1 µF, 16 V, X5R, 10%	Panasonic	ECJ0EB1A104K
2	3	C301, C307, C309	Capacitor	6032-28	Tantalum, 10 µF, 16 V, 10%	Kemet Corporation	T491C106K016AT
3	2	C312, C313	Capacitor	603	Ceramic, 1 µF, 10 V, X5R, 10%	Panasonic	ECJ1VB1A105K
4	1	C501	Capacitor	3216-18	Tantalum, 1 µF, 16 V, 20%	Kemet Corporation	T491A105M016AT
5	1	C502	Capacitor	805	Ceramic, 2.2 µF, 25 V, X5R 10%	Murata Manufacturing Co., Ltd.	GRM219R61E225KA12D
6	2	C504, C505	Capacitor	402	Ceramic, 12 pF, NPO, 50 V, 5%	Panasonic	ECJ-0EC1H120J
7	1	CR301	Diode	DO-214AA	Schottky diode, 50 V, 2 A, SMC	Micro Commercial Components Corp.	S2A-TP
8	1	CR302	Diode	DO-214AB	Schottky diode, 30 V, 3 A, SMC	Micro Commercial Components Corp.	SK33-TP
9	2	CR303, CR501	LED	603	Green, 4 V 5 m, candela	Panasonic	LNJ314G8TRA
10	1	CR502	Diode	SOD-123	Switching, 75 V, 150 mA	Diodes, Inc.	1N4148W-7-F
11	1	F301	Fuse	1210	6.0 V, 2.2 A trip current resettable fuse	Tyco Electronics/ Raychem	NANOSMDC110F-2
12	1	J104	Connector		120-pin, female, PC mount, right angle	AMP	5650874-4
13	1	J301	Connector	0.08", PCMT	RAPC722, power supply connector	Switchcraft, Inc.	RAPC722X
14	1	J303	Connector	4-pin	Male, straight, 100 mil	Samtec, Inc.	TSW-110-08-G-D
15	4	J304, J305, J314, J315	Connector	3-pin	Male, straight, 100 mil	Samtec, Inc.	TWS-103-08-G-S
16	10	J310 to J313, J401, J404, J406, J503, J505, J603	Connector	603	2-pin solder jumper, 0 Ω, 1/10 W, 5%	Panasonic	ERJ-3GEY0R00V
17	1	J316	Connector	2-pin	Male, straight, 100 mil	Samtec, Inc.	TSW-102-08-G-S
18	1	J501	Connector	4-pin	USB, PC mount, right angle, Type B, female	AMP	USB-B-S-S-B-TH-R
19	1	L501	Ferrite bead	805	500 mA, 600 Ω @ 100 MHz	Steward	HZ0805E601R-10
20	5	R101, R201, R524, R603, R604	Resistor	402	0 Ω, 1/16 W, 5%	Panasonic	ERJ-2GE0R00X
21	8	R102 to R104, R202, R508, R509, R518, R519	Resistor	402	10 kΩ, 1/16 W, 1%	Panasonic	ERJ-2RKF1002X
22	10	R301 to R304, R311, R313, R314, R316, R521, R522	Resistor	402	332 Ω, 1/16 W, 1%	Panasonic	ERJ-2RKF3320X
23	2	R309, R310	Resistor	402	1 kΩ, 1/16 W, 1%	Panasonic	ERJ-2RKF1001X
24	2	R317, R503	Resistor	402	499 Ω, 1/16 W, 1%	Panasonic	ERJ-2RKF4990X
25	1	R401	Resistor	402	20 kΩ, 1/16 W, 1%	Panasonic	ERJ-2RKF2002X
26	8	R404, R405, R407, R408, R410, R411, R413, R414	Resistor	402	49.9 Ω, 1/16 W, 1%	Panasonic	ERJ-2RKF49R9X

Item	Qty	Reference Designation	Device	Package	Description	Manufacturer	Mfg Part Number
27	4	R406, R409, R412, R415	Resistor	402	40.2 Ω, 1/16 W, 1%	Panasonic	ERJ-2RKF40R2X
28	1	R502	Resistor	402	100 kΩ, 1/16 W, 1%	Panasonic	ERJ-2RKF1003X
29	13	R504 to R507, R510, R511 to R515, R520, R525, R526	Resistor	402	24.9 Ω, 1/16 W, 1%	Panasonic	ERJ-2RKF24R9X
30	3	R516, R517, R523	Resistor	402	2 kΩ, 1/16 W, 1%	Panasonic	ERJ-2RKF2001X
31	1	RZ101	Resistor		Resistor array, 22 Ω, 1/4 W, 5%	Panasonic	EXB-2HV220JX
32	1	S501	Switch		Momentary (normally open), 100 GE, 5 mm, SPST	Panasonic	EVQPLDA15
33	1	T301	Choke	2020	10 µH, 5 A, 50 V, 190 Ω @ 100 MHz	Murata Manufacturing Co., Ltd.	DLW5BSN191SQ2L
34	2	U101, U201	IC	TQFP 80	3.3 V, IDT72V283L7-5PF	Integrated Device Technology, Inc.	IDT72V283L7-5PFG
35	1	U102	IC	SOIC-20	74VHC541, octal buffer/line driver, three-state	Fairchild Semiconductor	74VHC541M
36	1	U301	IC	SOIC-16	IC line receiver quad CMOS	National Semiconductor Corporation	DS90LV048ATM/NOPB
37	1	U302	IC	SOIC-14	IC gate exclusive OR quad 2 in	Fairchild	74VCX86M
38	1	U401	IC	SOIC-8	IC translator DL TTL/CMOS-PECL	ON Semiconductor	MC100EPT22DG
39	1	U402	IC	20-TSSOP	IC driver clock dual 1:5 diff	ON Semiconductor	MC100EP29DTG
40	1	U403	IC	SOIC-8	IC translator DL LVPECL-LVTTL	Motorola	MC100EPT23DG
41	1	U501	IC	SOT23-5	Tiny logic UHS 2-input OR gate	Fairchild Semiconductor	NC7SZ32M5X
42	1	U502	IC	128 TQFP	IC MCU USB periph high speed	Cypress Semiconductor Corporation	CY7C68013A-128AXC
43	1	U503	IC	8-DIP	IC SRL EEPROM 16 × 8, 2.5 V	Microchip Technology Inc.	24LC00/P
44	1	U504	IC	8-SSOP	IC D-type flip-flop w/clear preset	Texas Instruments Incorporated	SN74LVC2G74DCTR
45	1	U505	IC	SOIC-14	Low voltage hex inverter	Fairchild Semiconductor	74LVQ04SC
46	1	U601	IC	SOIC-20	Octal D-type flip-flop	Fairchild Semiconductor	74LCX574WMX
47	1	VR301	IC	SOT-223	IC reg LDO 1.5 A 3.3 V	Analog Devices, Inc.	ADP3339AKCZ-3.3-RL
48	1	Y501	Crystal	Crystal	Oscillator, 24 MHz	Ecliptek Corporation	EUAA-12-24.000M

[1] This BOM is RoHS compliant.

ORDERING GUIDE

Model	Description
HSC-ADC-EVALB-DCZ[1]	Dual FIFO Version of USB Evaluation Kit
HSC-ADC-FPGA-8Z[1]	Quad/Octal Serial LVDS to Dual Parallel CMOS Interface, Supports All Quad/ Octal ADCs in This Family Except the AD9289 (Not Included in Evaluation Kit)
HSC-ADC-FPGA-9289	Quad Serial LVDS to Dual Parallel CMOS Interface for the AD9289 Only (Not Included in Evaluation Kit)
HSC-ADC-DEMUX[2]	Adapter for AD9480-LVDS and AD9430-LVDS Evaluation Boards (Not Included in Evaluation Kit)
HSC-ADC-AD922xFFA[2]	Adapter for AD922x Family (Not Included in Evaluation Kit)
HSC-ADC-AD9283FFA[2]	Adapter for the AD9283 and AD9057 (Not Included in Evaluation Kit)

[1] Z = RoHS Compliant part.
[2] If an adapter is needed, send an email to highspeed.converters@analog.com.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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