12MHz, 400V/μs Op Amp

FEATURES

- **12MHz Gain-Bandwidth**
- **400V/μs Slew Rate**
- **1.25mA Maximum Supply Current**
- Unity Gain Stable
- C-Load™ Op Amp Drives All Capacitive Loads
- 10nV/√Hz Input Noise Voltage
- 800μV Maximum Input Offset Voltage
- 300nA Maximum Input Bias Current
- 70nA Maximum Input Offset Current
- 12V/mV Minimum DC Gain, R_L=1k
- 230ns Settling Time to 0.1%, 10V Step
- 280ns Settling Time to 0.01%, 10V Step
- ±12V Minimum Output Swing into 500Ω
- ±2.5V Minimum Output Swing into 150Ω
- Specified at ±2.5V, ±5V, and ±15V

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Data Acquisition Systems
- Photodiode Amplifiers

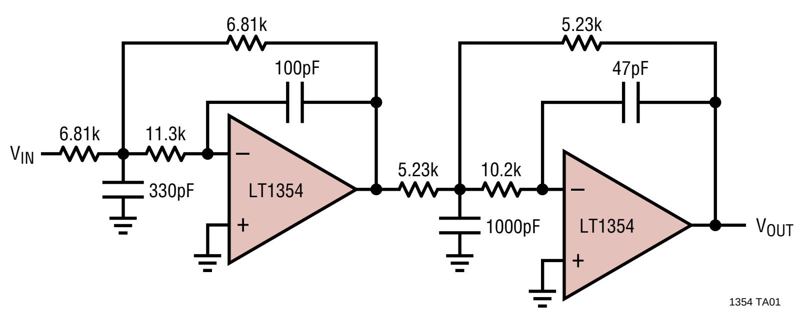
DESCRIPTION

The LT®1354 is a low power, high speed, high slew rate operational amplifier with outstanding AC and DC performance. The LT1354 has much lower supply current, lower input offset voltage, lower input bias current, and higher DC gain than devices with comparable bandwidth. The circuit topology is a voltage feedback amplifier with the slewing characteristics of a current feedback amplifier. The amplifier is a single gain stage with outstanding settling characteristics which makes the circuit an ideal choice for data acquisition systems. The output drives a 500Ω load to ±12V with ±15V supplies and a 150Ω load to ±2.5V on ±5V supplies. The amplifier is also stable with any capacitive load which makes it useful in buffer or cable driver applications.

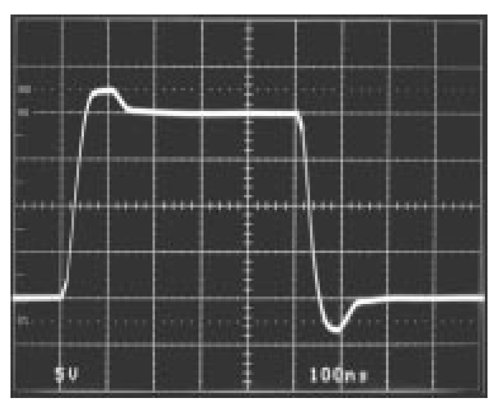
The LT1354 is a member of a family of fast, high performance amplifiers using this unique topology and employing Linear Technology Corporation's advanced bipolar complementary processing. For dual and quad amplifier versions of the LT1354 see the LT1355/LT1356 data sheet. For higher bandwidth devices with higher supply current see the LT1357 through LT1365 data sheets. Singles, duals, and quads of each amplifier are available.

TYPICAL APPLICATION

100kHz, 4th Order Butterworth Filter



A_V = –1 Large-Signal Response

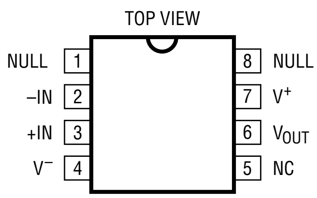


1354 TA02

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage (Transient Only, Note 1) ... ±10V
Input Voltage .... $\pm V_S$
Output Short-Circuit Duration (Note 2) .... Indefinite
Operating Temperature Range .... −40°C to 85°C
Specified Temperature Range (Note 6) ... −40°C to 85°C
Maximum Junction Temperature (See Below)
Plastic Package .... 150°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

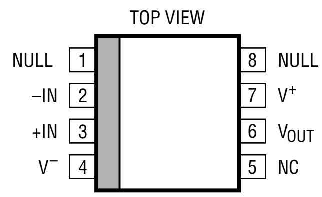
PACKAGE/ORDER INFORMATION



N8 PACKAGE, 8-LEAD PLASTIC DIP
T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LT1354CN8



S8 PACKAGE, 8-LEAD PLASTIC SOIC
T_{JMAX} = 150°C, θ_{JA} = 190°C/W

ORDER PART NUMBER

LT1354CS8

S8 PART MARKING

1354

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V ±5V ±2.5V		0.3 0.3 0.4	0.8 0.8 1.0	mV mV mV
I_{OS}	Input Offset Current		±2.5V to ±15V		20	70	nA
I_B	Input Bias Current		±2.5V to ±15V		80	300	nA
e_n	Input Noise Voltage	f = 10kHz	±2.5V to ±15V		10		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f = 10kHz	±2.5V to ±15V		0.6		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	V_{CM} = ±12V Differential	±15V ±15V	70	160 11		MΩ MΩ
C_{IN}	Input Capacitance		±15V		3		pF
	Input Voltage Range $^+$		±15V ±5V ±2.5V	12.0 2.5 0.5	13.4 3.5 1.1		V V V
	Input Voltage Range $^-$		±15V ±5V ±2.5V		−13.2 −3.4 −0.9	−12.0 −2.5 −0.5	V V V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±12V V_{CM} = ±2.5V V_{CM} = ±0.5V	±15V ±5V ±2.5V	80 78 68	97 84 75		dB dB dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±15V		92	106		dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12V, R_L = 1k V_{OUT} = ±10V, R_L = 500Ω V_{OUT} = ±2.5V, R_L = 1k V_{OUT} = ±2.5V, R_L = 500Ω V_{OUT} = ±2.5V, R_L = 150Ω V_{OUT} = ±1V, R_L = 500Ω	±15V ±15V ±5V ±5V ±5V ±2.5V	12 5 12 5 1 5	36 15 36 15 4 20		V/mV V/mV V/mV V/mV V/mV V/mV

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OUT}	Output Swing	$R_L = 1k$, $V_{IN} = ±40mV$ $R_L = 500Ω$, $V_{IN} = ±40mV$ $R_L = 500Ω$, $V_{IN} = ±40mV$ $R_L = 150Ω$, $V_{IN} = ±40mV$ $R_L = 500Ω$, $V_{IN} = ±40mV$	±15V ±15V ±5V ±5V ±2.5V	13.3 12.0 3.5 2.5 1.3	13.8 12.5 4.0 3.1 1.7		±V ±V ±V ±V ±V
I_{OUT}	Output Current	$V_{OUT} = ±12V$ $V_{OUT} = ±2.5V$	±15V ±5V	24.0 16.7	30 25		mA mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = ±3V$	±15V	30	42		mA
SR	Slew Rate	$A_V = –2$, (Note 3)	±15V ±5V	200 70	400 120		V/µs V/µs
	Full Power Bandwidth	10V Peak, (Note 4) 3V Peak, (Note 4)	±15V ±5V		6.4 6.4		MHz MHz
GBW	Gain-Bandwidth	$f = 200kHz$, $R_L = 2k$	±15V ±5V ±2.5V	9.0 7.5	12.0 10.5 9.0		MHz MHz MHz
t_r, t_f	Rise Time, Fall Time	$A_V = 1$, 10%-90%, 0.1V	±15V ±5V		14 17		ns ns
	Overshoot	$A_V = 1$, 0.1V	±15V ±5V		20 18		% %
	Propagation Delay	50% V_{IN} to 50% V_{OUT}, 0.1V	±15V ±5V		16 19		ns ns
t_s	Settling Time	10V Step, 0.1%, $A_V = –1$ 10V Step, 0.01%, $A_V = –1$ 5V Step, 0.1%, $A_V = –1$ 5V Step, 0.01%, $A_V = –1$	±15V ±15V ±5V ±5V		230 280 240 380		ns ns ns ns
	Differential Gain	$f = 3.58MHz$, $A_V = 2$, $R_L = 1k$	±15V ±5V		2.2 2.1		% %
	Differential Phase	$f = 3.58MHz$, $A_V = 2$, $R_L = 1k$	±15V ±5V		3.1 3.1		Deg Deg
R_O	Output Resistance	$A_V = 1$, $f = 100kHz$	±15V		0.7		Ω
I_S	Supply Current		±15V ±5V		1.0 0.9	1.25 1.20	mA mA

$0°C \le T_A \le 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V ±5V ±2.5V	● ● ●			1.0 1.0 1.2	mV mV mV
	Input V_{OS} Drift	(Note 5)	±2.5V to ±15V	●		5	8	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			100	nA
I_B	Input Bias Current		±2.5V to ±15V	●			450	nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = ±12V$ $V_{CM} = ±2.5V$ $V_{CM} = ±0.5V$	±15V ±5V ±2.5V	● ● ●	79 77 67			dB dB dB
PSRR	Power Supply Rejection Ratio	$V_S = ±2.5V$ to $±15V$		●	90			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = ±12V$, $R_L = 1k$ $V_{OUT} = ±10V$, $R_L = 500Ω$ $V_{OUT} = ±2.5V$, $R_L = 1k$ $V_{OUT} = ±2.5V$, $R_L = 500Ω$ $V_{OUT} = ±2.5V$, $R_L = 150Ω$ $V_{OUT} = ±1V$, $R_L = 500Ω$	±15V ±15V ±5V ±5V ±5V ±2.5V	● ● ● ● ● ●	10.0 3.3 10.0 3.3 0.6 3.3			V/mV V/mV V/mV V/mV V/mV V/mV

ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OUT}	Output Swing	$R_L = 1k$, $V_{IN} = \pm40mV$	±15V	●	13.2			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±15V	●	11.5			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±5V	●	3.4			±V
		$R_L = 150\Omega$, $V_{IN} = \pm40mV$	±5V	●	2.3			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±2.5V	●	1.2			±V
I_{OUT}	Output Current	$V_{OUT} = \pm11.5V$	±15V	●	23.0			mA
		$V_{OUT} = \pm2.3V$	±5V	●	15.3			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = \pm3V$	±15V	●	24			mA
SR	Slew Rate	$A_V = -2$, (Note 3)	±15V	●	150			V/µs
			±5V	●	60			V/µs
GBW	Gain-Bandwidth	$f = 200kHz$, $R_L = 2k$	±15V	●	7.5			MHz
			±5V	●	6.0			MHz
I_S	Supply Current		±15V	●			1.45	mA
			±5V	●			1.40	mA

$-40°C \le T_A \le 85°C$, $V_{CM} = 0V$ unless otherwise noted. (Note 6)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V	●			1.5	mV
			±5V	●			1.5	mV
			±2.5V	●			1.7	mV
	Input V_{OS} Drift	(Note 5)	±2.5V to ±15V	●		5	8	µV/°C
I_{OS}	Input Offset Current		±2.5V to ±15V	●			200	nA
I_B	Input Bias Current		±2.5V to ±15V	●			550	nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm12V$	±15V	●	78			dB
		$V_{CM} = \pm2.5V$	±5V	●	76			dB
		$V_{CM} = \pm0.5V$	±2.5V	●	66			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.5V$ to $\pm15V$		●	90			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm12V$, $R_L = 1k$	±15V	●	7.0			V/mV
		$V_{OUT} = \pm10V$, $R_L = 500\Omega$	±15V	●	1.7			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 1k$	±5V	●	7.0			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 500\Omega$	±5V	●	1.7			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 150\Omega$	±5V	●	0.4			V/mV
		$V_{OUT} = \pm1V$, $R_L = 500\Omega$	±2.5V	●	1.7			V/mV
V_{OUT}	Output Swing	$R_L = 1k$, $V_{IN} = \pm40mV$	±15V	●	13.0			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±15V	●	11.0			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±5V	●	3.4			±V
		$R_L = 150\Omega$, $V_{IN} = \pm40mV$	±5V	●	2.1			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±2.5V	●	1.2			±V
I_{OUT}	Output Current	$V_{OUT} = \pm11V$	±15V	●	22			mA
		$V_{OUT} = \pm2.1V$	±5V	●	14			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = \pm3V$	±15V	●	23			mA
SR	Slew Rate	$A_V = -2$, (Note 3)	±15V	●	120			V/µs
			±5V	●	50			V/µs
GBW	Gain Bandwith	$f = 200kHz$, $R_L = 2k$	±15V	●	7.0			MHz
			±5V	●	5.5			MHz
I_S	Supply Current		±15V	●			1.50	mA
			±5V	●			1.45	mA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full specified temperature range.

Note 1: Differential inputs of ±10V are appropriate for transient operation only, such as during slewing. Large, sustained differential inputs will cause excessive power dissipation and may damage the part. See Input Considerations in the Applications Information section of this data sheet for more dutails.

Note 2: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 3: Slew rate is measured between ±10V on the output with ±6V input for ±15V supplies and ±1V on the output with ±1.75V input for ±5V supplies.

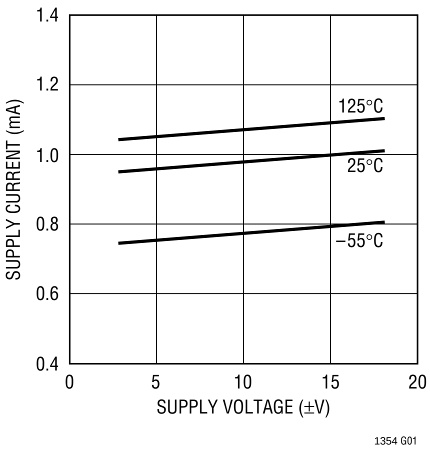
Note 4: Full power bandwidth is calculated from the slew rate measurement: FPBW = $SR/2\pi V_P$.

Note 5: This parameter is not 100% tested.

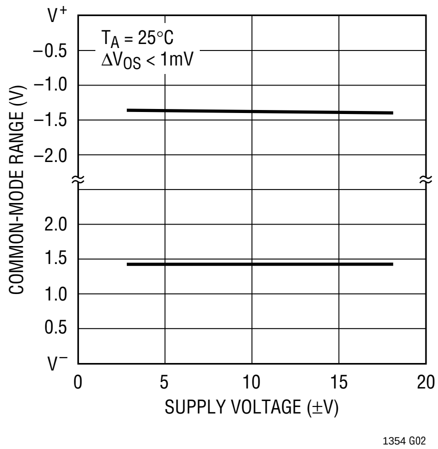
Note 6: The LT1354 is designed, characterized and expected to meet these extended temperature limits, but is not tested at –40°C and at 85°C. Guaranteed I grade parts are available; consult factory.

TYPICAL PERFORMANCE CHARACTERISTICS

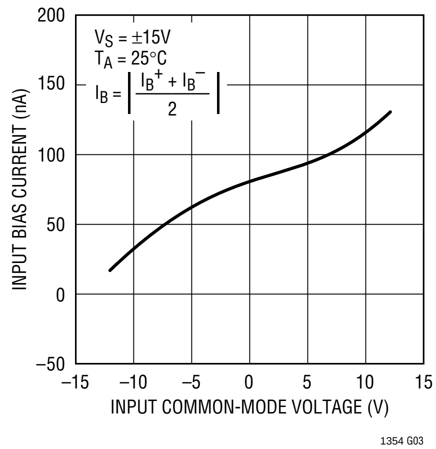
Supply Current vs Supply Voltage and Temperature



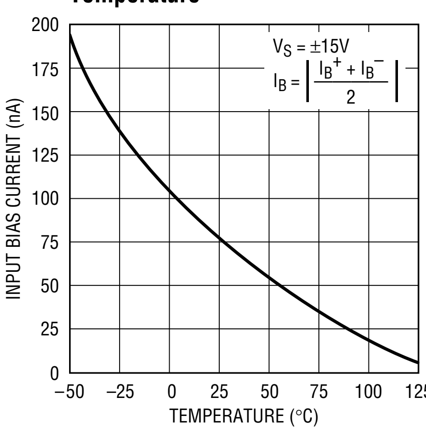
Input Common-Mode Range vs Supply Voltage



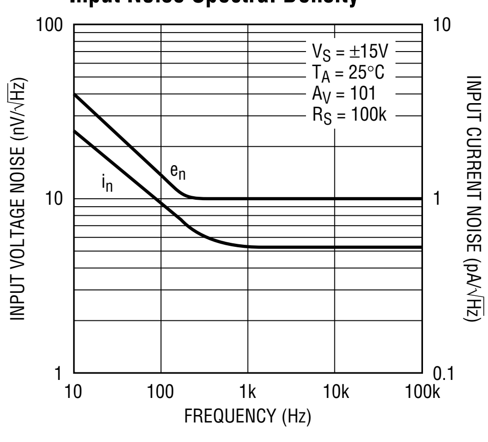
Input Bias Current vs Input Common-Mode Voltage



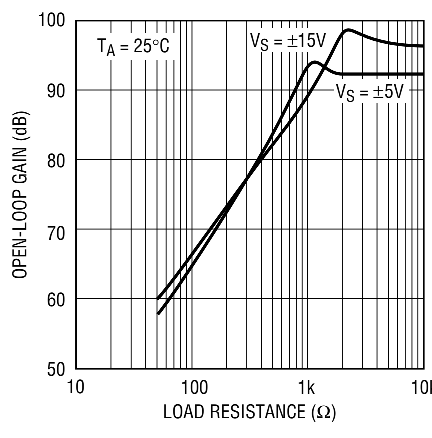
Input Bias Current vs Temperature



Input Noise Spectral Density

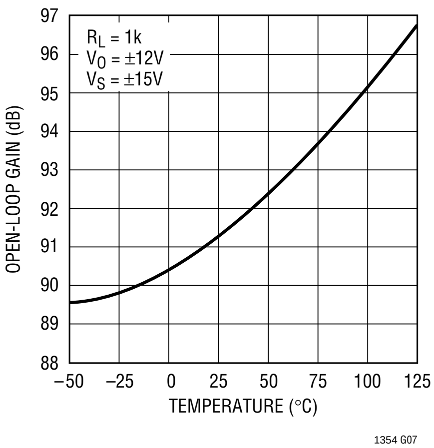


Open-Loop Gain vs Resistive Load

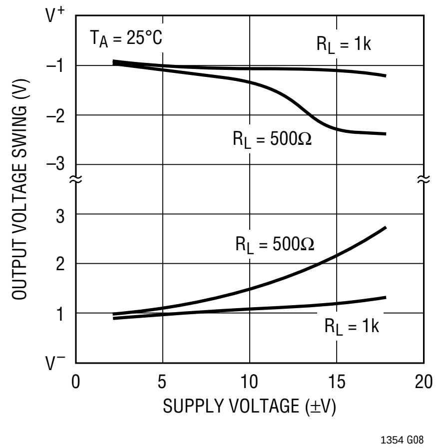


TYPICAL PERFORMANCE CHARACTERISTICS

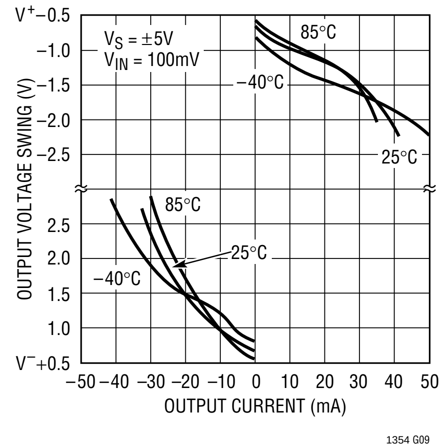
Open-Loop Gain vs Temperature



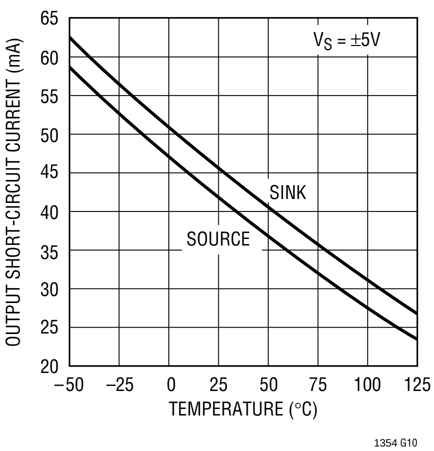
Output Voltage Swing vs Supply Voltage



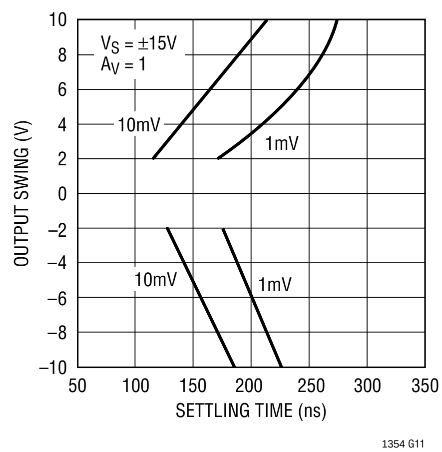
Output Voltage Swing vs Load Current



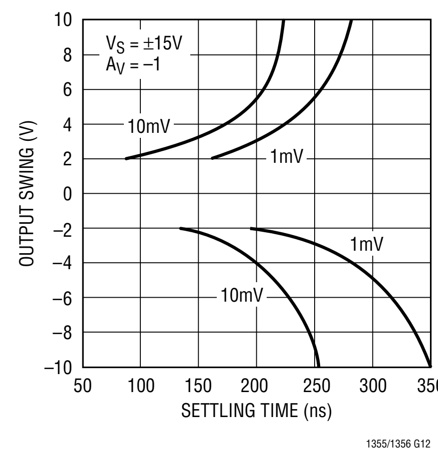
Output Short-Circuit Current vs Temperature



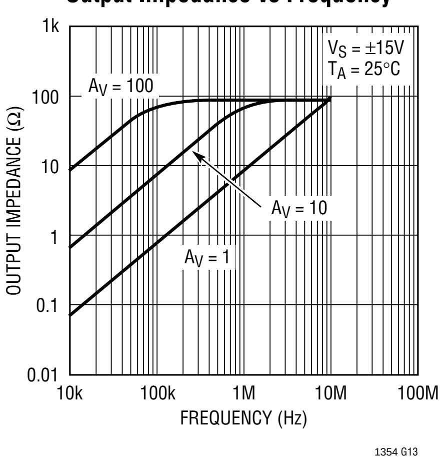
Settling Time vs Output Step (Noninverting)



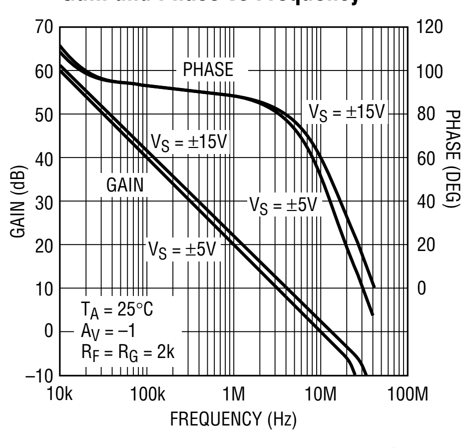
Settling Time vs Output Step (Inverting)



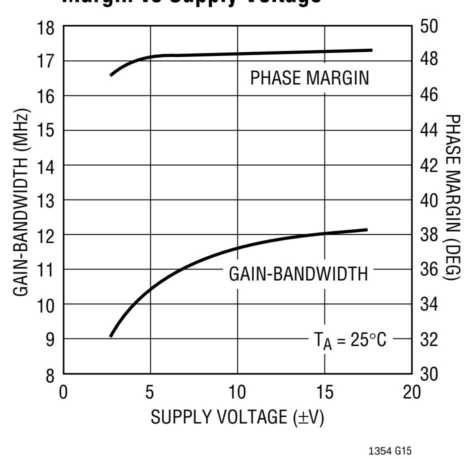
Output Impedance vs Frequency



Gain and Phase vs Frequency

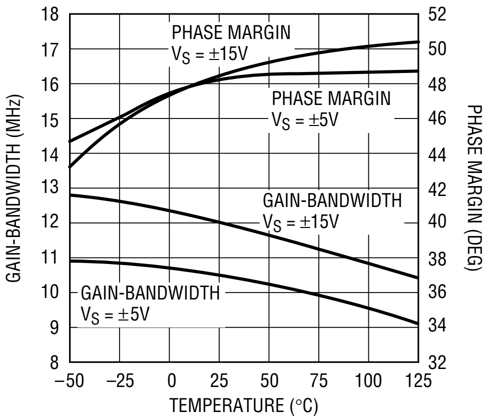


Gain-Bandwidth and Phase Margin vs Supply Voltage



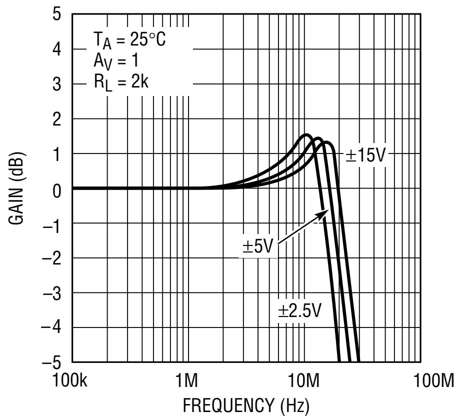
TYPICAL PERFORMANCE CHARACTERISTICS

Gain-Bandwidth and Phase Margin vs Temperature



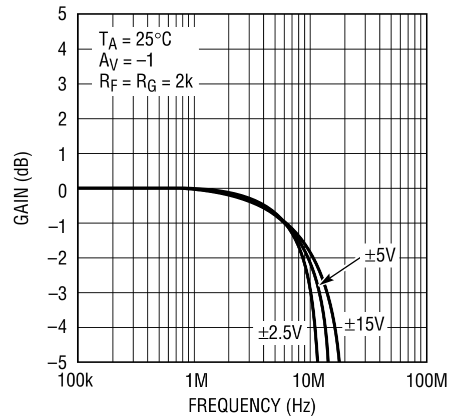
1354 G16

Frequency Response vs Supply Voltage (A_V = 1)



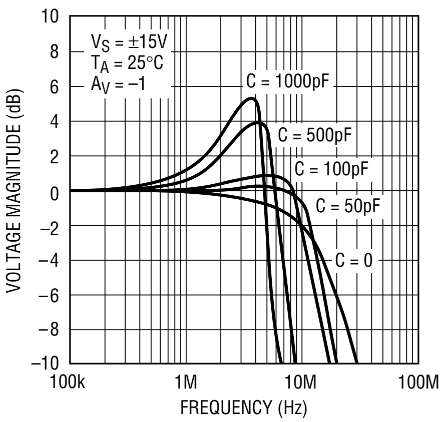
1354 G17

Frequency Response vs Supply Voltage (A_V = –1)



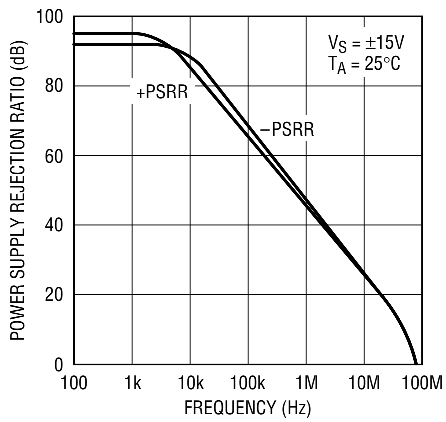
1354 G18

Frequency Response vs Capacitive Load



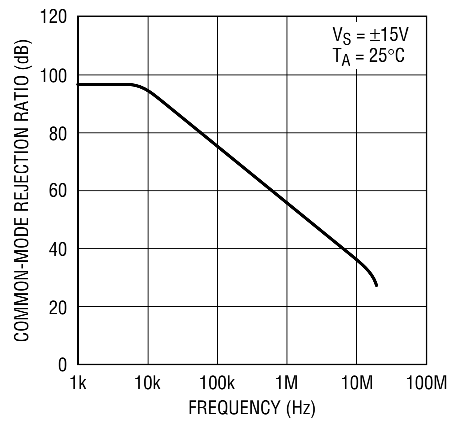
1354 G19

Power Supply Rejection Ratio vs Frequency



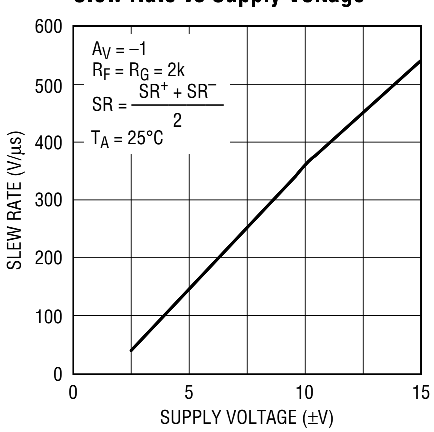
1354 G20

Common-Mode Rejection Ratio vs Frequency



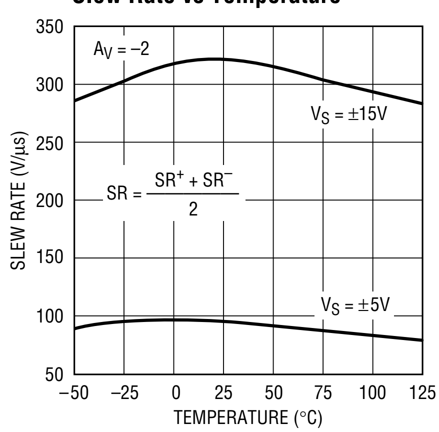
1354 G21

Slew Rate vs Supply Voltage



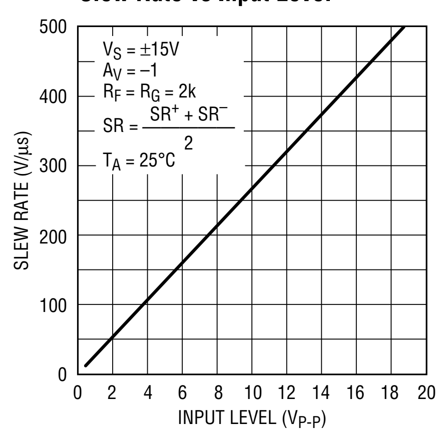
1354 G22

Slew Rate vs Temperature



1354 G23

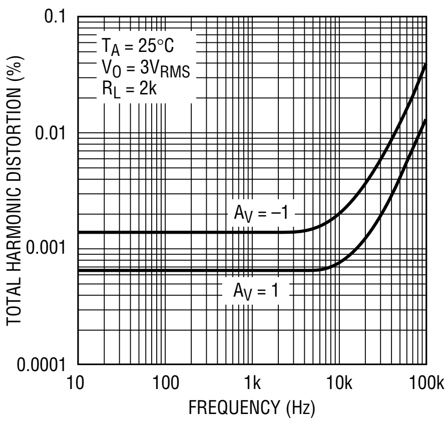
Slew Rate vs Input Level



1354 G24

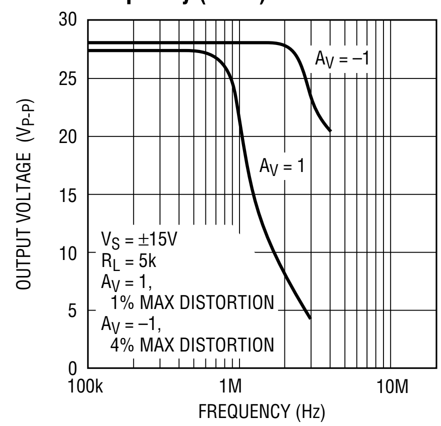
TYPICAL PERFORMANCE CHARACTERISTICS

Total Harmonic Distortion vs Frequency



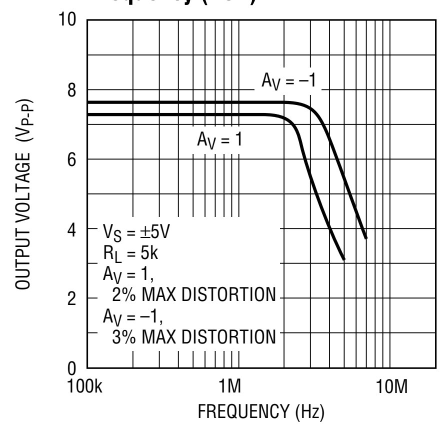
1354 G25

Undistorted Output Swing vs Frequency (±15V)



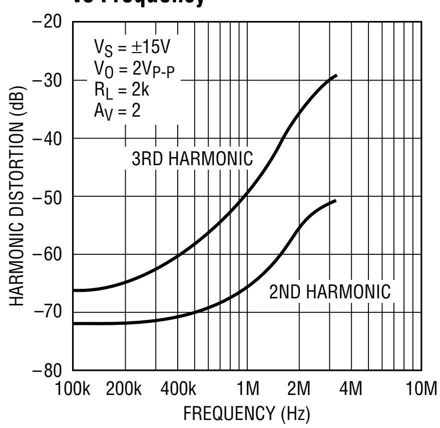
1355/1356 G26

Undistorted Output Swing vs Frequency (±5V)



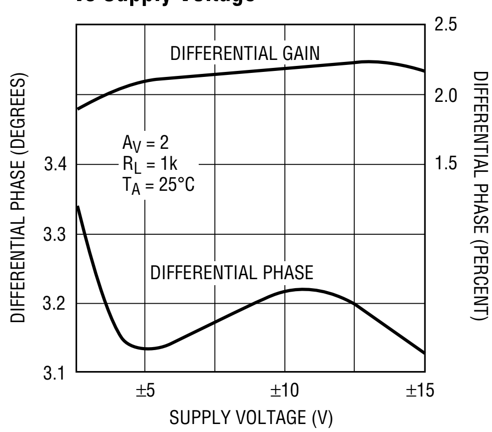
1354 G27

2nd and 3rd Harmonic Distortion vs Frequency



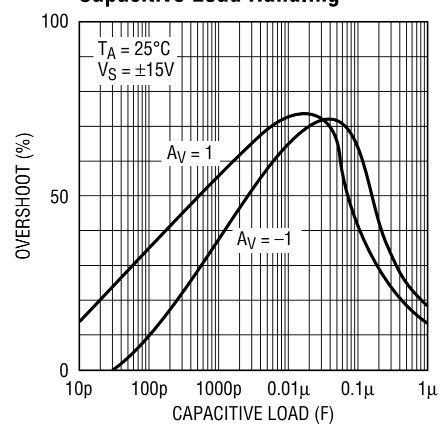
1354 G28

Differential Gain and Phase vs Supply Voltage



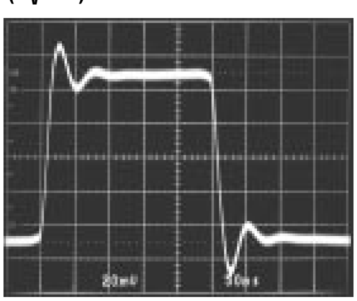
1354 G29

Capacitive Load Handling



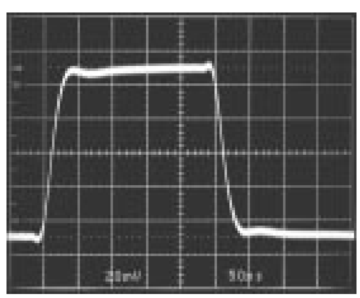
1354 G30

Small-Signal Transient (A_V = 1)



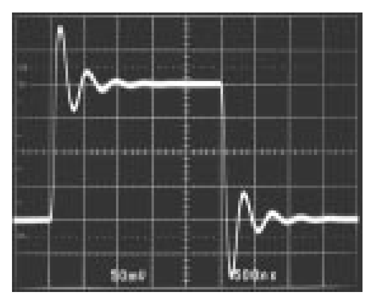
1354 TA31

Small-Signal Transient (A_V = –1)



1354 TA32

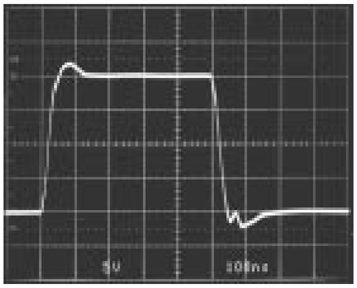
Small-Signal Transient (A_V = –1, C_L = 1000pF)



1354 TA33

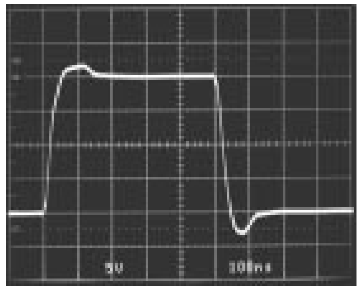
TYPICAL PERFORMANCE CHARACTERISTICS

Large-Signal Transient ($A_V = 1$)



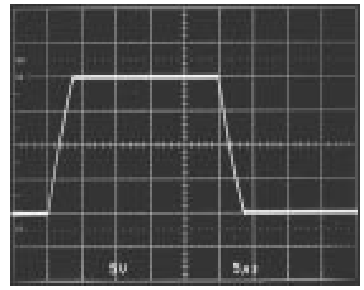
1354 TA34

Large-Signal Transient ($A_V = -1$)



1354 TA35

Large-Signal Transient ($A_V = 1$, $C_L = 10{,}000pF$)

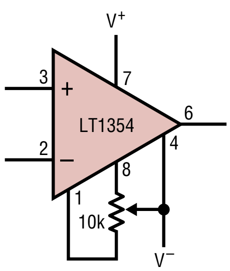


1354 TA36

APPLICATIONS INFORMATION

The LT1354 may be inserted directly into many high speed amplifier applications improving both DC and AC performance, provided that the nulling circuitry is removed. The suggested nulling circuit for the LT1354 is shown below.

Offset Nulling



1354 AI01

Layout and Passive Components

The LT1354 amplifier is easy to apply and tolerant of less than ideal layouts. For maximum performance (for example fast settling time) use a ground plane, short lead lengths, and RF-quality bypass capacitors (0.01µF to 0.1µF). For high drive current applications use low ESR bypass capacitors (1µF to 10µF tantalum). Sockets should be avoided when maximum frequency performance is required, although low profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole which can cause peaking or oscillations. For feedback resistors greater than 5kΩ, a parallel capacitor of value

$$C_F > (R_G \bullet C_{IN})/R_F$$

should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a large feedback resistor is used, C_F should be greater than or equal to C_{IN}.

Capacitive Loading

The LT1354 is stable with any capacitive load. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response as shown in the typical performance curves.The photo of the small-signal response with 1000pF load shows 43% peaking. The large signal response with a 10,000pF load shows the output slew rate being limited to 5V/µs by the short-circuit current. Coaxial cable can be driven directly, but for best pulse fidelity a resistor of value equal to the characteristic impedance of the cable (i.e., 75Ω) should be placed in series with the output. The other end of the cable should be terminated with the same value resistor to ground.

APPLICATIONS INFORMATION

Input Considerations

Each of the LT1354 inputs is the base of an NPN and a PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input bias current can be positive or negative. The offset current does not depend on NPN/PNP beta matching and is well controlled. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized.

The inputs can withstand transient differential input voltages up to 10V without damage and need no clamping or source resistance for protection. Differential inputs, however, generate large supply currents (tens of mA) as required for high slew rates. If the device is used with sustained differential inputs, the average supply current will increase, excessive power dissipation will result and the part may be damaged. *The part should not be used as a comparator, peak detector or other open-loop application with large, sustained differential inputs*. Under normal, closed-loop operation, an increase of power dissipation is only noticeable in applications with large slewing outputs and is proportional to the magnitude of the differential input voltage and the percent of the time that the inputs are apart. Measure the average supply current for the application in order to calculate the power dissipation.

Power Dissipation

The LT1354 combines high speed and large output drive in a small package. Because of the wide supply voltage range, it is possible to exceed the maximum junction temperature under certain conditions. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) as follows:

LT1354CN8: $T_J = T_A + (P_D \bullet 130°C/W)$
LT1354CS8: $T_J = T_A + (P_D \bullet 190°C/W)$

Worst case power dissipation occurs at the maximum supply current and when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 supply voltage). Therefore P_{DMAX} is:

$$P_{DMAX} = (V^+ - V^-)(I_{SMAX}) + (V^+/2)^2/R_L$$

Example: LT1354CS8 at 70°C, $V_S = ±15V$, $R_L = 100Ω$ (Note: the minimum short-circuit current at 70°C is 24mA, so the output swing is guaranteed only to 2.4V with 100Ω.)

$$P_{DMAX} = (30V \bullet 1.45mA) + (15V – 2.4V)(24mA) = 346mW$$

$$T_{JMAX} = 70°C + (346mW \bullet 190°C/W) = 136°C$$

Circuit Operation

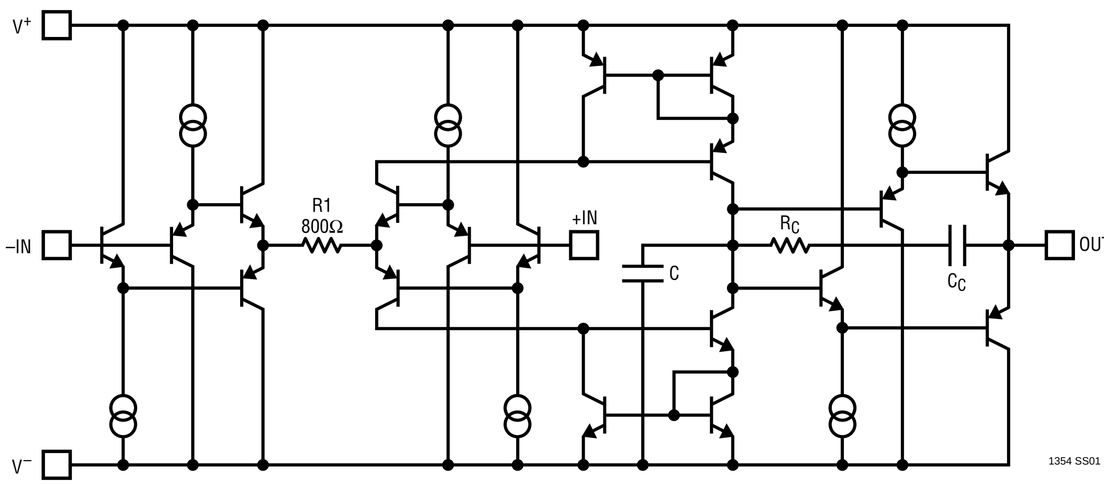
The LT1354 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the simplified schematic. The inputs are buffered by complementary NPN and PNP emitter followers which drive an 800Ω resistor. The input voltage appears across the resistor generating currents which are mirrored into the high impedance node. Complementary followers form an output stage which buffers the gain node from the load. The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the gain node capacitance. This current is the differential input voltage divided by R1, so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 10V output step in a gain of 10 has only a 1V input step, whereas the same output step in unity gain has a 10 times greater input step. The curve of Slew Rate vs Input Level illustrates this relationship. The LT1354 is tested for slew rate in a gain of –2 so higher slew rates can be expected in gains of 1 and –1, and lower slew rates in higher gain configurations.

The RC network across the output stage is bootstrapped when the amplifier is driving a light or moderate load and has no effect under normal operation. When driving a capacitive load (or a low value resistive load) the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance

APPLICATIONS INFORMATION

slows down the amplifier which improves the phase margin by moving the unity gain frequency away from the pole formed by the output impedance and the capacitive load. The zero created by the RC combination adds phase to ensure that even for very large load capacitances, the total phase lag can never exceed 180 degrees (zero phase margin) and the amplifier remains stable.

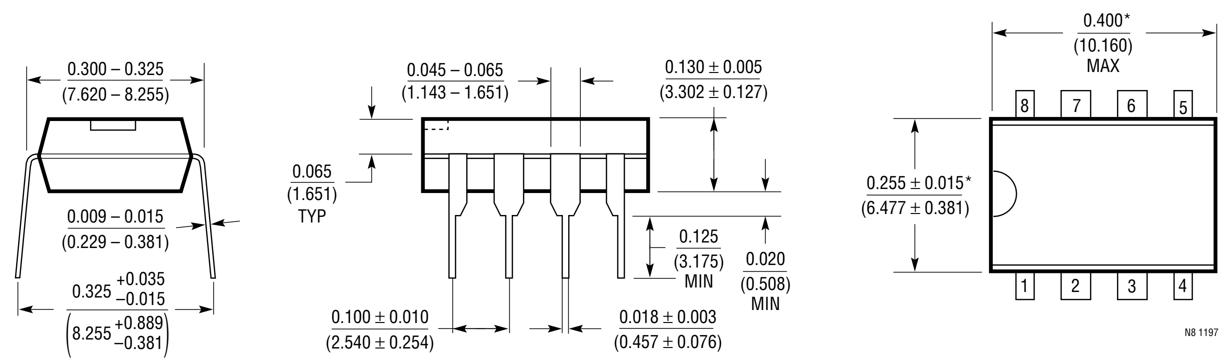
SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

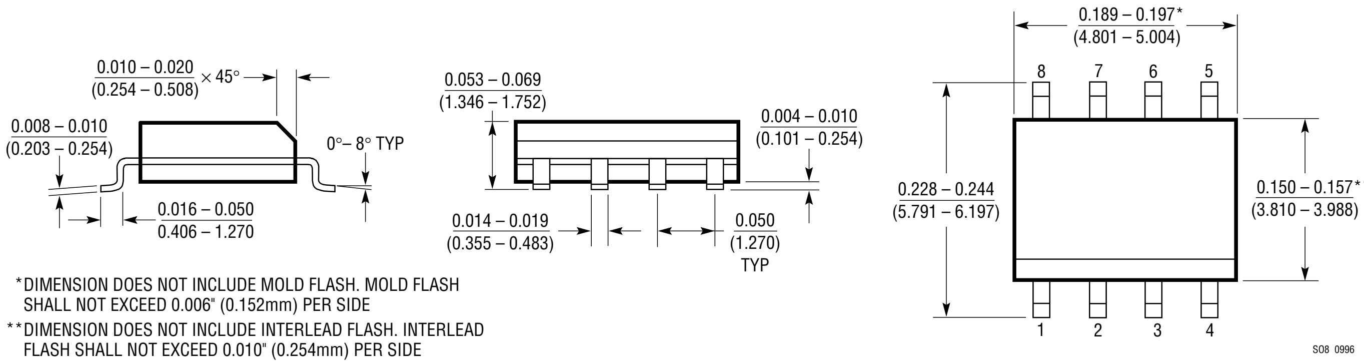


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

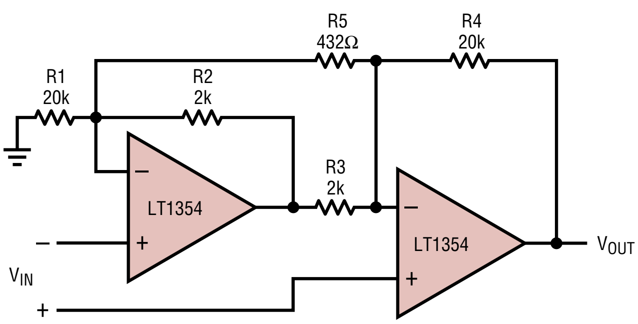
S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATIONS

Instrumentation Amplifier

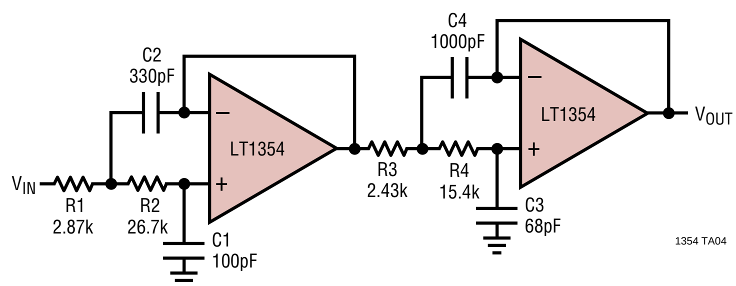


$$A_V = \frac{R4}{R3}\left[1 + \frac{1}{2}\left(\frac{R2}{R1} + \frac{R3}{R4}\right) + \frac{R2 + R3}{R5}\right] = 104$$

TRIM R5 FOR GAIN
TRIM R1 FOR COMMON MODE REJECTION
BW = 120kHz

1354 TA03

100kHz, 4th Order Butterworth Filter (Sallen-Key)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1355/LT1356	Dual/Quad 1mA, 12MHz, 400V/µs Op Amp	Good DC Precision, Stable with All Capacitive Loads
LT1357	2mA, 25MHz, 600V/µs Op Amp	Good DC Precision, Stable with All Capacitive Loads
LT1358/LT1359	Dual/Quad 2mA, 25MHz, 600V/µs Op Amp	Good DC Precision, Stable with All Capacitive Loads

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