3A, 0.95V to 10V, Very Low Dropout Linear Regulator with Programmable Current Limit

FEATURES

- **Single Supply V_{IN} Range: 0.95V to 10V**
- **Dropout Voltage: 95mV Typical**
- **Output Current: 3A**
- **Adjustable Output Voltage: 200mV to 9.7V**
- **Single Capacitor Soft-Starts Reference and Lowers Output Noise**
- Stable with Low ESR, Ceramic Output Capacitors
- 0.075% Typical Load Regulation from 1mA to 3A
- Quiescent Current: 1.9mA Typical
- Quiescent Current in Shutdown: 22µA Typical
- Power Good (PWRGD) Flag (Status Valid in Shutdown)
- Current Limit Protection with Foldback
- Programmable Current Limit
- Output Current Monitor: $I_{OUT}/2650$
- Thermal Limiting with Hysteresis
- Reverse Battery, Reverse Output, and Reverse Current Protection
- 20-Lead 3mm × 4mm QFN Package

APPLICATIONS

- High Efficiency Linear Regulators
- Battery-Powered Systems
- Logic Supplies
- Post Regulator for Switching Supplies
- Wireless Modems
- FPGA Core Supplies

DESCRIPTION

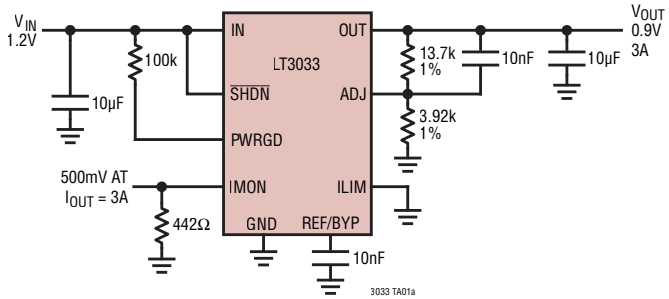
The LT®3033 is a very low dropout voltage (VLDO™) linear regulator that operates from a single input supply down to 0.95V. The device supplies 3A output current with 95mV typical dropout voltage. The LT3033 is ideal for low input voltage to low output voltage applications, providing comparable electrical efficiency to a switching regulator.

The LT3033 optimizes stability and transient response with low ESR ceramic output capacitors as small as 10µF. Other features include programmable current limit, an output current monitor and a power good flag to indicate output voltage regulation. In shutdown, quiescent current typically drops to 22µA. Internal protection circuitry includes reverse-battery protection, current limiting with foldback, thermal limiting with hysteresis and reverse-current protection.

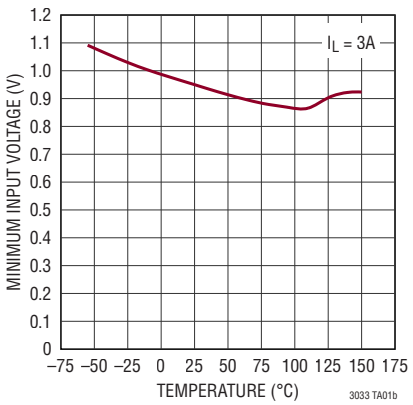
The LT3033 is available as an adjustable device with an output voltage down to the 200mV reference. The device is available in a thermally enhanced, low profile 3mm × 4mm × 0.75mm QFN package.

TYPICAL APPLICATION

1.2V to 0.9V, 3A VLDO Regulator



Minimum Input Voltage vs Temperature



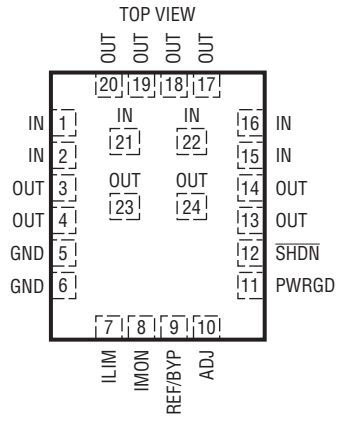
Rev. A

ABSOLUTE MAXIMUM RATINGS

(Note 1)

IN Pin Voltage ..... ±10V
OUT Pin Voltage ..... ±10V
Input-to-Output Differential Voltage ..... ±10V
ADJ Pin Voltage ..... ±10V
REF/BYP Pin Voltage ..... 1V, –0.3V
$\overline{SHDN}$ Pin Voltage ..... ±10V
PWRGD Pin Voltage ..... 10V, –0.3V
ILIM Pin Voltage ..... ±7V
IMON Pin Voltage ..... ±10V
Output Short-Circuit Duration ..... Indefinite
Operating Junction Temperature (Notes 2, 3)
E-/I-grades ..... –40°C to 125°C
Storage Temperature Range
QFN Package ..... –65°C to 150°C

PIN CONFIGURATION



UDC PACKAGE
20-LEAD (3mm × 4mm) QFN, IN/OUT EXPOSED PADS

T_{JMAX} = 125°C, θ_{JA} = 38°C/W, θ_{JC} = 3.4°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3033EUDC#PBF	LT3033EUDC#TRPBF	LGVQ	20-Lead (3mm × 4mm) Plastic QFN	–40°C to 125°C
LT3033IUDC#PBF	LT3033IUDC#TRPBF	LGVQ	20-Lead (3mm × 4mm) Plastic QFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage (Notes 4, 6)	I_{LOAD} = 3A, T_A > 0°C I_{LOAD} = 3A, T_A ≤ 0°C			0.95 0.95	1.05 1.14	V V
ADJ Pin Voltage (Notes 5, 6, 7)	V_{IN} = 1.5V, I_{LOAD} = 1mA 1.14V < V_{IN} < 10V, 1mA < I_{LOAD} < 3A	 ●	197 194	200 200	203 206	mV mV
Line Regulation (Note 13)	V_{IN} = 1.14V to 10V, I_{LOAD} = 1mA	●		0.1	1.25	mV
Load Regulation (Note 13)	V_{IN} = 1.14V, I_{LOAD} = 1mA to 3A	 ●		0.15	1 2	mV mV
Dropout Voltage V_{IN} = $V_{OUT(NOMINAL)}$ (Notes 8, 9)	I_{LOAD} = 100mA I_{LOAD} = 100mA	 ●		45	70 165	mV mV
	I_{LOAD} = 500mA I_{LOAD} = 500mA	 ●		55	85 175	mV mV
	I_{LOAD} = 1.5A I_{LOAD} = 1.5A	 ●		70	105 195	mV mV
	I_{LOAD} = 3A I_{LOAD} = 3A	 ●		95	135 240	mV mV
GND Pin Current V_{IN} = $V_{OUT(NOMINAL)}$ + 0.4V (Notes 9, 10)	I_{LOAD} = 0mA I_{LOAD} = 1mA I_{LOAD} = 100mA I_{LOAD} = 500mA I_{LOAD} = 1.5A I_{LOAD} = 3A	● ● ● ● ● ●		1.9 2 3.2 6 13 27	3.5 3.8 7 14 36 60	mA mA mA mA mA mA
Output Voltage Noise	C_{OUT} = 10µF, I_{LOAD} = 3A, BW = 10Hz to 100kHz, $C_{REF/BYP}$ = 10nF, V_{OUT} = 1.2V, C_{FF} = 10nF			60		μV_{RMS}
ADJ Pin Bias Current (Notes 9, 11)	V_{ADJ} = 0.2V, V_{IN} = 1.5V			5	40	nA
Shutdown Threshold	V_{OUT} = Off to On V_{OUT} = On to Off	● ●	 0.25	0.65 0.63	0.95	V V
$\overline{SHDN}$ Pin Current (Note 12)	$V_{\overline{SHDN}}$ = 0V, V_{IN} = 10V $V_{\overline{SHDN}}$ = 10V, V_{IN} = 10V	● ●		 5.8	±1 15	µA µA
Quiescent Current in Shutdown	V_{IN} = 6V, $V_{\overline{SHDN}}$ = 0V			22	37	µA
PWRGD Trip Point	% of Nominal Output Voltage, Output Rising	●	88	92	95	%
PWRGD Trip Point Hysteresis	% of Nominal Output Voltage, Output Falling			1.9		%
PWRGD Output Low Voltage	I_{PWRGD} = 100µA	●		40	150	mV
PWRGD Leakage Current	$V_{\overline{SHDN}}$ = 0V, V_{PWRGD} = 10V	●			1	µA
Ripple Rejection (Note 13)	V_{IN} – V_{OUT} = 1V, V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 3A			60		dB
	V_{IN} – V_{OUT} = 1V, V_{RIPPLE} = 50mV_{RMS}, f_{RIPPLE} = 10kHz, I_{LOAD} = 3A			60		dB
	V_{IN} – V_{OUT} = 1V, V_{RIPPLE} = 50mV_{RMS}, f_{RIPPLE} = 1MHz, I_{LOAD} = 3A			52		dB
Internal Current Limit (Note 9)	V_{IN} = 4V, V_{OUT} = 0V V_{IN} = 1.14V, ΔV_{OUT} = –0.1V	● ●	3.6 3.1	4.5	5.4	A A
Programmable Current Limit (Note 9)	V_{IN} = 1.5V, R_{ILIM} = 332, V_{OUT} = 0V V_{IN} = 1.5V, R_{ILIM} = 162, V_{OUT} = 0V	● ●	1.32 2.64	1.5 3	1.68 3.36	A A
Input Reverse Leakage Current (Note 14)	V_{IN} = –10V, V_{OUT} = 0V				5	µA
Reverse Output Current (Notes 15, 16)	V_{OUT} = 1.2V, V_{IN} = 0V			0.1	15	µA
Current Monitor Ratio (Note 17) Ratio = I_{OUT}/I_{MON}	I_{LOAD} = 0.1A, 0.5A, 1.5A, 3A T_A > 0°C V_{IN} = 1.5V, V_{OUT} = 1.2V T_A ≤ 0°C		2517.5 2491	2650 2650	2782.5 2809	A/A A/A

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3033 is tested and specified under pulse load conditions such that $T_J \approx T_A$. The LT3033E is 100% tested at T_A = 25°C and performance is guaranteed from 0°C to 125°C. Performance of the LT3033E over the full –40°C and 125°C operating junction temperature range is assured by design, characterization and correlation with statistical process controls. The LT3033I is guaranteed over the full –40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 3: The LT3033 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature exceeds the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: Minimum input voltage is the voltage required by the LT3033 to regulate the output voltage and supply the rated 3A output current. This specification is tested at V_{OUT} = 0.2V. For higher output voltages, the minimum input voltage required for regulation equals the regulated output voltage V_{OUT} plus the dropout voltage or 1.14V, whichever is greater.

Note 5: Maximum junction temperature limits operating conditions. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. Limit the output current range if operating at maximum input voltage. Limit the input-to-output voltage differential range if operating at maximum output current.

Note 6: The LT3033 typically supplies 3A output current with a 0.95V input supply. The guaranteed minimum input voltage for 3A output current is 1.14V, especially if cold temperature operation is required.

Note 7: The LT3033 is tested and specified for these conditions with ADJ tied to OUT.

Note 8: Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout the output voltage equals: ($V_{IN} – V_{DROPOUT}$).

Note 9: The LT3033 is tested and specified for these conditions with an external resistor divider (3.92k and 19.6k) setting V_{OUT} to 1.2V. The external resistor divider adds 50µA of load current.

Note 10: GND pin current is tested with $V_{IN} = V_{OUT(NOMINAL)} + 0.4V$ and a current source load. GND pin current increases in dropout. See GND pin current curves in the Typical Performance Characteristics section.

Note 11: Adjust pin bias current flows into the ADJ pin.

Note 12: Shutdown pin current flows into the $\overline{SHDN}$ pin.

Note 13: The LT3033 is tested and specified for this condition with an external resistor divider (3.92k and 11.8k) setting V_{OUT} to 0.8V. The external resistor divider adds 50µA of load current. The specification refers to the change in the 0.2V reference voltage, not the 0.8V output voltage.

Note 14: Input reverse leakage current flows out of the IN pin.

Note 15: Reverse output current is tested with IN grounded and OUT forced to the rated output voltage. This current flows into the OUT pin and out of the GND pin.

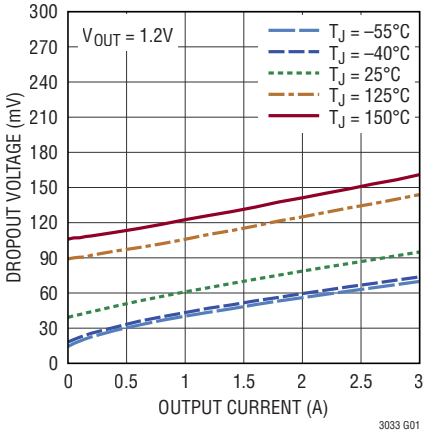
Note 16: Reverse current is higher for the case of (rated_output) < V_{OUT} < V_{IN}, because the no-load recovery circuitry is active in this region and is trying to restore the output voltage to its nominal value.

Note 17: For detailed information on how to calculate the output current from the IMON pin, please see the Applications Information section. If the current monitor function is not needed, the IMON pin must be tied to GND.

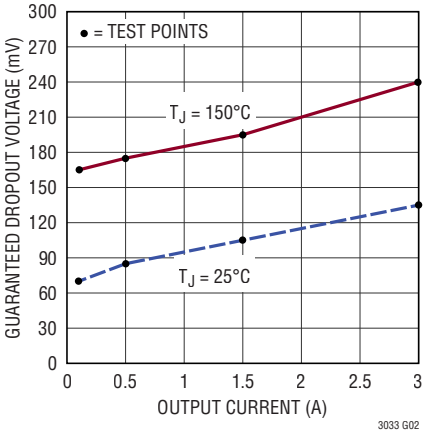
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

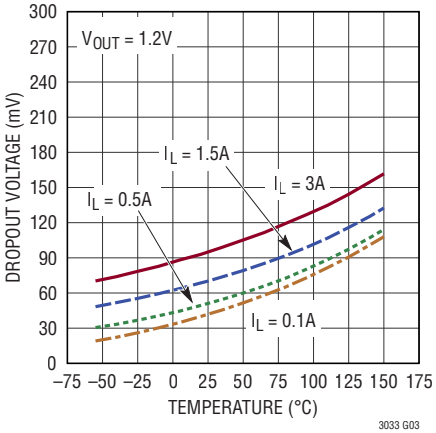
Dropout Voltage



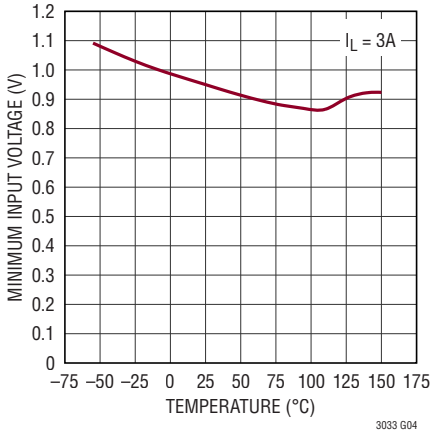
Guaranteed Dropout Voltage



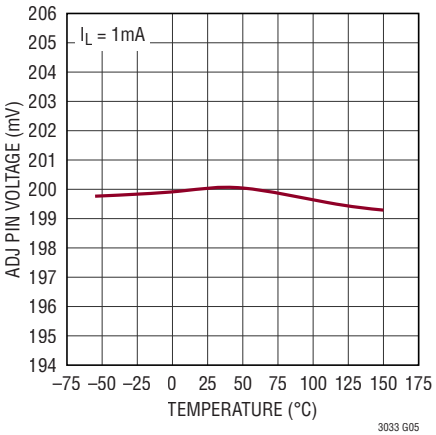
Dropout Voltage



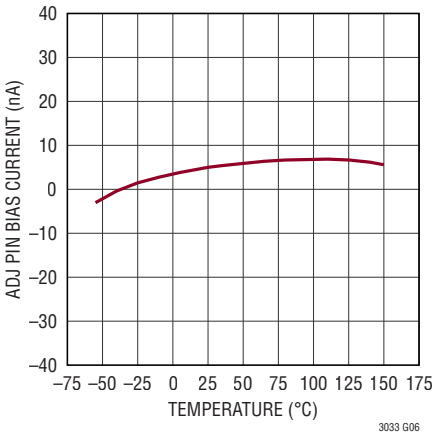
Minimum Input Voltage



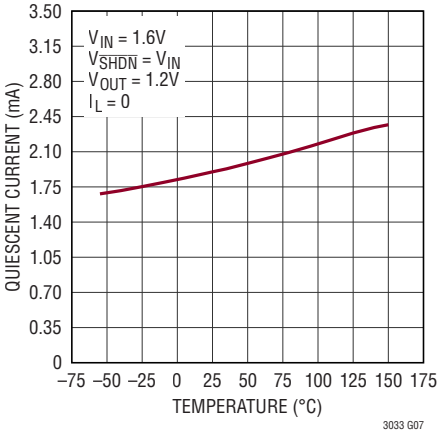
ADJ Pin Voltage



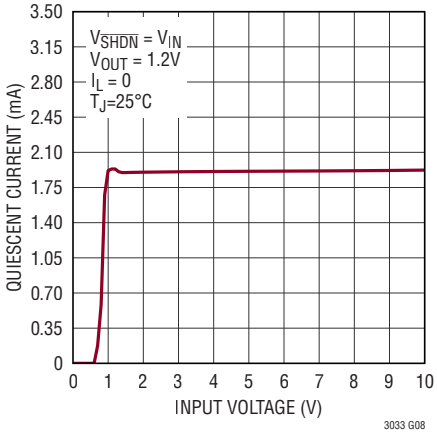
ADJ Pin Bias Current



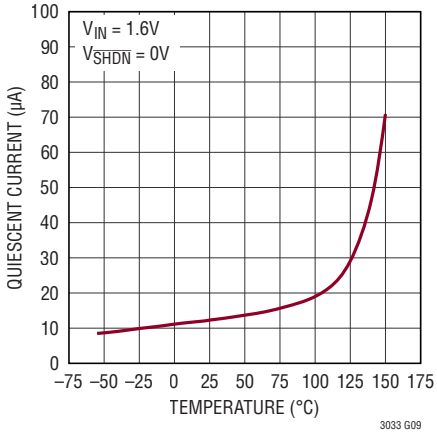
Quiescent Current



Quiescent Current

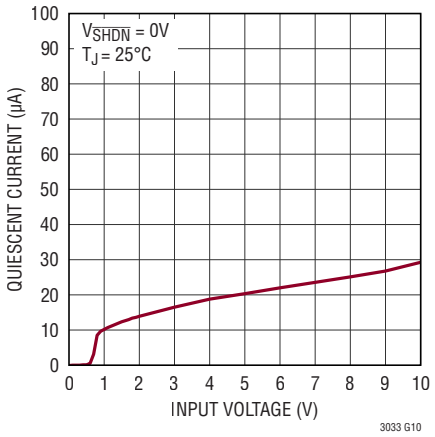


Quiescent Current in Shutdown

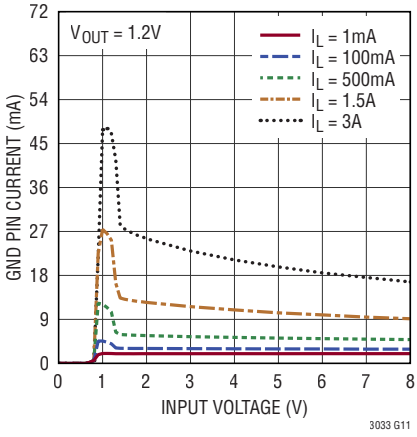


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

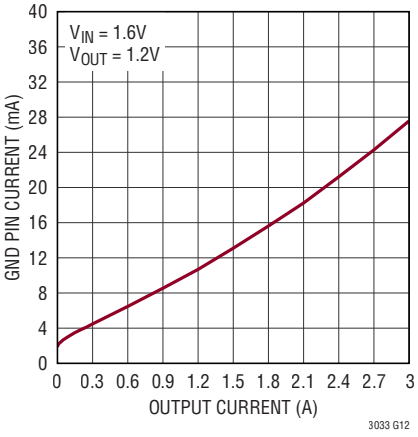
Quiescent Current in Shutdown



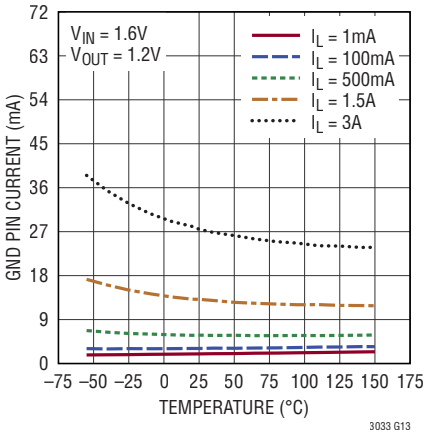
GND Pin Current



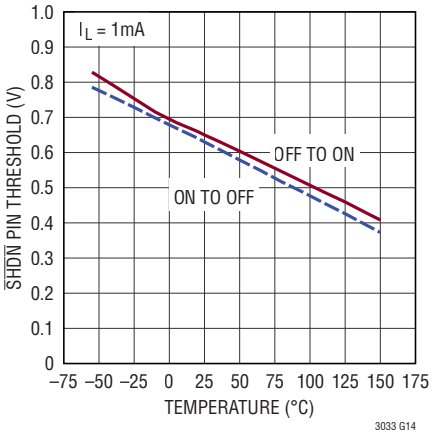
GND Pin Current



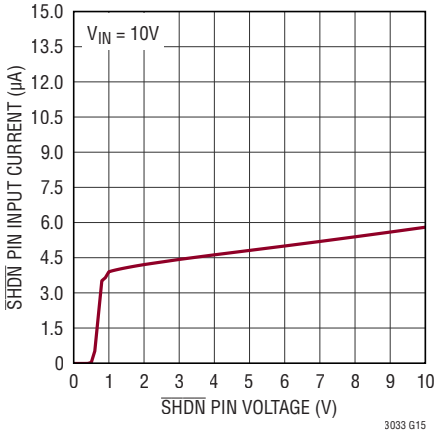
GND Pin Current



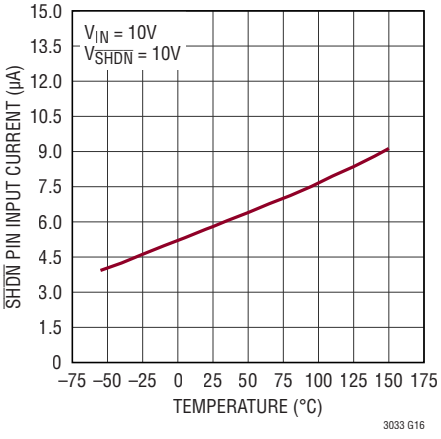
$\overline{SHDN}$ Pin Threshold



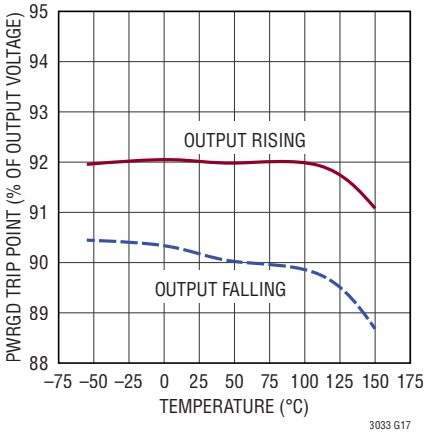
$\overline{SHDN}$ Pin Input Current



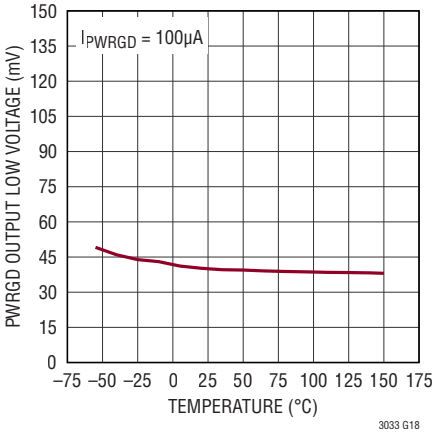
$\overline{SHDN}$ Pin Input Current



PWRGD Trip Point



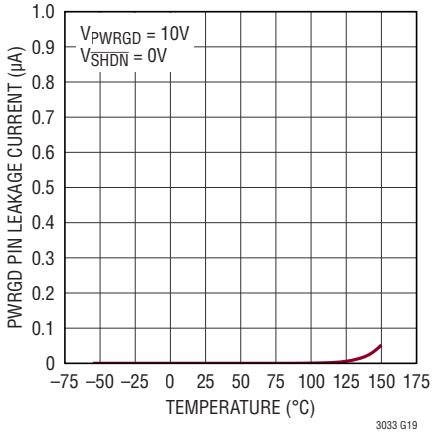
PWRGD Output Low Voltage



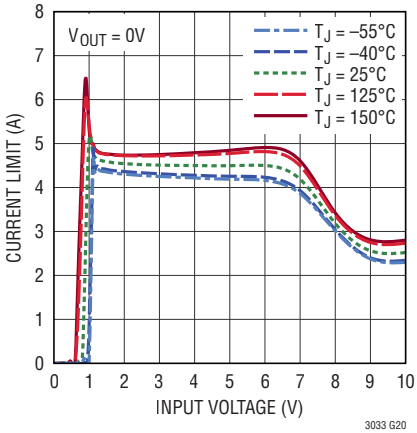
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

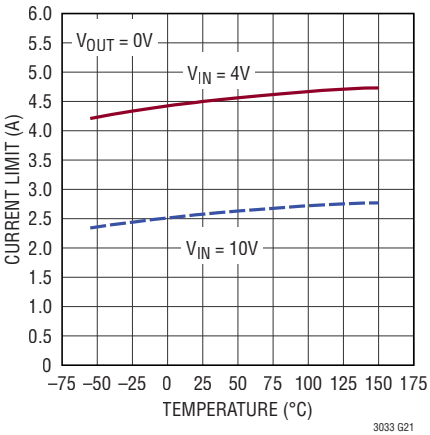
PWRGD Pin Leakage Current



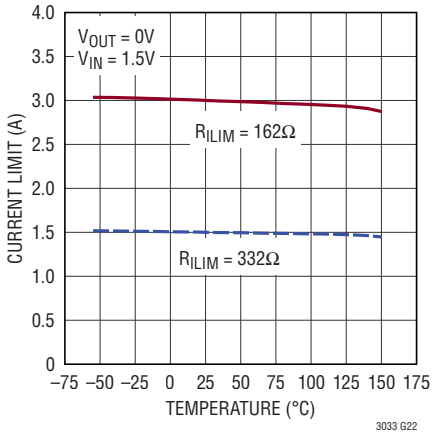
Internal Current Limit



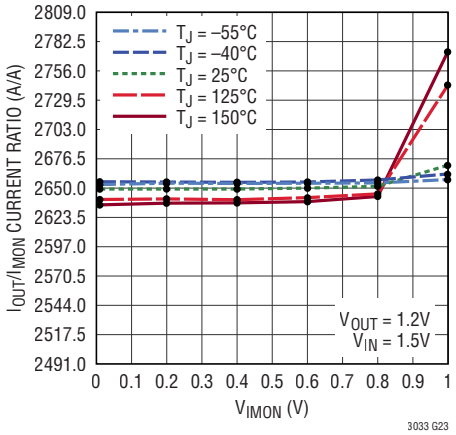
Internal Current Limit



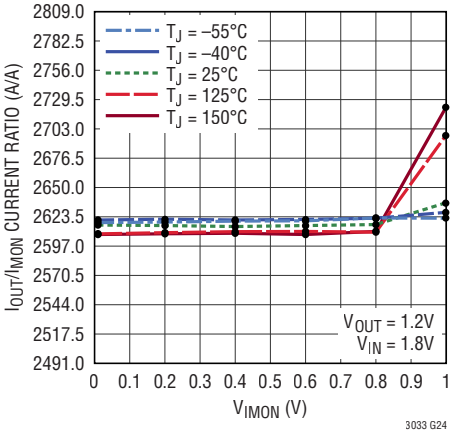
Programmable Current Limit



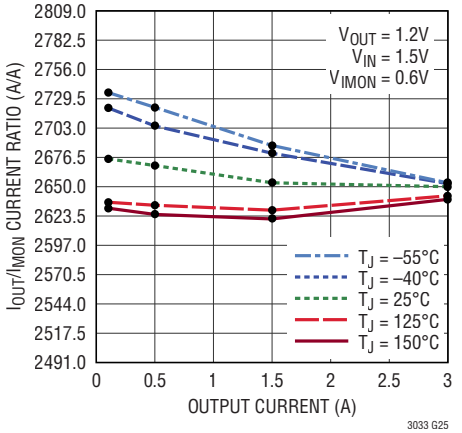
I_{OUT}/I_{MON} Current Ratio, I_{OUT} = 3A



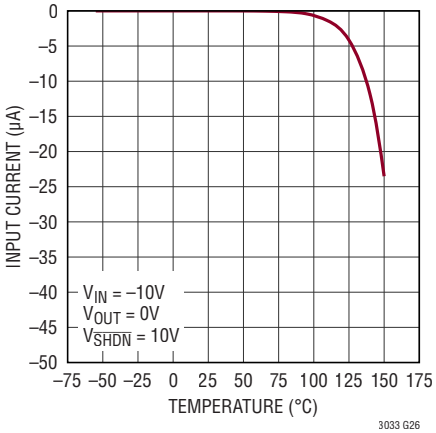
I_{OUT}/I_{MON} Current Ratio, I_{OUT} = 3A



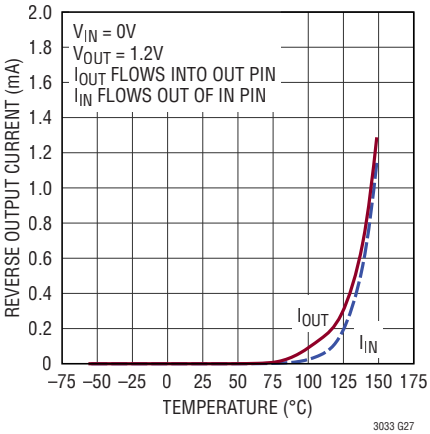
I_{OUT}/I_{MON} Current Ratio



Input Reverse Leakage Current

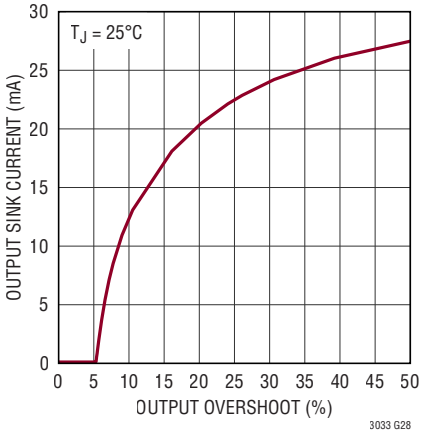


Reverse Output Current

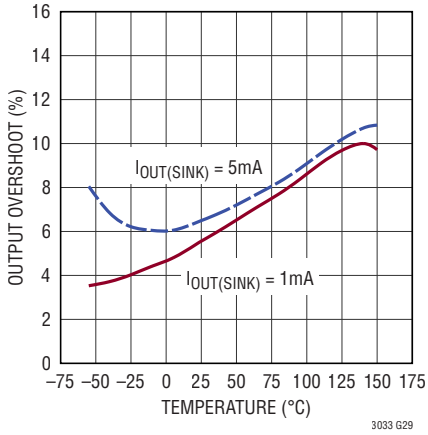


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

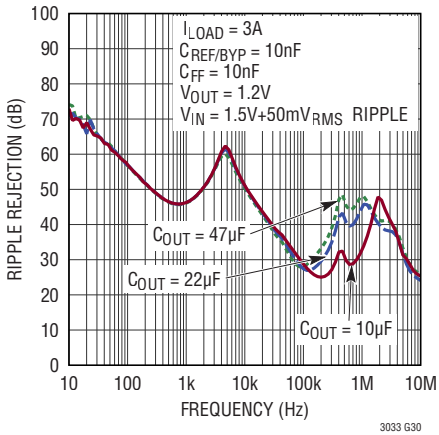
No-Load Recovery Threshold



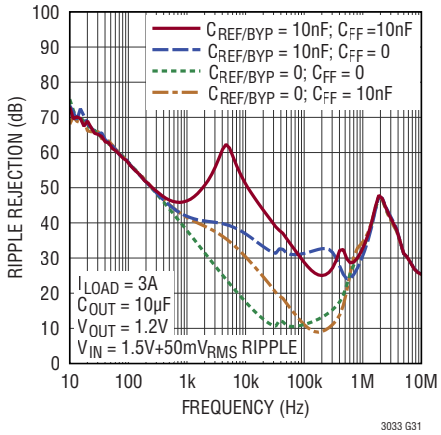
No-Load Recovery Threshold



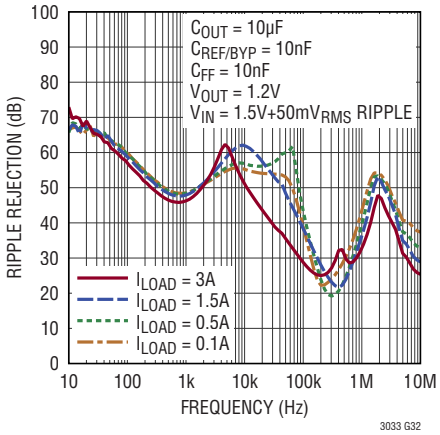
Input Ripple Rejection



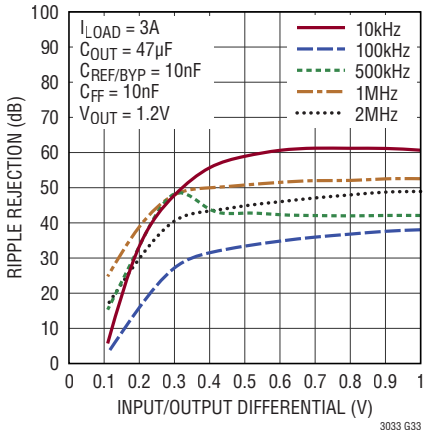
Input Ripple Rejection



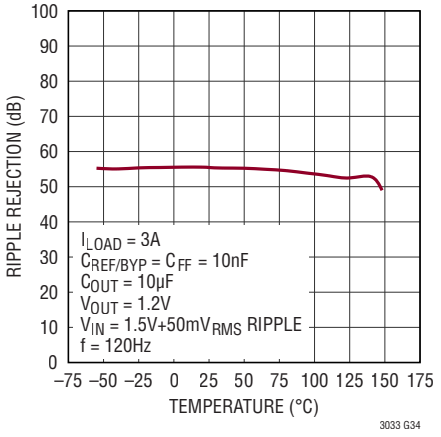
Input Ripple Rejection



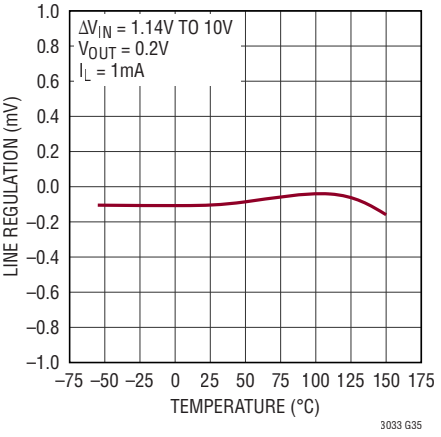
Input Ripple Rejection



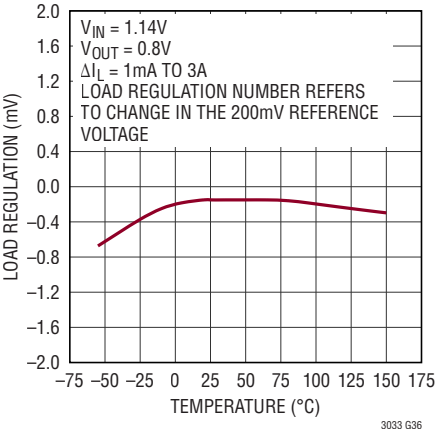
Input Ripple Rejection



Line Regulation



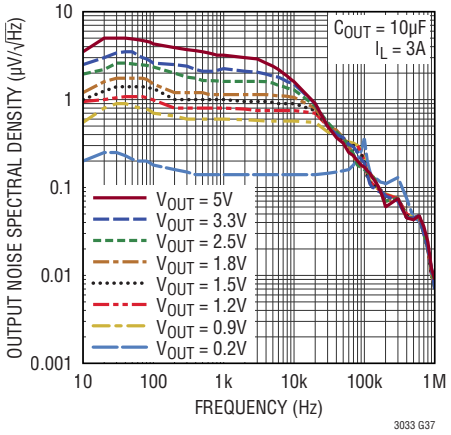
Load Regulation



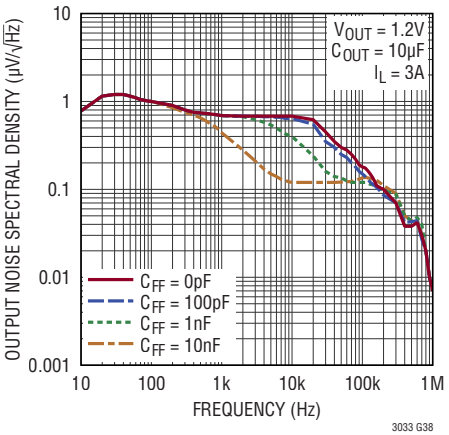
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

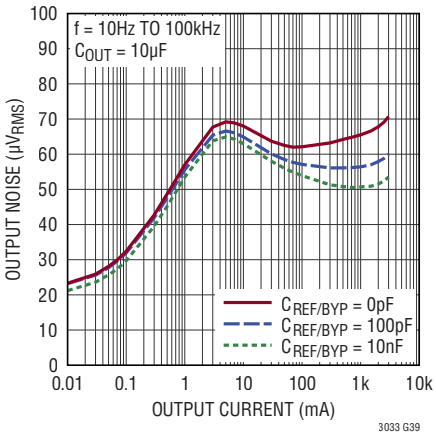
Output Noise Spectral Density
$C_{REF/BYP}$ = 0, C_{FF} = 0



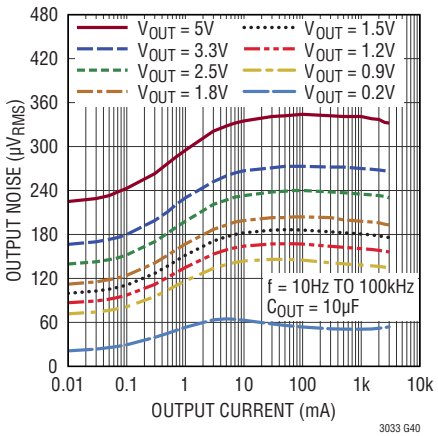
Output Noise Spectral Density
$C_{REF/BYP}$ = 10nF



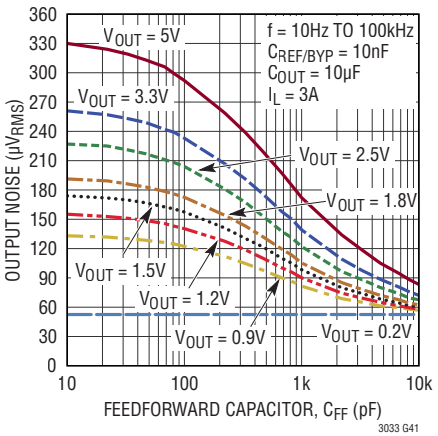
RMS Output Noise
V_{OUT} = 0.2V, C_{FF} = 0



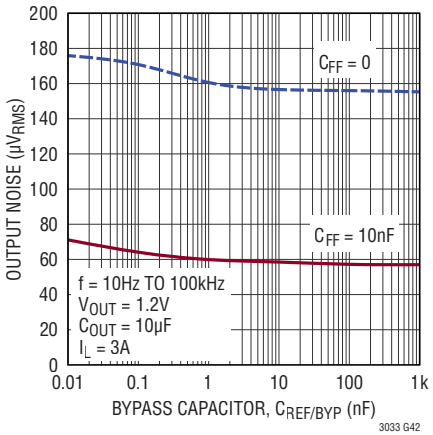
RMS Output Noise
$C_{REF/BYP}$ = 10nF, C_{FF} = 0



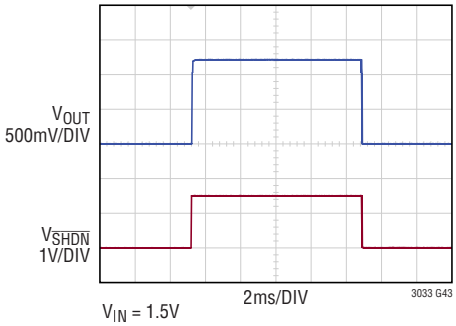
RMS Output Noise vs Feedforward Capacitor (C_{FF})



RMS Output Noise vs Bypass Capacitor ($C_{REF/BYP}$)

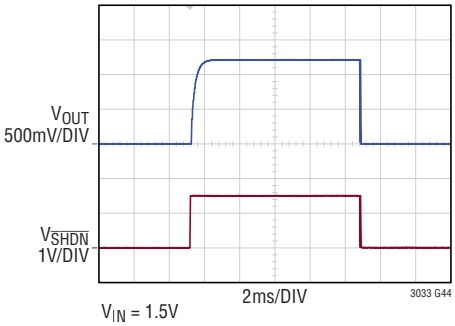


$\overline{SHDN}$ Transient Response
$C_{REF/BYP}$ = 0



V_{IN} = 1.5V
V_{OUT} = 1.2V
R_L = 0.4Ω
C_{OUT} = 10μF

$\overline{SHDN}$ Transient Response
$C_{REF/BYP}$ = 10nF

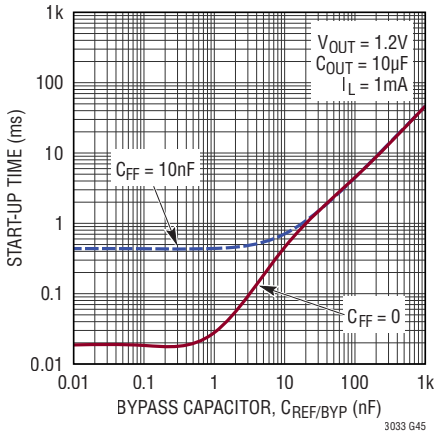


V_{IN} = 1.5V
V_{OUT} = 1.2V
R_L = 0.4Ω
C_{OUT} = 10μF

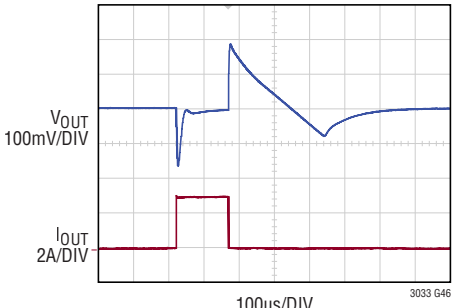
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

Start-Up Time

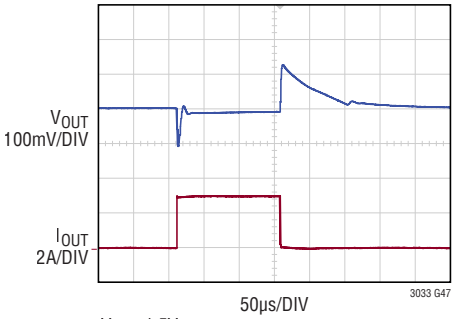


Transient Response
C_{FF} = 0



V_{IN} = 1.5V
V_{OUT} = 1.2V
I_{OUT} = 30mA to 3A
C_{OUT} = 47µF
t_{RISE} = t_{FALL} = 100ns

Transient Response
C_{FF} = 10nF



V_{IN} = 1.5V
V_{OUT} = 1.2V
I_{OUT} = 30mA to 3A
C_{OUT} = 47µF
t_{RISE} = t_{FALL} = 100ns

PIN FUNCTIONS

IN (Pins 1, 2, 15, 16, Exposed Pad Pins 21, 22): Input. These pins supply power to the device. The LT3033 requires a bypass capacitor at IN if located more than six inches from the main input filter capacitor. Include a bypass capacitor in battery-powered circuits as a battery's output impedance rises with frequency. A minimum bypass capacitor of 10µF suffices. The LT3033 withstands reverse voltages on the IN pin with respect to ground and the OUT pin. In the case of a reversed input, which occurs if a battery is plugged in backwards, the LT3033 behaves as if a diode is in series with its input. No reverse current flows into the LT3033 and no reverse voltage appears at the load. The device protects itself and the load.

OUT (Pins 3, 4, 13, 14, 17, 18, 19, 20, Exposed Pad Pins 23, 24): Output. These pins supply power to the load. Use a minimum output capacitor of 10µF to prevent oscillations. Large load transient applications require larger output capacitors to limit peak voltage transients. See the Applications Information section for more information on output capacitance and reverse-output characteristics.

GND (Pins 5, 6): Ground. Connect the bottom of the external resistor divider, directly to GND for optimum regulation.

ILIM (Pin 7): Current Limit Programming Pin. This pin is the collector of a current mirror PNP that is 1/2650th the size of the output power PNP. This pin is also the input to the current limit amplifier. Current limit threshold is set by connecting a resistor between the ILIM pin and GND. For detailed information on how to set the ILIM pin resistor value, please see the Applications Information section. If not used, tie ILIM to ground.

IMON (Pin 8): Output Current Monitor. This pin is the collector of a PNP current mirror that outputs 1/2650th of the power PNP current. For detailed information on how to calculate the output current from the IMON pin, please see the Applications Information section. If the IMON pin is not used, tie IMON to GND.

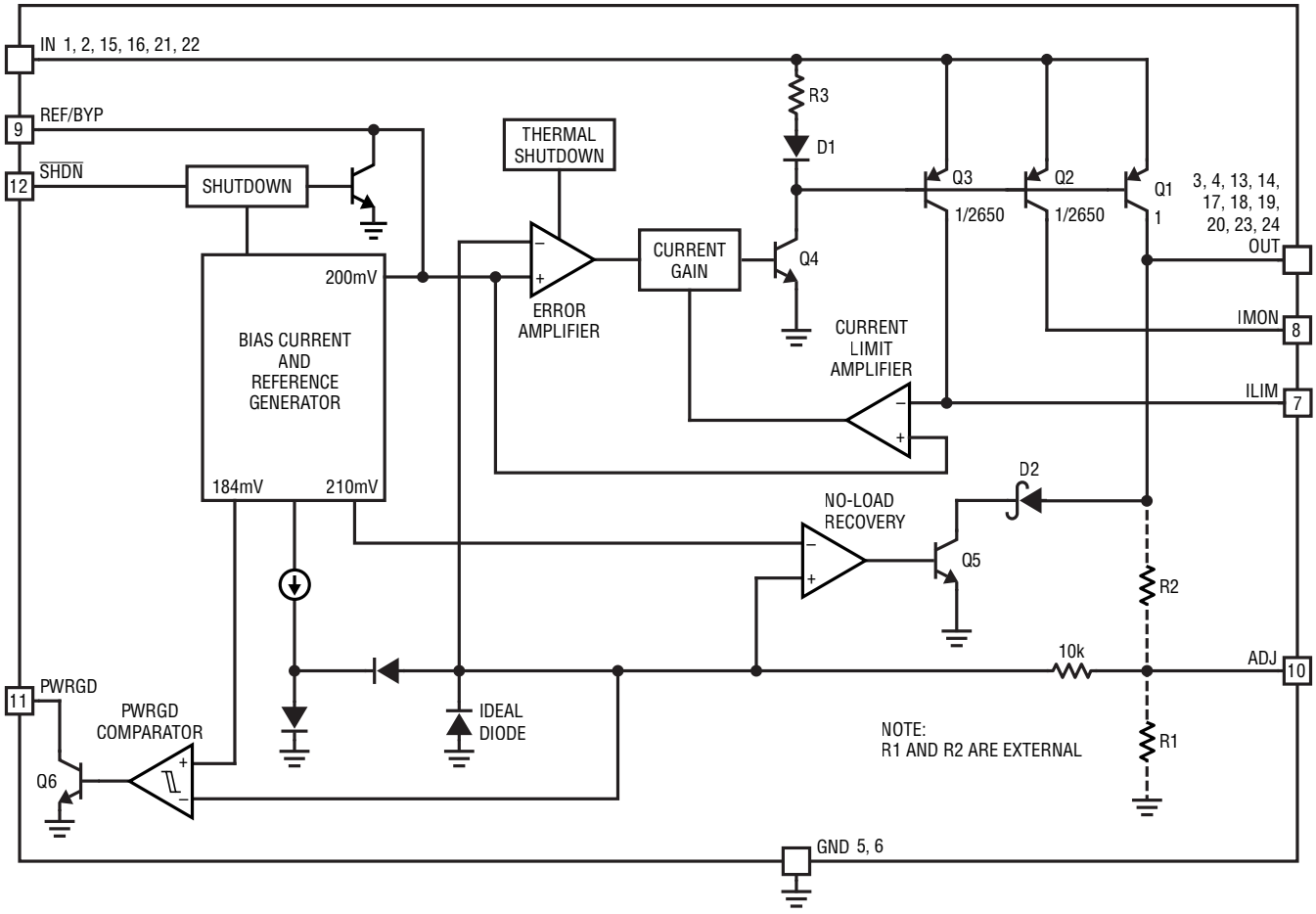
REF/BYP (Pin 9): Reference/Bypass. Connecting a single capacitor from this pin to GND bypasses the LT3033's reference noise and soft-starts the reference. A 10nF bypass capacitor typically reduces output voltage noise to $60\mu V_{RMS}$ in a 10Hz to 100kHz bandwidth. Soft-start time is directly proportional to the REF/BYP capacitor value. If the LT3033 is placed in shutdown, REF/BYP is actively pulled low by an internal device to reset soft-start. If low noise or soft-start performance is not required, this pin must be left floating (unconnected). Do not drive this pin with any active circuitry.

ADJ (Pin 10): Adjust. This pin is the error amplifier inverting terminal. Its 5nA typical input bias current flows into the pin (see curve of ADJ Pin Bias Current vs Temperature in the Typical Performance Characteristics). The ADJ pin reference voltage is 200mV (referred to GND).

PWRGD (Pin 11): Power Good. The PWRGD flag is an open-collector flag to indicate that the output voltage has increased above 92% of the nominal output voltage. There is no internal pull-up on this pin; a pull-up resistor must be used. The PWRGD pin actively pulls low if the output is less than 90.1% of the nominal output voltage. The maximum pull-down current of the PWRGD pin in the low state is 100µA. The PWRGD flag status is valid in shutdown.

$\overline{\text{SHDN}}$ (Pin 12): Shutdown. Pulling the $\overline{\text{SHDN}}$ pin low puts the LT3033 into a low power state and turns the output off. Drive the $\overline{\text{SHDN}}$ pin with either logic or an open-collector/drain device with a pull-up resistor. The resistor supplies the pull-up current to the open collector/drain logic, normally several microamperes, and the $\overline{\text{SHDN}}$ pin current, typically 5.8µA. If unused, connect the $\overline{\text{SHDN}}$ pin to V_{IN}. The LT3033 does not function if the $\overline{\text{SHDN}}$ pin is not connected.

BLOCK DIAGRAM

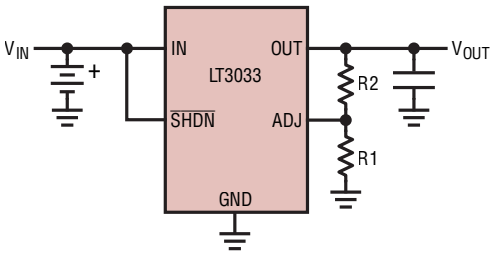


APPLICATIONS INFORMATION

The LT3033 very low dropout linear regulator is capable of 0.95V input supply operation. It supplies 3A output current and dropout voltage is typically 95mV. Quiescent current is typically 1.9mA and drops to 22µA in shutdown. The LT3033 incorporates several protection features, making it ideal for use in battery-powered systems. The device protects itself against reverse-input and reverse-output voltages. If the output is held up by a backup battery when the input is pulled to ground in a battery backup application, the LT3033 behaves as if a diode is in series with its output, preventing reverse current flow. In dual supply applications where the regulator load is returned to a negative supply, pulling the output below ground by as much as 10V does not affect start-up or normal operation.

Adjustable Operation

The LT3033's output voltage range is 0.2V to 9.7V. Figure 1. Adjustable Operation shows that the external resistor ratio sets output voltage. The device regulates the output to maintain ADJ at 200mV referred to ground. If R1's current is at least 50µA, the ADJ pin bias current can be neglected and R2's current is equal to R1's current. Use Figure 1's formula to calculate output voltage. In shutdown, the output is off and the divider current is zero. Curves of ADJ Pin Voltage vs Temperature and ADJ Pin Bias Current vs Temperature appear in the Typical Performance Characteristics section.



V_{OUT}: 200mV • (1 + R2/R1) + (I_{ADJ} • R2)
V_{ADJ}: 200mV
I_{ADJ}: 5nA AT 25°C
OUTPUT RANGE: 0.2V TO 9.7V

Figure 1. Adjustable Operation

Specifications for output voltages greater than 200mV are proportional to the ratio of desired output voltage to 200mV (V_{OUT}/200mV). For example, load regulation for an output current change of 1mA to 3A is typically 150µV at V_{ADJ} = 200mV. At V_{OUT} = 1.5V, load regulation is:

1.5V/200mV • 150µV = 1.125mV

Table 1 shows 1% resistor divider values for some common output voltages with a resistor divider current equaling or about 50µA.

Table 1

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
0.9	3.92	13.7
1.0	3.92	15.8
1.2	3.92	19.6
1.5	3.92	25.5
1.8	3.92	31.6
2.5	3.92	45.3
3.3	3.92	60.4
5	3.92	95.3

Bypass Capacitance, Output Voltage Noise and Transient Response

The LT3033 regulator provides low output voltage noise over the 10Hz to 100kHz bandwidth while operating at full load with the addition of a reference bypass capacitor ($C_{REF/BYP}$) from the REF/BYP pin to GND. A good quality, low leakage capacitor is recommended. This capacitor bypasses the internal reference of the regulator, providing a low frequency noise pole. With the use of 10nF for $C_{REF/BYP}$, the output voltage noise decreases to as low as 160µV_{RMS} when the output voltage is set for 1.2V. For higher output voltages (generated by using a feedback resistor divider), the output voltage noise gains up accordingly when using $C_{REF/BYP}$ by itself.

To lower the output voltage noise for higher output voltages, include a feedforward capacitor (C_{FF}) from V_{OUT} to the ADJ pin. A good quality, low leakage capacitor is recommended. This capacitor bypasses the error amplifier of the regulator, providing a low frequency noise pole. With the use of 10nF for both C_{FF} and $C_{REF/BYP}$, output voltage

APPLICATIONS INFORMATION

noise decreases to 60μV_{RMS} when the output voltage is set to 1.2V by a 50μA feedback resistor divider. If the current in the feedback resistor divider is doubled, C_{FF} must also be doubled to achieve equivalent noise performance.

Higher values of output voltage noise are often measured if care is not exercised with regard to circuit layout and testing. Crosstalk from nearby traces induces unwanted noise onto the LT3033's output. Power supply ripple rejection must also be considered. The LT3033 regulator does not have unlimited power supply rejection and will pass a small portion of the input noise through to the output.

Using a feedforward capacitor (C_{FF}) from V_{OUT} to the ADJ pin has the added benefit of improving transient response for output voltages greater than 0.2V. With no feedforward capacitor, the settling time will increase as the output voltage is raised above 0.2V (see Transient Response in the Typical Performance Characteristics section).

During start-up, the internal reference soft-starts if a reference bypass capacitor is present. Regulator start-up time is directly proportional to the size of the bypass capacitor, slowing to 0.5ms with a 10nF bypass capacitor (See Start-Up Time in the Typical Performance Characteristics section). The reference bypass capacitor is actively pulled low during shutdown to reset the internal reference.

Start-up time is also affected by the use of a feedforward capacitor. Start-up time is directly proportional to the size of the feedforward capacitor and output voltage, and is inversely proportional to the feedback resistor divider current, slowing to 0.4ms with a 10nF feedforward capacitor and a 10μF output capacitor for an output voltage set to 1.2V by a 50μA feedback resistor divider.

Input Capacitance and Stability

The LT3033 design is stable with a minimum of 10μF capacitor placed at the IN pin. Very low ESR ceramic capacitors may be used. However, in cases where long wires connect the power supply to the LT3033's input and ground, use of low value input capacitors combined with an output load current of greater than 20mA may result in instability. The resonant LC tank circuit formed by the wire inductance and the input capacitor is the cause and not a result of LT3033 instability.

The self-inductance, or isolated inductance, of a wire is directly proportional to its length. However, the wire diameter has less influence on its self-inductance. For example, the self-inductance of a 2-AWG isolated wire with a diameter of 0.26" is about half the inductance of a 30-AWG wire with a diameter of 0.01". One foot of 30-AWG wire has 465nH of self-inductance.

Several methods exist to reduce a wire's self-inductance. One method divides the current flowing towards the LT3033 between two parallel conductors. In this case, placing the wires further apart reduces the inductance; up to a 50% reduction when placed only a few inches apart. Splitting the wires connects two equal inductors in parallel. However, when placed in close proximity to each other, mutual inductance adds to the overall self-inductance of the wires. The most effective technique to reducing overall inductance is to place the forward and return current conductors (the input wire and the ground wire) in close proximity. Two 30-AWG wires separated by 0.02" reduce the overall self-inductance to about one-fifth of a single wire.

If a battery, mounted in close proximity, powers the LT3033, a 10μF input capacitor suffices for stability. However, if a distantly located supply powers the LT3033, use a larger value input capacitor. Use a rough guideline of 1μF (in addition to the 10μF minimum) per eight inches of wire length. The minimum input capacitance needed to stabilize the application also varies with power supply output impedance variations. Placing additional capacitance on the LT3033's output also helps. However, this requires an order of magnitude more capacitance in comparison with additional LT3033 input bypassing. Series resistance between the supply and the LT3033 input also helps stabilize the application; as little as 0.1Ω to 0.5Ω suffices. This impedance dampens the LC tank circuit at the expense of dropout voltage. A better alternative is to use higher ESR tantalum or electrolytic capacitors at the LT3033 input in place of ceramic capacitors.

APPLICATIONS INFORMATION

Output Capacitance and Transient Response

The LT3033's design is stable with a wide range of output capacitors, but is optimized for low ESR ceramic capacitors. The output capacitor's ESR affects stability, most notably with small value capacitors. Use a minimum output capacitor of 10µF with an ESR of less than 0.1Ω to prevent oscillations. The LT3033 is a low voltage device and output load transient response is a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for large load current changes. Ceramic capacitors require extra consideration. Manufacturers make ceramic capacitors with a variety of dielectrics; each with a different behavior across temperature and applied voltage. The most common dielectrics are Z5U, Y5V, X5R and X7R. Z5U and Y5V dielectrics provide high C-V products in a small package at low cost, but exhibit strong voltage and temperature coefficients. X5R and X7R dielectrics yield highly stable characteristics and are more suitable for use as the output capacitor at fractionally increased cost. X7R works over a larger temperature range and exhibits better temperature stability whereas X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors. The X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases, but expected capacitance at operating voltage should be verified. Figure 2 and Figure 3 show voltage coefficient and temperature coefficient comparisons between Y5V and X5R material.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients. The resulting voltages produced can cause appreciable amounts of noise. A ceramic capacitor produced Figure 4's trace in response to light tapping from a pencil. Similar vibration induced behavior can masquerade as increased output voltage noise.

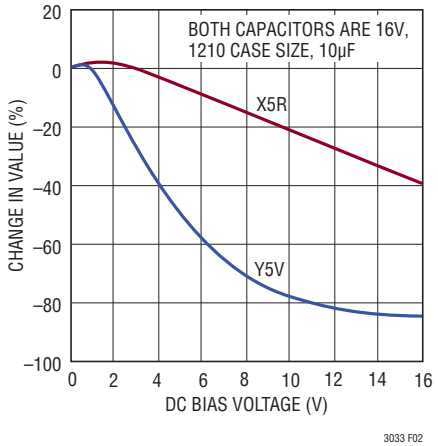


Figure 2. Ceramic Capacitor DC Bias Characteristics

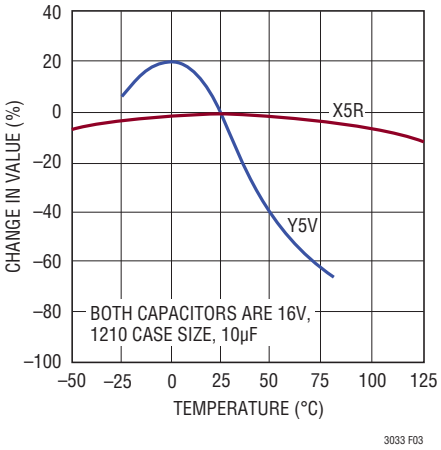


Figure 3. Ceramic Capacitor Temperature Characteristics

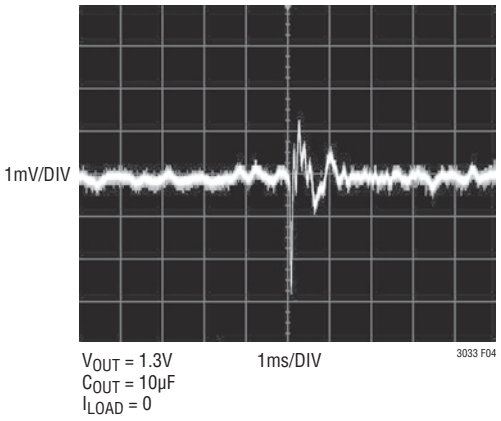


Figure 4. Noise Resulting from Tapping on a Ceramic Capacitor

APPLICATIONS INFORMATION

No-Load/Light-Load Recovery

A possible transient load step that occurs is where the output current changes from its maximum level to zero current or a very small load current. The output voltage responds by overshooting until the regulator lowers the amount of current it delivers to the new level. The regulator loop response time and the amount of output capacitance control the amount of overshoot. Once the regulator has decreased its output current, the current provided by the resistor divider (which sets V_{OUT}) is the only current remaining to discharge the output capacitor from the level to which it overshot. The amount of time it takes for the output voltage to recover easily extends to milliseconds with minimum divider current and many microfarads of output capacitance.

To eliminate this problem, the LT3033 incorporates a no-load or light load recovery circuit. This circuit is a voltage-controlled current sink that significantly improves the light load transient response time by discharging the output capacitor quickly and then turning off. The current sink turns on when the output voltage exceeds 5.3% of the nominal output voltage. The current sink level is then proportional to the overdrive above the threshold up to a maximum of about 27mA. Consult the curve in the Typical Performance Characteristics for the No-Load Recovery Threshold.

If external circuitry forces the output above the no-load recovery circuit's threshold, the current sink turns on in an attempt to restore the output voltage to nominal. The current sink remains on until the external circuitry releases the output. However, if the external circuitry pulls the output voltage above the input voltage or the input falls below the output, the LT3033 turns the current sink off and shuts down the bias current/reference generator circuitry.

PWRGD Flag

The PWRGD flag indicates that the ADJ pin voltage is within 8% of the regulated voltage. The PWRGD pin is an open-collector output, capable of sinking 100µA of current when the ADJ pin voltage is below 90.1% of the regulated voltage. There is no internal pull-up on the PWRGD pin; an external pull-up resistor must be used. As the ADJ pin voltage rises above 92% of its regulated voltage, the PWRGD pin switches to a high impedance state and the external pull-up resistor pulls the PWRGD pin voltage up. During normal operation, an internal glitch filter prevents the PWRGD pin from switching to a low voltage state if the ADJ pin voltage falls below the regulated voltage by more than 10% in a short transient (<40µs typical) event.

The use of a feedforward capacitor, CFF, can result in the ADJ pin being pulled artificially high during start-up transients, which causes the PWRGD flag to assert early. To avoid this problem, ensure that the REF/BYP capacitor is significantly larger than the feedforward capacitor, causing REF/BYP time constant to dominate over the time constant of the resistor divider network.

IMON Pin Operation (Current Monitor)

The IMON pin is the collector of a PNP which mirrors the LT3033 output PNP at a ratio of 1:2650 (see Block Diagram). Additional circuitry compensates for early voltage variation by regulating the collector of the IMON mirror PNP at the output voltage. This circuitry is active for $V_{IMON} \leq (V_{OUT} – 400mV)$. Use the IMON pin where the early voltage compensation circuit is active and calculate the output current from the simple equation:

$$I_{OUT} = 2650 \bullet (V_{IMON}/R_{IMON})$$

The IMON mirror ratio is affected by power dissipation in the LT3033; the IMON pin current increases at a rate of approximately two percent per watt of power dissipation in the device.

ILIM Pin Operation

The ILIM pin is the collector of a PNP which mirrors the LT3033 output PNP at a ratio of 1:2650 (see Block Diagram). The ILIM pin is also the input to the current limit amplifier. If the output load increases to the point where it causes the ILIM pin voltage to reach 0.198V, the current limit amplifier takes control of the output regulation so that the ILIM pin regulates at 0.198V, regardless of the output voltage. The current limit threshold (I_{LIMIT}) is set by connecting a resistor (R_{ILIM}) from ILIM to GND:

$$R_{ILIM} = 2650 \bullet (0.198V/I_{LIMIT}) – 14\Omega$$

In cases where the IN to OUT differential voltage exceeds 5V, fold-back current limit lowers the internal current limit

APPLICATIONS INFORMATION

level, possibly causing it to override the external programmable current limit. See the Internal Current Limit vs V_{IN} graph in the Typical Performance Characteristics section. If the external programmable current limit is not needed, tie the ILIM pin to GND. The external programmable current limit is affected by power dissipation in the LT3033; it decreases at a rate of approximately four percent per watt.

Paralleling Devices

Paralleling multiple LT3033s together produces higher output current. Tie the individual OUT pins together and tie the individual IN pins together. IMON pins combined with an external NPN or NMOS current mirror create a simple amplifier. This amplifier injects current into or out of the feedback divider of the slave LT3033 to force the IMON currents from each LT3033 to be equal. Figure 5 shows an implementation with inexpensive 2N3904 NPN devices. 100Ω resistors provide 113mV emitter degeneration at full load to guarantee good current mirror matching. The feedback resistors of the slave LT3033 are split into sections to ensure adequate headroom for the slave 2N3904. A 10nF, 5.1k capacitor and resistor combination added to the IMON pin of the slave device frequency compensates the feedback loop.

This circuit architecture is scalable to as many LT3033s as are needed simply by extending the current mirror and adding slave LT3033 devices. In addition to higher output currents, this architecture also benefits heat spreading by spreading the devices on the printed circuit board.

Thermal Considerations

The LT3033's maximum rated junction temperature of 125°C limits its power handling capability. Two components comprise the power dissipation of the device:

1. Output current multiplied by the input-to-output voltage differential:

   $(I_{LOAD}) \bullet (V_{IN} - V_{OUT})$ and

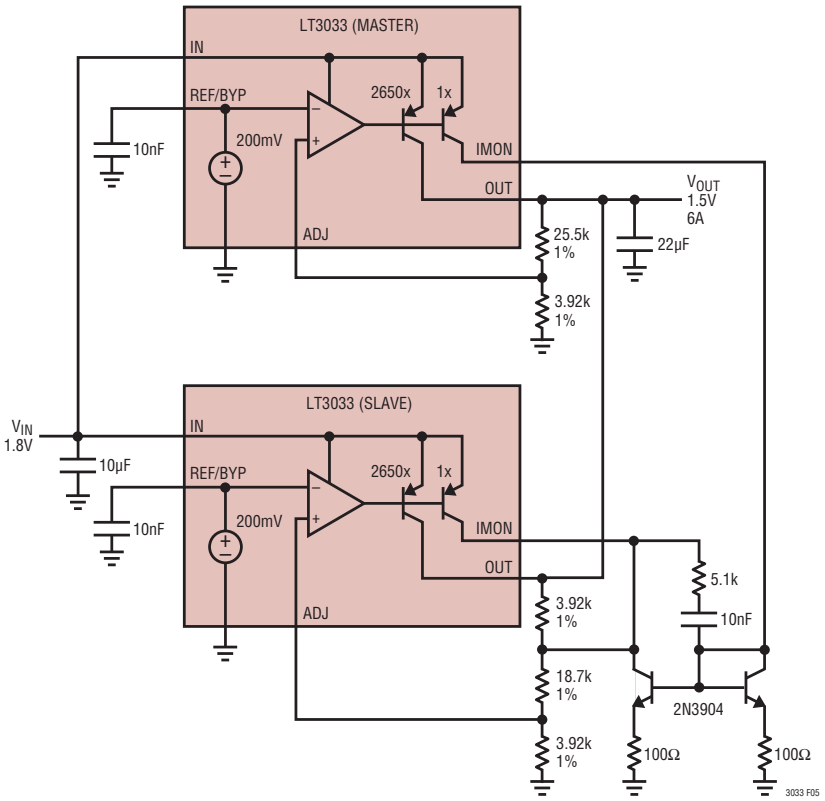


Figure 5. Paralleling Devices

APPLICATIONS INFORMATION

2. GND pin current multiplied by the input voltage:

$(I_{GND}) \bullet (V_{IN})$

GND pin current is found by examining the GND pin current curves in the Typical Performance Characteristics. Power dissipation equals the sum of the two components listed. The LT3033's internal thermal limiting (with hysteresis) protects the device during overload conditions. For normal continuous conditions, do not exceed the maximum junction temperature rating of 125°C (E- and I-grades). Carefully consider all sources of thermal resistance from junction to ambient including other heat sources mounted in proximity to the LT3033.

The underside of the LT3033 UDC package has exposed metal from the lead frame to the die attachment. Heat transfers directly from the die junction to the printed circuit board metal, allowing maximum junction temperature control. The multiple IN and OUT pins of the LT3033 also assist in spreading heat to the PCB. Copper board stiffeners and plated throughholes can also be used to spread the heat generated by power devices. Table 2 lists thermal resistance as a function of copper area in a fixed board size. All measurements are taken in still air on a 4-layer FR-4 board with 1oz solid internal planes, and 2oz external trace planes with a total board thickness of 1.6mm. For more information on thermal resistance and high thermal conductivity test boards, refer to JEDEC standard JESD51, notably JESD51-12 and JESD51-7. Achieving low thermal resistance necessitates attention to detail and careful PCB layout.

Table 2. Measured Thermal Resistance for UDC Package

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE*	BACKSIDE		
2500mm^2	2500mm^2	2500mm^2	38°C/W
1000mm^2	2500mm^2	2500mm^2	40°C/W
225mm^2	2500mm^2	2500mm^2	41°C/W
100mm^2	2500mm^2	2500mm^2	45°C/W

*Device is mounted on topside

PCB Layout Considerations

Given the probable high power consumption in the LT3033, care must be taken in the layout of the PCB to achieve good thermal performance. *Figure 6 shows a recommended layout that improves thermal resistance. The vias next to the input and output exposed pads as shown in Figure 6 help improve the thermal resistance with 30°C/W as measured on the demo board of the LT3033. Refer to the LT3033's DC2362A demo board manual for further details.*

Calculating Junction Temperature

Example: Given an output voltage of 1.5V, an input voltage range of 1.8V to 1.9V, an output load current range of 1mA to 3A and a maximum ambient temperature of 70°C, what is the maximum junction temperature for an application using the UDC package?

The power dissipated by the device equals:

$I_{LOAD(MAX)} \bullet (V_{IN(MAX)} - V_{OUT}) + I_{GND} \bullet (V_{IN(MAX)})$

where:

$I_{LOAD(MAX)} = 3A$

$V_{IN(MAX)} = 1.9V$

I_{GND} at ($I_{LOAD} = 3A$, $V_{IN} = 1.9V$) = 27mA

so:

$P = 3A \bullet (1.9V - 1.5V) + 27mA \bullet (1.9V) = 1.25W$

The thermal resistance is about 40°C/W depending on the copper area. So the junction temperature rise above ambient is approximately equal to:

$1.25W \bullet (40°C/W) = 50°C$

The maximum junction temperature equals the maximum junction temperature rise above ambient plus the maximum ambient temperature or:

$T_{JMAX} = 70°C + 50°C = 120°C$

APPLICATIONS INFORMATION

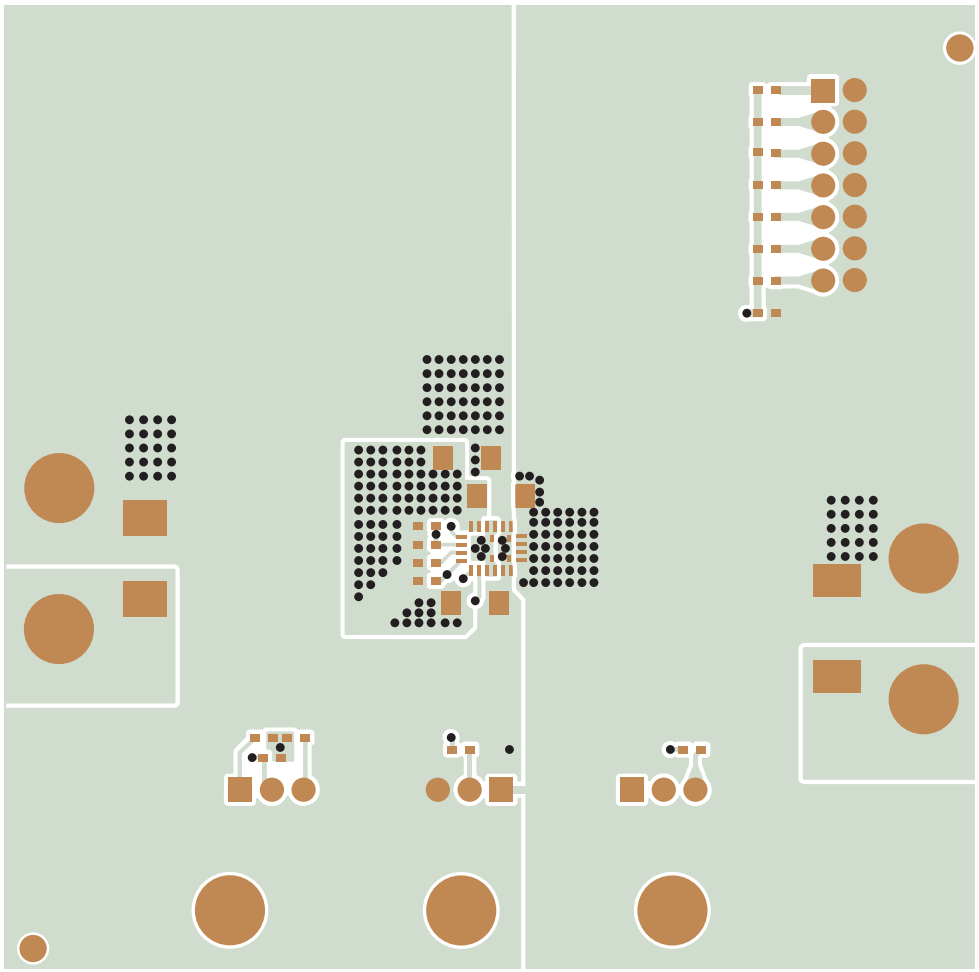


Figure 6. Recommended Layout (Demo Board DC2362A)

APPLICATIONS INFORMATION

Protection Features

The LT3033 incorporates several protection features that make it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device also protects against reverse-input voltages, reverse-output voltages and reverse output to-input voltages.

Current limit protection and thermal overload protection protect the device against current overload conditions at its output. For normal operation, do not exceed 125°C (E- and I-grades) junction temperature. The typical thermal shutdown temperature is 175°C and the thermal shutdown circuit incorporates about 6°C of hysteresis.

The IN pins withstand reverse voltages of 10V. The LT3033 limits current flow to less than 10µA and no negative voltage appears at OUT. The device protects both itself and the load against batteries that are plugged in backwards. The LT3033 incurs no damage if OUT is pulled below ground. If IN is left open circuited or grounded, OUT can be pulled below ground by 10V. No current flows from the pass transistor connected to OUT. However, current flows in (but is limited by) the resistor divider that sets the output voltage. Current flows from the bottom resistor in the divider and from the ADJ pin's internal clamp through the top resistor in the divider to the external circuitry pulling OUT below ground. If IN is powered by a voltage source, OUT sources current equal to its current limit capability and the LT3033 protects itself by thermal limiting. In this case, grounding $\overline{SHDN}$ turns off the LT3033 and stops OUT from sourcing current.

The LT3033 incurs no damage if the ADJ pin is pulled above or below ground by 10V. If IN is left open-circuited or grounded and ADJ is pulled above ground, ADJ acts like a 10k resistor in series with two diodes. ADJ acts like a 10k resistor if pulled below ground. If IN is powered by a voltage source and ADJ is pulled below its reference voltage, the LT3033 attempts to source its current limit capability at OUT. The output voltage increases to $V_{IN} – V_{DROPOUT}$ with $V_{DROPOUT}$ set by whatever load current the LT3033 supports. This condition can potentially damage external circuitry powered by the LT3033 if the output voltage increases to an unregulated high voltage. If IN is powered by a voltage source and ADJ is pulled above its reference voltage, two situations can occur. If ADJ is pulled slightly above its reference voltage, the LT3033 turns off the pass transistor, no output current is sourced and the output voltage decreases to either the voltage at ADJ or less. If ADJ is pulled above its no-load recovery threshold, the no-load recovery circuitry turns on and attempts to sink current. OUT is actively pulled low and the output voltage clamps at a Schottky diode above ground. Please note that the behavior described above applies to the LT3033 only. If a resistor divider is connected under the same conditions, there will be additional R current.

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage or is left open circuit. In the case where the input is grounded, there is less than 5µA of reverse output current. If the LT3033 IN pin is forced below the OUT pin or the OUT pin is pulled above the IN pin, input current drops to less than 30µA typically. This occurs if the LT3033 input is connected to a discharged (low voltage) battery and either a backup battery or a second regulator circuit holds up the output. The state of the $\overline{SHDN}$ pin has no effect on the reverse output current if OUT is pulled above IN.

APPLICATIONS INFORMATION

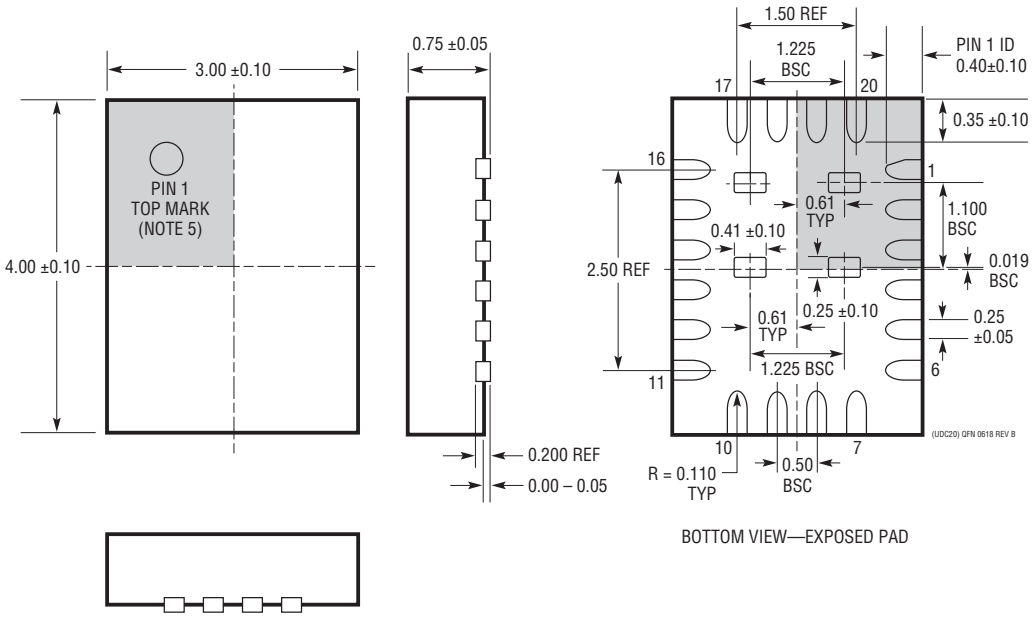
Overload Recovery

Like many IC power regulators, the LT3033 has safe operating area (SOA) protection. The safe area protection decreases current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The protective design provides some output current at all values of input-to-output voltage up to the specified maximum operational input voltage of 10V.

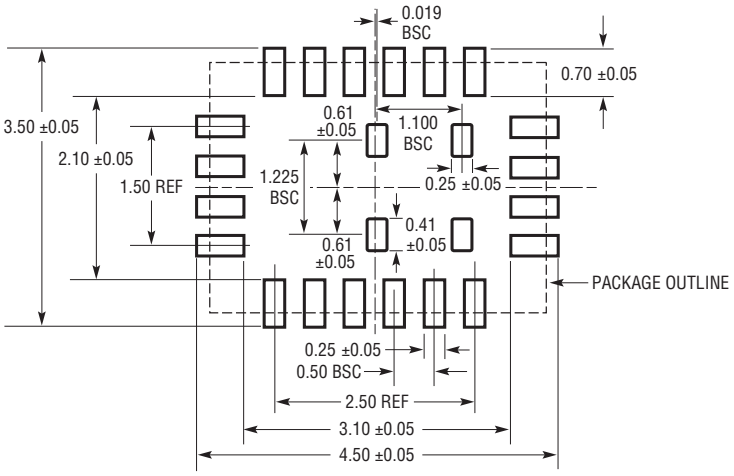
When power is first applied, as input voltage rises, the output follows the input, allowing the regulator to start-up into heavy loads. During start-up, as the input voltage is rising, the input-to-output voltage differential is small, allowing the regulator to supply large output currents. With a high input voltage, an event can occur wherein removal of an output short will not allow the output to recover. The event occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations occur immediately after the removal of a short-circuit or if the shutdown pin is pulled high after the input voltage has already been turned on. The load line intersects the output current curve at two points creating two stable output operating points for the regulator. With this double intersection, the input power supply may need to be cycled down to zero and brought up again to make the output recover.

PACKAGE DESCRIPTION

UDC Package
20-Lead Plastic QFN (3mm × 4mm)
(Reference LTC DWG # 05-08-1536 Rev B)
Exposed Pad Variation AB



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE



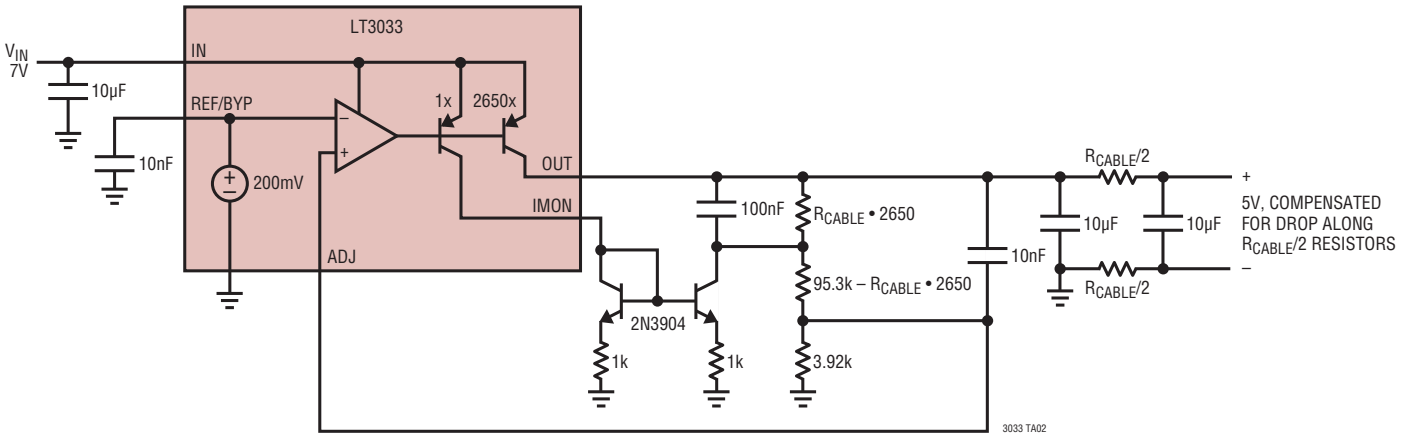
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	02/19	Edited Part Marking in the Order Information Section. Changed from 3033 to LGVQ.	2

TYPICAL APPLICATION

Cable Drop Compensation



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3020	100mA, Low Voltage VLDO Linear Regulator	V_{IN}: 0.9V to 10V, V_{OUT}: 0.2V to 9.5V, V_{DO} = 0.15V, I_Q = 120µA, Noise: < 250µV_{RMS}, Stable with 2.2µF Ceramic Capacitors, DFN-8, MS8 Packages
LT3021	500mA, Low Voltage, VLDO Linear Regulator	V_{IN}: 0.9V to 10V, Dropout Voltage: 160mV Typical, Adjustable Output (V_{REF} = $V_{OUT(MIN)}$ = 200mV), Fixed Output Voltages: 1.2V, 1.5V, 1.8V, Stable with Low ESR, Ceramic Output Capacitors, 16-Pin DFN (5mm × 5mm) and 8-Lead SO Packages
LT3022	1A, Low Voltage, VLDO Linear Regulator	V_{IN}: 0.9V to 10V, Dropout Voltage: 145mV Typical
LTC®3025	300mA Micropower VLDO Linear Regulator	V_{IN} = 0.9V to 5.5V, Dropout Voltage: 45mV, Low Noise 80µV_{RMS}, Low I_Q: 54µA, 2mm × 2mm 6-Lead DFN Package
LTC3025-1/ LTC3025-2/ LTC3025-3/ LTC3025-4	500mA Micropower VLDO Linear Regulator in 2mm × 2mm DFN	V_{IN} = 0.9V to 5.5V, Dropout Voltage: 75mV, Low Noise 80µV_{RMS}, Low I_Q: 54µA, Fixed Output: 1.2V (LTC3025-2), 1.5V (LTC3025-3), 1.8V (LTC3025-4); Adjustable Output Range: 0.4V to 3.6V (LTC3025-1), 2mm × 2mm 6-Lead DFN Package
LTC3026	1.5A, Low Input Voltage VLDO Linear Regulator	V_{IN}: 1.14V to 3.5V (Boost Enabled), 1.14V to 5.5V (with External 5V), V_{DO} = 0.1V, I_Q = 950µA, Stable with 10µF Ceramic Capacitors, 10-Lead eMSOP and DFN-10 Packages
LTC3035	300mA VLDO Linear Regulator with Charge Pump Bias Generator	V_{IN} = 1.7V to 5.5V, V_{OUT}: 0.4V to 3.6V, Dropout Voltage: 45mV, I_Q: 100µA, 3mm × 2mm DFN-8
LT3070	5A, Low Noise, Programmable V_{OUT}, 85mV Dropout Linear Regulator with Digital Margining	85mV Dropout Voltage, Digitally Programmable V_{OUT}: 0.8V to 1.8V, Digital Output Margining: ±1%, ±3% or ±5%, Low Output Noise: 25µV_{RMS}; Directly Parallelable, Stable with Low ESR Ceramic Output Capacitors (15µF Minimum), 28-Lead 4mm × 5mm QFN Package
LT3071	5A, Low Noise, Programmable V_{OUT}, 85mV Dropout Linear Regulator with Analog Margining	85mV Dropout Voltage, Digitally Programmable V_{OUT}: 0.8V to 1.8V, Analog Margining: ±10%, Low Output Noise: 25µV_{RMS}; Directly Parallelable, IMON Output Current Monitor, Stable with Low ESR Ceramic Output Capacitors (15µF Minimum), 28-Lead 4mm × 5mm QFN Package
LT1764/LT1764A	3A, Fast Transient Response, Low Noise LDO	340mV Dropout Voltage, Low Noise: 40µV_{RMS}, V_{IN} = 2.7V to 20V, TO-220V and DD Packages. A Version Stable with Ceramic Capacitors.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for LDO Voltage Regulators ***category:***

Click to view products by Analog Devices ***manufacturer:***

Other Similar products are found below :

AP7363-SP-13 L79M05TL-E TCR3DF185,LM(CT TCR3DF24,LM(CT TCR3DF285,LM(CT TCR3DF31,LM(CT TCR3DF45,LM(CT MP2013GQ-33-Z 059985X NCP4687DH15T1G 701326R TCR2EN28,LF(S NCV8170AXV250T2G TCR3DF27,LM(CT TCR3DF19,LM(CT TCR3DF125,LM(CT TCR2EN18,LF(S AP2112R5A-3.3TRG1 AP7315-25W5-7 IFX30081LDVGRNXUMA1 NCV47411PAAJR2G AP2113KTR-G1 AP2111H-1.2TRG1 ZLDO1117QK50TC AZ1117IH-1.8TRG1 AZ1117ID-ADJTRG1 TCR3DG12,LF MIC5514-3.3YMT-T5 MIC5512-1.2YMT-T5 MIC5317-2.8YM5-T5 SCD7912BTG NCP154MX180270TAG SCD33269T-5.0G NCV8170BMX330TCG NCV8170AMX120TCG NCP706ABMX300TAG NCP153MX330180TCG NCP114BMX075TCG MC33269T-3.5G CAT6243-ADJCMT5T TCR3DG33,LF AP2127N-1.0TRG1 TCR4DG35,LF LT1117CST-3.3 TAR5S15U(TE85L,F) TAR5S18U(TE85L,F) TCR3UG19A,LF TCR4DG105,LF NCV8170AMX360TCG MIC94310-NYMT-T5