20V, 500mA, Ultralow Noise, Ultrahigh PSRR Linear Regulator

FEATURES

- **Ultralow RMS Noise: 0.8μV_{RMS} (10Hz to 100kHz)**
- **Ultralow Spot Noise: 2nV/√Hz at 10kHz**
- **Ultrahigh PSRR: 76dB at 1MHz**
- **Output Current: 500mA**
- **Wide Input Voltage Range: 1.8V to 20V**
- **Single Capacitor Improves Noise and PSRR**
- **100μA SET Pin Current: ±1% Initial Accuracy**
- Single Resistor Programs Output Voltage
- High Bandwidth: 1MHz
- Programmable Current Limit
- Low Dropout Voltage: 260mV
- Output Voltage Range: 0V to 15V
- Programmable Power Good
- Fast Start-Up Capability
- Precision Enable/UVLO
- Parallelable for Lower Noise and Higher Current
- Internal Current Limit with Foldback
- Minimum Output Capacitor: 10μF Ceramic
- Reverse-Battery and Reverse-Current Protection
- 12-Lead MSOP Package

ENHANCED PRODUCT FEATURES

- Supports Defense and Aerospace Applications (AQEC Standard)
- Military Temperature Range (–55°C to 150°C)
- Controlled Manufacturing Baseline
- One Assembly/Test Site
- One Fabrication Site
- Product Change Notification
- Qualification Data Available on Request

APPLICATIONS

- RF Power Supplies: PLLs, VCOs, Mixers, LNAs, PAs
- Very Low Noise Instrumentation
- High Speed/High Precision Data Converters
- Medical Applications: Imaging, Diagnostics
- Precision Power Supplies
- Post-Regulator for Switching Supplies

DESCRIPTION

The LT®3045-EP is a high performance low dropout linear regulator featuring LTC's ultralow noise and ultrahigh PSRR architecture for powering noise sensitive applications. Designed as a precision current reference followed by a high performance voltage buffer, the LT3045-EP can be easily paralleled to further reduce noise, increase output current and spread heat on the PCB.

The device supplies 500mA at a typical 260mV dropout voltage. Operating quiescent current is nominally 2.2mA and drops to <<1μA in shutdown. The LT3045-EP's wide output voltage range (0V to 15V) while maintaining unity-gain operation provides virtually constant output noise, PSRR, bandwidth and load regulation, independent of the programmed output voltage. Additionally, the regulator features programmable current limit, fast start-up capability and programmable power good to indicate output voltage regulation.

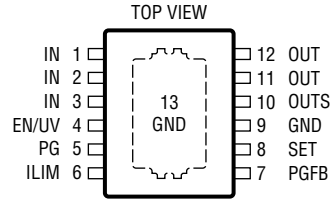
The LT3045-EP is stable with a minimum 10μF ceramic output capacitor. Built-in protection includes reverse-battery protection, reverse-current protection, internal current limit with foldback and thermal limit with hysteresis. The LT3045-EP is available in thermally enhanced 12-Lead MSOP package. Additional application and technical information can be found in LT3045 data sheet.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

IN Pin Voltage ..... ±22V
EN/UV Pin Voltage ..... ±22V
IN-to-EN/UV Differential ..... ±22V
PG Pin Voltage (Note 10) ..... –0.3V, 22V
ILIM Pin Voltage (Note 10) ..... –0.3V, 1V
PGFB Pin Voltage (Note 10) ..... –0.3V, 22V
SET Pin Voltage (Note 10) ..... –0.3V, 16V
SET Pin Current (Note 7) ..... ±20mA
OUTS Pin Voltage (Note 10) ..... –0.3V, 16V
OUTS Pin Current (Note 7) ..... ±20mA
OUT Pin Voltage (Note 10) ..... –0.3V, 16V
OUT-to-OUTS Differential (Note 14) ..... ±1.2V
IN-to-OUT Differential ..... ±22V
IN-to-OUTS Differential ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Operating Junction Temperature Range (Note 9)
H-Grade, ... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 Sec)
MSE Package ..... 300°C

PIN CONFIGURATION



MSE PACKAGE
12-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 33°C/W, θ_{JC} = 8°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3045HMSE#Z-EP	3045EP	12-Lead Plastic MSOP	–55°C to 150°C

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range		●	2		20	V
Minimum IN Pin Voltage (Note 2)	I_{LOAD} = 500mA, V_{IN} UVLO Rising V_{IN} UVLO Hysteresis	●		1.78 75	2	V mV
Output Voltage Range	$V_{IN} > V_{OUT}$	●	0		15	V
SET Pin Current (I_{SET})	V_{IN} = 2V, I_{LOAD} = 1mA, V_{OUT} = 1.3V 2V < V_{IN} < 20V, 0V < V_{OUT} < 15V, 1mA < I_{LOAD} < 500mA (Note 3)	 ●	99 98	100 100	101 102	µA µA
Fast Start-Up Set Pin Current	V_{PGFB} = 289mV, V_{IN} = 2.8V, V_{SET} = 1.3V			2		mA
Output Offset Voltage V_{OS} ($V_{OUT} – V_{SET}$) (Note 4)	V_{IN} = 2V, I_{LOAD} = 1mA, V_{OUT} = 1.3V 2V < V_{IN} < 20V, 0V < V_{OUT} < 15V, 1mA < I_{LOAD} < 500mA (Note 3)	 ●	–1 –2		1 2	mV mV
Line Regulation: ΔI_{SET} Line Regulation: ΔV_{OS}	V_{IN} = 2V to 20V, I_{LOAD} = 1mA, V_{OUT} = 1.3V V_{IN} = 2V to 20V, I_{LOAD} = 1mA, V_{OUT} = 1.3V (Note 4)	● ●		0.5 0.5	±2 ±3	nA/V µV/V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Load Regulation: ΔI_{SET}	I_{LOAD} = 1mA to 500mA, V_{IN} = 2V, V_{OUT} = 1.3V			3		nA
Load Regulation: ΔV_{OS}	I_{LOAD} = 1mA to 500mA, V_{IN} = 2V, V_{OUT} = 1.3V (Note 4)	●		0.1	0.5	mV
Change in I_{SET} with V_{SET}	V_{SET} = 1.3V to 15V, V_{IN} = 20V, I_{LOAD} = 1mA	●		30	400	nA
Change in V_{OS} with V_{SET}	V_{SET} = 1.3V to 15V, V_{IN} = 20V, I_{LOAD} = 1mA (Note 4)	●		0.03	0.6	mV
Change in I_{SET} with V_{SET}	V_{SET} = 0V to 1.3V, V_{IN} = 20V, I_{LOAD} = 1mA	●		150	600	nA
Change in V_{OS} with V_{SET}	V_{SET} = 0V to 1.3V, V_{IN} = 20V, I_{LOAD} = 1mA (Note 4)	●		0.3	2	mV
Dropout Voltage	I_{LOAD} = 1mA, 50mA			220	275	mV
		●			330	mV
	I_{LOAD} = 300mA (Note 5)			220	280	mV
		●			350	mV
	I_{LOAD} = 500mA (Note 5)			260	350	mV
		●			450	mV
GND Pin Current V_{IN} = $V_{OUT(NOMINAL)}$ (Note 6)	I_{LOAD} = 10µA			2.2		mA
	I_{LOAD} = 1mA	●		2.4	4	mA
	I_{LOAD} = 50mA	●		3.5	5.5	mA
	I_{LOAD} = 100mA	●		4.3	7	mA
	I_{LOAD} = 500mA	●		15	25	mA
Output Noise Spectral Density (Notes 4, 8)	I_{LOAD} = 500mA, Frequency = 10Hz, C_{OUT} = 10µF, C_{SET} = 0.47µF, V_{OUT} = 3.3V			500		nV/√Hz
	I_{LOAD} = 500mA, Frequency = 10Hz, C_{OUT} = 10µF, C_{SET} = 4.7µF, 1.3V ≤ V_{OUT} ≤ 15V			70		nV/√Hz
	I_{LOAD} = 500mA, Frequency = 10kHz, C_{OUT} = 10µF, C_{SET} = 0.47µF, 1.3V ≤ V_{OUT} ≤ 15V			2		nV/√Hz
	I_{LOAD} = 500mA, Frequency = 10kHz, C_{OUT} = 10µF, C_{SET} = 0.47µF, 0V ≤ V_{OUT} < 1.3V			5		nV/√Hz
Output RMS Noise (Notes 4, 8)	I_{LOAD} = 500mA, BW = 10Hz to 100kHz, C_{OUT} = 10µF, C_{SET} = 0.47µF, V_{OUT} = 3.3V			2.5		μV_{RMS}
	I_{LOAD} = 500mA, BW = 10Hz to 100kHz, C_{OUT} = 10µF, C_{SET} = 4.7µF, 1.3V ≤ V_{OUT} ≤ 15V			0.8		μV_{RMS}
	I_{LOAD} = 500mA, BW = 10Hz to 100kHz, C_{OUT} = 10µF, C_{SET} = 4.7µF, 0V ≤ V_{OUT} < 1.3V			1.8		μV_{RMS}
Reference Current RMS Output Noise (Notes 4, 8)	BW = 10Hz to 100kHz			6		nA_{RMS}
Ripple Rejection 1.3V ≤ V_{OUT} ≤ 15V V_{IN} – V_{OUT} = 2V (Avg) (Notes 4, 8)	V_{RIPPLE} = 500mV_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 500mA, C_{OUT} = 10µF, C_{SET} = 4.7µF			117		dB
	V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 10kHz, I_{LOAD} = 500mA, C_{OUT} = 10µF, C_{SET} = 0.47µF			90		dB
	V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 100kHz, I_{LOAD} = 500mA, C_{OUT} = 10µF, C_{SET} = 0.47µF			77		dB
	V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 1MHz, I_{LOAD} = 500mA, C_{OUT} = 10µF, C_{SET} = 0.47µF			76		dB
	V_{RIPPLE} = 80mV_{P-P}, f_{RIPPLE} = 10MHz, I_{LOAD} = 500mA, C_{OUT} = 10µF, C_{SET} = 0.47µF			53		dB
Ripple Rejection 0V ≤ V_{OUT} < 1.3V V_{IN} – V_{OUT} = 2V (Avg) (Notes 4, 8)	V_{RIPPLE} = 500mV_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 500mA, C_{OUT} = 10µF, C_{SET} = 0.47µF			104		dB
	V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 10kHz, I_{LOAD} = 500mA, C_{OUT} = 10µF, C_{SET} = 0.47µF			85		dB
	V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 100kHz, I_{LOAD} = 500mA, C_{OUT} = 10µF, C_{SET} = 0.47µF			72		dB
	V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 1MHz, I_{LOAD} = 500mA, C_{OUT} = 10µF, C_{SET} = 0.47µF			64		dB
	V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 10MHz, I_{LOAD} = 500mA, C_{OUT} = 10µF, C_{SET} = 0.47µF			54		dB
EN/UV Pin Threshold	EN/UV Trip Point Rising (Turn-On), V_{IN} = 2V	●	1.18	1.24	1.32	V
EN/UV Pin Hysteresis	EN/UV Trip Point Hysteresis, V_{IN} = 2V			130		mV
EN/UV Pin Current	$V_{EN/UV}$ = 0V, V_{IN} = 20V	●			±1	µA
	$V_{EN/UV}$ = 1.24V, V_{IN} = 20V			0.03		µA
	$V_{EN/UV}$ = 20V, V_{IN} = 0V	●		8	15	µA
Quiescent Current in Shutdown ($V_{EN/UV}$ = 0V)	V_{IN} = 6V			0.3	1	µA
	T_J ≤ 150°C (H-Grade)	●			20	µA
Internal Current Limit (Note 12)	V_{IN} = 2V, V_{OUT} = 0V	●	570	710	850	mA
	V_{IN} = 12V, V_{OUT} = 0V			700		mA
	V_{IN} = 20V, V_{OUT} = 0V	●	230	330	430	mA
Programmable Current Limit	Programming Scale Factor: 2V < V_{IN} < 20V (Note 11)			150		mA • kΩ
	V_{IN} = 2V, V_{OUT} = 0V, R_{ILIM} = 300Ω	●	450	500	550	mA
	V_{IN} = 2V, V_{OUT} = 0V, R_{ILIM} = 1.5kΩ	●	90	100	110	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PGFB Trip Point	PGFB Trip Point Rising	●	291	300	309	mV
PGFB Hysteresis	PGFB Trip Point Hysteresis			7		mV
PGFB Pin Current	V_{IN} = 2V, V_{PGFB} = 300mV (Current Flows Out of Pin)			25		nA
PG Output Low Voltage	I_{PG} = 100µA	●		30	100	mV
PG Leakage Current	V_{PG} = 20V	●			1	µA
Reverse Input Current	V_{IN} = –20V, $V_{EN/UV}$ = 0V, V_{OUT} = 0V, V_{SET} = 0V	●			100	µA
Reverse Output Current	V_{IN} = 0, V_{OUT} = 5V, SET = Open			14	25	µA
Minimum Load Required (Note 13)	V_{OUT} < 1V	●	10			µA
Thermal Shutdown	T_J Rising Hysteresis			165 8		°C °C
Start-Up Time	$V_{OUT(NOM)}$ = 5V, I_{LOAD} = 500mA, C_{SET} = 0.47µF, V_{IN} = 6V, V_{PGFB} = 6V $V_{OUT(NOM)}$ = 5V, I_{LOAD} = 500mA, C_{SET} = 4.7µF, V_{IN} = 6V, V_{PGFB} = 6V $V_{OUT(NOM)}$ = 5V, I_{LOAD} = 500mA, C_{SET} = 4.7µF, V_{IN} = 6V, R_{PG1} = 50kΩ, R_{PG2} = 700kΩ (with Fast Start-Up to 90% of V_{OUT})			55 550 10		ms ms ms
Thermal Regulation	10ms Pulse			–0.01		%/W

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The EN/UV pin threshold must be met to ensure device operation.

Note 3: Maximum junction temperature limits operating conditions. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current, especially due to the internal current limit foldback which starts to decrease current limit at $V_{IN} – V_{OUT}$ > 12V. If operating at maximum output current, limit the input voltage range. If operating at the maximum input voltage, limit the output current range.

Note 4: OUTS ties directly to OUT.

Note 5: Dropout voltage is the minimum input-to-output differential voltage needed to maintain regulation at a specified output current. The dropout voltage is measured when output is 1% out of regulation. This definition results in a higher dropout voltage compared to hard dropout — which is measured when $V_{IN} = V_{OUT(NOMINAL)}$. For lower output voltages, below 1.5V, dropout voltage is limited by the minimum input voltage specification. Please consult the LT3045 Typical Performance Characteristics for curves of dropout voltage as a function of output load current and temperature measured in a typical application circuit.

Note 6: GND pin current is tested with $V_{IN} = V_{OUT(NOMINAL)}$ and a current source load. Therefore, the device is tested while operating in dropout. This is the worst-case GND pin current. GND pin current decreases at higher input voltages. Note that GND pin current does not include SET pin or ILIM pin current but Quiescent current does include them.

Note 7: SET and OUTS pins are clamped using diodes and two 25Ω series resistors. For less than 5ms transients, this clamp circuitry can carry more than the rated current. Refer to LT3045 Applications Information for more information.

Note 8: Adding a capacitor across the SET pin resistor decreases output voltage noise. Adding this capacitor bypasses the SET pin resistor's thermal noise as well as the reference current's noise. The output noise then equals the error amplifier noise. Use of a SET pin bypass capacitor also increases start-up time.

Note 9: The LT3045-EP is tested and specified under pulsed load conditions such that $T_J \approx T_A$. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 10: Parasitic diodes exist internally between the ILIM, PG, PGFB, SET, OUTS, and OUT pins and the GND pin. Do not drive these pins more than 0.3V below the GND pin during a fault condition. These pins must remain at a voltage more positive than GND during normal operation.

Note 11: The current limit programming scale factor is specified while the internal backup current limit is not active. Note that the internal current limit has foldback protection for $V_{IN} – V_{OUT}$ differentials greater than 12V.

Note 12: The internal back-up current limit circuitry incorporates foldback protection that decreases current limit for $V_{IN} – V_{OUT}$ > 12V. Some level of output current is provided at all $V_{IN} – V_{OUT}$ differential voltages. Consult the LT3045 Typical Performance Characteristics graph for current limit vs $V_{IN} – V_{OUT}$.

Note 13: For output voltages less than 1V, the LT3045-EP requires a 10µA minimum load current for stability.

Note 14: Maximum OUT-to-OUTS differential is guaranteed by design.

PIN FUNCTIONS

IN (Pins 1, 2, 3): Input. These pins supply power to the regulator. The LT3045-EP requires a bypass capacitor at the IN pin. In general, a battery's output impedance rises with frequency, so include a bypass capacitor in battery-powered applications. While a 4.7µF input bypass capacitor generally suffices, applications with large load transients may require higher input capacitance to prevent input supply droop. Consult the LT3045 Applications Information section on the proper use of an input capacitor and its effect on circuit performance, in particular PSRR. The LT3045-EP withstands reverse voltages on IN with respect to GND, OUTS and OUT. In the case of a reversed input, which occurs if a battery is plugged-in backwards, the LT3045-EP acts as if a diode is in series with its input. Hence, no reverse current flows into the LT3045-EP and no negative voltage appears at the load. The device protects itself and the load.

EN/UV (Pin 4): Enable/UVLO. Pulling the LT3045-EP's EN/UV pin low places the part in shutdown. Quiescent current in shutdown drops to less than 1µA and the output voltage turns off. Alternatively, the EN/UV pin can set an input supply undervoltage lockout (UVLO) threshold using a resistor divider between IN, EN/UV and GND. The LT3045-EP typically turns on when the EN/UV voltage exceeds 1.24V on its rising edge, with a 130mV hysteresis on its falling edge. The EN/UV pin can be driven above the input voltage and maintain proper functionality. If unused, tie EN/UV to IN. Do not float the EN/UV pin.

PG (Pin 5): Power Good. PG is an open-collector flag that indicates output voltage regulation. PG pulls low if PGFB is below 300mV. If the power good functionality is not needed, float the PG pin. A parasitic substrate diode exists between PG and GND pins of the LT3045-EP; do not drive PG more than 0.3V below GND during normal operation or during a fault condition.

ILIM (Pin 6): Current Limit Programming Pin. Connecting a resistor between ILIM and GND programs the current limit. For best accuracy, Kelvin connect this resistor directly to the LT3045-EP's GND pin. The programming scale factor is nominally 150mA•kΩ. The ILIM pin sources current proportional (1:500) to output current; therefore, it also serves as a current monitoring pin with a 0V to 300mV range. If the programmable current limit functionality is not needed, tie ILIM to GND. A parasitic substrate diode exists between ILIM and GND pins of the LT3045-EP; do not drive ILIM more than 0.3V below GND during normal operation or during a fault condition.

PGFB (Pin 7): Power Good Feedback. The PG pin pulls high if PGFB increases beyond 300mV on its rising edge, with 7mV hysteresis on its falling edge. Connecting an external resistor divider between OUT, PGFB and GND sets the programmable power good threshold with the following transfer function: $0.3V \bullet (1 + R_{PG2}/R_{PG1})$. As discussed in the LT3045 Applications Information section, PGFB also activates the fast start-up circuitry. Tie PGFB to IN if power good and fast start-up functionalities are not needed, and if reverse input protection is additionally required, tie the anode of a 1N4148 diode to IN and its cathode to PGFB. See the LT3045 Typical Applications section for details. A parasitic substrate diode exists between PGFB and GND pins of the LT3045-EP; do not drive PGFB more than 0.3V below GND during normal operation or during a fault condition.

SET (Pin 8): SET. This pin is the inverting input of the error amplifier and the regulation set-point for the LT3045-EP. SET sources a precision 100µA current that flows through an external resistor connected between SET and GND. The LT3045-EP's output voltage is determined by $V_{SET} = I_{SET} \bullet R_{SET}$. Output voltage range is from zero to 15V. Adding a capacitor from SET to GND improves noise,

PIN FUNCTIONS

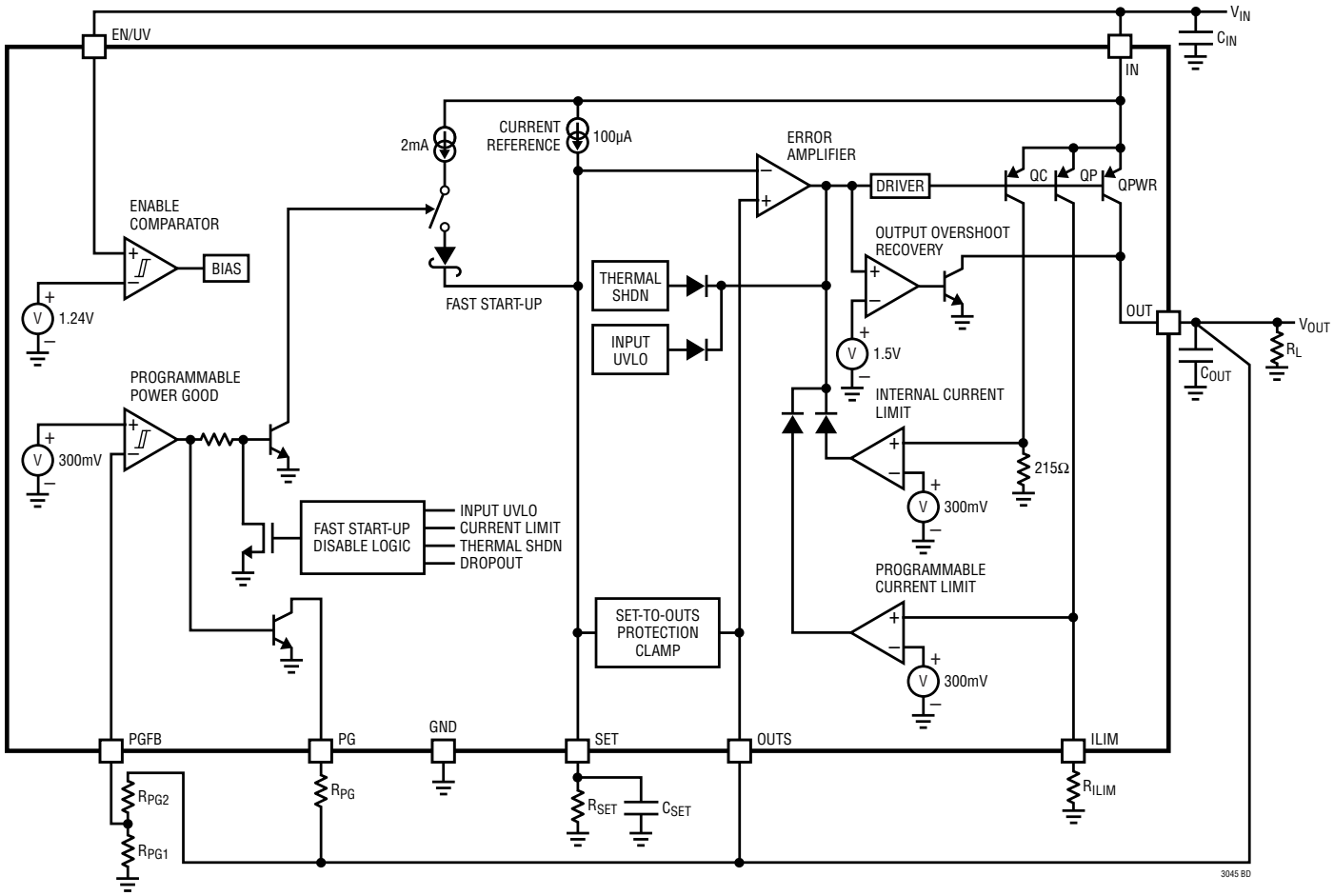
PSRR and transient response at the expense of increased start-up time. For optimum load regulation, Kelvin connect the ground side of the SET pin resistor directly to the load. A parasitic substrate diode exists between SET and GND pins of the LT3045-EP; do not drive SET more than 0.3V below GND during normal operation or during a fault condition.

GND (Pin 9, Exposed Pad Pin 13): Ground. The exposed backside is an electrical connection to GND. To ensure proper electrical and thermal performance, solder the exposed backside to the PCB ground and tie it directly to the GND pin.

OUTS (Pin 10): Output Sense. This pin is the noninverting input to the error amplifier. For optimal transient performance and load regulation, Kelvin connect OUTS directly to the output capacitor and the load. Also, tie the GND connections of the output capacitor and the SET pin capacitor directly together. A parasitic substrate diode exists between OUTS and GND pins of the LT3045-EP; do not drive OUTS more than 0.3V below GND during normal operation or during a fault condition.

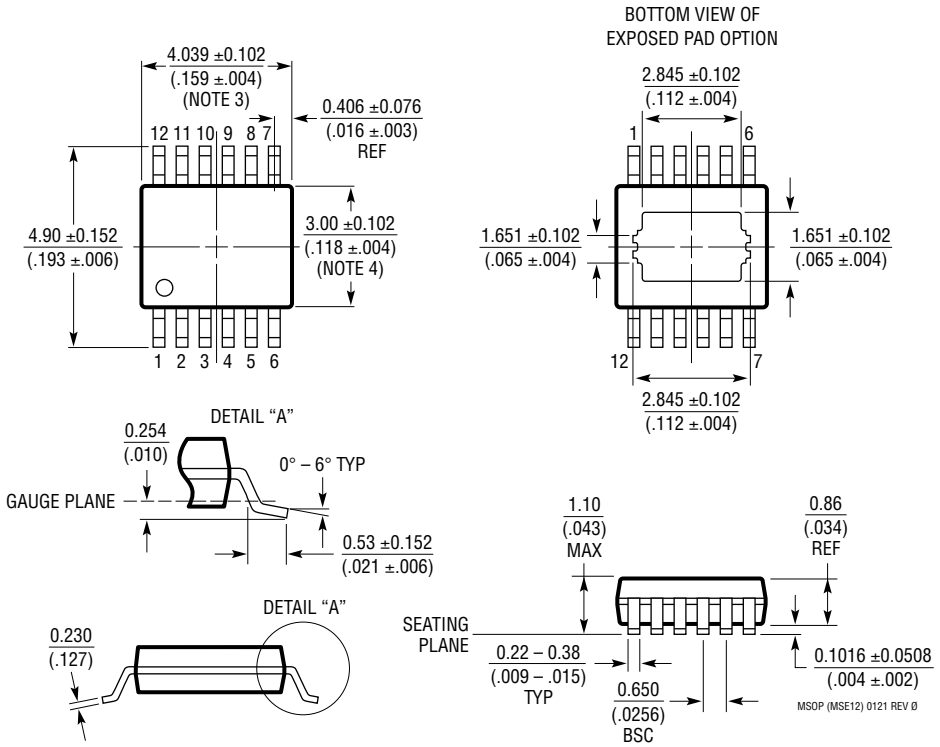
OUT (Pins 11, 12): Output. This pin supplies power to the load. For stability, use a minimum 10µF output capacitor with an ESR below 20mΩ and an ESL below 2nH. Large load transients require larger output capacitance to limit peak voltage transients. Refer to the LT3045 Applications Information section for more information on output capacitance. A parasitic substrate diode exists between OUT and GND pins of the LT3045-EP; do not drive OUT more than 0.3V below GND during normal operation or during a fault condition.

BLOCK DIAGRAM

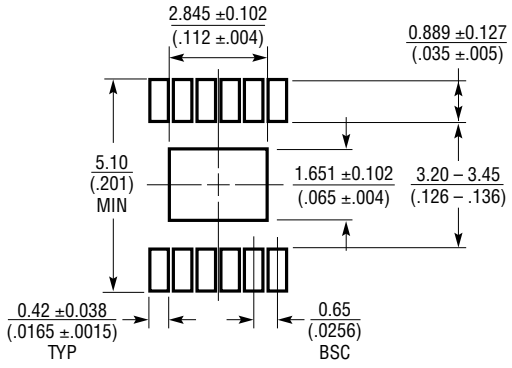


PACKAGE DESCRIPTION

MSE Package
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-7085 Rev Ø)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL NOT EXCEED 0.254mm (.010") PER SIDE.



RECOMMENDED SOLDER PAD LAYOUT

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