ANALOG DEVICES | ADI Power by Linear™

LT3086-EP

40V, 2.1A Low Dropout Adjustable Linear Regulator with Monitoring and Cable Drop Compensation

FEATURES

- **Wide Input Voltage Range: 1.4V to 40V**
- **1 Resistor Sets Output Voltage: 0.4V to 32V**
- **Output Current: 2.1A**
- **±1% Tolerance Over Line, Load and Temperature**
- **Output Current Monitor: $I_{MON} = I_{OUT}/1000$**
- **Temperature Monitor with Programmable Thermal Limit**
- **Programmable Cable Drop Compensation**
- **Parallel Multiple Devices for Higher Current**
- **Dropout Voltage: 330mV**
- 1 Capacitor Soft-Starts Output and Decreases Noise
- Low Output Noise: $40\mu V_{RMS}$ (10Hz to 100kHz)
- Precision, Programmable External Current Limit
- Power Good Flag with Programmable Threshold
- Ceramic Output Capacitors: 10µF Minimum
- Quiescent Current in Shutdown: <1µA
- Reverse-Battery, -Current and -Output Protection
- Available in 16-Lead TSSOP

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range (–55°C to 125°C)
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Product change notification
- Qualification data available on request

DESCRIPTION

The LT®3086-EP is a multi-feature, low dropout, low noise 2.1A linear regulator that operates over a 1.4V to 40V input supply range. Dropout voltage at 2.1A is typically 330mV. One resistor sets output voltage from 0.4V to 32V. Output voltage tolerance is guaranteed to ±1% over line, load and temperature. The LT3086-EP is stable with ceramic output capacitors, requiring a minimum of 10µF.

The LT3086-EP's programmable cable drop compensation cancels output voltage errors caused by resistive connections to the load. A master/slave configuration allows paralleling of multiple devices for higher load current and heat spreading without external ballast resistor requirements.

Output current and temperature monitoring along with a power good flag provide system diagnostic and debug capability. Internal fault circuitry includes thermal shutdown and current limit with foldback. Thermal limit and current limit are also externally programmable.

The LT3086-EP is available in the thermally enhanced 16-Lead TSSOP package. Additional application and technical information can be found in the LT3086 data sheet.

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APPLICATIONS

- Programmable Linear Regulator
- Post Regulator for Switching Supplies
- USB Power Supplies
- High Reliability Power Supplies

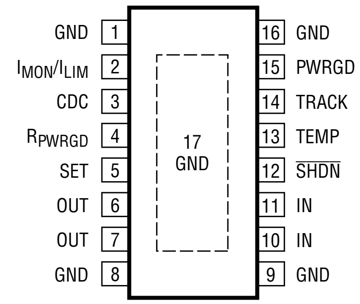
ABSOLUTE MAXIMUM RATINGS

(Note 1)

IN Pin Voltage ....±45V
OUT Pin Voltage..±36V
Input-to-Output Differential Voltage (Note 2) ....±45V
SET Pin Voltage ....–0.3, 36V
$\overline{\text{SHDN}}$ Pin Voltage ....±45V
CDC Pin (Internally Clamped, Current into Pin).......<8mA
I_{MON} Pin Voltage ....–0.3, 7V
I_{LIM} Pin Voltage...–0.3, 2V
TRACK Pin Voltage .... –0.3, Internally Clamped at 1.25V
TEMP Pin Voltage 0V, 5V
PWRGD Pin Voltage..–0.3, 36V
R_{PWRGD} Pin Voltage..–0.3, 36V
Output Short-Circuit Duration .... Indefinite
Operating Junction Temperature (Notes 3, 5, 12)
EP-Grade .... –55°C to 125°C
Storage Temperature Range ....–65 to 150°C
Lead Temperature (Soldering, 10 sec)
(TSSOP) ....300°C

PIN CONFIGURATION

TOP VIEW



FE PACKAGE
16-LEAD PLASTIC TSSOP
T_{JMAX} = 150°C, θ_{JA} = 25°C/W TO 33°C/W*, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3086FE#Z-EP	3086FE-EP	16-Lead Plastic TSSOP	–55°C to 125°C
LT3086FE#TRZ-EP	3086FE-EP	16-Lead Plastic TSSOP	–55°C to 125°C

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$.

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
Minimum Input Voltage (Note 4)		$I_{LOAD} = 2.1A$, $\Delta V_{OUT} = –1\%$		●		1.4	1.55	V
Reference Voltage (Notes 3, 5)	V_{SET}	$1.55V < V_{IN} < 40V$, $1mA < I_{LOAD} < 2.1A$	$(T_J < 125°C)$	●	396	400	404	mV
Reference Current	I_{SET}	$1.55V < V_{IN} < 40V$, $1mA < I_{LOAD} < 2.1A$		●	49.5	50	50.5	µA
Line Regulation	V_{SET} I_{SET}	$V_{IN} = 1.55V$ to $40V$, $I_{LOAD} = 1mA$ $V_{IN} = 1.55V$ to $40V$, $I_{LOAD} = 1mA$	$(T_J < 125°C)$	● ●	 –0.12	0.1 –0.03	0.8	mV µA
Load Regulation (Notes 6, 7)	V_{SET} I_{SET}	$I_{LOAD} = 1mA$ to $2.1A$, $V_{IN} = V_{OUT} + 0.55V$ $I_{LOAD} = 1mA$ to $2.1A$, $V_{IN} = V_{OUT} + 0.55V$	$(T_J < 125°C)$ $(T_J < 125°C)$	● ●		0.25 0.02	1 0.08	mV µA
Minimum Load Current (Note 16)				●			1	mA
Dropout Voltage $V_{IN} = V_{OUT(NOMINAL)}$, (Notes 7, 8)		$I_{LOAD} = 1mA$		 ●		10	65 100	mV mV
		$I_{LOAD} = 100mA$		 ●		100	135 160	mV mV
		$I_{LOAD} = 500mA$		 ●		150	195 235	mV mV
		$I_{LOAD} = 1.5A$		 ●		260	335 425	mV mV
		$I_{LOAD} = 2.1A$		 ●		330	415 540	mV mV
GND Pin Current $V_{IN} = V_{OUT(NOMINAL)} + 0.55V$, (Notes 7, 9)		$I_{LOAD} = 0µA$ $I_{LOAD} = 1mA$ $I_{LOAD} = 100mA$ $I_{LOAD} = 500mA$ $I_{LOAD} = 1.5A$ $I_{LOAD} = 2.1A$		● ● ● ● ● ●		1.2 1.3 1.8 4.5 23 44	2.4 2.6 3.6 9 46 88	mA mA mA mA mA mA
Quiescent Current in Shutdown		$V_{IN} = 40V$, $V_{\overline{SHDN}} = 0V$				0.1	1	µA
Output Voltage Noise		$C_{SET} = 0.01µF$, $C_{OUT} = 10µF$, $I_{LOAD} = 2.1A$ $V_{OUT} = 5V$, BW = 10Hz to 100kHz				40		$µV_{RMS}$
Shutdown Threshold		V_{OUT} = Off to On V_{OUT} = On to Off		● ●	1.12 0.85	1.22 1.03	1.32	V V
$\overline{SHDN}$ Pin Current (Note 10) $1.55V < V_{IN} < 40V$		$V_{\overline{SHDN}} = 0V$ $V_{\overline{SHDN}} = 40V$		● ●		 15	1 35	µA µA
TEMP Voltage (Note 13)		$T_J = 25°C$ $T_J = 125°C$				0.25 1.25		V V
TEMP Error (Note 13)		$0°C < T_J < 125°C$, $I_{TEMP} = 0$ $0°C < T_J < 125°C$, $I_{TEMP} = 0µA$ to $80µA$			–0.09 –0.1		0.09	V V
I_{TEMP} Thermal Limit Current Threshold		$25°C < T_J < 125°C$			95	100	105	µA
I_{MON} Output Current $V_{IN} = V_{OUT(NOMINAL)} + 0.55V$ (Note 15)		$I_{LOAD} = 20mA$, $R_{MON} = 1k\Omega$ $I_{LOAD} = 500mA$, $R_{MON} = 330\Omega$ $I_{LOAD} = 1A$, $R_{MON} = 330\Omega$ $I_{LOAD} = 1.5A$, $R_{MON} = 330\Omega$ $I_{LOAD} = 2.1A$, $R_{MON} = 330\Omega$		● ● ● ● ●	5 440 0.95 1.43 2.02	20 500 1.00 1.50 2.10	75 560 1.05 1.57 2.18	µA µA mA mA mA
Output Current Sharing Error (Note 14)		$R_{MON} = 330\Omega$, $I_{OUT(MASTER)} = 2.1A$			–10	0	10	%
TRACK Pin Pull-Up Current		$V_{TRACK} = 750mV$		●	7	15	25	µA
R_{PWRGD} Reference Voltage		$1.55V < V_{IN} < 40V$		●	390	400	410	mV
R_{PWRGD} Reference Current		$1.55V < V_{IN} < 40V$		●	48.75	50	51.25	µA
R_{PWRGD} Reference Voltage Hysteresis		$1.55V < V_{IN} < 40V$				2.4		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
R_{PWRGD} Reference Current Hysteresis	1.55V < V_{IN} < 40V			300		nA
PWRGD V_{OL}	I_{PWRGD} = 200µA (Fault Condition)	●		55	200	mV
PWRGD Internal Time Delay	V_{OL} TO V_{OH} (Rising Edge)	●	8	17	25	µs
PWRGD Pin Leakage Current	V_{PWGRD} = 32V, V_{RPWGRD} = 500mV	●			1	µA
CDC Reference Voltage	1.55V < V_{IN} < 40V, I_{MON} = 0V	●	390	400	410	mV
CDC/V_{IMON} Voltage Gain	1.55V < V_{IN} < 40V, 0 < I_{CDC} < 20µA, V_{IMON} = 800mV to 0	●	0.320	0.333	0.343	V/V
Ripple Rejection	V_{IN} = 1.9V (AVG), V_{RIPPLE} = 0.5V_{P-P}, V_{OUT} = 1V f_{RIPPLE} = 120Hz, I_{LOAD} = 2.1A		65	80		dB
Internal Current Limit	V_{IN} = 1.55V V_{IN} = $V_{OUT(NOMINAL)}$ + 0.55V (Notes 7, 12), ΔV_{OUT} = –5%	● ●	2.2 2.2	2.4	2.9	A A
I_{LIM} Threshold Voltage	1.55V < V_{IN} < 40V	●	775	800	825	mV
Input Reverse-Leakage Current	V_{IN} = –40V, V_{OUT} = 0	●			2	mA
Reverse-Output Current (Note 11)	V_{OUT} = 32V, V_{IN} = 0, $V_{\overline{SHDN}}$ = 0			1	10	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Absolute maximum input-to-output differential voltage is not achievable with all combinations of rated IN pin and OUT pin voltages. With the IN pin at 45V, the OUT pin may not be pulled below 0V. The total IN to OUT differential voltage must not exceed ±45V.

Note 3: The LT3086-EP is tested and specified under pulse load conditions such that $T_J \cong T_A$. The LT3086-EP is 100% tested over the –55°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 4: The LT3086-EP is tested and specified for these conditions with the SET pin connected to the OUT pin, V_{OUT} = 0.4V.

Note 5: Maximum junction temperature limits operating conditions. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. Limit the output current range if operating at large input-to-output voltage differentials. Limit the input-to-output voltage differential if operating at maximum output current. Current limit foldback limits the maximum output current as a function of input-to-output voltage. See Current Limit vs V_{IN} – V_{OUT} in the Typical Performance Characteristics section.

Note 6: Load regulation is Kelvin-sensed at the package.

Note 7: To satisfy minimum input voltage requirements, the LT3086-EP is tested and specified for these conditions with a 32k resistor between OUT and SET for a 2V output voltage.

Note 8: Dropout voltage is the minimum input-to-output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage equals: (V_{IN} – $V_{DROPOUT}$). For low output voltages and certain load conditions, minimum input voltage requirements limit dropout voltage. See the Minimum Input Voltage curve in the Typical Performance Characteristics section.

Note 9: GND pin current is tested with V_{IN} = $V_{OUT(NOMINAL)}$ + 0.55V and PWRGD pin floating. GND pin current increases in dropout. See GND pin current curves in the Typical Performance Characteristics section and the LT3086 data sheet.

Note 10: $\overline{SHDN}$ pin current flows into the $\overline{SHDN}$ pin.

Note 11: Reverse-output current is tested with the IN pin grounded and the OUT pin forced to a voltage. The current flows into the OUT pin and out of the GND pin.

Note 12: The IC includes overtemperature protection circuitry that protects the device during momentary overload conditions. Junction temperature exceeds 125°C when the overtemperature circuitry is active unless thermal limit is externally set by loading the TEMP pin. Continuous operation above the specified maximum junction temperature may impair device reliability.

Note 13: The TEMP output voltage represents the average die temperature next to the power transistor while the center of the transistor can be significantly hotter during high power conditions. Due to power dissipation and temperature gradients across the die, the TEMP output voltage measurement does not guarantee that absolute maximum junction temperature is not exceeded.

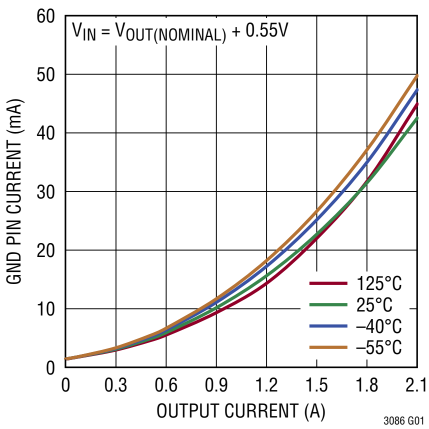
Note 14: Output current sharing error is the difference in output currents of a slave relative to its master when two LT3086-EP regulators are paralleled. The device is tested as a slave with V_{TRACK} = 0.693V, R_{MON} = 330Ω and V_{SET} = 0.4V, conditions when an ideal master is outputting 2.1A. The specification limits account for the slave output tracking error from 2.1A and the worst-case error that can be contributed by a master: the maximum deviation of V_{SET} from 0.4V and I_{MON} from 2.1mA.

Note 15: The LT3086-EP is tested and specified for these conditions with the I_{MON} and I_{LIM} pins tied together.

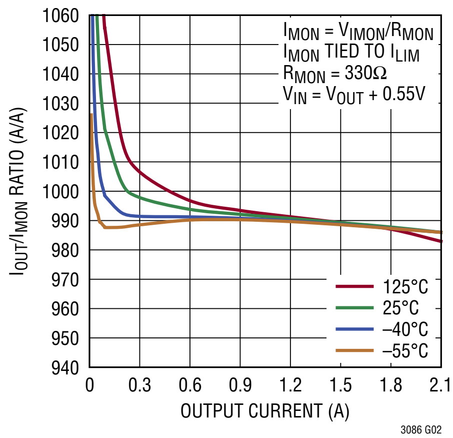
Note 16: The LT3086-EP requires a minimum load current to ensure proper regulation and stability.

TYPICAL PERFORMANCE CHARACTERISTICS

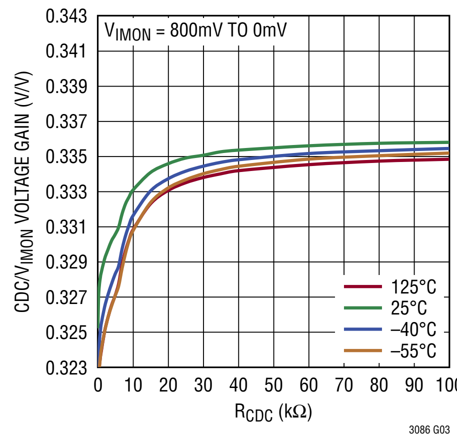
GND Pin Current vs I_{LOAD}



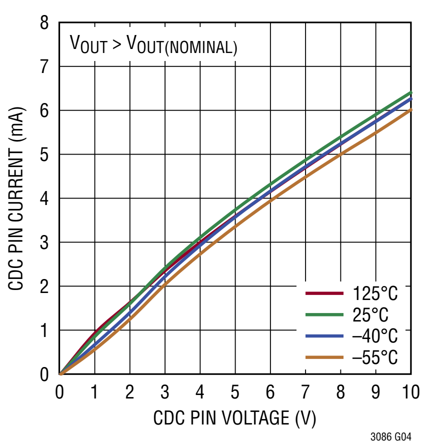
I_{OUT}/I_{MON} Ratio



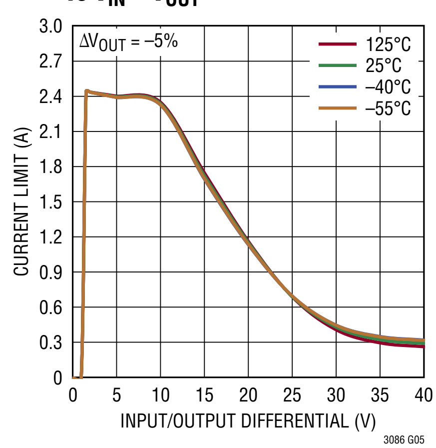
CDC Amplifier Gain



CDC Pin Internal Clamp Fault Current



Internal Current Limit vs $V_{IN} – V_{OUT}$



PIN FUNCTIONS (TSSOP)

GND (Pins 1, 8, 9, 16, Exposed Pad Pin 17): Ground. The exposed pad of the TSSOP package is an electrical connection to GND. To ensure proper electrical and thermal performance, tie the exposed pad or tab directly to the remaining GND pins of the relevant package and the PCB ground. GND pin current is typically 1.2mA at zero load and increases to about 44mA at full load.

I_{LIM} (Pin 2): External Current Limit Programming. This pin externally programs current limit if connected to I_{MON} and a resistor to GND. Current limit activates if the voltage at I_{LIM} equals 0.8V. Current limit equals: 1000 • (0.8V/R_{MON}). An internal clamp typically limits the I_{LIM} voltage to 1V. *If external current limit is set to less than 1A, connect a series 1k-10nF network in parallel with the R_{MON} resistor for stability.* Internal current limit foldback overrides externally programmed current limit if $V_{IN}-V_{OUT}$ differential voltage is excessive. If external current limit programming is not used, then ground this pin.

I_{MON} (Pin 2): Output Current Monitor. This pin sources a current equal to 1/1000 of output load current. Connecting a resistor from I_{MON} to GND programs a load current dependent voltage for monitoring by an ADC. If I_{MON} connects to I_{LIM}, current limit is externally programmable.

CDC (Pin 3): Cable Drop Compensation. Connecting a single resistor (R_{CDC}) between the CDC and SET pins provides programmable cable drop compensation that cancels output voltage errors caused by resistive connections to the load. A resistor (R_{MON}) from I_{MON} to GND is also required to enable Cable Drop Compensation. Choose R_{MON} first based on required current limit.

$$R_{MON} = 0.8V \bullet 1000/I_{LIM}$$

Calculate the value of R_{CDC} with this formula:

$$R_{CDC} = (R_{MON} \bullet R_{SET})/(3000 \bullet R_{WIRE})$$

where R_{WIRE} is the total cable or wire resistance to and from the load. From a practical application standpoint, LTC recommends limiting cable drop compensation to 20% of V_{OUT} for applications needing good regulation. The limiting factor is variations in wire temperature as copper wire resistance changes about 19% for a 50°C temperature change. If output regulation requirements are loose (e.g., when using a secondary regulator), cable drop compensation of up to 50% may be used.

R_{PWRGD} (Pin 4): Power Good Threshold Voltage Programming. This pin is the input to the power good comparator. Connecting a resistor between OUT and R_{PWRGD} programs an adjustable power good threshold voltage. The threshold voltage is 0.4V on the R_{PWRGD} pin, and a 50µA current source is connected from R_{PWRGD} to GND. If the voltage at R_{PWRGD} is less than 0.4V, the PWRGD flag asserts and pulls low. If the voltage at R_{PWRGD} is greater than 0.4V, the PWRGD flag de-asserts and becomes high impedance. For most applications, PWRGD is pulled high with a pull-up resistor. Calculate the value of R_{PWRGD} with this formula:

$$R_{PWRGD} = (X \bullet V_{OUT(NOMINAL)} - 0.4V)/50\mu A$$

where X is normally in the 85% to 95% range.

A 17µs deglitching filter suppresses false tripping of the PWRGD flag at the rising edge of PWRGD with instant reset. Hysteresis at the R_{PWRGD} pin is typically 0.6% on the 0.4V threshold and the 50µA current source.

SET (Pin 5): Output Voltage Programming. This pin is the error amplifier's inverting terminal. It regulates to 0.4V and a 50µA current source is connected from SET to GND. Connecting a single resistor from OUT to SET programs output voltage. Calculate the value of the required resistor from the formula:

$$R_{SET} = (V_{OUT} - 0.4V)/50\mu A$$

Connecting a capacitor in parallel with R_{SET} provides output voltage soft-start capability, improves transient response and decreases output voltage noise.

The LT3086-EP error amplifier design is configured so that the regulator always operates in unity-gain.

OUT (Pins 6, 7): Output. These pin(s) supply power to the load. Connect all OUT pins together on the DHD and FE packages for proper operation. Stability requirements demand a minimum 10µF ceramic output capacitor with an ESR less than 100mΩ to prevent oscillations. Large load transients require larger output capacitance to limit peak voltage transients. Permissible output voltage range is 0.4V to 32V. ***The LT3086-EP requires a 1mA minimum load current to ensure proper regulation and stability.***

PIN FUNCTIONS (TSSOP)

IN (Pins 10, 11): Input. These pin(s) supply power to the device. Connect all IN pins together for proper operation. The LT3086-EP requires a local IN bypass capacitor if it is located more than a few inches from the main input filter capacitor. In general, battery output impedance rises with frequency, so adding a bypass capacitor in battery powered circuits is advisable. A 10µF minimum input capacitor generally suffices. The IN pin(s) withstand a reverse voltage of 45V. The device limits current flow and no negative voltage appears at OUT. The device protects itself and the load against batteries that are plugged in backwards.

$\overline{\text{SHDN}}$ (Pin 12): Shutdown/UVLO. Pulling the $\overline{\text{SHDN}}$ pin typically below 1V puts the LT3086-EP into a low power state and turns the output off. Quiescent current in shutdown is typically less than 1µA. The $\overline{\text{SHDN}}$ pin turn-on threshold is typically 1.22V. This pin may either be used as a shutdown function or as an undervoltage lockout function. If using this pin as an undervoltage lockout function, use a resistor divider between IN and GND with the tap point tied to $\overline{\text{SHDN}}$. If using the pin as a shutdown function, drive the pin with either logic or an open-collector/drain with a pull-up resistor. The resistor supplies the pull-up current to the open-collector/drain logic, normally several microamperes, and the $\overline{\text{SHDN}}$ pin current, typically less than 10µA at 6V. If unused, connect the $\overline{\text{SHDN}}$ pin to IN.

TEMP (Pin 13): Die Junction Temperature. This pin outputs a voltage indicating the LT3086-EP average die junction temperature. At 25°C, this pin typically outputs 250mV. The TEMP pin slope equals 10mV/°C so that at 125°C, this pin typically outputs 1.25V. This pin does not read temperatures less than 0°C. The TEMP pin is not meant to be an accurate temperature sensor, but is useful for debug, monitoring and calculating thermal resistance of the package mounted to the PCB. The TEMP pin also incorporates the ability to program a thermal limit temperature lower than the internal typical thermal shutdown temperature of 165°C. Tying a resistor from TEMP to GND programs the thermal limit temperature with a 100µA trip point. Calculate the value of the resistor from the formula:

$$R_{TEMP} = \frac{\left(T_{SHDN} \bullet \frac{10mV}{°C}\right)}{100µA}$$

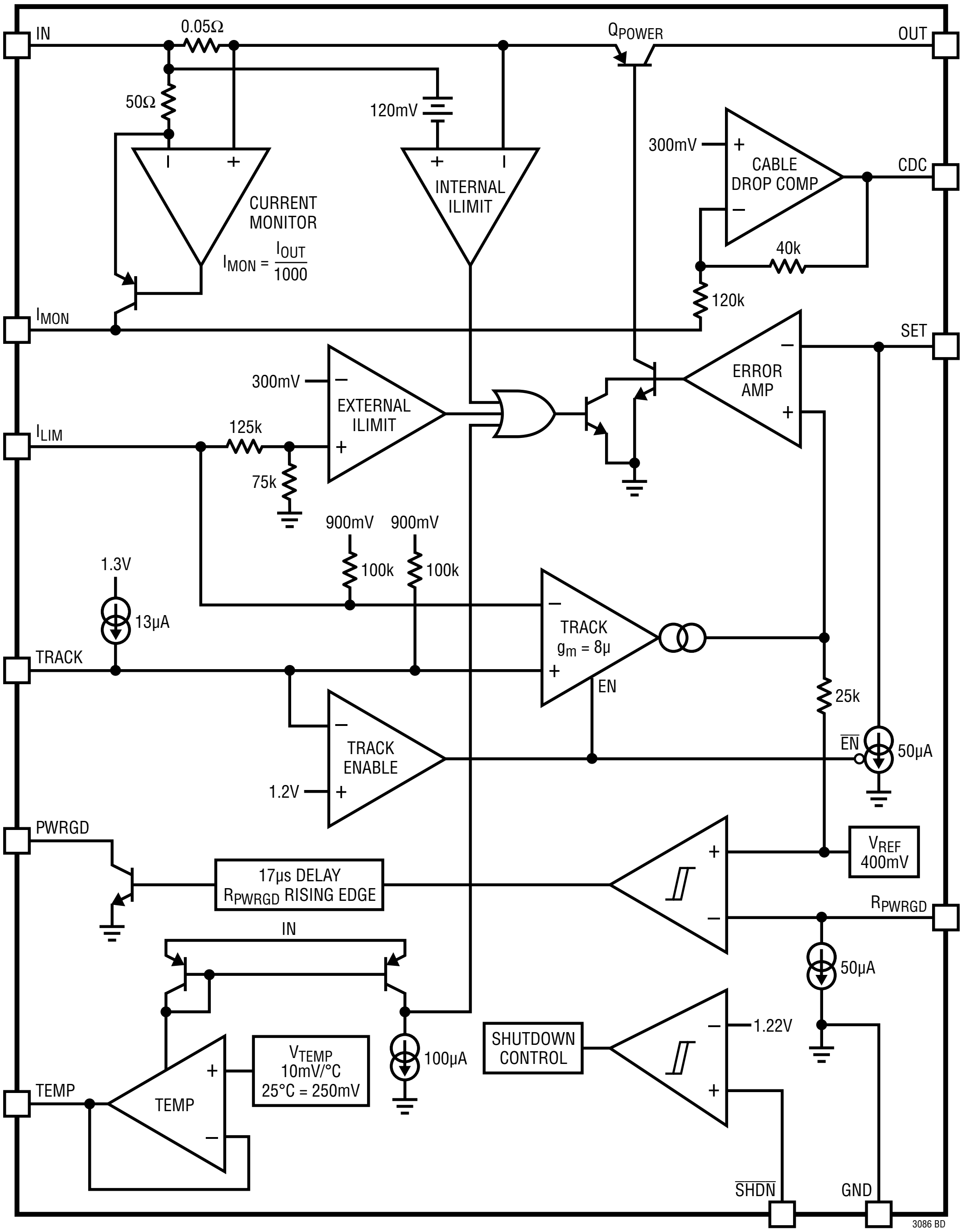
where T_{SHDN} is the desired die thermal limit temperature.

There are several degrees of hysteresis in the thermal shutdown that cycles the regulator output on and off. Limit the capacitance on the TEMP pin to less than 100pF. To prevent saturation in the TEMP output device, ensure that V_{IN} is higher than V_{TEMP} by 250mV.

TRACK (Pin 14): Track pin for paralleling. The TRACK pin allows multiple LT3086-EPs to be paralleled in a master/slave(s) configuration for higher output current applications. This also allows heat to be spread out on the PCB. This circuit technique does not require ballast resistors and does not degrade load regulation. Tying the TRACK pin of the slave device(s) to the I_{MON}/I_{LIM} pins of the master device enables this function. If the TRACK function is unused, TRACK is in a default clamped high state. A TRACK pin voltage below 1.2V on slave device (s) shuts off the internal 50µA reference current at SET such that only the 50µA reference current of the master device is active. All SET pins must be tied together in a master/slave configuration.

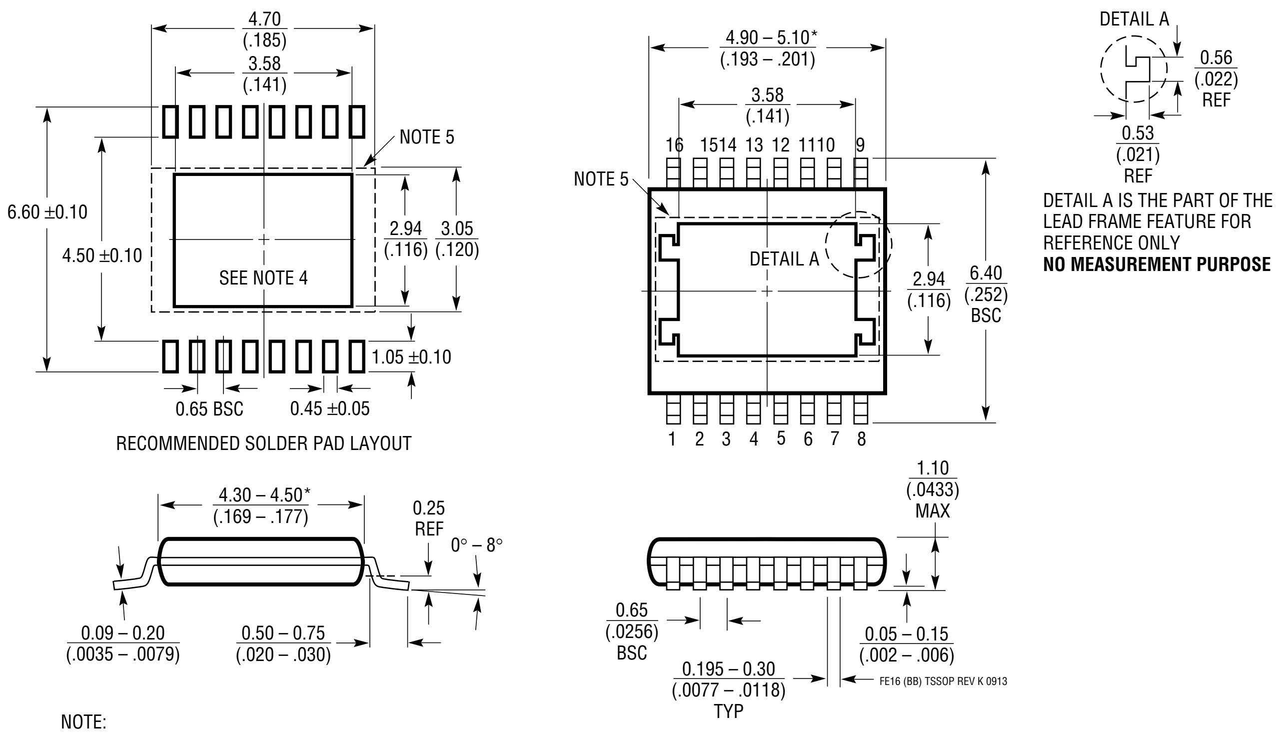
PWRGD (Pin 15): Power Good Flag. The PWRGD pin is an open-collector logic pin connected to the output of the power good comparator. PWRGD asserts low if the R_{PWRGD} pin is less than 400mV. The maximum low output level of 200mV over temperature is defined for 200µA of sink current. If R_{PWRGD} is greater than 400mV, the PWRGD pin de-asserts and becomes high impedance. The PWRGD pin may be pulled to 36V without damaging any internal circuitry regardless of the input voltage.

BLOCK DIAGRAM



PACKAGE DESCRIPTION

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev K)
Exposed Pad Variation BB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
5. BOTTOM EXPOSED PADDLE MAY HAVE METAL PROTRUSION IN THIS AREA. THIS REGION MUST BE FREE OF ANY EXPOSED TRACES OR VIAS ON PBC LAYOUT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

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