Triple Monolithic Step-Down Regulator with LDO

FEATURES

- **Wide Input Range: 4V to 36V**
- **One 2.4A and Two 1.5A Output Switching Regulators with Internal Power Switches**
- **Low Dropout Linear Regulator with External Transistor**
- **Antiphase Switching Reduces Ripple**
- Independent Run, Tracking/Soft-Start, and Power Good Indicators Ease Supply Sequencing
- Uses Small Inductors and Ceramic Capacitors
- Adjustable, 250kHz to 2.5MHz Switching Frequency, Synchronizable Over the Full Range
- User Programmable Overvoltage and Undervoltage Lockouts
- Thermally Enhanced, 38-Lead 5mm × 7mm QFN Package

APPLICATIONS

- DSL and Cable Modems
- Distributed Power Regulation
- DSP Power
- Automotive

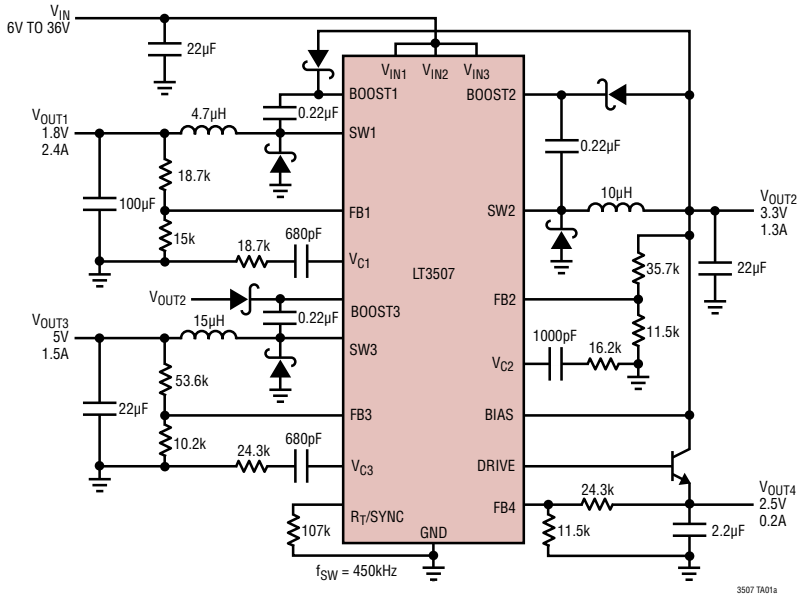
DESCRIPTION

The LT®3507 is a triple, current mode, DC/DC converter with internal power switches and a low dropout regulator. The switching converters are step-down converters capable of generating one 2.4A output and two 1.5A outputs. All three converters are synchronized to a single oscillator. The 2.4A output runs with opposite phase to the other two converters, reducing input ripple current. Each regulator has independent shutdown and soft-start circuits, and generates a power good signal when its output is in regulation, easing power supply sequencing and interfacing with microcontrollers and DSPs.

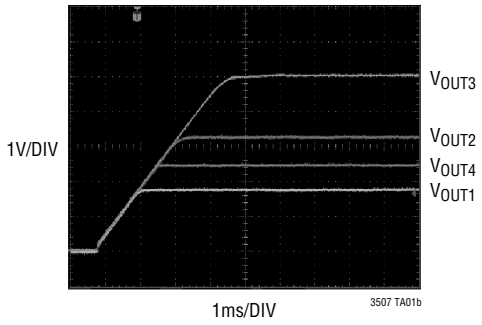
The switching frequency is set with a single resistor yielding a range of 250kHz to 2.5MHz. The high switching frequency allows the use of small inductors and capacitors resulting in a very small triple output supply. The constant switching frequency, combined with low impedance ceramic capacitors, results in low, predictable output ripple. With its wide input voltage range of 4V to 36V, the LT3507 regulates a broad array of power sources including 5V logic rails, unregulated wall transformers, lead acid batteries and distributed power supplies.

TYPICAL APPLICATION

5V, 3.3V, 2.5V and 1.8V Step-Down Regulator



Start-Up Waveforms—Coincident Tracking

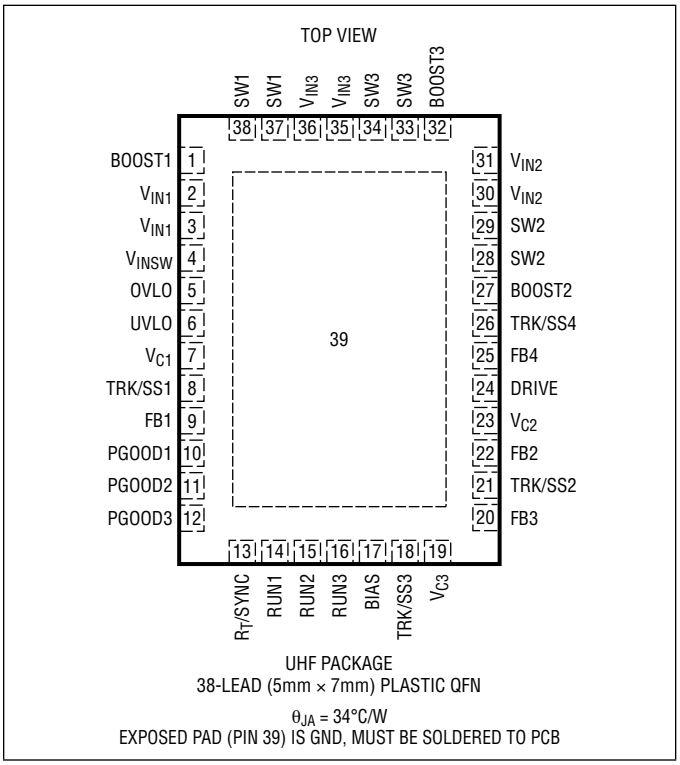


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} Pins ..... –0.3V to 36V
BOOST Pins 55V
BOOST Above SW 25V
PGOOD Pins 36V
BIAS Pin 16V
TRK/SS, V_C, FB, R_T/SYNC Pins 6V
RUN, OVLO, UVLO Pins ..... V_{IN1}
DRIVE Pin 5V
Operating Junction Temperature Range (Notes 2, 5)
LT3507E, LT3507I ..... –40°C to 125°C
LT3507H ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN

θ_{JA} = 34°C/W
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3507EUHF#PBF	LT3507EUHF#TRPBF	3507	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 125°C
LT3507IUHF#PBF	LT3507IUHF#TRPBF	3507	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 125°C
LT3507HUHF#PBF	LT3507HUHF#TRPBF	3507	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN1}, V_{IN2}, V_{IN3} = 12V, V_{BOOST1}, V_{BOOST2}, V_{BOOST3} = 17V, unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Operating Voltage	Internal UVLO on V_{IN1}	●		3.8	4	V
Input Quiescent Current	Not Switching, V_{BIAS} = 3.3V			2	3.5	mA
Bias Quiescent Current	Not Switching, V_{BIAS} = 3.3V			5	7.5	mA
Shutdown Current	$V_{RUN1,2,3}$ = 0V				1	µA
Reference Voltage Line Regulation	5V < V_{IN1} < 36V			0.01		%/V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN1}, V_{IN2}, V_{IN3} = 12V, V_{BOOST1}, V_{BOOST2}, V_{BOOST3} = 17V, unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_C Source Current	V_C = 0.6V			20		µA
V_C Sink Current	V_C = 0.6V			30		µA
V_C Clamp Voltage				1.7		V
Switching Frequency	R_T = 40.2k	●	0.9		1.1	MHz
Switching Phase	SW1 to SW2,3, R_T = 40.2k			180		Deg
Foldback Frequency	V_{FB} = 0V, R_T = 40.2k			120		kHz
Frequency Shift Threshold on FB				0.4		V
RUN Threshold				1	1.5	V
PGOOD Output Voltage Low	I_{PGOOD} = 200µA			0.2	0.4	V
PGOOD Pin Leakage	V_{PGOOD} = 2V			10	400	nA
PGOOD Threshold Offset	V_{FB} Rising		58	80	105	mV
Feedback Pin Voltage		●	788	800	812	mV
Feedback Pin Bias Current		●		–50	–500	nA
Error Amplifier Transconductance				330		µS
Error Amplifier Voltage Gain				500		V/V
V_C Switching Threshold				0.9		V
Switch Leakage Current				0.01	10	µA
Minimum Boost Voltage Above Switch (Note 4)				1.8	2.5	V
Converter 1						
V_{C1} to Switch Current Gain				5		A/V
Switch 1 Current Limit (Note 3)	Duty Cycle = 15%	●	3	4.3	6	A
Switch 1 V_{CESAT}	I_{SW1} = 2A			400	600	mV
BOOST1 Operating Current	I_{SW1} = 2A			40	60	mA
Converter 2						
V_{C2} to Switch Current Gain				3.6		A/V
Switch 2 Current Limit (Note 3)	Duty Cycle = 15%	●	2	2.9	4	A
Switch 2 V_{CESAT}	I_{SW2} = 1.5A			350	500	mV
BOOST2 Operating Current	I_{SW2} = 1.5A			40	60	mA
Converter 3						
V_{C3} to Switch Current Gain				3.6		A/V
Switch 3 Current Limit (Note 3)	Duty Cycle = 15%	●	2	2.9	4	A
Switch 3 V_{CESAT}	I_{SW3} = 1.5A			350	500	mV
BOOST3 Operating Current	I_{SW3} = 1.5A			40	60	mA
LDO Regulator						
Feedback Pin Voltage		●	788	800	812	mV
Feedback Pin Bias Current				–150	–500	nA
Error Amplifier Voltage Gain				1100		V/V
Line Regulation	V_{IN} from 5V to 36V			0.05		%/V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN1}, V_{IN2}, V_{IN3} = 12V, V_{BOOST1}, V_{BOOST2}, V_{BOOST3} = 17V, unless otherwise noted (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Load Regulation	I_{DRIVE} from 0.1mA to 10mA			0.005		%/mA
DRIVE Output Current Limit		●	10	15	22.5	mA
Dropout Voltage, V_{IN1} to DRIVE	I_{DRIVE} = 10mA, V_{IN1} = 5V			1.7	2.0	V
Dropout Voltage, BIAS to DRIVE	I_{DRIVE} = 10mA, V_{IN1} = 5V			0.5	0.8	V
Over/Undervoltage Lockout						
Undervoltage Lockout Threshold			1.15	1.20	1.25	V
Overvoltage Lockout Threshold			1.15	1.20	1.25	V
Undervoltage Lockout Hysteresis Current	V(UVLO) < 1.2V		7	10	13	µA
Overvoltage Lockout Hysteresis Current	V(OVLO) > 1.2V		–7	–10	–13	µA
Input Bias Current (OVLO and UVLO)	V(OVLO) = 1.0V, V(UVLO) = 1.5V			–100	–200	nA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3507E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3507I is guaranteed to meet performance specifications from –40°C to 125°C junction temperature. The LT3507H is guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 3: Current limit is guaranteed by design and/or correlation to static test. Slope compensation reduces current limit at higher duty cycles.

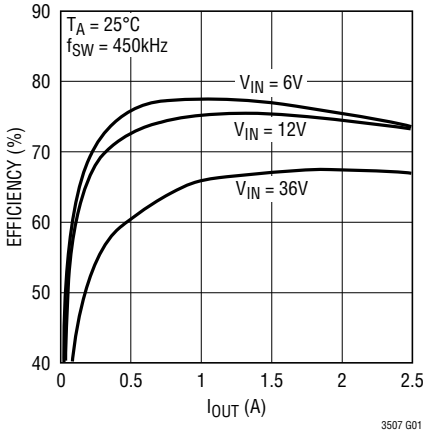
Note 4: This is the minimum voltage across the boost capacitor needed to guarantee full saturation of the internal power switch.

Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating range when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

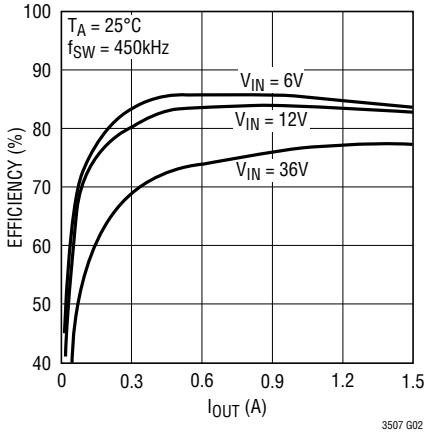
Note 6: Positive currents flow into pins, negative currents flow out of pins. Minimum and maximum specifications refer to absolute values.

TYPICAL PERFORMANCE CHARACTERISTICS

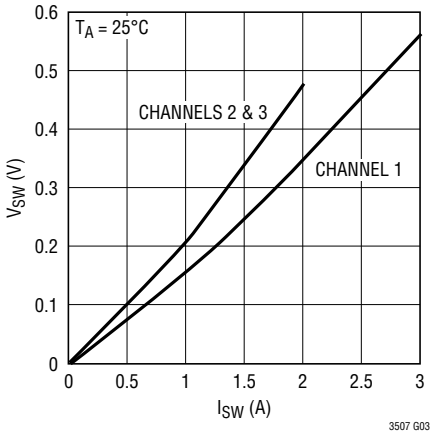
Efficiency vs Load Current, Channel 1, V_{OUT} = 1.8V



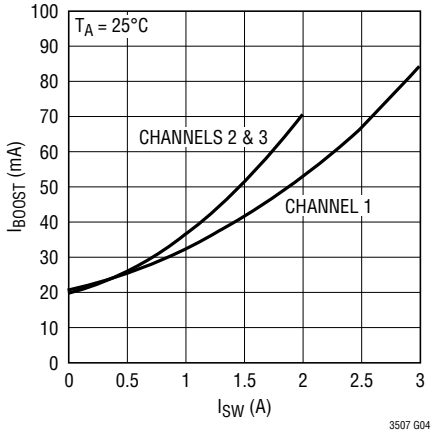
Efficiency vs Load Current, Channels 2 and 3, V_{OUT} = 3.3V



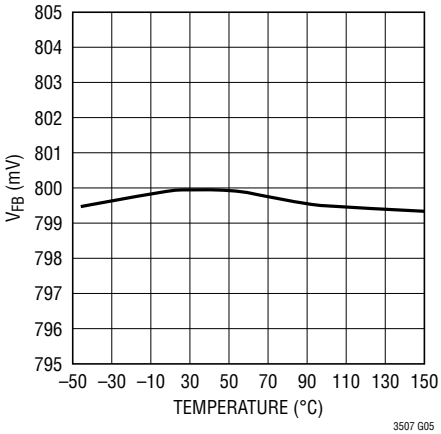
Switch V_{CESAT} vs Switch Current, Channels 1, 2 and 3



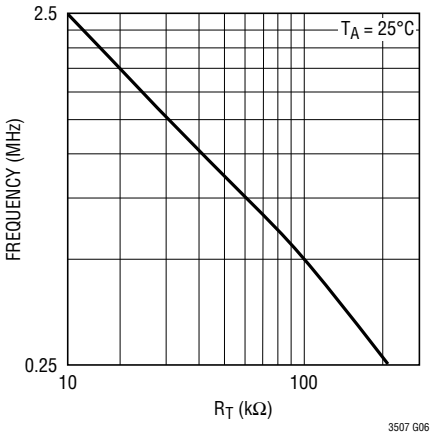
BOOST Pin Current vs Switch Current, Channels 1, 2 and 3



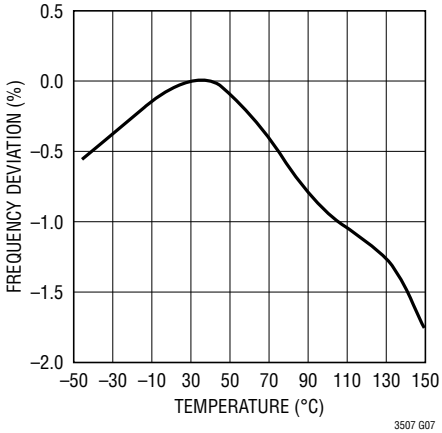
V_{FB} vs Temperature



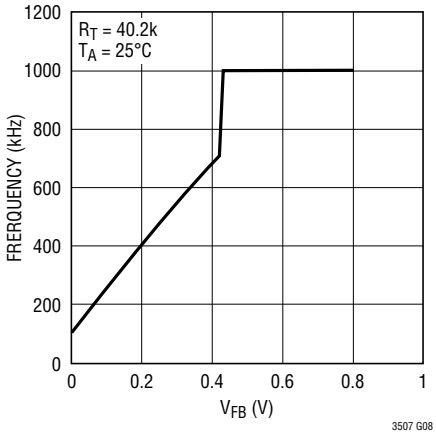
Frequency vs R_T



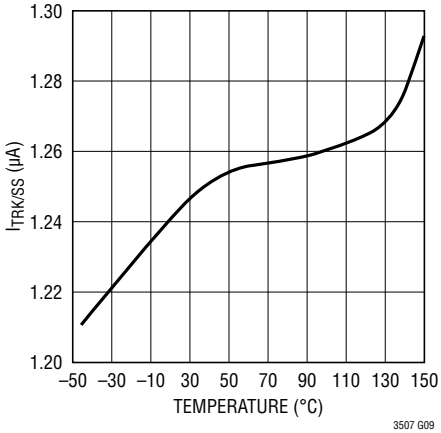
Frequency vs Temperature



Frequency vs V_{FB} (Foldback)

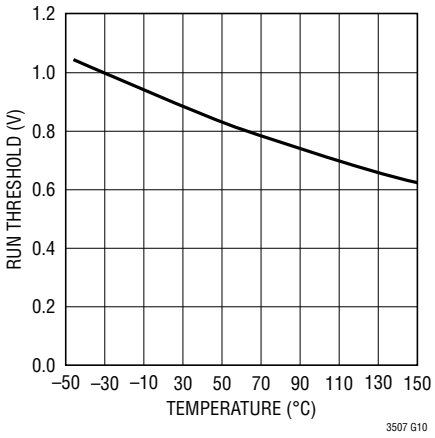


$I_{TRK/SS}$ vs Temperature

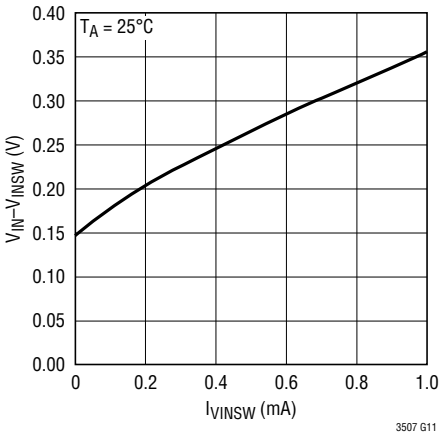


TYPICAL PERFORMANCE CHARACTERISTICS

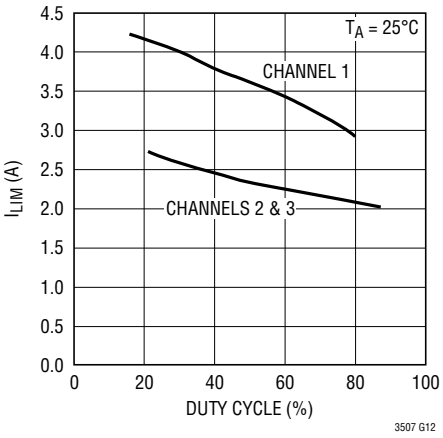
RUN Threshold vs Temperature



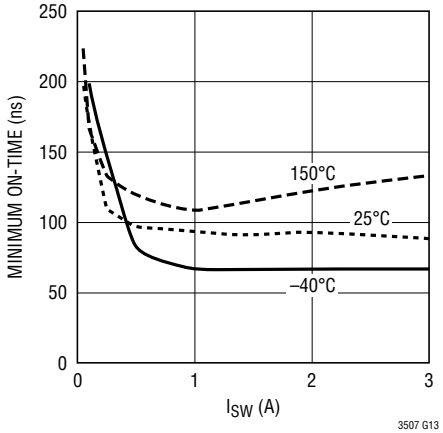
V_{IN1}-V_{INSW} Voltage Drop vs I_{VINSW}



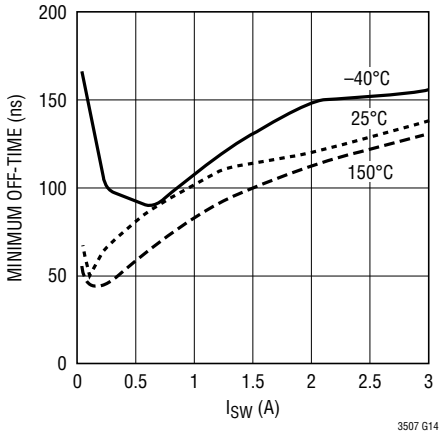
Current Limit vs Duty Cycle



Minimum On-Time vs I_{SW}



Minimum Off-Time vs I_{SW}



PIN FUNCTIONS

BOOST1, BOOST2, BOOST3 (Pins 1, 27, 32): The BOOST pins are used to provide drive voltages, higher than the input voltage, to the internal bipolar NPN power switches. These pins must be tied through a diode from V_{OUT}, V_{IN} or another supply greater than 2.5V.

V_{IN1} (Pins 2, 3): The V_{IN1} pins supply power to the internal switch of the 2.4A regulator and to the LT3507's internal reference and start-up circuitry. V_{IN1} must be above the internal UVLO threshold of 3.8V (typical) for any of the four channels to operate. These pins must be locally bypassed (Note 6).

V_{INSW} (Pin 4): The V_{INSW} pin is a switched V_{IN1} for the user programmable undervoltage and overvoltage detection. It is connected to V_{IN1} when any of the RUN pins are pulled high, and high impedance when all RUN pins are low or open.

OVLO (Pin 5): The LT3507 goes into overvoltage shutdown when this pin goes above 1.2V. If unused, the OVLO pin should be tied to GND.

UVLO (Pin 6): The LT3507 goes into undervoltage shutdown when this pin drops below 1.2V. If unused, the UVLO pin should be tied to V_{INSW}.

V_{C1}, V_{C2}, V_{C3} (Pins 7, 23, 19): The V_C pins are the outputs of the internal error amps. The voltages on these pins control the peak switch currents. These pins are normally used to compensate the control loops. Each switching regulator can be shut down by pulling its respective V_C pin to ground with an NMOS or NPN transistor.

TRK/SS1, TRK/SS2, TRK/SS3, TRK/SS4 (Pins 8, 21, 18, 26): The TRK/SS pins allow a regulator to track the output of another regulator. When the TRK/SS pin is below 0.8V, the FB pin regulates to the TRK/SS voltage. This pin can also be used as a soft-start by connecting a capacitor from TRK/SS to ground. The TRK/SS pins should be left open if neither feature is used.

FB1, FB2, FB3 (Pins 9, 22, 20): The FB pins are the negative inputs of the error amplifiers. The LT3507 regulates each feedback pin to the lesser of 0.8V or the TRK/SS pin voltage. Connect the feedback resistor divider taps to these pins.

PGOOD1, PGOOD2, PGOOD3 (Pins 10, 11, 12): The PGOOD pins are the open-collector outputs of an internal comparator. PGOOD remains low until the FB pin is within 10% of the final regulation voltage. As well as indicating output regulation, the PGOOD pins can sequence the switching regulators. These pins must be left unconnected if unused. The PGOOD outputs are valid when V_{IN} is greater than 3.8V and any of the RUN pins are high. They are not valid when all RUN pins are low.

R_T/SYNC (Pin 13): The R_T/SYNC pin requires a resistor to ground or a clock signal to set the operating frequency of the LT3507.

RUN1, RUN2, RUN3 (Pins 14, 15, 16): The RUN pins are used to shut down the individual switching regulators. When all three RUN pins are low, the LT3507 shuts down and draws less than 1µA from V_{IN1}.

BIAS (Pin 17): The BIAS pin supplies the current to the LT3507's internal regulator. This pin should be tied to the lowest available voltage source above 3V (either V_{IN}, V_{OUT} or any other available supply). The LDO pass transistor's base current is supplied from the BIAS pin if it is at least 0.8V above the LDO DRIVE output.

DRIVE (Pin 24): The DRIVE pin provides the base drive for an external NPN transistor used for the LDO regulator.

FB4 (Pin 25): The FB4 pin is the negative input to the LDO error amplifier. It is regulated to 0.8V through the LDO feedback resistor divider.

V_{IN2} (Pins 30, 31)/V_{IN3} (Pins 35, 36): The V_{IN2} and V_{IN3} pins supply power to the internal switches of the 1.5A converters. These pins must be locally bypassed (Note 6).

SW1 (Pins 37, 38)/SW2 (Pins 28, 29)/SW3 (Pins 33, 34): The SW pins are the outputs of the internal power switches. Connect these pins to the inductors and switching diodes.

Exposed Pad (Pin 39): Ground. The underside Exposed Pad metal of the package provides both electrical contact to ground and good thermal contact to the printed circuit board. The Exposed Pad must be soldered to a grounded pad on the circuit board for proper operation.

Note 6: V_{INX} pins that are connected together may share a bypass capacitor.

BLOCK DIAGRAM

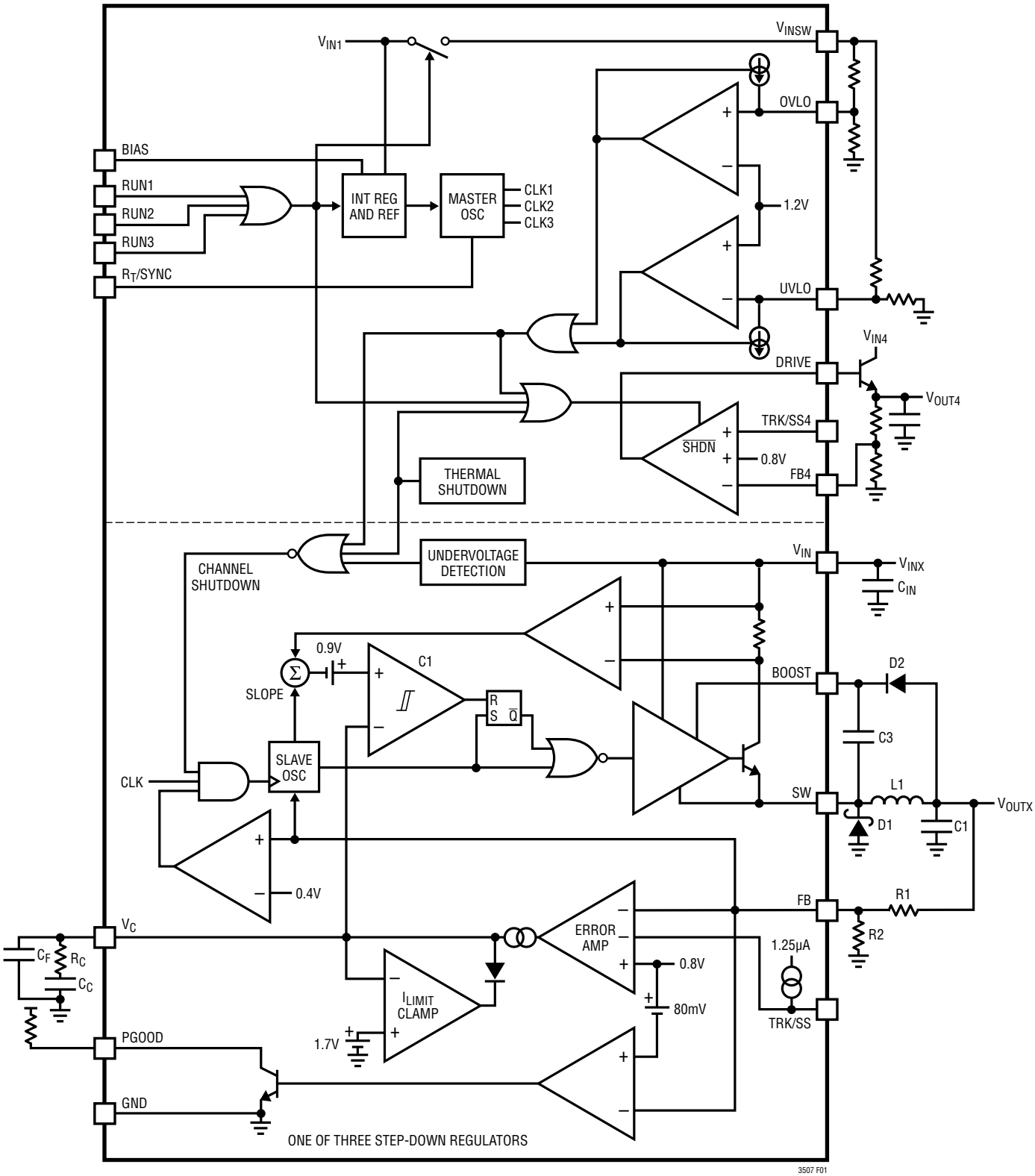


Figure 1. LT3507 Block Diagram with Typical External Components

OPERATION

The LT3507 contains three independent, constant frequency, current mode, switching regulators with internal power switches plus a low dropout linear regulator. The three regulators share common circuitry including input source, voltage reference and oscillator, but are otherwise independent. Operation can be best understood by referring to the Block Diagram (Figure 1).

If the RUN pins are tied to ground, the LT3507 is shut down and draws <1µA from the input source tied to V_{IN1}. If any of the RUN pins are driven above 1V, the internal bias circuits turn on, including the internal regulator, reference, and master oscillator. Each switching regulator will only begin to operate when its corresponding RUN pin reaches >1.25V. The master oscillator generates three clock signals, with the signal for Channel 1 out of phase by 180°.

The three switchers are current mode regulators. Instead of directly modulating the duty cycle of the power switch, the feedback loop controls the peak current in the switch during each cycle. Compared to voltage mode control, current mode control improves loop dynamics and provides cycle-by-cycle current limit.

The Block Diagram shows only one of the three step-down switching regulators. A pulse from the slave oscillator sets the RS flip-flop and turns on the internal NPN bipolar power switch. Current in the switch and the external inductor begins to increase. When this current exceeds a level determined by the voltage at V_C, current comparator C1 resets the flip-flop, turning off the switch. The current in the inductor flows through the external Schottky diode and begins to decrease. The cycle begins again at the next pulse from the oscillator. In this way, the voltage on the V_C pin controls the current through the inductor to the output. The internal error amplifier regulates the output voltage by continually adjusting the V_C pin voltage. The threshold for switching on the V_C pin is >0.9V and an active clamp of 1.8V limits the output current.

Each switcher contains an extra, independent oscillator to perform frequency foldback during overload conditions. This slave oscillator is normally synchronized to the master oscillator. A comparator senses when V_{FB} is less than 50% of its regulated value and switches the regulator from the master oscillator to a slower slave oscillator. V_{FB} is less than 50% of its regulated value during start-up, short-circuit and overload conditions. Frequency foldback helps limit switch current under these conditions.

The TRK/SS pins override the 0.8V reference for the FB pins when the TRK/SS pins are below 0.8V. This allows either coincident or ratiometric supply tracking on start-up as well as a soft-start capability.

The switch drivers operate either from V_{IN} or from the BOOST pin. An external capacitor and diode are used to generate a voltage at the BOOST pin that is higher than the input supply. This allows the driver to saturate the internal bipolar NPN power switch for efficient operation.

The BIAS pin allows the internal circuitry to draw its current from a lower voltage supply than the input, also reducing power dissipation and increasing efficiency. If the voltage on the BIAS pin falls below 3V, then its quiescent current will flow from V_{IN}.

A power good comparator trips when the FB pin is at 90% of its regulated value. The PGOOD output is an open-collector transistor that is off when the output is in regulation, allowing an external resistor to pull the PGOOD pin high. Power good is valid when the LT3507 is enabled and V_{IN} > 3.5V.

The LDO regulator uses an external NPN pass transistor to form a linear regulator. The loop is internally compensated to be stable with a load capacitance of 2.2µF or greater.

The LDO is disabled when all three of the RUN pins are low.

The overvoltage and undervoltage detection shuts down the LT3507 if the OVLO pin >1.2V or the UVLO pin <1.2V. Input overvoltage and undervoltage values are set by resistor dividers to V_{INSW}. Hysteresis is provided by 10µA currents activated when either pin trips. The hysteresis voltage at V_{IN} is the top resistor times 10µA.

APPLICATIONS INFORMATION

STEP-DOWN CONSIDERATIONS

FB Resistor Network

The output voltage is programmed with a resistor divider (refer to the Block Diagram) between the output and the FB pin. Choose the resistors according to:

$$R1 = R2\left(\frac{V_{OUT}}{800mV} - 1\right)$$

The parallel combination of R1 and R2 should be 10k or less to avoid bias current errors.

Input Voltage Range

The minimum operating voltage is determined either by the LT3507's internal undervoltage lockout (4V) or by its maximum duty cycle. The duty cycle is the fraction of time that the internal switch is on and is determined by the input and output voltages:

$$DC = \frac{V_{OUT} + V_F}{V_{IN} - V_{SW} + V_F}$$

where V_F is the forward voltage drop of the catch diode (~0.4V) and V_{SW} is the voltage drop of the internal switch (~0.3V at maximum load). This leads to a minimum input voltage of:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_F}{DC_{MAX}} - V_F + V_{SW}$$

The duty cycle is the fraction of time that the internal switch is on during a clock cycle. The maximum duty cycle is generally given by $DC_{MAX} = 1 - t_{OFF(MIN)} \bullet f_{SW}$. However, unlike most fixed frequency regulators, the LT3507 will not switch off at the end of each clock cycle if there is sufficient voltage across the boost capacitor (C3 in Figure 1) to fully saturate the output switch. Forced switch off for a minimum time will only occur at the end of a clock cycle when the boost capacitor needs to be recharged. This operation has the same effect as lowering the clock frequency for a fixed off time, resulting in a higher duty cycle and lower minimum input voltage. The resultant duty cycle depends on the charging times of the boost capacitor and can be approximated by the following equation:

$$DC_{MAX} = \frac{1}{1 + \frac{1}{B}}$$

where B is the output current capacity divided by the typical boost current from the BOOST pin current vs switch current in the Typical Performance Characteristics section.

The maximum operating voltage without pulse-skipping is determined by the minimum duty cycle DC_{MIN}:

$$V_{IN(PS)} = \frac{V_{OUT} + V_F}{DC_{MIN}} - V_F + V_{SW}$$

with $DC_{MIN} = t_{ON(MIN)} \bullet f_{SW}$.

Thus both the maximum and minimum input voltages are a function of the switching frequency and output voltages. Therefore the maximum switching frequency must be set to a value that accommodates all the input and output voltage parameters and must meet both of the following criteria for each channel:

$$f_{MAX1} = \left(\frac{V_{OUT} + V_F}{V_{IN(PS)} - V_{SW} + V_F}\right) \bullet \frac{1}{t_{ON(MIN)}}$$

$$f_{MAX2} = \left(1 - \frac{V_{OUT} + V_F}{V_{IN(MIN)} - V_{SW} + V_F}\right) \bullet \frac{1}{t_{OFF(MIN)}}$$

The values of $t_{ON(MIN)}$ and $t_{OFF(MIN)}$ are functions of I_{SW} and temperature (see chart in the Typical Performance Characteristics section). Worst-case values for switch currents greater than 0.5A are $t_{ON(MIN)}$ = 130ns (for $T_J > 125°C$ $t_{ON(MIN)}$ = 155ns) and $t_{OFF(MIN)}$ = 170ns.

f_{MAX1} is the frequency at which the minimum duty cycle is exceeded. The regulator will skip ON pulses in order to reduce the overall duty cycle at frequencies above f_{MAX1}. It will continue to regulate but with increased inductor current and greatly increased output ripple. The increased peak inductor current in pulse-skipping will also stress the switch transistor at high voltages and high switching frequency. If the LT3507 is allowed to pulse-skip and

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the input voltage is greater than 20V, then the switching frequency must be kept below 1.1MHz to prevent damage to the LT3507.

f_{MAX2} is the frequency at which the maximum duty cycle is exceeded. If there is sufficient charge on the BOOST capacitor, the regulator will skip OFF periods to increase the overall duty cycle at frequencies about f_{MAX2}. It will continue to regulate but with increased inductor current and greatly increased output ripple.

Note that the restriction on the operating input voltage refers to steady-state limits to keep the output in regulation; the circuit will tolerate input voltage transients up to the absolute maximum rating.

Switching Frequency

Once the upper and lower bounds for the switching frequency are found from the duty cycle requirements, the frequency may be set within those bounds. Lower frequencies result in lower switching losses, but require larger inductors and capacitors. The user must decide the best trade-off.

The switching frequency is set by a resistor connected from the R_T/SYNC pin to ground, or by forcing a clock signal into R_T/SYNC. The LT3507 applies a voltage of ~1.25V across this resistor and uses the current to set the oscillator speed. The switching frequency is given by the following formula:

$$f_{SW} = \frac{55}{R_T + 12}$$

where f_{SW} is in MHz and R_T is in kΩ.

The frequency sync signal will support V_H logic levels from 1.8V to 5V CMOS or TTL. The duty cycle is not important, but it needs a minimum on time of 100ns and a minimum off time of 100ns. If the sync circuit is to be powered from one of the LT3507 outputs there may be start-up problems if the driving gate is high impedance without a supply or pulls high or low at some intermediate supply voltage. The circuit shown in Figure 2 prevents these problems by isolating the clock sync circuit until the clock is operating. The Schottky diode should be a low leakage type such as the BAS70 from On Semi or CMOD6263 from Central Semi. R_T should be set to provide a frequency within ±25% of the final sync frequency.

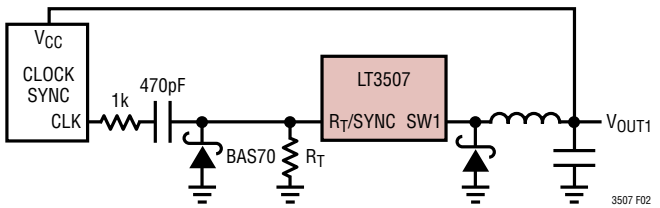

Figure 2. Clock Powered from LT3507 Output

Inductor Selection and Maximum Output Current

The current in the inductor is a triangle wave with an average value equal to the load current. The peak switch current is equal to the output current plus half the peak-to-peak inductor ripple current. The LT3507 limits its switch current in order to protect itself and the system from overload faults. Therefore, the maximum output current that the LT3507 will deliver depends on the switch current limit, the inductor value and the input and output voltages.

When the switch is off, the potential across the inductor is the output voltage plus the catch diode drop. This gives the peak-to-peak ripple current in the inductor:

$$\Delta I_L = (1 - DC)\frac{V_{OUT} + V_F}{L \bullet f}$$

where f is the switching frequency of the LT3507 and L is the value of the inductor. The peak inductor and switch current is:

$$I_{SWPK} = I_{LPK} = I_{OUT} + \frac{\Delta I_L}{2}$$

To maintain output regulation, this peak current must be less than the LT3507's switch current limit, I_{LIM}. For SW1, I_{LIM} is at least 3A at low duty cycles and decreases linearly to 2.4A at DC = 0.8. For SW2 and SW3, I_{LIM} is at least 2A for at low duty cycles and decreases linearly to 1.6A at DC = 0.8.

The minimum inductance can now be calculated as:

$$L_{MIN} = \frac{1 - DC_{MIN}}{2 \bullet f} \bullet \frac{V_{OUT} + V_F}{I_{LIM} - I_{OUT}}$$

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However, it's generally better to use an inductor larger than the minimum value. The minimum inductor has large ripple currents which increase core losses and require large output capacitors to keep output voltage ripple low. Select an inductor greater than L_{MIN} that keeps the ripple current below 30% of I_{LIM}.

The inductor's RMS current rating must be greater than the maximum load current and its saturation current should be greater than I_{LPK}. For highest efficiency, the series resistance (DCR) should be less than 0.1Ω. Table 1 lists several vendors and types that are suitable.

Table 1. Inductors

PART NUMBER	VALUE (µH)	I_{SAT} (A)	DCR (Ω)	HEIGHT (mm)
Sumida				
CDC5D23-2R2	2.2	2.16	0.030	2.5
CDRH5D28-2R6	2.6	2.60	0.013	3.0
CDRH6D26-5R6	5.6	2.00	0.027	2.8
CDH113-100	10	2.00	0.047	3.7
Coilcraft				
DO1606T-152	1.5	2.10	0.060	2.0
LPS6225-222ML	2.2	4.00	0.045	2.4
DO1608C-332	3.3	2.00	0.080	2.9
MSS6132-472ML	4.7	2.60	0.056	3.2
DO1813P-682HC	6.8	2.20	0.080	5.0
Cooper				
SD414-2R2	2.2	2.73	0.061	1.35
DRA73-6R8-R	6.8	2.96	0.041	3.55
UP1B-100	10	1.90	0.111	5.0
Toko				
(D62F)847FY-2R4M	2.4	2.5	0.037	2.7
(D73LF)817FY-2R2M	2.2	2.7	0.03	3.0

This analysis is valid for continuous mode operation ($I_{OUT} > I_{LIM}/2$). For details of maximum output current in discontinuous mode operation, see Linear Technology's Application Note AN44. Finally, for duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid subharmonic oscillations. This minimum inductance is:

$$SW1: L_{MIN} = \left(V_{OUT} + V_F\right) \bullet \frac{0.45}{f_{SW}}$$

$$SW2,\ SW3: L_{MIN} = \left(V_{OUT} + V_F\right) \bullet \frac{0.9}{f_{SW}}$$

with L_{MIN} in µH and f_{SW} in MHz.

Output Capacitor Selection

The output capacitor filters the inductor current to generate an output with low voltage ripple. It also stores energy in order to satisfy transient loads and stabilize the LT3507's control loop. Because the LT3507 operates at a high frequency, minimal output capacitance is necessary. In addition, the control loop operates well with or without the presence of output capacitor series resistance (ESR). Ceramic capacitors, which achieve very low output ripple and small circuit size, are therefore an option.

You can estimate output ripple with the following equations:

$$V_{RIPPLE} = \frac{\Delta I_L}{8 \bullet f \bullet C_{OUT}} \text{ for ceramic capacitors}$$

and

$V_{RIPPLE} = \Delta I_L \bullet$ ESR for electrolytic capacitors (tantalum and aluminum)

where ΔI_L is the peak-to-peak ripple current in the inductor. The RMS content of this ripple is very low so the RMS current rating of the output capacitor is usually not of concern. It can be estimated with the formula:

$$I_{C(RMS)} = \frac{\Delta I_L}{\sqrt{12}}$$

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Another constraint on the output capacitor is that it must have greater energy storage than the inductor; if the stored energy in the inductor transfers to the output, the resulting voltage step should be small compared to the regulation voltage. For a 5% overshoot, this requirement indicates:

$$C_{OUT} > 10 \bullet L \bullet \left(\frac{I_{LIM}}{V_{OUT}} \right)^2$$

The low ESR and small size of ceramic capacitors make them the preferred type for LT3507 applications. Not all ceramic capacitors are the same, however. Many of the higher value capacitors use poor dielectrics with high temperature and voltage coefficients. In particular, Y5V and Z5U types lose a large fraction of their capacitance with applied voltage and at temperature extremes. Because loop stability and transient response depend on the value of C_{OUT}, this loss may be unacceptable. Use X7R and X5R types.

Electrolytic capacitors are also an option. The ESRs of most aluminum electrolytic capacitors are too large to deliver low output ripple. Tantalum, as well as newer, lower-ESR organic electrolytic capacitors intended for power supply use are suitable. Chose a capacitor with a low enough ESR for the required output ripple. Because the volume of the capacitor determines its ESR, both the size and the value will be larger than a ceramic capacitor that would give similar ripple performance. One benefit is that the larger capacitance may give better transient response for large changes in load current. Table 2 lists several capacitor vendors.

Table 2. Low ESR Surface Mount Capacitors

VENDOR	TYPE	SERIES
Taiyo-Yuden	Ceramic	
AVX	Ceramic Tantalum	 TPS
Kemet	Tantalum Tantalum Organic Aluminum Organic	T491,T494,T495 T520 A700
Sanyo	Tantalum or Aluminum Organic	POSCAP
Panasonic	Aluminum Organic	SP CAP
TDK	Ceramic	

Diode Selection

The catch diode (D1 from Figure 2) conducts current only during switch off time. Average forward current in normal operation can be calculated from:

$$I_{D(AVG)} = \frac{I_{OUT}\left(V_{IN} - V_{OUT}\right)}{V_{IN}}$$

The only reason to consider a diode with a larger current rating than necessary for nominal operation is for the worst-case condition of shorted output. The diode current will then increase to the typical peak switch current. Peak reverse voltage is equal to the regulator input voltage. Use a diode with a reverse voltage rating greater than the input voltage, but not higher than 40V. Using higher breakdown Schottky diodes may result in undesirable behavior. The programmable OVLO can protect the diode from excessive reverse voltage by shutting down the regulator if the input voltage exceeds the maximum rating of the diode. Table 3 lists several Schottky diodes and their manufacturers.

Table 3. Schottky Diodes

PART NUMBER	V_R (V)	I_{AVE} (A)	V_F AT 1A (mV)	V_F AT 2A (mV)
On Semiconductor				
MBRM120E	20	1	530	595
MBRM140	40	1	550	
Diodes Inc				
B120	20	1	500	
B140	40	1	500	
B220	20	2		500
B240	40	2		500
DFLS140L	40	1	550	
DFLS240L	40	2		550

Boost Pin Considerations

The capacitor and diode tied to the BOOST pin generate a voltage that is higher than the input voltage. In most cases, a small ceramic capacitor and fast switching diode (such as the CMDSH-3 or MMSD914LT1) will work well. The capacitor value is a function of the switching frequency,

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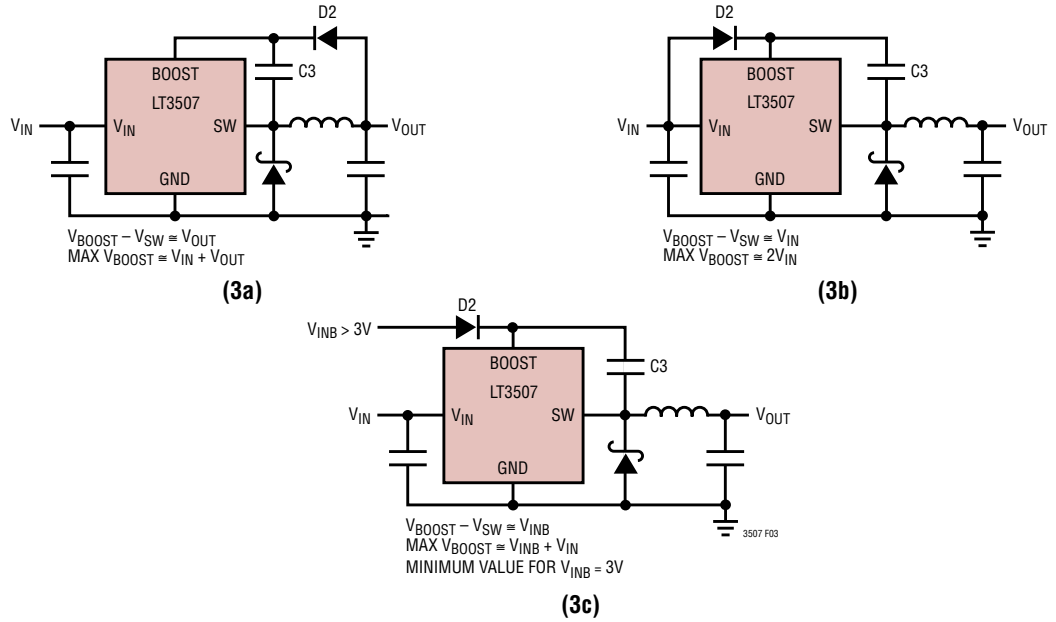

Figure 3. Generating the Boost Voltage

peak current, duty cycle and boost voltage; in general a value of (0.1µF • 1MHz/f_{SW}) works well. Figure 3 shows three ways to arrange the boost circuit. The BOOST pin must be more than 2.5V above the SW pin for full efficiency. For outputs of 3.3V and higher, the standard circuit (Figure 3a) is best. For outputs between 2.8V and 3.3V, use a small Schottky diode (such as the BAT54). For lower output voltages, the boost diode can be tied to the input (Figure 3b). The circuit in Figure 3a is more efficient because the BOOST pin current comes from a lower voltage source. Finally, as shown in Figure 3c, the anode of the boost diode can be tied to another source that is at least 3V. For example, if you are generating 3.3V and 1.8V and the 3.3V is on whenever the 1.8V is on, the 1.8V boost diode can be connected to the 3.3V output. In this case, the 3.3V output cannot be set to track the 1.8V output (see Output Voltage Tracking).

In any case, be sure that the maximum voltage at the BOOST pin is less than 55V and the voltage difference between the BOOST and SW pins is less than 25V.

The minimum operating voltage of an LT3507 application is limited by the internal undervoltage lockout (4V for Channel 1, 3V for Channels 2 and 3) and by the maximum duty cycle. The boost circuit also limits the minimum input voltage for proper start-up. If the input voltage ramps slowly, or the LT3507 turns on when the output is already in regulation, the boost capacitor may not be fully charged. Because the boost capacitor charges with the energy stored in the inductor, the circuit will rely on some minimum load current to get the boost circuit running properly. This minimum load will depend on input and output voltages, and on the arrangement of the boost circuit. The minimum load current generally goes to zero once the circuit has started. Figure 4 shows a plot of minimum load to start and to run as a function of input voltage. Even without an output load current, in many cases the discharged output capacitor will present a load to the switcher that will allow it to start.

The boost current is generally small but can become significant at high duty cycles. The required boost current is:

$$I_{BOOST} = \left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{I_{OUT}}{40}\right)$$

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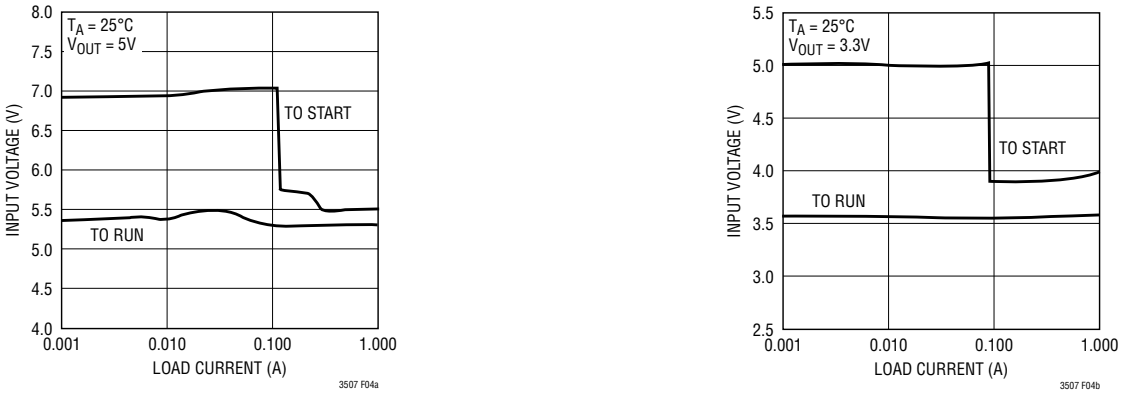

Figure 4. The Minimum Input Voltage Depends on Output Voltage, Load Current and Boost Circuit

Converter with Backup Output Regulator

There is another situation to consider in systems where the output will be held high when the input to the LT3507 is absent. If the V_{IN} and one of the RUN pins are allowed to float, then the LT3507's internal circuitry will pull its quiescent current through its SW pin. This is acceptable if the system can tolerate a few mA of load in this state. With all three RUN pins grounded, the LT3507 enters shutdown mode and the SW pin current drops to <50µA. However, if the V_{IN} pin is grounded while the output is held high, then parasitic diodes inside the LT3507 can pull large currents from the output through the SW pin and the V_{IN} pin. A Schottky diode in series with the input to the LT3507, as shown in Figure 5, will protect the LT3507 and the system from a shorted or reversed input.

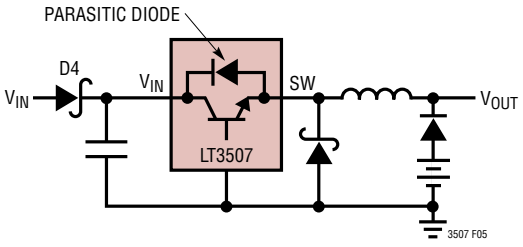

Figure 5. Diode D4 Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output

Input Capacitor Selection

Bypass the input of the LT3507 circuit with a 10µF or higher ceramic capacitor of X7R or X5R type. A lower value or a less expensive Y5V type will work if there is additional bypassing provided by bulk electrolytic capacitors, or if the input source impedance is low. The following paragraphs describe the input capacitor considerations in more detail.

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT3507 input and to force this switching current into a tight local loop, minimizing EMI. The input capacitor must have low impedance at the switching frequency to do this effectively and it must have an adequate ripple current rating. With three switchers operating at the same frequency but with different phases and duty cycles, calculating the input capacitor RMS current is not simple; however, a conservative value is the RMS input current for the phase delivering the most power ($V_{OUT} \bullet I_{OUT}$):

$$I_{IN(RMS)} = I_{OUT} \bullet \frac{\sqrt{V_{OUT}\left(V_{IN} - V_{OUT}\right)}}{V_{IN}} < \frac{I_{OUT}}{2}$$

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and is largest when V_{IN} = 2V_{OUT} (50% duty cycle). As the second, lower power channel draws input current, the input capacitor's RMS current actually decreases as the out-of-phase current cancels the current drawn by the higher power channel. Considering that the maximum load current from a single phase (if SW2 and SW3 are both at maximum current) is ~3A, RMS ripple current will always be less than 1.5A.

The high frequency of the LT3507 reduces the energy storage requirements of the input capacitor, so that the capacitance required is often less than 10µF. The combination of small size and low impedance (low equivalent series resistance or ESR) of ceramic capacitors makes them the preferred choice. The low ESR results in very low voltage ripple. Ceramic capacitors can handle larger magnitudes of ripple current than other capacitor types of the same value. Use X5R and X7R types.

An alternative to a high value ceramic capacitor is a lower value along with a larger electrolytic capacitor, for example a 1µF ceramic capacitor in parallel with a low ESR tantalum capacitor. For the electrolytic capacitor, a value larger than 10µF will be required to meet the ESR and ripple current requirements. Because the input capacitor is likely to see high surge currents when the input source is applied, tantalum capacitors should be surge rated. The manufacturer may also recommend operation below the rated voltage of the capacitor. Be sure to place the 1µF ceramic as close as possible to the V_{IN} and GND pins on the IC for optimal noise immunity.

A final caution is in order regarding the use of ceramic capacitors at the input. A ceramic input capacitor can combine with stray inductance to form a resonant tank circuit. If power is applied quickly (for example by plugging the circuit into a live power source), this tank can ring, doubling the input voltage and damaging the LT3507. The solution is to either clamp the input voltage or dampen the tank circuit by adding a lossy capacitor in parallel with the ceramic capacitor. For details, see Application Note 88.

Frequency Compensation

The LT3507 uses current mode control to regulate the output. This simplifies loop compensation. In particular, the LT3507 does not depend on the ESR of the output capacitor for stability so you are free to use ceramic capacitors to achieve low output ripple and small circuit size.

The components tied to the V_C pin provide frequency compensation. Generally, a capacitor and a resistor in series to ground determine loop gain. In addition, there is a lower value capacitor in parallel. This capacitor filters noise at the switching frequency and is not part of the loop compensation.

Loop compensation determines the stability and transient performance. Designing the compensation network is a bit complicated and the best values depend on the application and the type of output capacitor. A practical approach is to start with one of the circuits in this data sheet that is similar to your application and tune the compensation network to optimize the performance. Check stability across all operating conditions, including load current, input voltage and temperature. The LT1375 data sheet contains a more thorough discussion of loop compensation and describes how to test the stability using a transient load. Application Note 76 is an excellent source as well.

Figure 6 shows an equivalent circuit for the LT3507 control loop. The error amp is a transconductance amplifier with finite output impedance. The power section, consisting of the modulator, power switch and inductor is modeled as a transconductance amplifier generating an output current proportional to the voltage at the V_C pin. The gain of the power stage (g_{mp}) is 5S for Channel 1 and 3.6S for Channels 2 and 3. Note that the output capacitor integrates this

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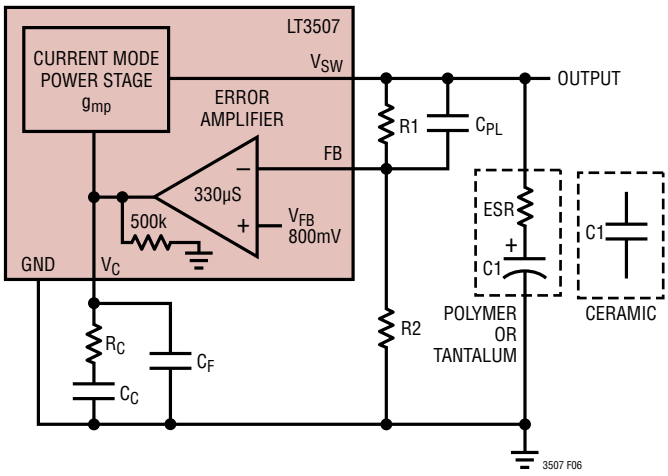

Figure 6. Loop Response Model

current and that the capacitor on the V_C pin (C_C) integrates the error amplifier output current, resulting in two poles in the loop. In most cases, a zero is required and comes either from the output capacitor ESR or from a resistor in series with C_C. This model works well as long as the inductor current ripple is not too low ($\Delta I_{RIPPLE} > 5\% I_{OUT}$) and the loop crossover frequency is less than $f_{SW}/5$. A phase lead capacitor (C_{PL}) across the feedback divider may improve the transient response.

SHUTDOWN

The RUN pins are used to place the individual switching regulators and the internal bias circuits in shutdown mode. When all three RUN pins are pulled low, the LT3507 is in shutdown mode and draws less than 1µA from the input supply. When any RUN pin is pulled high (>1.25V) the internal reference, the LDO and selected channel are all turned on.

The RUN pins draw a small amount of current to power the reference. The current is less than 3µA at 1.8V, so the RUN pin can be driven directly from 1.8V logic. The RUN pins are rated up to 36V and can be connected directly to the input voltage.

A RUN pin cannot be pulled up by logic powered by its own output, i.e., RUN1 can't be pulled up by logic powered by OUT1.

POWER GOOD INDICATORS

The PGOOD pin is the open-collector output of an internal comparator. PGOOD remains low until the FB pin is within 10% of the final regulation voltage. Tie the PGOOD to any supply with a pull-up resistor that will supply less than 200µA. Note that this pin will be open when the LT3507 is in shutdown mode (all three RUN pins at ground) regardless of the voltage at the FB pin. PGOOD is valid when the LT3507 is enabled (any RUN pin is high) and V_{IN} is greater than ~3.5V.

OUTPUT SEQUENCING

The LT3507 outputs can be sequenced in several ways. The circuits in Figure 7 show some examples of these. In each case channel 1 starts first, followed by channel 2, then channel 3. The sequence shown is not a requirement; the LT3507 can sequence the channels in any order. Note that these circuits sequence the outputs during start-up. When shut down the three channels turn off simultaneously.

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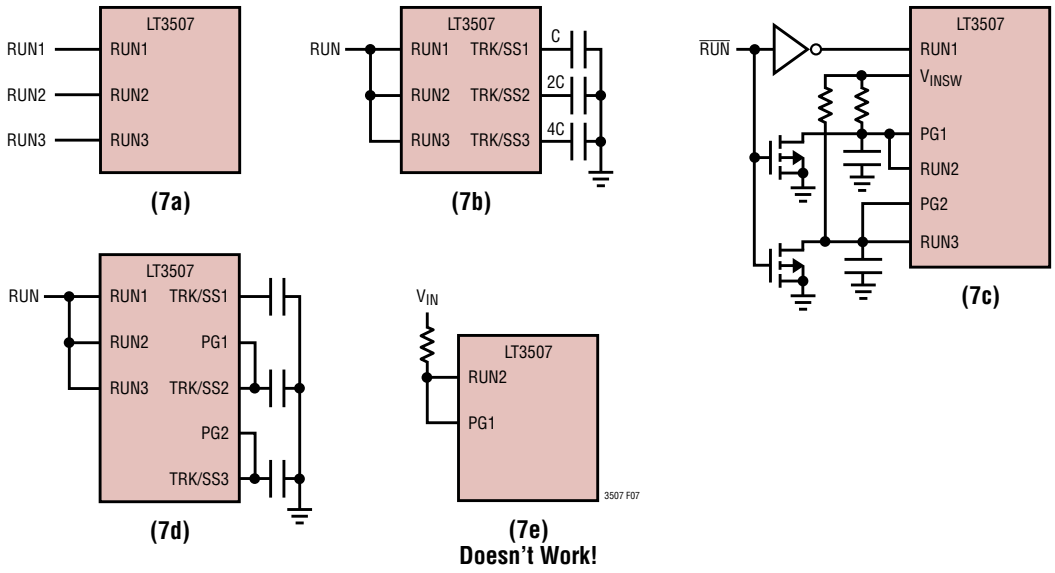

Figure 7. Output Sequencing

The most obvious method is to bring the RUN pins up individually in the sequence desired (Figure 7a). This is the ideal solution if full independent control of all three channels is needed. This is also a simple solution, but it does require three logic inputs.

Another possibility is to use the soft-start feature to slow the start-up of specific channels (Figure 7b). All three RUN pins are tied together and the difference in soft-start capacitance will determine the start-up sequence. The larger capacitor on channel 2 slows its start-up with respect to channel 1, and channel 3 is even slower. The capacitor on the delayed channel should be at least twice the value of the capacitor on the faster channel. A larger ratio may be required, depending on the output capacitance and load on each channel. Make sure to test the circuit in the system before deciding on final values for these capacitors. Also remember that the delayed channels will start rising right away, just at a slower rate than the faster channels.

The PG pins can be also used to sequence the three outputs. In Figure 7c, the PG pins drive the RUN pins directly. Channel 2 will be held off until channel 1 is in regulation and channel 3 is held off until channel 2 is in regulation. The resistors pull up to V_{INSW} so that there is no current draw in shutdown. They should be sized to provide at least 1µA into the RUN pin. The capacitors keep channels 2 and 3 off until the power good comparators are functioning (the power good comparators are disabled in shutdown). The FETs are necessary to insure the RUN2 and RUN3 pins are held low during shutdown.

In Figure 7d, the PG pins pull down the TRK/SS pins of the delayed channels. This is a simple solution requiring no extra components. Channel 2 is held off by the PG1 output pulling TRK/SS2 down until channel 1 is at 90% of its final value. PG1 then goes high impedance and allows the channel 2 soft-start circuit to charge the soft-start capacitor bringing channel 2 up. Similarly, channel 3 is held off by PG2.

The circuits in Figure 7a and 7b leave the power good indicators free. However, the circuits in Figures 7c and 7d have another advantage. As well as sequencing the outputs at start-up, they also disable the slaved channels if the master channel falls out of regulation (due to a short circuit or a collapsing input voltage).

Finally, be aware that **the circuit in Figure 7e does not work**, because the power good comparators are disabled in shutdown.

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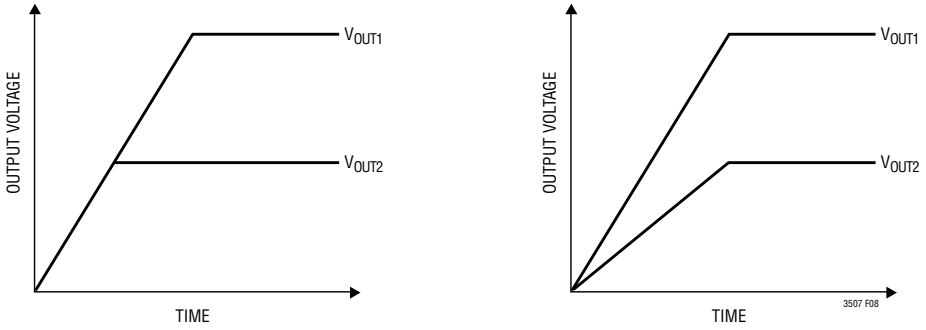
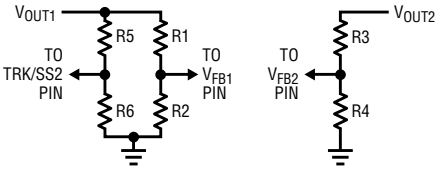


(8a) Coincident Tracking (8b) Ratiometric Tracking

Figure 8. Two Different Modes of Output Voltage Tracking



Tracking Setup

SELECTING VALUES FOR R5 AND R6

	COINCIDENT	RATIOMETRIC
R5 =	R3	R1
R6 =	R4	$\frac{R1}{V_{OUT1}/1V-1}$

$$\left(\frac{R1}{R2}=\frac{V_{OUT1}}{0.8}-1,\ \frac{R3}{R4}=\frac{V_{OUT2}}{0.8}-1\right)$$

Figure 9. Setup for Coincident and Ratiometric Tracking

OUTPUT VOLTAGE TRACKING

The LT3507 allows the user to program how the output ramps up by means of the TRK/SS pins. Through these pins, any channel output can be set up to either coincidently or ratiometrically track any other channel output. This example will show the channel 2 output tracking the channel 1 output, as shown in Figure 8. The TRK/SS2 pin acts as a clamp on channel 2's reference voltage. V_{OUT2} is referenced to the TRK/SS2 voltage when the TRK/SS2 < 0.8V and to the internal precision reference when TRK/SS2 > 0.8V.

To implement the coincident tracking in Figure 8a, connect an extra resistive divider to the output of channel 1 and connect its midpoint to the TRK/SS2 pin (Figure 9). The ratio of this divider should be selected the same as that of channel 2's feedback divider (R5 = R3 and R6 = R4). In this tracking mode, V_{OUT1} must be set higher than V_{OUT2}. To implement the ratiometric tracking in Figure 8b, change the extra divider ratio to R5 = R1 and R6 = R2 + ΔR. The extra resistance on R6 should be set so that the TRK/SS2 voltage is ≥1V when V_{OUT1} is at its final value.

The need for this extra resistance is best understood with the help of the equivalent input circuit shown in Figure 10. At the input stage of the error amplifier, two common anode diodes are used to clamp the equivalent reference voltage and an additional diode is used to match the shifted common mode voltage. The top two current sources are of the same amplitude. In the coincident mode, the TRK/SS2 voltage is substantially higher than 0.8V at steady state and effectively turns off D1. D2 and D3 will therefore conduct the same current and offer tight matching between V_{FB2} and the internal precision 0.8V reference. In the ratiometric mode with R6 = R2, TRK/SS2 equals 0.8V at steady state. D1 will divert part of the bias current and make V_{FB2} slightly lower than 0.8V. Although this error

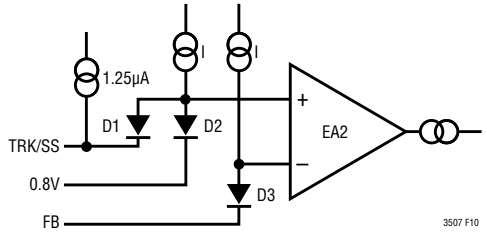


Figure 10. Equivalent Input Circuit of Error Amplifier

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is minimized by the exponential I-V characteristic of the diodes, it does impose a finite amount of output voltage deviation. Further, when channel 1's output experiences dynamic excursions (under load transient, for example), channel 2 will be affected as well. Setting R6 to a value that pushes the TRK/SS2 voltage to 1V at steady state will eliminate these problems while providing near ratiometric tracking.

The example shows channel 2 tracking channel 1, however any channel may be set up to track any other channel.

If a capacitor is tied from the TRK/SS pin to ground, then the internal pull-up current will generate a voltage ramp on this pin. This results in a ramp at the output, limiting the inductor current and therefore input current during start-up. A good value for the soft-start capacitor is C_{OUT}/10,000, where C_{OUT} is the value of the output capacitor.

MULTIPLE INPUT SUPPLIES

V_{IN1}, V_{IN2} and V_{IN3} are independent and can be powered with different voltages provided V_{IN1} is present when V_{IN2} or V_{IN3} is present. Each supply must be bypassed as close to the V_{IN} pins as possible.

For applications requiring large inductors due to high V_{IN} to V_{OUT} ratios, a 2-stage step-down approach may reduce inductor size by allowing an increase in frequency. A dual step-down application steps down the input voltage (V_{IN1}) to the highest output voltage, then uses that voltage to power the other outputs (V_{IN2} and V_{IN3}). V_{OUT1} must be able to provide enough current for its output plus the input current at V_{IN2} and V_{IN3} when V_{OUT2} and V_{OUT3} are at maximum load. The Typical Applications section shows a 36V to 15V, 1.8V and 1.2V 2-stage converter using this approach.

For applications with multiple voltages, the LT3507 can accommodate input voltages as low as 3V on V_{IN2} and V_{IN3}. This can be useful in applications regulating outputs from a PCI Express bus, where the 12V input is power limited and the 3.3V input has power available to drive other outputs. In this case, tie the 12V input to V_{IN1} and the 3.3V input to V_{IN2} and V_{IN3}.

LOW DROPOUT REGULATOR

The low dropout regulator comprises an error amp, loop compensation and a base drive amp. It uses the same 0.8V reference as the switching regulators. It requires an external NPN pass transistor and 2.2µF of output capacitance for stability. The internal compensation is stable with loads up to 300mA.

The dropout characteristics will be determined by the pass transistor. The collector-emitter saturation characteristics will limit the dropout voltage. Table 4 lists some suitable NPN transistors with their saturation specifications.

The base drive voltage has a maximum voltage of 5V. This will limit the maximum output of the regulator to 5V – V_{BESAT} where V_{BESAT} is the base-emitter saturation voltage of the pass transistor.

Table 4. NPN Pass Transistors and Saturation Characteristics

PART NUMBER	V_{CESAT}	V_{BESAT}	I_C (mA)	I_B (mA)
On Semiconductor				
NSS30071	0.25	0.85	500	5
NSS30101	0.2	0.85	1000	10
Fairchild				
KSC3265	0.4		500	20

The LDO is always on when any of the switcher channels is on. The LDO may be shut down if it is unused by pulling the FB4 pin up with a 30µA current source. The FB4 pin will clamp at about 1.25V and the LDO will shut off reducing power consumption. This pull-up can be sourced from one of the LT3507 outputs provided that channel is always on when the other channels are on.

The output stage of the LDO will drive the NPN base from the BIAS voltage if it is at least 0.8V above the LDO DRIVE voltage.

APPLICATIONS INFORMATION

FB Resistor Network

The output voltage of the LDO regulator is programmed with a resistor divider (Refer to Block Diagram) between the emitter of the external NPN pass resistor and the feedback pin, FB4. Choose the resistors according to

$$R1 = R2\left(\frac{V_{OUT4}}{800mV} - 1\right)$$

The parallel combination of R1 and R2 should be 10k or less to avoid bias current errors.

PROGRAMMABLE OVERVOLTAGE AND UNDERVOLTAGE LOCKOUT

The LT3507 provides two input pins that allow user-programmable overvoltage and undervoltage lockout. Both the trip levels and hysteresis can be set by resistor values.

V_{INSW} provides a switched V_{IN1} to minimize power consumption in shutdown. V_{INSW} is connected to V_{IN1} when the LT3507 is operating, with a saturation voltage of about 0.3V. It is high impedance when the LT3507 is in shutdown (all three RUN pins low).

The programmable lockout is a pair of comparators with the trip level set at 1.2V. The OVLO comparator trips when the OVLO pin exceeds 1.2V while the UVLO comparator trips when the UVLO pin drops below 1.2V. These comparators shut down all four regulators until the input voltage recovers.

The comparators also activate current sources that generate hysteresis to eliminate chatter. The UVLO comparator activates a 10µA current sink on the UVLO pin. The OVLO comparator activates a 10µA current source on the OVLO pin. These currents generate hysteresis voltage through the resistance of the divider string.

Figure 11 shows a typical connection. The threshold voltages are:

$$V_{OVTH} = 0.3V + 1.2V \bullet \left(1 + \frac{R3}{R4}\right)$$

$$V_{UVTH} = 0.3V + 1.2V \bullet \left(1 + \frac{R1}{R2}\right)$$

The hysteresis voltages are:

V_{OVHYST} = 10µA • R3

V_{UVHYST} = 10µA • R1

If the overvoltage lockout is not used, the OVLO pin must be tied to ground. If the undervoltage lockout is not used, the UVLO pin must be tied to V_{INSW}.

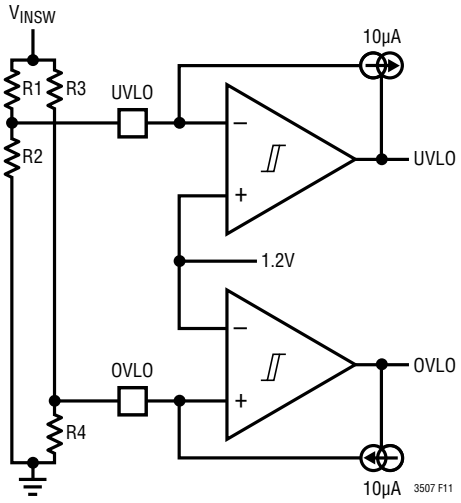


Figure 11. Undervoltage and Overvoltage Lockout Circuit

APPLICATIONS INFORMATION

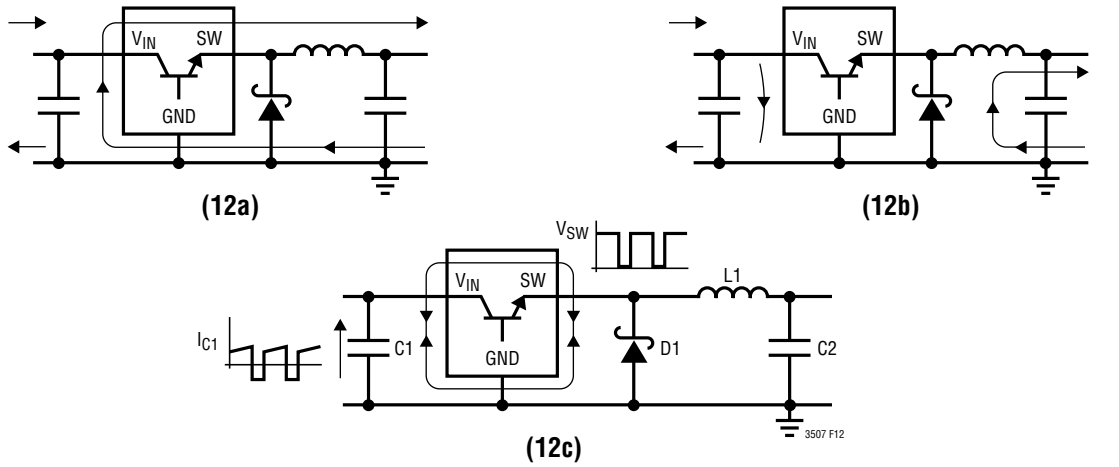


Figure 12. Subtracting the Current When the Switch is ON (12a) From the Current When the Switch is OFF (12b) Reveals the Path of the High Frequency Switching Current (12c) Keep this Loop Small. The Voltage on the SW and Boost Nodes Will Also be Switched; Keep These Nodes as Small as Possible. Finally, Make Sure the Circuit is Shielded with a Local Ground Plane

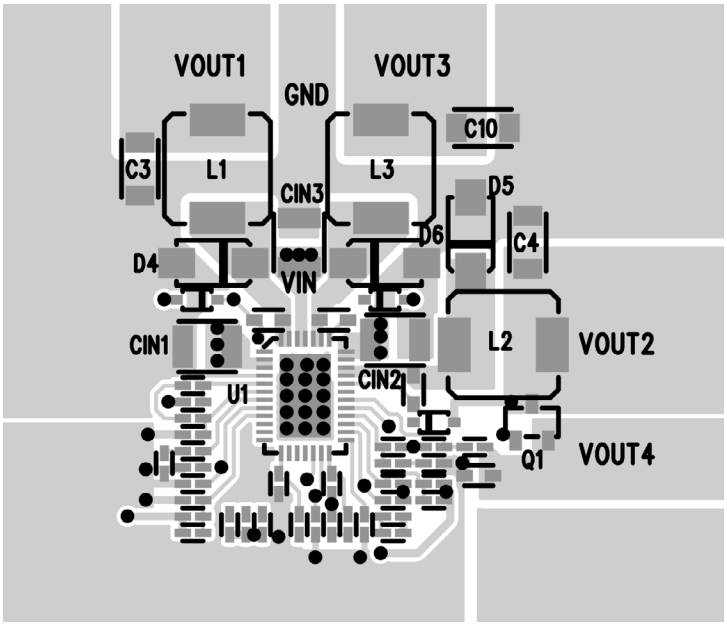


Figure 13. Power Path Components and Topside Layout

PCB LAYOUT

For proper operation and minimum EMI, care must be taken during printed circuit board (PCB) layout. Figure 12 shows the high current paths in the step-down regulator circuit. Note that in the step-down regulators large, switched currents flow in the power switch, the catch diode and the input capacitor. The loop formed by these components should be as small as possible. Place these components, along with the inductor and output capacitor, on the same side of the circuit board and connect them on that layer. Place a local, unbroken ground plane below these components and tie this ground plane to system ground at one location, ideally at the ground terminal of the output capacitor C2. Additionally, keep the SW and BOOST nodes as small as possible. Figure 13 shows an example of proper PCB layout.

APPLICATIONS INFORMATION

THERMAL CONSIDERATIONS

The high output current capability of the LT3507 will require careful attention to power dissipation of all the components to insure a safe thermal design. The PCB must provide heat sinking to keep the LT3507 cool. The Exposed Pad on the bottom of the package must be soldered to a ground plane. This ground should be tied to other copper layers below with thermal vias; these layers will spread the heat dissipated by the LT3507. Place additional vias near the catch diodes. Adding more copper to the top and bottom layers and tying this copper to the internal planes with vias can reduce thermal resistance further. With these steps, the thermal resistance from die (or junction) to ambient can be reduced to θ_{JA} = 34°C/W or less. With 100 LFPM airflow, this resistance can fall by another 25%. Further increases in airflow will lead to lower thermal resistance.

The maximum allowed power dissipation by the LT3507 can be determined by:

$$P_{DISS(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where T_{JMAX} is the maximum die temperature of 125°C (150°C for H-grade).

However, take care in determining T_A since the catch diodes also dissipate power and must be located close to the LT3507. Another potential heat source is the LDO pass transistor. In a compact layout the pass transistor will be located close to the LT3507. The inductors will also dissipate some power due to their series resistance and they must be close to the LT3507. All of these heat sources will increase the effective ambient temperature seen by the LT3507.

A thorough analysis of eight heat sources in a small PCB area is beyond the scope of this data sheet, however a number of thermal analysis programs are available to calculate the temperature rise in each component (such as PCAnalyze from K&K Associates or BETAsoft from Mentor). The power dissipation of each component will be needed to accurately calculate the thermal characteristics of the system.

The contributors to power dissipation inside the LT3507 are switch DC loss, switch AC loss, boost current, quiescent current and LDO drive current. The total dissipation within the LT3507 can be expressed as:

$$P_{DISS} = \sum_{i=1}^{3}\left(P_{SWDCi} + P_{SWACi} + P_{BSTi}\right) + P_Q + P_{LDO}$$

The switch DC and AC losses in channel i are:

$$P_{SWDCi} = \frac{R_{SWi}\left(I_{OUTi}\right)^2 V_{OUTi}}{V_{INi}}$$

$$P_{SWACi} = 17ns\left(I_{OUTi}\right)\left(V_{INi}\right)\left(f\right)$$

where R_{SWi} is the equivalent switch resistance (0.18Ω for channel 1 and 0.22Ω for channels 2 and 3) and f is the operating frequency.

The boost loss in channel i is:

$$P_{BSTi} = \frac{V_{OUTi}\left(V_{BOOSTi}\right)\left(\frac{I_{OUTi}}{50} + 0.02A\right)}{V_{INi}}$$

The quiescent loss is:

$$P_Q = V_{IN1}(I_{Q(VIN1)}) + V_{BIAS}(I_{Q(BIAS)})$$

If the BIAS pin does not have a voltage of at least 3V applied, then V_{IN1} must replace V_{BIAS} in the equation. Also, $I_{Q(VIN1)}$ can be reduced by 0.2mA (typ) if the LDO is shut off (see the LDO section).

The LDO drive loss is:

$$P_{LDO} = (V_{BIAS} - V_{LDO(OUT)} - 0.7V)\left(\frac{I_{OUT(LDO)}}{\beta_{PASS}}\right),$$

if $V_{BIAS} \geq V_{LDO(OUT)} + 1.5V$

or

$$P_{LDO} = (V_{IN1} - V_{LDO(OUT)} - 0.7V)\left(\frac{I_{OUT(LDO)}}{\beta_{PASS}}\right),$$

if $V_{BIAS} < V_{LDO(OUT)} + 1.5V$

where β_{PASS} is the current gain of the external pass transistor.

APPLICATIONS INFORMATION

Next, the power in the external components must be taken into account. The diode power is given by:

$$P_{DIODE} = \frac{V_F\left(V_{IN} - V_{OUT} - V_F\right)I_{OUT}}{V_{IN}}$$

where V_F is the forward drop of the diode at I_{OUT}.

The inductor power is:

$$P_{IND} = (I_{OUT})^2\ ESR_{IND}$$

where ESR_{IND} is the inductor equivalent series resistance.

The LDO pass transistor power is:

$$P_{NPN} = I_{OUTLDO}(V_C - V_{OUTLDO})$$

where V_C is the collector voltage on the NPN pass transistor.

Example: An LT3507 design requirements are:

V_{IN} = 8V, f = 500kHz

V1 = 2.5V at I1 = 1.6A

V2 = 3.3V at I2 = 0.8A (used for boost, bias and V4)

V3 = 1.2V at I3 = 1A

V4 = 3V at I4 = 0.2A (from 3.3V output)

T_A = 50°C, T_{JMAX} = 125°C

θ_{JA} = 34°C/W

Schottky V_F = 0.45V and Inductor ESR = 0.05Ω

$$P_{DISS(MAX)} = \frac{125°C - 50°C}{34°C/W} = 2.2W$$

$$P_{SWDC1} = \frac{0.18\Omega\left(1.6A\right)^2 2.5V}{8V} = 0.14W$$

$$P_{SWAC1} = 17ns\left(1.6A\right)\left(8V\right)\left(500k\right) = 0.11W$$

$$P_{BST1} = \frac{2.5V\left(3.3V\right)\left(\frac{1.6A}{50} + 0.02A\right)}{8V} = 0.06W$$

Similarly, P_{SWDC2} = 0.09W, P_{SWAC2} = 0.07W, P_{BST2} = 0.06W, P_{SWDC3} = 0.03W, P_{SWAC3} = 0.07W and P_{BST2} = 0.03W. Remember, the total current from channel 2 is I2 + I4 since the LDO pass transistor draws from V2. Ignore bias and boost currents.

$$P_Q = 8V\left(3.5mA\right) + 3.3V\left(7.5mA\right) = 0.05W$$

$$P_{LDO} = 8V\left(\frac{0.2A}{100}\right) = 0.02W$$

The total dissipation on the LT3507 is the sum of all these and is equal to 0.73W. Note that this is less than half of $P_{DISS(MAX)}$. Next, the power dissipation of the external components are:

$$P_{DIODE1} = \frac{0.45V\left(8V - 2.5V - 0.45\right)1.6A}{8V} = 0.46W$$

$$P_{IND1} = \left(1.6A\right)^2 0.05\Omega = 0.13W$$

Similarly, P_{DIODE2} = 0.24W, P_{IND2} = 0.05W, P_{DIODE3} = 0.36W and P_{IND3} = 0.05W. And finally:

$$P_{NPN} = 0.2A(3.3V - 3V) = 0.06W$$

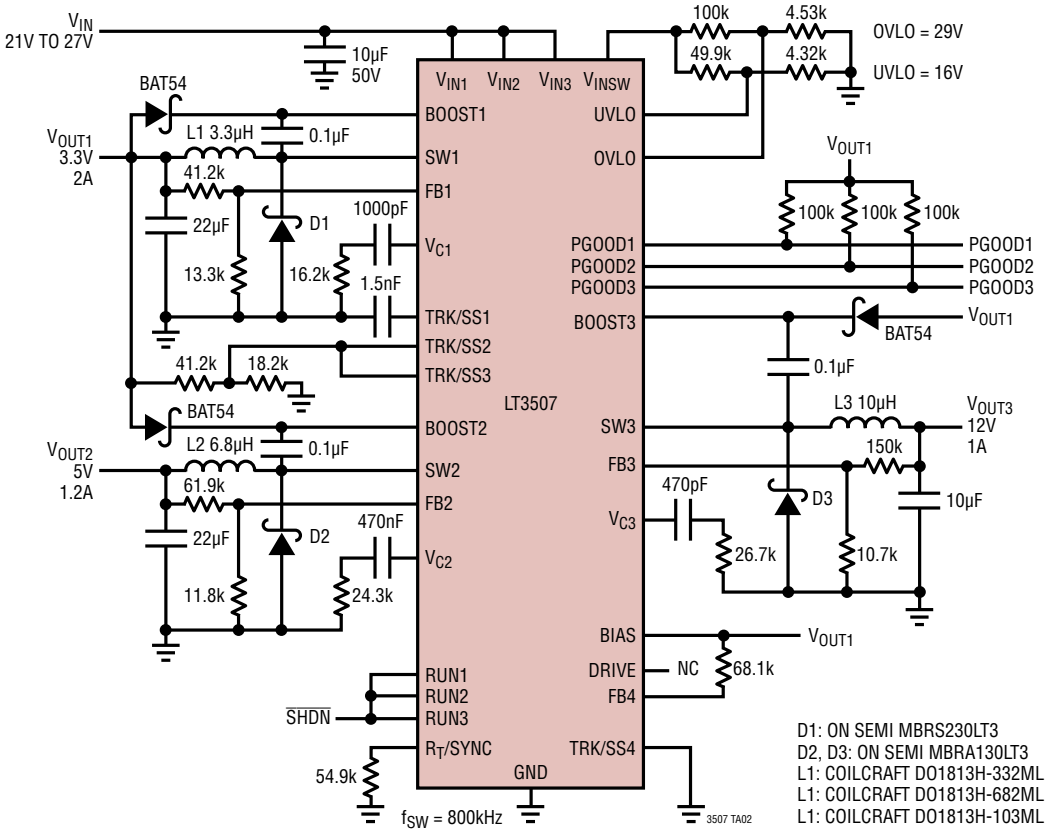
Thus the total power dissipated by the LT3507 and external components is 2.08W. The thermal analysis will use these power dissipations to calculate the internal component temperatures. Make sure that none of the components exceed their rated temperature limits.

RELATED LINEAR TECHNOLOGY PUBLICATIONS

Application Notes 19, 35, 44, 76 and 88 contain more detailed descriptions and design information for buck regulators and other switching regulators. The LT1375 data sheet has a more extensive discussion of output ripple, loop compensation, and stability testing. Design Note 318 shows how to generate a dual polarity output supply using a buck regulator.

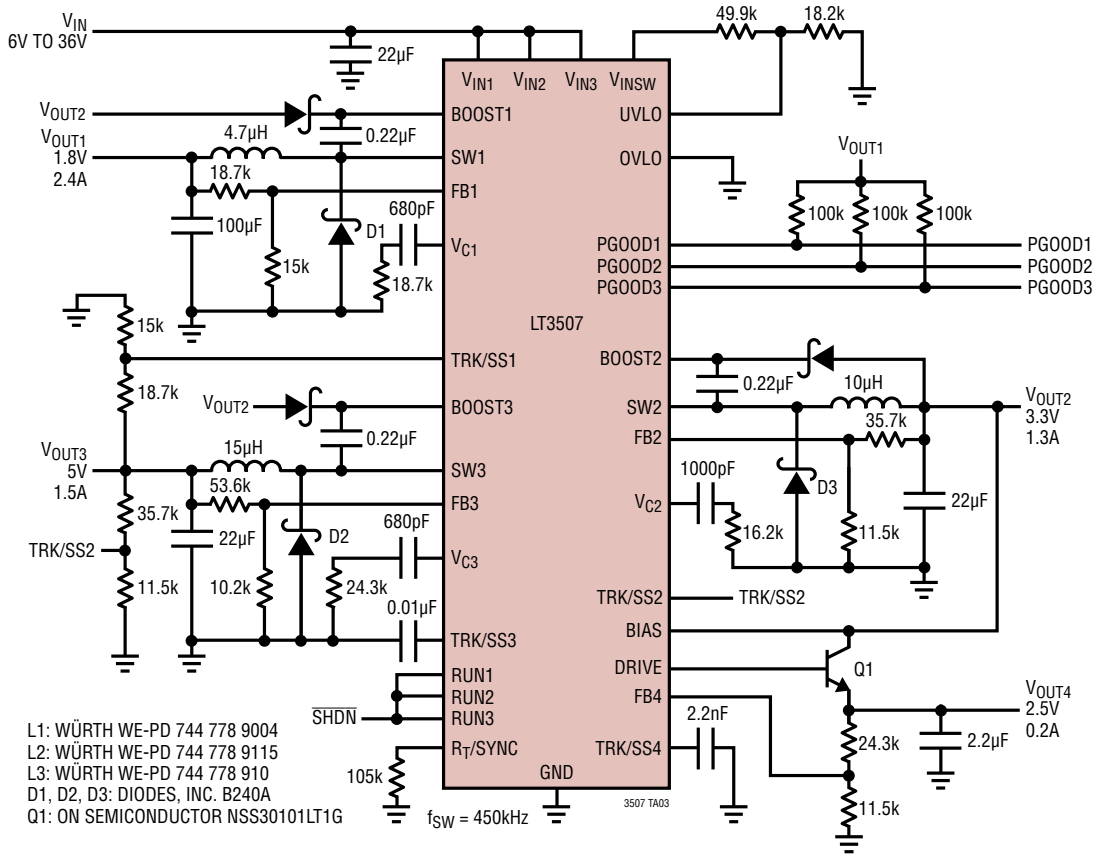
TYPICAL APPLICATIONS

3.3V, 5V and 12V from a 24V Input with Ratiometric Tracking



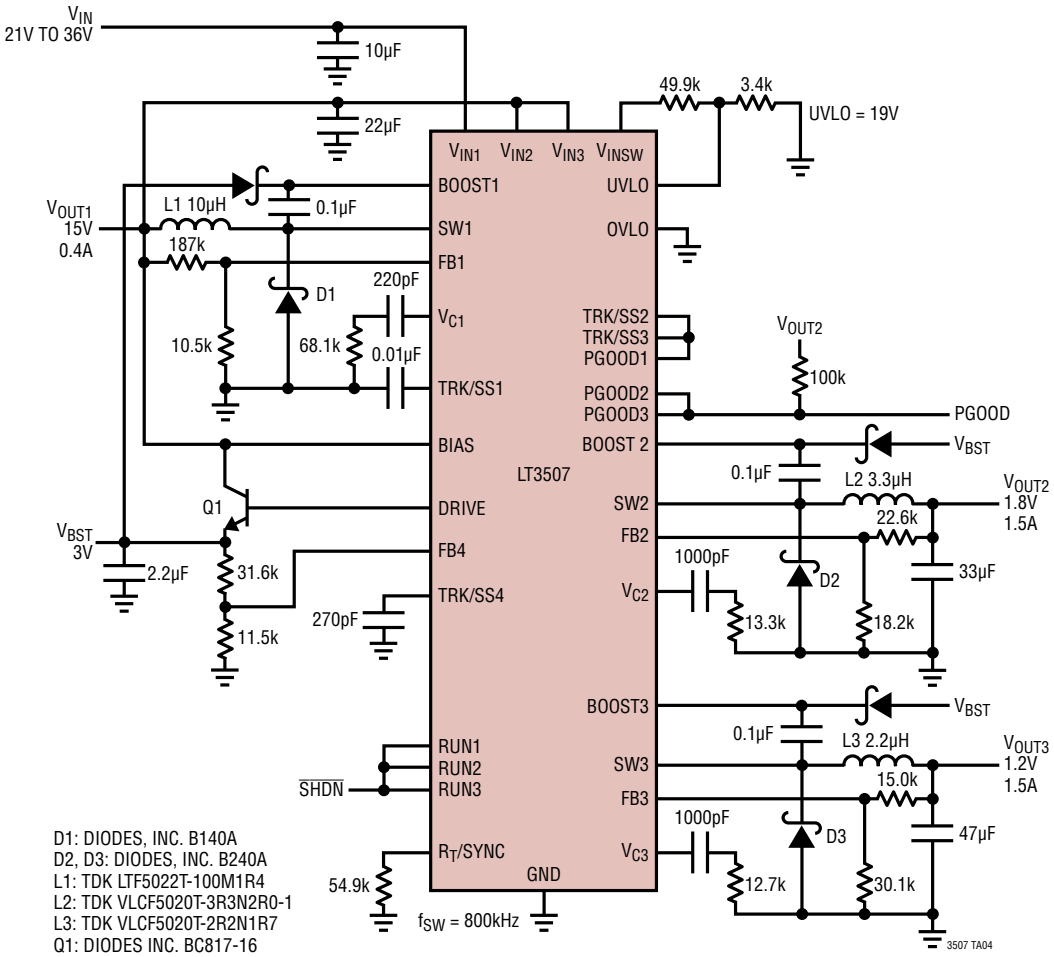
TYPICAL APPLICATIONS

5V, 3.3V, 2.5V and 1.8V with Coincident Tracking



TYPICAL APPLICATIONS

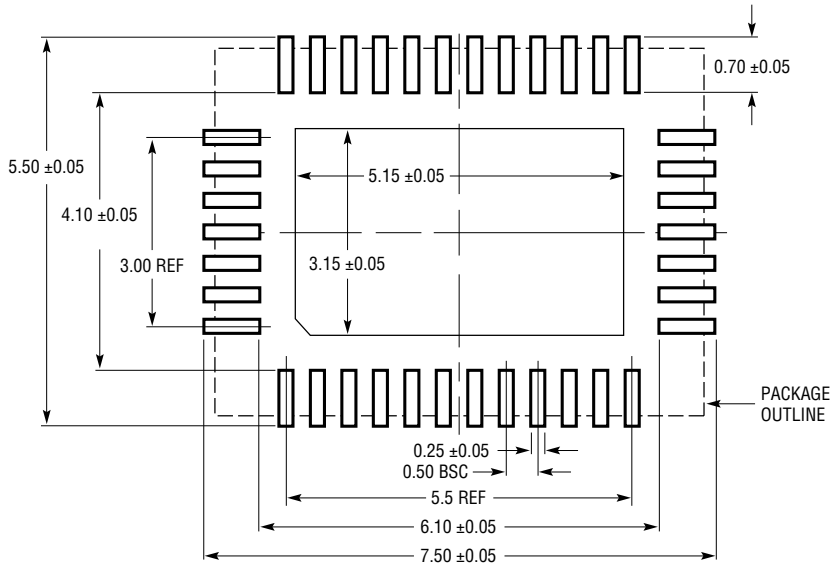
15V, 1.8V and 1.2V 2-Stage Step Down



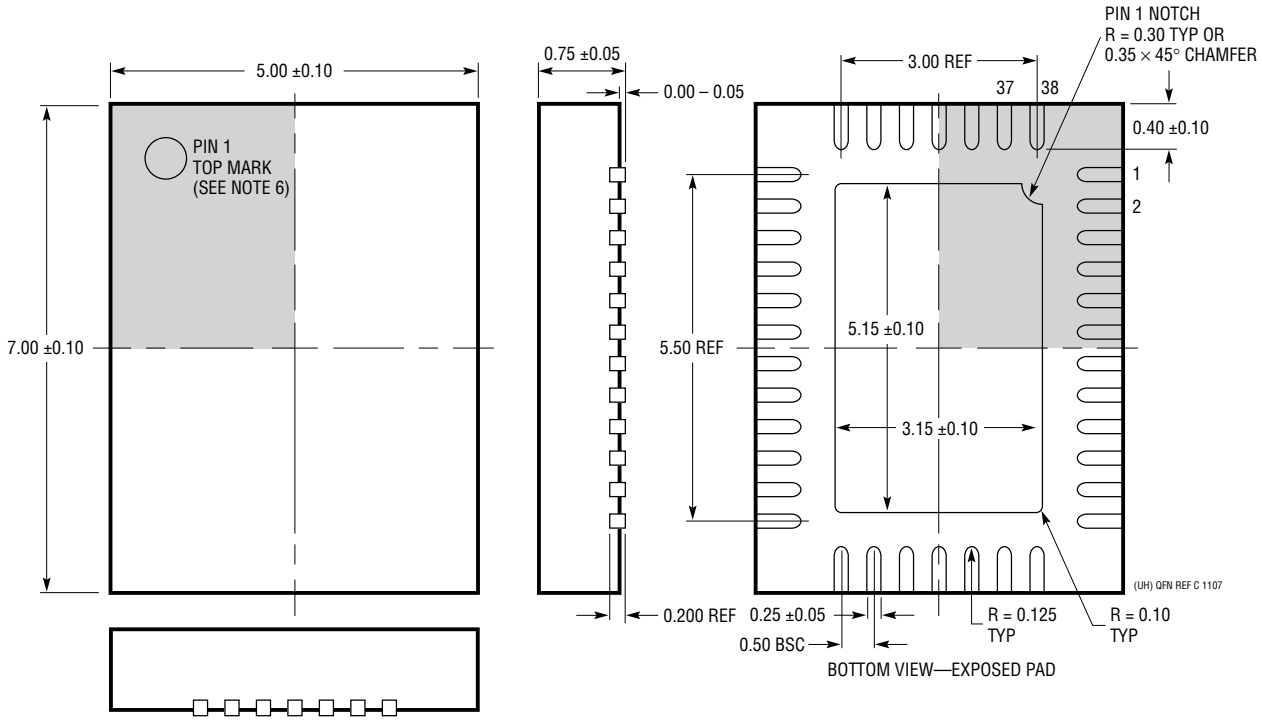
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT3507#packaging for the most recent package drawings.

UHF Package
38-Lead Plastic QFN (5mm × 7mm)
(Reference LTC DWG # 05-08-1701 Rev C)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

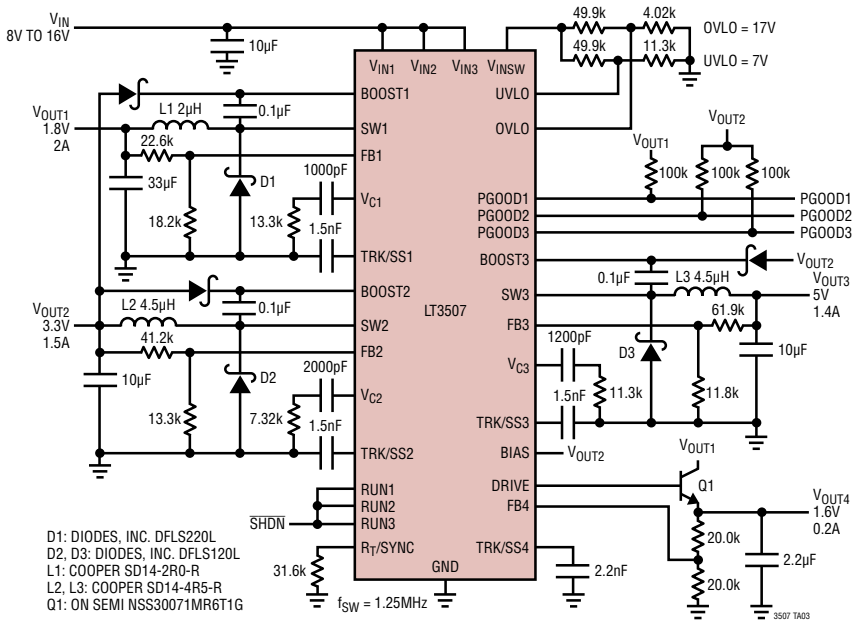
NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	01/16	Added Clarifications to Conditions on Electrical Characteristics.	4
		Added Note 6.	4
		Clarified V_{IN1} Pin Function description.	7
		Clarified PGOOD1, PGOOD2, PGOOD3 Pin Function description, 3.5V becomes 3.8V.	7
		Clarified Operation V_C pin >1V becomes V_C pin >0.9V.	9
		Clarified last paragraph in Operation description.	9
		Clarified first paragraph of Input Voltage Range.	10
		Added clarification in second paragraph of Diode Selection.	13
		Replaced >1.5V with >1.25V in Shutdown description.	17
		Clarified Figure 10.	19
		Clarified Low Dropout Regulator first paragraph.	20
		Clarified Typical Application Schematic.	26
		Clarified Typical Application Schematic.	30

TYPICAL APPLICATIONS

12V to 5V, 3.3V, 1.8V and 1.6V with 1.5mm Maximum Height



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1939	25V, 2A, 2.5MHz High Efficiency DC/DC Converter and LDO Controller	$V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 25V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5mA, I_{SD} < 10µA, 3 × 3 DFN-10 Package
LT1940	Dual 25V, 1.4A (I_{OUT}), 1.1MHz, High Efficiency Step-Down DC/DC Converter	$V_{IN(MIN)}$ = 3.3V, $V_{IN(MAX)}$ = 25V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 3.8mA, I_{SD} < 30µA, TSSOP16E Package
LT3480	36V with Transient Protection to 60V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode® Operation	$V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 38V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 70µA, I_{SD} < 1µA, 3 × 3 DFN-10, MSOP-10E Package
LT3481	34V with Transient Protection to 36V, 2A (I_{OUT}), 2.8MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	$V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 34V, $V_{OUT(MIN)}$ = 1.26V, I_Q = 50µA, I_{SD} < 1µA, 3 × 3 DFN-10, MSOP-10E Package
LT3493	36V, 1.4A (I_{OUT}), 750kHz High Efficiency Step-Down DC/DC Converter	$V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 1.9mA, I_{SD} < 1µA, 2 × 3 DFN-6 Package
LT3500	36V, 40Vmax, 2A, 2.5MHz High Efficiency DC/DC Converter and LDO Controller	$V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5mA, I_{SD} < 10µA, 3 × 3 DFN-10 Package
LT3501/ LT3510	25V, Dual 3A/2A (I_{OUT}), 1.5MHz High Efficiency Step-Down DC/DC Converter	$V_{IN(MIN)}$ = 3.3V, $V_{IN(MAX)}$ = 25V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 3.7mA, I_{SD} = 10µA, TSSOP-20E Package
LT3505	36V with Transient Protection to 40V, 1.4A (I_{OUT}), 3MHz, High Efficiency Step-Down DC/DC Converter	$V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 34V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 2mA, I_{SD} = 2µA, 3 × 3 DFN-8, MSOP-8E Package
LT3506/ LT3506A	25V, Dual 1.6A (I_{OUT}), 575kHz/1.1MHz High Efficiency Step-Down DC/ DC Converter	$V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 25V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 3.8mA, I_{SD} = 30µA, TSSOP-16E, 5 × 4 DFN-16 Package
LT3508	36V with Transient Protection to 40V, Dual 1.4A (I_{OUT}), 3MHz, High Efficiency Step-Down DC/DC Converter	$V_{IN(MIN)}$ = 3.7V, $V_{IN(MAX)}$ = 37V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 4.6mA, I_{SD} = 1µA, 4 × 4 QFN-24, TSSOP-16E Package
LT3684	34V with Transient Protection to 36V, 2A (I_{OUT}), 2.8MHz, High Efficiency Step-Down DC/DC Converter	$V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 34V, $V_{OUT(MIN)}$ = 1.26V, I_Q = 850µA, I_{SD} < 1µA, 3 × 3 DFN-10, MSOP-10E Package
LT3685	36V with Transient Protection to 60V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter	$V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 38V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 70µA, I_{SD} < 1µA, 3 × 3 DFN-10, MSOP-10E Package

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