High Power, Constant Current, Constant Voltage, Step-Down Controller

FEATURES

- **Control Pin Provides Accurate Control of Regulated Output Current**
- **±1.5% Voltage Regulation Accuracy**
- **±6% Current Regulation Accuracy**
- 6V to 36V Input Voltage Range
- Wide Output Voltage Range Up to (V_{IN} – 2V)
- Average Current Mode Control
- <1µA Shutdown Current
- Up to 94% Efficiency
- Additional Pin for Thermal Control of Load Current
- Thermally Enhanced 4mm × 4mm QFN and 20-Pin FE Package

APPLICATIONS

- General Purpose Industrial
- Super-Cap Charging
- Applications Needing Extreme Short-Circuit Protection and/or Accurate Output Current Limit
- Constant Current or Constant Voltage Source

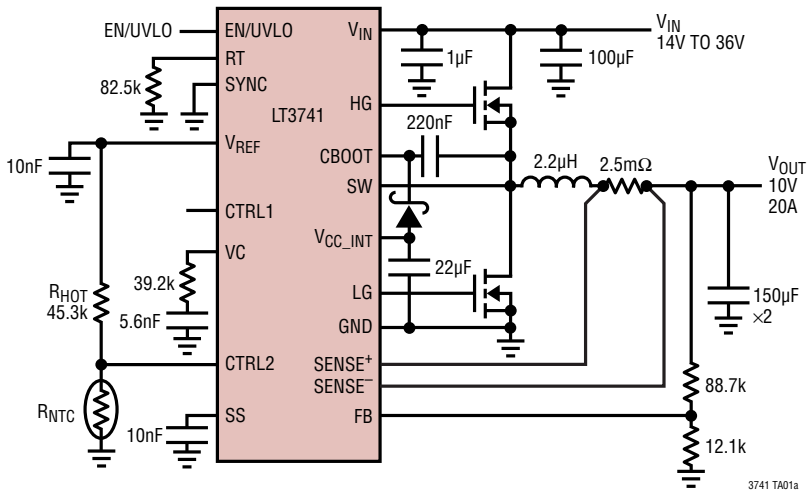
DESCRIPTION

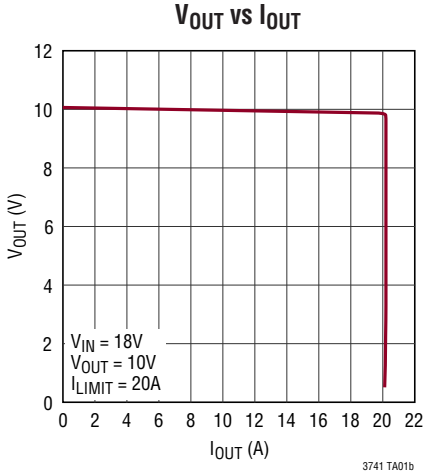
The LT®3741 and LT3741-1 are fixed frequency synchronous step-down DC/DC controllers designed to accurately regulate the output current at up to 20A. The average current-mode controller will maintain inductor current regulation over a wide output voltage range of 0V to (V_{IN} – 2V). The regulated current is set by an analog voltage on the CTRL pins and an external sense resistor. Due to its unique topology, the LT3741 is capable of sourcing and sinking current. If sinking current is not required, or for parallel applications, use the LT3741-1. The regulated voltage and overvoltage protection are set with a voltage divider from the output to the FB pin. Soft-Start is provided to allow a gradual increase in the regulated current during startup. The switching frequency is programmable from 200kHz to 1MHz through an external resistor on the RT pin or through the use of the SYNC pin and an external clock signal.

Additional Features include an accurate external reference voltage for use with the CTRL pins, an accurate UVLO/EN pin that allows for programmable UVLO hysteresis, and thermal shutdown.

TYPICAL APPLICATION

10V/20A Constant Current, Constant Voltage Step-Down Converter

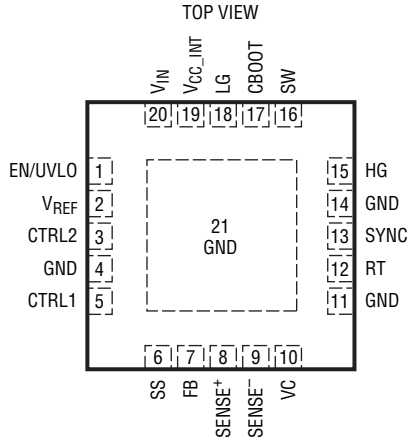




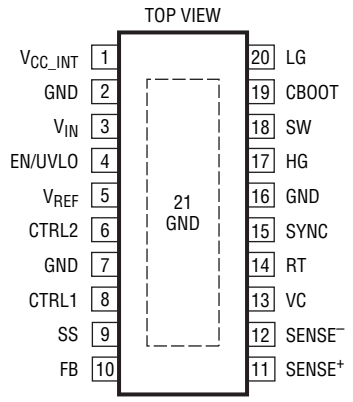
ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN} Voltage 40V
EN/UVLO Voltage 6V
V_{REF} Voltage 3V
CTRL1 and CTRL2 Voltage 3V
$SENSE^+$ Voltage 40V
$SENSE^-$ Voltage 40V
VC Voltage 3V
SW Voltage 40V
CBOOT 46V
RT Voltage 3V
FB Voltage 3V
SS Voltage 6V
V_{CC_INT} Voltage 6V
SYNC Voltage 6V
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
TSSOP ..... 300°C

PIN CONFIGURATION



UF PACKAGE
20-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB



FE PACKAGE
20-LEAD PLASTIC TSSOP
T_{JMAX} = 125°C, θ_{JA} = 38°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION http://www.linear.com/product/LT3741#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3741EUF#PBF	LT3741EUF#TRPBF	3741	20-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C
LT3741IUF#PBF	LT3741IUF#TRPBF	3741	20-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C
LT3741EFE#PBF	LT3741EFE#TRPBF	LT3741FE	20-Lead Plastic TSSOP	–40°C to 125°C
LT3741IFE#PBF	LT3741IFE#TRPBF	LT3741FE	20-Lead Plastic TSSOP	–40°C to 125°C
LT3741EUF-1#PBF	LT3741EUF-1#TRPBF	37411	20-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C
LT3741IUF-1#PBF	LT3741IUF-1#TRPBF	37411	20-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C
LT3741EFE-1#PBF	LT3741EFE-1#TRPBF	LT3741FE-1	20-Lead Plastic TSSOP	–40°C to 125°C
LT3741IFE-1#PBF	LT3741IFE-1#TRPBF	LT3741FE-1	20-Lead Plastic TSSOP	–40°C to 125°C

Consult ADI Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, $V_{EN/UVLO}$ = 5V, V_{SYNC} = 0V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range		●	6		36	V
V_{IN} Pin Quiescent Current (Note 2) Non-Switching Operation Shutdown Mode	 Not Switching $V_{EN/UVLO}$ = 0V, R_T = 40kΩ	 ●		 1.8 0.1	 2.5 1	 mA µA
EN/UVLO Pin Falling Threshold			1.49	1.55	1.61	V
EN/UVLO Hysteresis				130		mV
EN/UVLO Pin Current	V_{IN} = 6V, EN/UVLO = 1.45V			5.5		µA
SYNC Pin Threshold				1		V
CTRL1 Pin Control Range			0		1.5	V
CTRL1 Pin Current	CTRL1 = 1.5V			–100		nA
Reference						
Reference Voltage (V_{REF} Pin)		●	1.94	2	2.06	V
Inductor Current Sensing						
Full Range SENSE+ to SENSE–	V_{CTRL1} = 1.5V	●	48	51	54	mV
SENSE+ Pin Current	V_{SENSE}^+ = 6V			50		nA
SENSE– Pin Current	With V_{OUT} ~ 4V, V_{CTRL1} = 0V, V_{SENSE}^- = 6V			10		µA
Internal V_{CC} Regulator (V_{CC_INT} Pin)						
Regulation Voltage		●	4.7	5	5.2	V
NMOS FET Driver						
Non-Overlap time HG to LG	(Note 3)			100		ns
Non-Overlap time LG to HG	(Note 3)			60		ns
Minimum On-Time LG	(Note 3)			50		ns
Minimum On-Time HG	(Note 3)			80		ns
Minimum Off-Time LG	(Note 3)			65		ns
High Side Driver Switch On-Resistance Gate Pull Up Gate Pull Down	$V_{CBOOT} – V_{SW}$ = 5V			 2.3 1.3		 Ω Ω
Low Side Driver Switch On-Resistance Gate Pull Up Gate Pull Down	V_{CC_INT} = 5V			 2.3 1		 Ω Ω
Switching Frequency						
f_{SW}	R_T = 40kΩ R_T = 200kΩ	●	900 185	1000 200	1070 233	kHz kHz
Soft-Start						
Charging Current				11		µA
Voltage Regulation Amplifier						
Input Bias Current	FB = 1.3V			850		nA
g_m				800		µA/V
Feedback Regulation Voltage	CTRL1 = 1.5V, I_{SENSE}^- = 23µA, V_{SENSE}^+ = 2V	●	1.192	1.21	1.228	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, $V_{EN/UVLO}$ = 5V, V_{SYNC} = 0V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Current Control Loop g_m Amp						
Offset Voltage	V_{CM} =4V	●	–3	0	3	mV
Input Common Mode Range $V_{CM(LOW)}$ $V_{CM(HIGH)}$	 $V_{CM(HIGH)}$ Measured from V_{IN} to V_{CM}			 0 2		 V V
Output Impedance				3.5		MΩ
g_m			375	475	625	µA/V
Differential Gain				1.7		V/mV

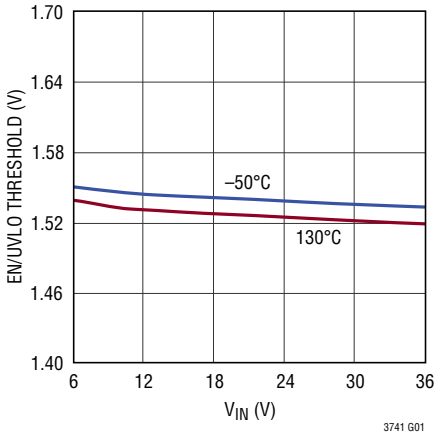
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3741E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3741I is guaranteed to meet performance specifications over the –40°C to 125°C operating junction temperature range.

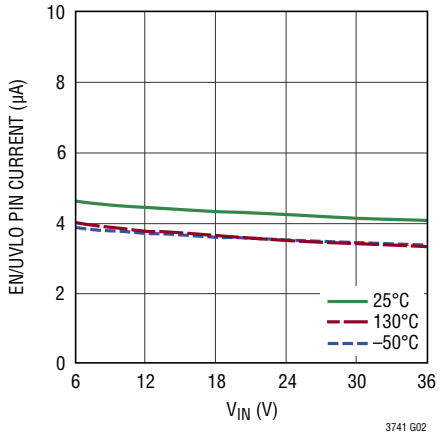
Note 3: The minimum on, off, and nonoverlap times are guaranteed by design and are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

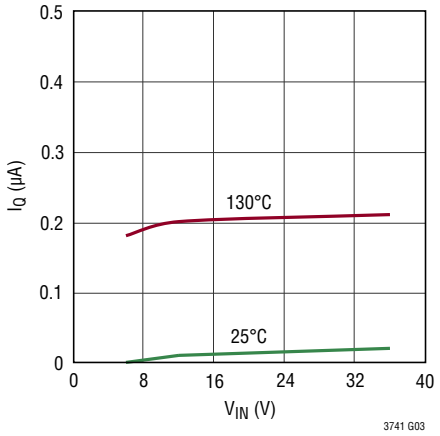
EN/UVLO Threshold (Falling)



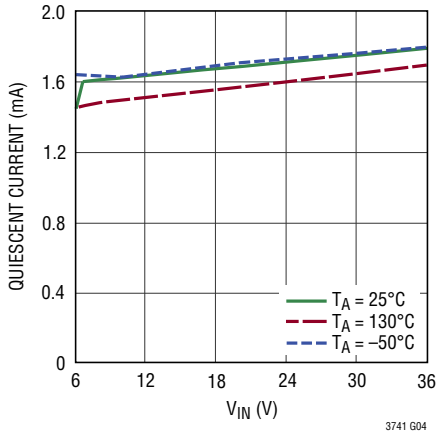
EN/UVLO Pin Current



I_Q in Shutdown

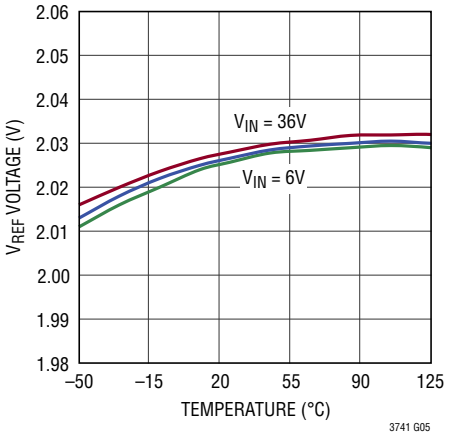


Quiescent Current (Non-Switching)

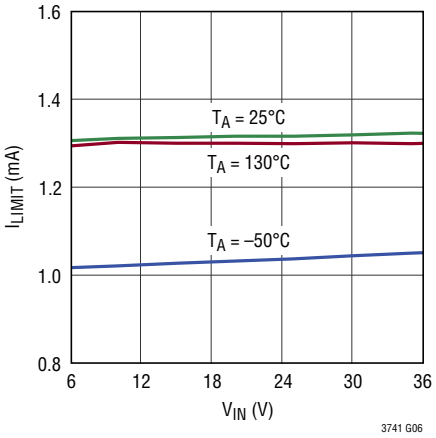


TYPICAL PERFORMANCE CHARACTERISTICS

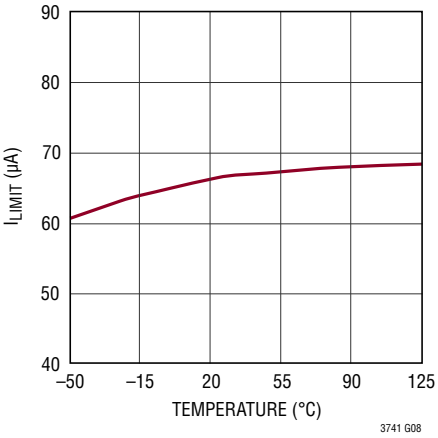
V_{REF} Pin Voltage



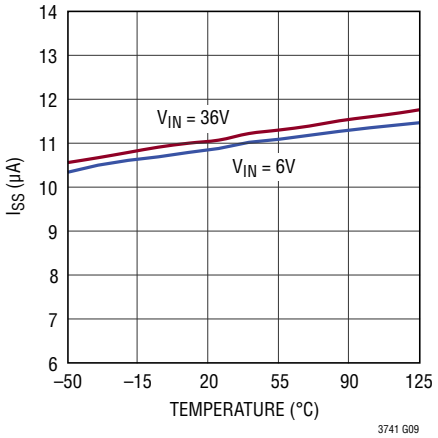
V_{REF} Current Limit



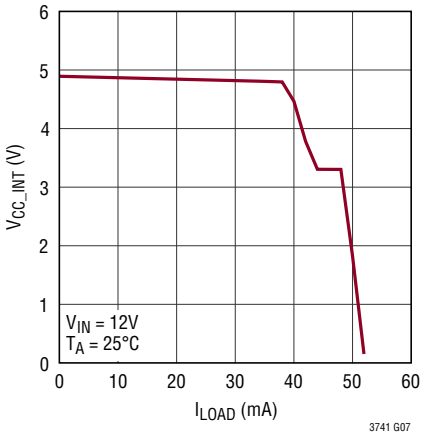
RT Pin Current Limit



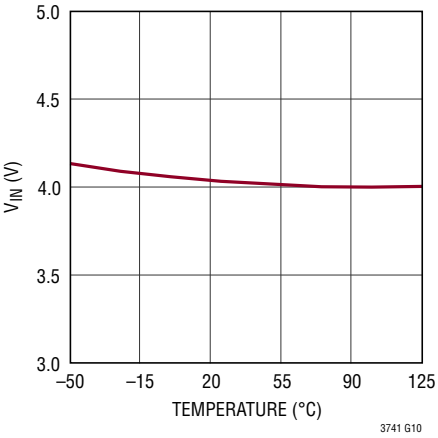
Soft-Start Pin Current



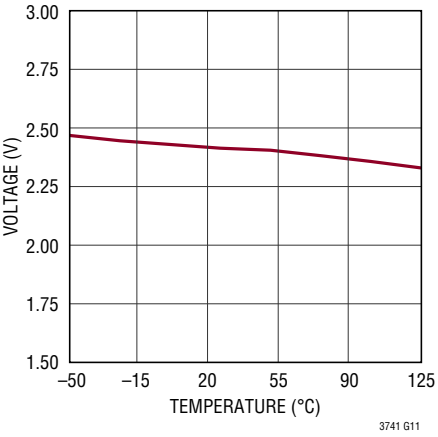
V_{CC_INT} Current Limit



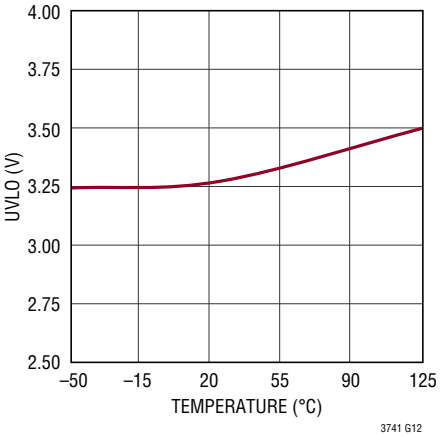
Internal UVLO



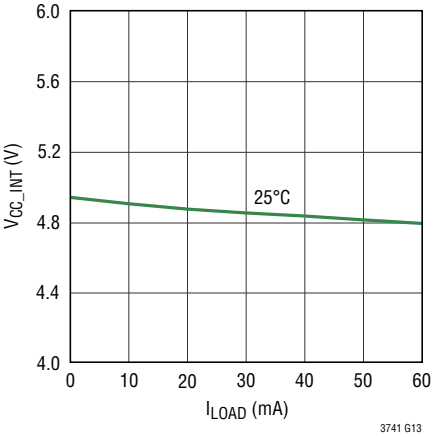
CBOOT-SW UVLO Voltage



V_{CC_INT} UVLO

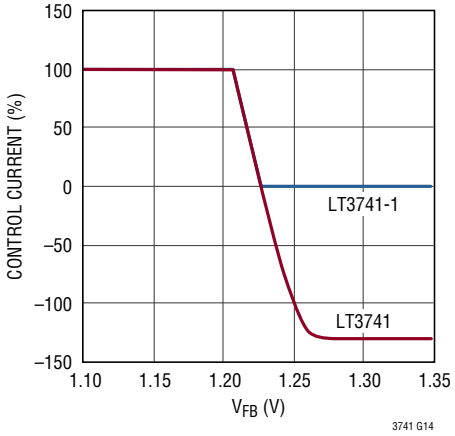


V_{CC_INT} Load Reg at 12V

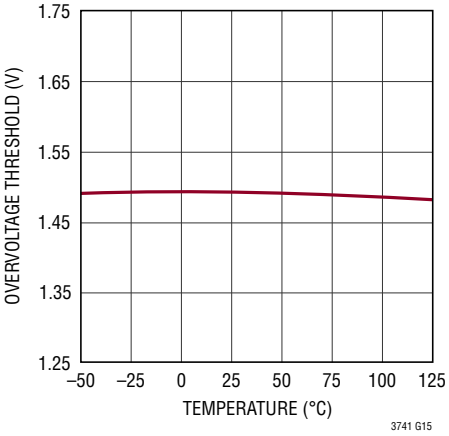


TYPICAL PERFORMANCE CHARACTERISTICS

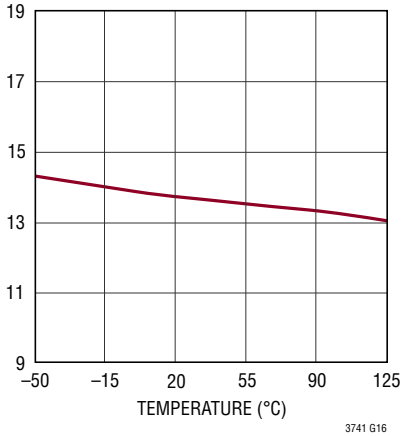
Regulated Current vs V_{FB}



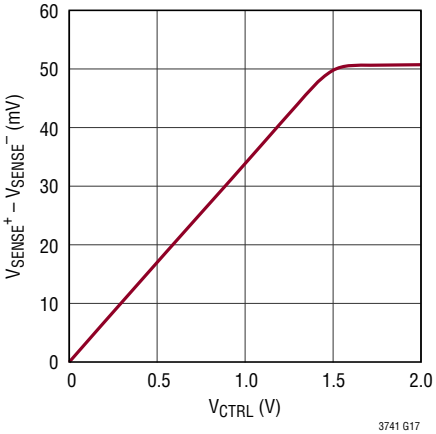
Overvoltage Threshold



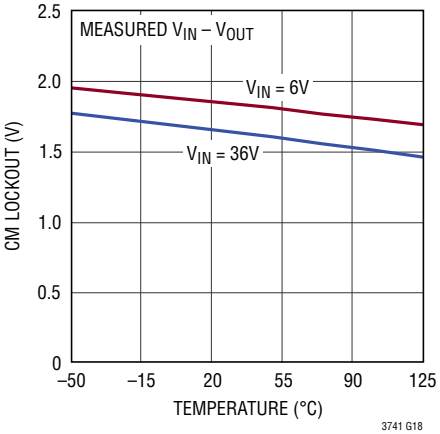
Overvoltage Timeout



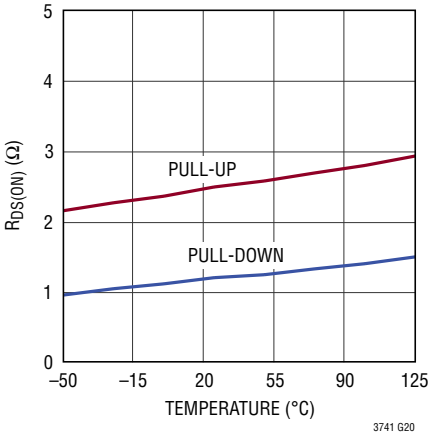
Regulated Sense Voltage



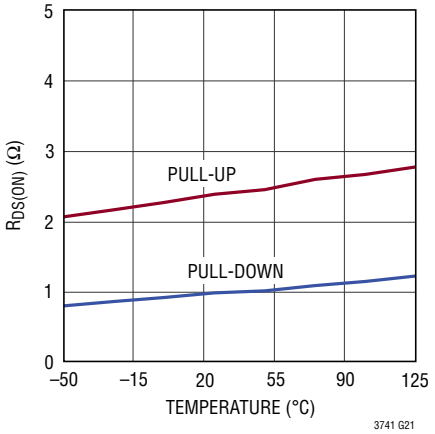
Common Mode Lockout



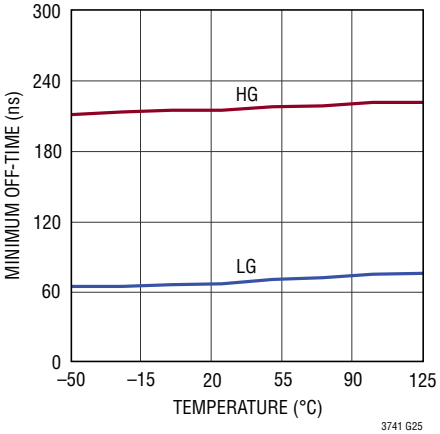
HG Driver $R_{DS(ON)}$



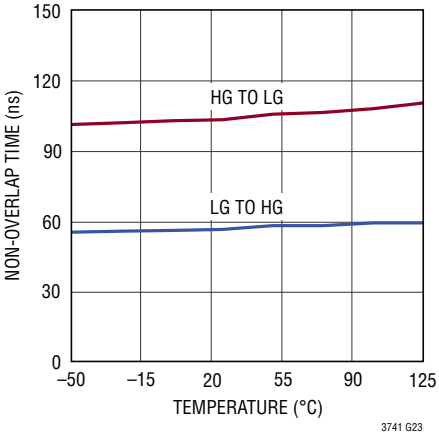
LG Driver $R_{DS(ON)}$



Minimum Off-Time

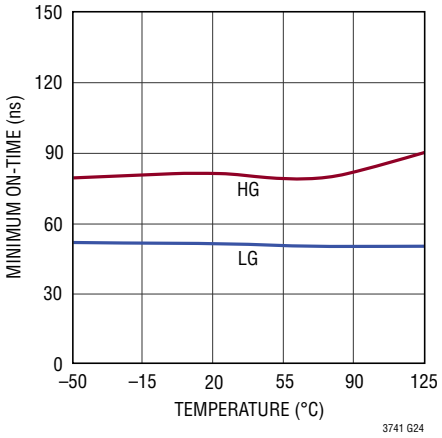


Non-Overlap Time

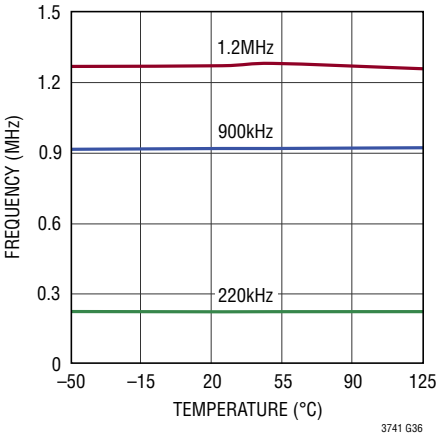


TYPICAL PERFORMANCE CHARACTERISTICS

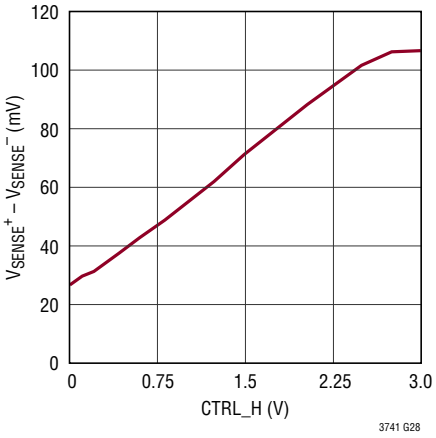
Minimum On-Time



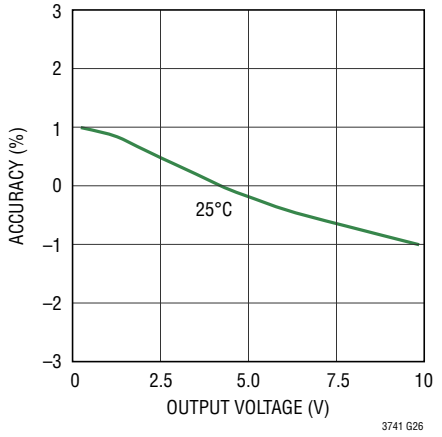
Oscillator Frequency



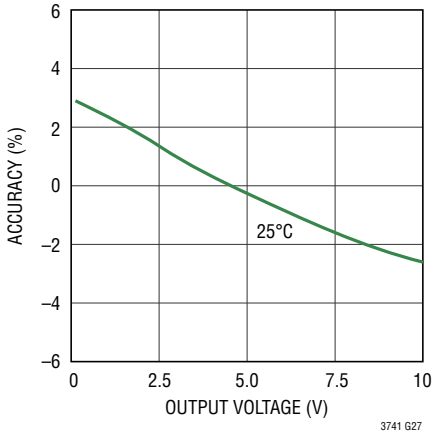
Overcurrent Threshold



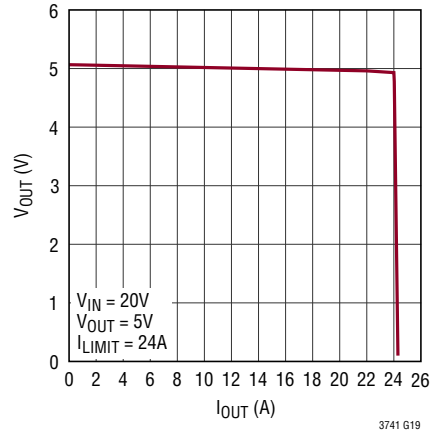
Current Regulation Accuracy
CTRL1 = 1.5V, V_{IN} = 12V



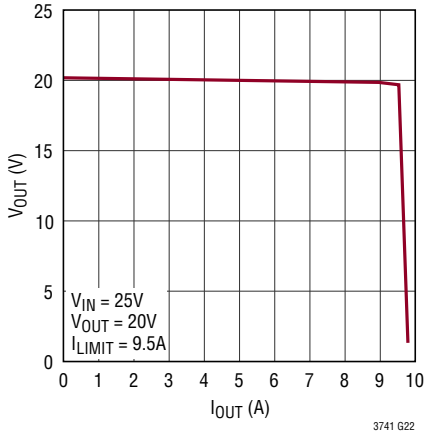
Current Regulation Accuracy
CTRL1 = 0.75V, V_{IN} = 12V



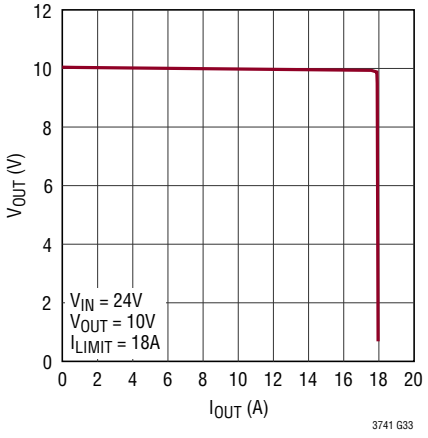
V_{OUT} vs I_{OUT}



V_{OUT} vs I_{OUT}

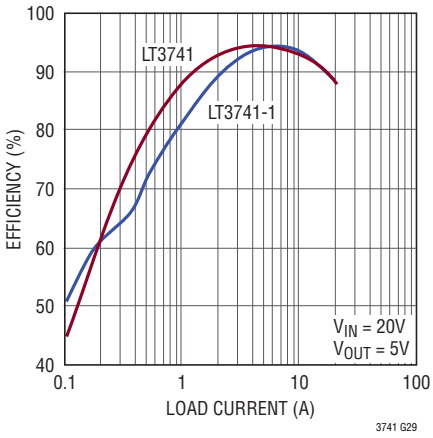


V_{OUT} vs I_{OUT}

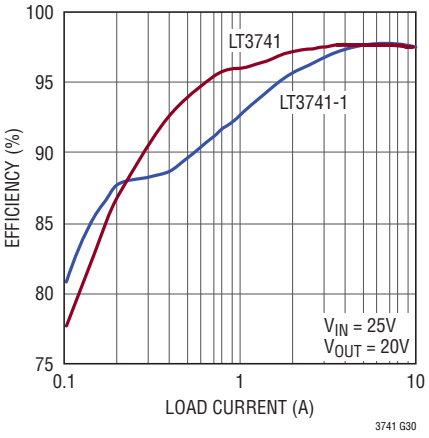


TYPICAL PERFORMANCE CHARACTERISTICS

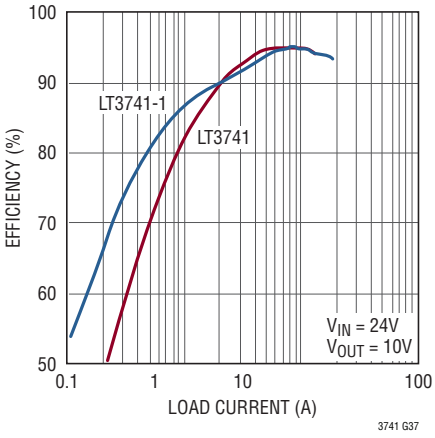
Efficiency and Power Loss vs Load Current



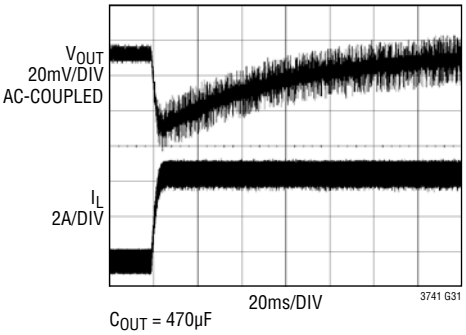
Efficiency and Power Loss vs Load Current



Efficiency and Power Loss vs Load Current

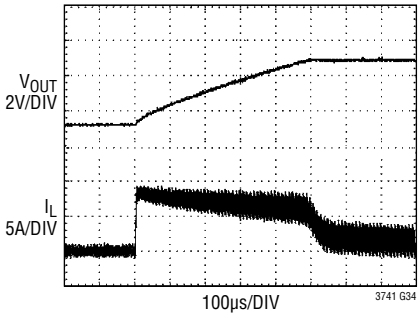


5A Load Step Recovery

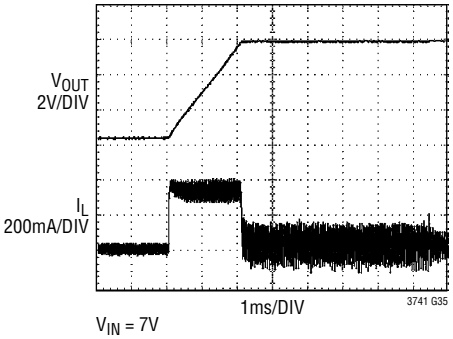


COUT = 470µF

Voltage Regulation with 10A Regulated Inductor Current

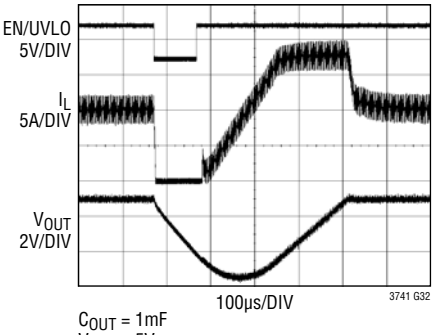


Common Mode Lockout — LT3741



VIN = 7V

Shutdown and Recovery 1.5nF Soft-Start Capacitor



COUT = 1mF
VOUT = 5V
10A LOAD
18A CURRENT LIMIT

PIN FUNCTIONS (QFN/TSSOP)

EN/UVLO (Pin 1/Pin 4): Enable Pin. The EN/UVLO pin acts as an enable pin and turns on the internal current bias core and subregulators at 1.55V. The pin does not have any pull-up or pull-down, requiring a voltage bias for normal part operation. Full shutdown occurs at approximately 0.5V.

V_{REF} (Pin 2/Pin 5): Buffered 2V reference capable of 0.5mA drive.

CTRL2 (Pin 3/Pin 6): Thermal control input used to reduce the regulated current level.

GND (Pins 4,11,14, Exposed Pad Pin 21/Pins 2,7,16, Exposed Pad Pin 21): Ground. The exposed pad must be soldered to the PCB

CTRL1 (Pin 5/Pin 8): The CTRL1 pin sets the high level regulated output current and overcurrent. The maximum input voltage is internally clamped to 1.5V. The overcurrent set point is equal to the high level regulated current level set by the CTRL1 pin with an additional 23mV offset between the $SENSE^+$ and $SENSE^-$ pins.

SS (Pin 6/Pin 9): The Soft-Start Pin. Place an external capacitor to ground to limit the regulated current during start-up conditions. The soft-start pin has a 11µA charging current. This pin controls regulated output current determined by CTRL1.

FB (Pin 7/Pin 10): Feedback Pin for Voltage Regulation and Overvoltage Protection. The feedback voltage is 1.21V. Overvoltage is also sensed through the FB pin. When the feedback voltage exceeds 1.5V, the overvoltage lockout prevents switching for 13µs to allow the inductor current to discharge.

$SENSE^+$ (Pin 8/Pin 11): $SENSE^+$ is the inverting input of the average current mode loop error amplifier. This pin is connected to the external current sense resistor, R_S. The voltage drop between $SENSE^+$ and $SENSE^-$ referenced to the voltage drop across an internal resistor produces the input voltages to the current regulation loop.

$SENSE^-$ (Pin 9/Pin 12): $SENSE^-$ is the non-inverting input of the average current mode loop error amplifier. The reference current, based on CTRL1 or CTRL2 flows out of the pin to the output side of the sense resistor, R_S.

VC (Pin 10/Pin 13): VC provides the necessary compensation for the average current loop stability. Typical compensation values are 20k to 50k for the resistor and 2nF to 5nF for the capacitor.

RT (Pin 12/Pin 14): A resistor to ground sets the switching frequency between 200kHz and 1MHz. When using the SYNC function, set the frequency to be 20% lower than the SYNC pulse frequency. This pin is current limited to 60µA. Do not leave this pin open.

SYNC (Pin 13/Pin 15): Frequency Synchronization Pin. This pin allows the switching frequency to be synchronized to an external clock. The R_T resistor should be chosen to operate the internal clock at 20% slower than the SYNC pulse frequency. This pin should be grounded when not in use. When laying out board, avoid noise coupling to or from SYNC trace.

HG (Pin 15/Pin 17): HG is the top-FET gate drive signal that controls the state of the high-side external power FET. The driver pull-up impedance is 2.3Ω and pull-down impedance is 1.3Ω.

SW (Pin 16/Pin 18): The SW pin is used internally as the lower-rail for the floating high-side driver. Externally, this node connects the two power-FETs and the inductor.

CBOOT (Pin 17/Pin 19): The CBOOT pin provides a floating 5V regulated supply for the high-side FET driver. An external Schottky diode is required from the V_{CC_INT} pin to the CBOOT pin to charge the CBOOT capacitor when the switch-pin is near ground.

LG (Pin 18/Pin 20): LG is the bottom-FET gate drive signal that controls the state of the low-side external power-FET. The driver pull-up impedance is 2.3Ω and pull-down impedance is 1.0Ω.

V_{CC_INT} (Pin 19/Pin 1): A regulated 5V output for charging the CBOOT capacitor. V_{CC_INT} also provides the power for the digital and switching subcircuits. Below 6V V_{IN}, tie this pin to the rail. V_{CC_INT} is current limited to 50mA. Shutdown operation disables the output voltage drive.

V_{IN} (Pin 20/Pin 3): Input Supply Pin. Must be locally bypassed with a 4.7µF low-ESR capacitor to ground.

BLOCK DIAGRAM (QFN Package)

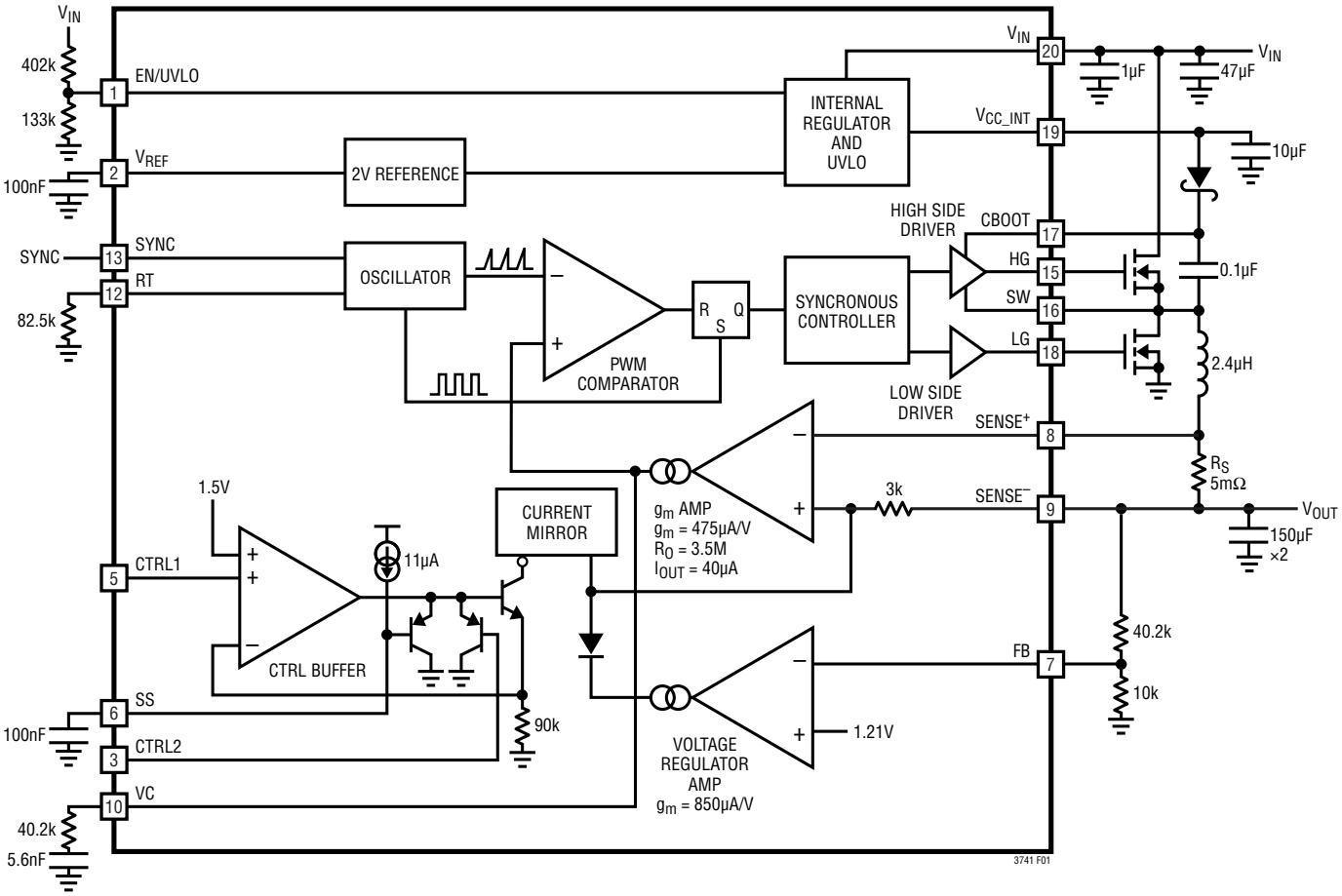


Figure 1. Block Diagram, LT3741

BLOCK DIAGRAM (QFN Package)

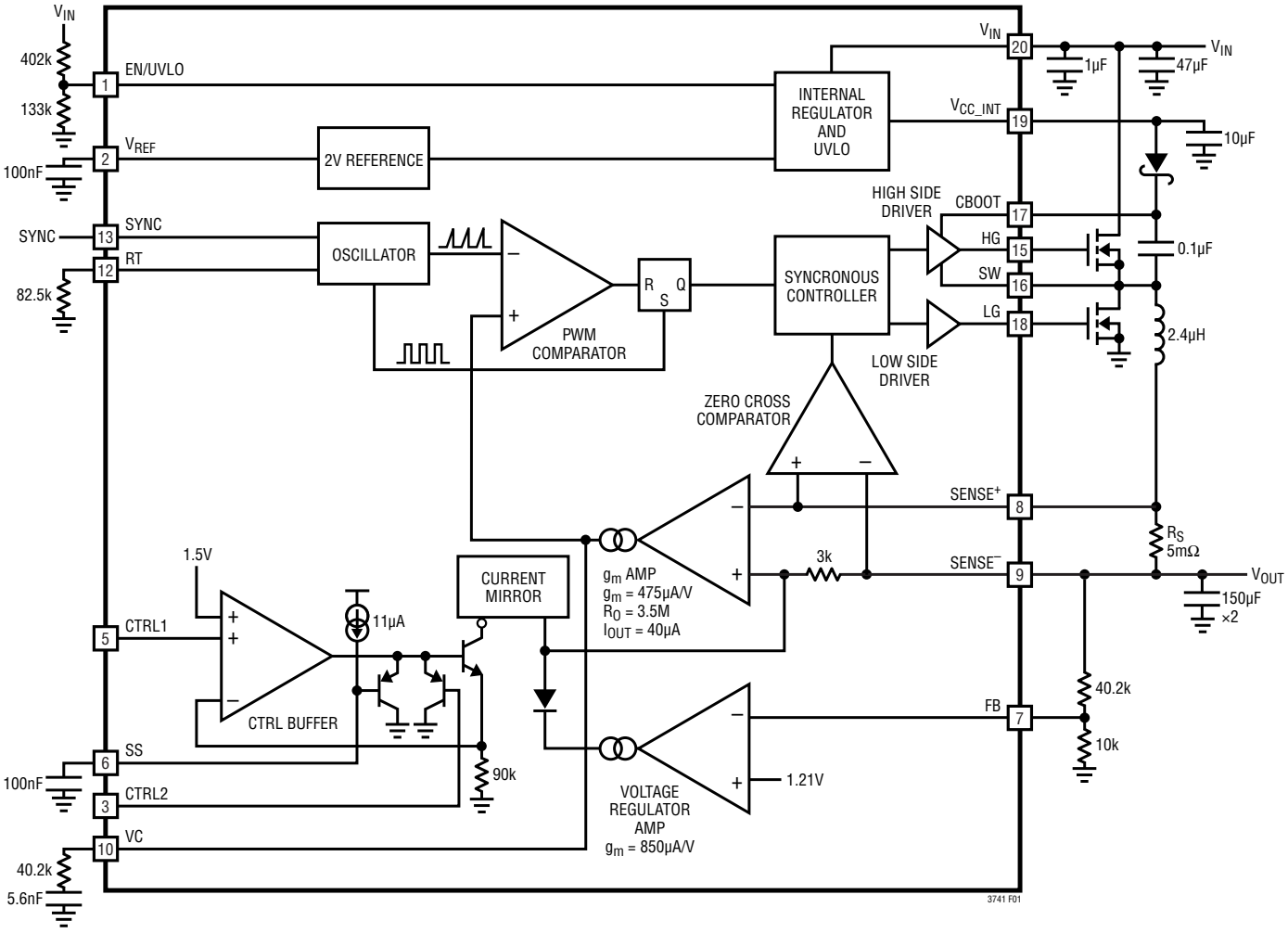


Figure 2. Block Diagram, LT3741-1

OPERATION

The LT3741 utilizes fixed-frequency, average current mode control to accurately regulate the inductor current, independently from the output voltage. This is an ideal solution for applications requiring a regulated current source. The control loop will regulate the current in the inductor at an accuracy of ±6%. Once the output has reached the regulation voltage determined by the resistor divider from the output to the FB pin and ground, the inductor current will be reduced by the voltage regulation loop. In voltage regulation, the output voltage has an accuracy of ±1.5%. For additional operation information, refer to the Block Diagram in Figure 1.

The current control loop has two reference inputs, determined by the voltage at the analog control pins, CTRL1 and CTRL2. The lower of the two analog voltages on CTRL1 and CTRL2 determines the regulated output current. The analog voltage at the CTRL1 pin is buffered and produces a reference voltage across an internal resistor. The internal buffer has a 1.5V clamp on the output, limiting the analog control range of the CTRL1 and CTRL2 pins from 0V to 1.5V – corresponding to a 0mV to 51mV range on the sense resistor, R_S. The average current-mode control loop uses the internal reference voltage to regulate the inductor current, as a voltage drop across the external sense resistor, R_S.

A 2V reference voltage is provided on the V_{REF} pin to allow the use of a resistor voltage divider to the CTRL1 and CTRL2 pins. The V_{REF} pin can supply up to 500µA and is current limited to 1mA.

The error amplifier for the average current-mode control loop has a common mode lockout that regulates the inductor current so that the error amplifier is never operated out of the common mode range. The common mode range is from 0V to 2V below the V_{IN} supply rail.

The overcurrent set point is equal to the regulated current level set by the CTRL1 pin with an additional 23mV offset between the $SENSE^+$ and $SENSE^-$ pins. The overcurrent is limited on a cycle-by-cycle basis; shutting switching down once the overcurrent level is reached. Overcurrent is not soft-started.

The regulated output voltage is set with a resistor divider from the output back to the FB pin. The reference at the FB pin is 1.21V. If the output voltage level is high enough to engage the voltage loop, the regulated inductor current will be reduced to support the load at the output. If the voltage at the FB pin reaches 1.5V (~25% higher than the regulation level), an internal overvoltage flag is set, shutting down switching for 13µs.

The EN/UVLO pin functions as a precision shutdown pin. When the voltage at the EN/UVLO pin is lower than 1.55V, the internal reset flag is asserted and switching is terminated. Full shutdown occurs at approximately 0.5V with a quiescent current of less than 1µA in full shutdown. The EN/UVLO pin has 130mV of built-in hysteresis. In addition, a 5.5µA current source is connected to this pin that allows any amount of hysteresis to be added with a series resistor or resistor divider from V_{IN}.

During startup, the SS pin is held low until the internal reset goes low. Once reset goes low, the capacitor at the soft-start pin is charged with an 11µA current source. The internal buffers for the CTRL1 and CTRL2 signals are limited by the voltage at the soft-start pin, slowly ramping the regulated inductor current to the current determined by the voltage at the CTRL1 or CTRL2 pins.

The thermal shutdown is set at 163°C with 8°C hysteresis. During thermal shutdown, all switching is terminated and the part is in reset (forcing the SS pin low).

The switching frequency is determined by a resistor at the RT pin. The RT pin is also limited to 60µA, while not recommended, this limits the switching frequency to 2MHz when the RT pin is shorted to ground. The LT3741 may also be synchronized to an external clock through the use of the SYNC pin.

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Programming Inductor Current

The analog voltage at the CTRL1 pin is buffered and produces a reference voltage, V_{CTRL}, across an internal resistor. The regulated average inductor current is determined by:

$$I_O = \frac{V_{CTRL1}}{30 \bullet R_S}$$

where R_S is the external sense resistor and I_O is the average inductor current, which is equal to the output current. Figure 2 shows the maximum output current vs R_S. The maximum power dissipation in the resistor will be:

$$P_{RS} = \frac{(0.05V)^2}{R_S}$$

Table 1 contains several resistors values, the corresponding maximum current and power dissipation in the sense resistor. Susumu, Panasonic and Vishay offer accurate sense resistors. Figure 3 shows the power dissipation in R_S.

Table 1. Sense Resistor Values

MAXIMUM OUTPUT CURRENT (A)	RESISTOR, R_S (mΩ)	POWER DISSIPATION (W)
1	50	0.05
5	10	0.25
10	5	0.5
25	2	1.25

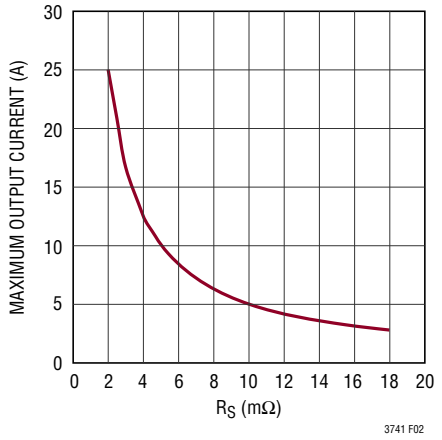

Figure 2. R_S Value Selection for Regulated Output Current

Inductor Selection

Size the inductor to have approximately 30% peak-to-peak ripple. The overcurrent set point is equal to the high level regulated current level set by the CTRL1 pin with an additional 23mV offset between the SENSE+ and SENSE– pins. The saturation current for the inductor should be at least 20% higher than the maximum regulated current. The following equation sizes the inductor for best performance:

$$L = \left(\frac{V_{IN} \bullet V_O - V_O^2}{0.3 \bullet f_S \bullet I_O \bullet V_{IN}} \right)$$

where V_O is the output voltage, I_O is the maximum regulated current in the inductor and f_S is the switching frequency. Using this equation, the inductor will have approximately 15% ripple at maximum regulated current.

Table 2. Recommended Inductor Manufacturers

VENDOR	WEBSITE
Coilcraft	www.coilcraft.com
Sumida	www.sumida.com
Vishay	www.vishay.com
Wurth Electronics	www.we-online.com
NEC-Tokin	www.nec-tokin.com

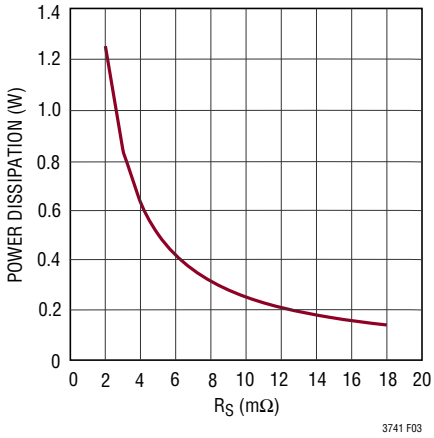

Figure 3. Power Dissipation in R_S

Switching MOSFET Selection

When selecting switching MOSFETs, the following parameters are critical in determining the best devices for a given application: total gate charge (Q_G), on-resistance

APPLICATIONS INFORMATION

($R_{DS(ON)}$), gate to drain charge (Q_{GD}), gate-to-source charge (Q_{GS}), gate resistance (R_G), breakdown voltages (maximum V_{GS} and V_{DS}) and drain current (maximum I_D). The following guidelines provide information to make the selection process easier.

Both of the switching MOSFETs need to have their maximum rated drain currents greater than the maximum inductor current. The following equation calculates the peak inductor current:

$$I_{MAX} = I_O + \left(\frac{V_{IN} \bullet V_O - V_O^2}{2 \bullet f_S \bullet L \bullet V_{IN}} \right)$$

where V_{IN} is the input voltage, L is the inductance value, V_O is the output voltage, I_O is the regulated output current and f_S is the switching frequency. During MOSFET selection, notice that the maximum drain current is temperature dependant. Most data sheets include a table or graph of the maximum rated drain current vs temperature.

The maximum V_{DS} should be selected to be higher than the maximum input supply voltage (including transient) for both MOSFETs. The signals driving the gates of the switching MOSFETs have a maximum voltage of 5V with respect to the source. During start-up and recovery conditions, the gate drive signals may be as low as 3V. To ensure that the LT3741 recovers properly, the maximum threshold should be less than 2V. For a robust design, select the maximum V_{GS} greater than 7V.

Power losses in the switching MOSFETs are related to the on-resistance, $R_{DS(ON)}$; the transitional loss related to the gate resistance, R_G; gate-to-drain capacitance, Q_{GD} and gate-to-source capacitance, Q_{GS}. Power loss to the on-resistance is an Ohmic loss, $I^2 R_{DS(ON)}$, and usually dominates for input voltages less than ~15V. Power losses to the gate capacitance dominate for voltages greater than ~12V. When operating at higher input voltages, efficiency can be optimized by selecting a high side MOSFET with higher $R_{DS(ON)}$ and lower C_{GD}. The power loss in the high side MOSFET can be approximated by:

P_{LOSS} = (ohmic loss) + (transition loss)

$$P_{LOSS} \approx \left(\frac{(V_O)}{V_{IN}} \bullet I_O^2 R_{DS(ON)} \bullet \rho_T \right) +$$

$$\left(\left(\frac{V_{IN} \bullet I_{OUT}}{5V} \right) \bullet \left((Q_{GD} + Q_{GS}) \bullet (2 \bullet R_G + R_{PU} + R_{PD}) \right) \bullet f_S \right)$$

where ρ_T is a temperature-dependant term of the MOSFET's on-resistance. Using 70°C as the maximum ambient operating temperature, ρ_T is roughly equal to 1.3. R_{PD} and R_{PU} are the LT3741 high side gate driver output impedance, 1.3Ω and 2.3Ω respectively.

A good approach to MOSFET sizing is to select a high side MOSFET, then select the low side MOSFET. The trade-off between $R_{DS(ON)}$, Q_G, Q_{GD} and Q_{GS} for the high side MOSFET is shown in the following example. V_O is equal to 4V. Comparing two N-channel MOSFETs, with a rated V_{DS} of 40V and in the same package, but with 8× different $R_{DS(ON)}$ and 4.5× different Q_G and Q_{GD}:

M1: $R_{DS(ON)}$ = 2.3mΩ, Q_G = 45.5nC,
Q_{GS} = 13.8nC, Q_{GD} = 14.4nC, R_G = 1Ω

M2: $R_{DS(ON)}$ = 18mΩ, Q_G = 10nC,
Q_{GS} = 4.5nC, Q_{GD} = 3.1nC, R_G = 3.5Ω

Power loss for both MOSFETs is shown in Figure 4. Observe that while the $R_{DS(ON)}$ of M1 is eight times lower, the power loss at low input voltages is equal, but four times higher at high input voltages than the power loss for M2.

Power loss within the low side MOSFET is almost entirely from the $R_{DS(ON)}$ of the FET. Select a low side FET with the lowest $R_{DS(ON)}$ while keeping the total gate charge Q_G to 30nC or less.

Another power loss related to switching MOSFET selection is the power lost to driving the gates. The total gate charge, Q_G, must be charged and discharged each switching cycle. The power is lost to the internal LDO within the LT3741. The power lost to the charging of the gates is:

$$P_{LOSS\_LDO} \approx (V_{IN} - 5V) \bullet (Q_{GLG} + Q_{GHG}) \bullet f_S$$

where Q_{GLG} is the low side gate charge and Q_{GHG} is the high side gate charge.

Whenever possible, utilize a switching MOSFET that minimizes the total gate charge to limit the internal power dissipation of the LT3741.

APPLICATIONS INFORMATION

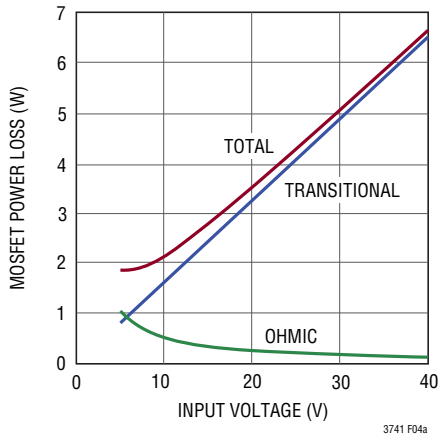

Figure 4a. Power Loss Example for M1

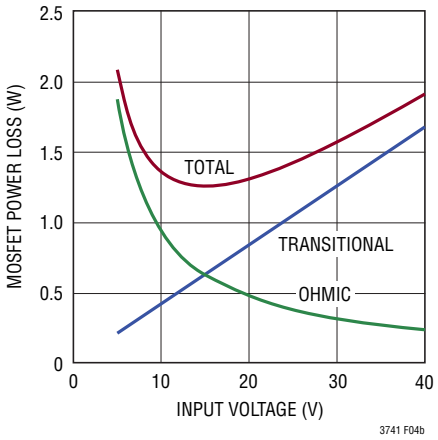

Figure 4b. Power Loss Example for M2

Figure 4

Table 3. Recommended Switching FETs

V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)	TOP FET	BOTTOM FET	MANUFACTURER
8	4	5-10	RJK0365DPA	RJK0330DPB	Renesas www.renesas.com
24	4	5	RJK0368DPA	RJK0332DPB	
24	2-4	20	RJK0365DPA	RJK0346DPA	
12	2-4	10	FDMS8680	FDMS8672AS	Fairchild www.fairchildsemi.com
36	4	20	Si7884BDP	SiR470DP	Vishay www.vishay.com
24	4	40	PSMN4R0-30YL	RJK0346DPA	NXP/Philips www.nxp.com

Input Capacitor Selection

The input capacitor should be sized at 4µF for every 1A of output current and placed very close to the high side MOSFET. A small 1µF ceramic capacitor should be placed near the V_{IN} and ground pins of the LT3741 for optimal noise immunity. The input capacitor should have a ripple current rating equal to half of the maximum output current. It is recommended that several low ESR ceramic capacitors be used as the input capacitance. Use only type X5R or X7R capacitors as they maintain their capacitance over a wide range of operating voltages and temperatures.

Output Capacitor Selection

The output capacitors need to have very low ESR (equivalent series resistance) to reduce output ripple. A minimum of 20µF/A of load current should be used in most designs. The capacitors also need to be surge rated to the maximum output current. To achieve the lowest possible ESR, several low ESR capacitors should be used in parallel. Many applications benefit from the use of high density POSCAP capacitors, which are easily destroyed when exposed to overvoltage conditions. To prevent this, select POSCAP capacitors that have a voltage rating that is at least 50% higher than the regulated voltage

C_{BOOT} Capacitor Selection

The C_{BOOT} capacitor must be sized less than 220nF and more than 50nF to ensure proper operation of the LT3741. Use 220nF for high current switching MOSFETs with high gate charge.

V_{CC_INT} Capacitor Selection

The bypass capacitor for the V_{CC_INT} pin should be larger than 5µF for stability and has no ESR requirement. It is recommended that the ESR be lower than 50mΩ to reduce noise within the LT3741. For driving MOSFETs with gate charges larger than 10nC, use 0.5µF/nC of total gate charge.

Soft-Start

Unlike conventional voltage regulators, the LT3741 utilizes the soft-start function to control the regulated inductor current. The charging current is 11µA and reduces the regulated current when the SS pin voltage is lower than CTRL1.

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Output Current Regulation

To adjust the regulated load current, an analog voltage is applied to the CTRL1 pin. Figure 5 shows the regulated voltage across the sense resistor for control voltages up to 2V. Figure 6 shows the CTRL1 voltage created by a voltage divider from V_{REF} to ground. When sizing the resistor divider, please be aware that the V_{REF} pin is current limited to 500µA. Above 1.5V, the control voltage has no effect on the regulated inductor current.

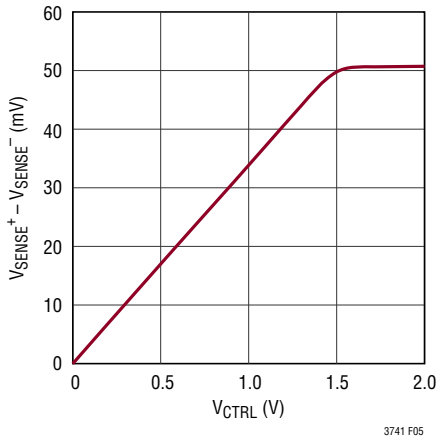

Figure 5. Sense Voltage vs CTRL Voltage

Voltage Regulation and Overvoltage Protection

The LT3741 uses the FB pin to regulate the output voltage and to provide a high speed overvoltage lockout to avoid high voltage conditions. The regulated output voltage is programmed using a resistor divider from the output and ground (Figure 7). When the output voltage exceeds 125% of the regulated voltage level (1.5V at the FB pin), the internal overvoltage flag is set, terminating switching. The regulated output voltage must be greater than 1.5V and is set by the equation:

$$V_{OUT} = 1.21V\left(1+\frac{R2}{R1}\right)$$

Programming Switching Frequency

The LT3741 has an operational switching frequency range between 200kHz and 1MHz. This frequency is programmed with an external resistor from the RT pin to ground. Do not leave this pin open under any condition. The RT pin is also current limited to 60µA. See Table 4 and Figure 8 for resistor values and the corresponding switching frequencies.

Table 4. Switching Frequency

SWITCHING FREQUENCY (MHz)	R_T (kΩ)
1	40.2
0.750	53.6
0.5	82.5
0.3	143
0.2	200

Thermal Shutdown

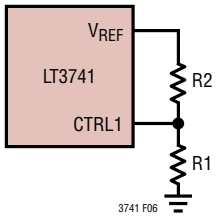

Figure 6. Analog Control of Inductor Current

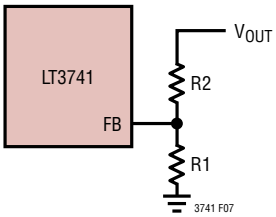

Figure 7. Output Voltage Regulation and Overvoltage Protection Feedback Connections

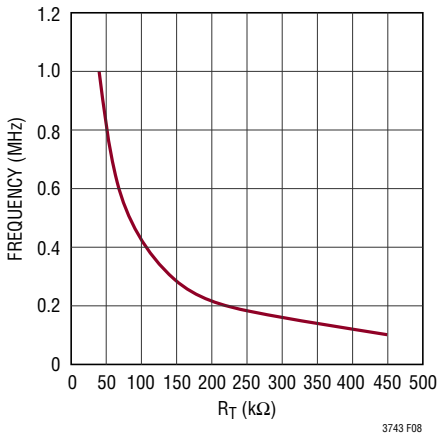

Figure 8. Frequency vs R_T Resistance

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The internal thermal shutdown within the LT3741 engages at 163°C and terminates switching and resets soft-start. When the part has cooled to 155°C, the internal reset is cleared and soft-start is allowed to charge.

Switching Frequency Synchronization

The nominal switching frequency of the LT3741 is determined by the resistor from the RT pin to ground and may be set from 200kHz to 1MHz. The internal oscillator may also be synchronized to an external clock through the SYNC pin. The external clock applied to the SYNC pin must have a logic low below 0.3V and a logic high higher than 1.25V. The input frequency must be 20% higher than the frequency determined by the resistor at the RT pin. Input signals outside of these specified parameters will cause erratic switching behavior and subharmonic oscillations. Synchronization is tested at 500kHz with a 200k R_T resistor. Operation under other conditions is guaranteed by design. When synchronizing to an external clock, please be aware that there will be a fixed delay from the input clock edge to the edge of switch. The SYNC pin must be grounded if the synchronization to an external clock is not required. When SYNC is grounded, the switching frequency is determined by the resistor at the RT pin.

Shutdown and UVLO

The LT3741 has an internal UVLO that terminates switching, resets all synchronous logic, and discharges the soft-start capacitor for input voltages below 4.2V. The LT3741 also has a precision shutdown at 1.55V on the EN/UVLO pin. Partial shutdown occurs at 1.55V and full shutdown is guaranteed below 0.5V with <1µA I_Q in the full shutdown state. Below 1.55V, an internal current source provides 5.5µA of pull-down current to allow for programmable UVLO hysteresis. The following equations determine the voltage divider resistors for programming the UVLO voltage and hysteresis as configured in Figure 9.

$$R2 = \frac{V_{HYST}}{5.5\mu A} - \frac{V_{UVLO}}{66\mu A}$$

$$R1 = \left(\frac{1.55V \bullet R2}{V_{UVLO} - 1.55V} \right)$$

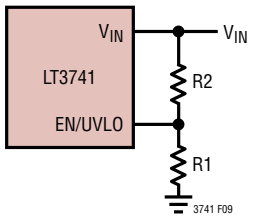

Figure 9. UVLO Configuration

The EN/UVLO pin has an absolute maximum voltage of 6V. To accommodate the largest range of applications, there is an internal Zener diode that clamps this pin. For applications where the supply range is greater than 4:1, size R2 greater than 375k.

Load Current Derating Using the CTRL2 Pin

The LT3741 is designed specifically for driving high power loads. In high current applications, derating the maximum current based on operating temperature prevents damage to the load. In addition, many applications have thermal limitations that will require the regulated current to be reduced based on load and/or board temperature. To achieve this, the LT3741 uses the CTRL2 pin to reduce the effective regulated current in the load. While CTRL1 programs the regulated current in the load, CTRL2 can be configured to reduce this regulated current based on the analog voltage at the CTRL2 pin. The load/board temperature derating is programmed using a resistor divider with a temperature dependant resistance (Figure 10). When the board/load temperature rises, the CTRL2 voltage will decrease. To reduce the regulated current, the CTRL2 voltage must be lower than voltage at the CTRL1 pin.

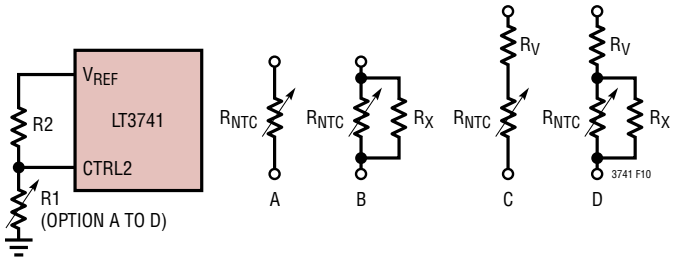

Figure 10. Load Current Derating vs Temperature Using NTC Resistor

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Average Current Mode Control Compensation

The use of average current mode control allows for precise regulation of the inductor and load currents. Figure 11 shows the average current mode control loop used in the LT3741, where the regulation current is programmed by a current source and a 3k resistor.

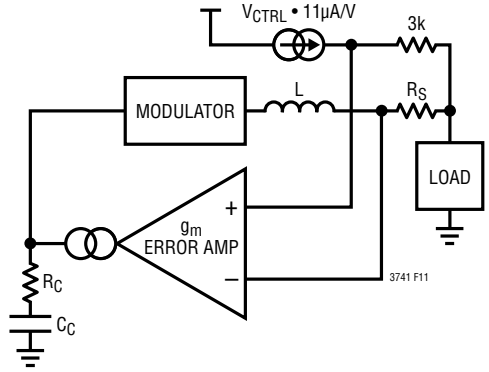


Figure 11. LT3741 Average Current Mode Control Scheme

To design the compensation network, the maximum compensation resistor needs to be calculated. In current mode controllers, the ratio of the sensed inductor current ramp to the slope compensation ramp determines the stability of the current regulation loop above 50% duty cycle. In the same way, average current mode controllers require the slope of the error voltage to not exceed the PWM ramp slope during the switch off-time.

Since the closed-loop gain at the switching frequency produces the error signal slope, the output impedance of the error amplifier will be the compensation resistor, R_C. Use the following equation as a good starting point for compensation component sizing:

$$R_C = \frac{f_S \bullet L \bullet 1000V}{V_O \bullet R_S}\ [\Omega],\ C_C = \frac{0.002}{f_S}[F]$$

where f_S is the switching frequency, L is the inductance value, V_O is the output voltage and R_S is the sense resistor. For most applications, a 4.7nF compensation capacitor is adequate and provides excellent phase margin with optimized bandwidth. Please refer to Table 6 for recommended compensation values.

Board Layout Considerations

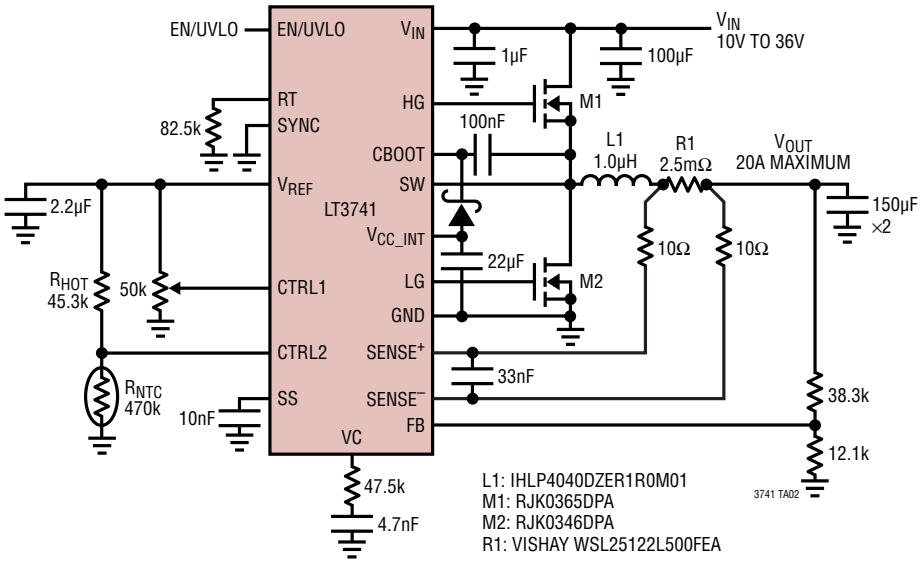
Average current mode control is relatively immune to the switching noise associated with other types of control schemes. Placing the sense resistor as close as possible to the $SENSE^+$ and $SENSE^–$ pins avoids noise issues. Due to sense resistor ESL (equivalent series inductance), a 10Ω resistor in series with the $SENSE^+$ and $SENSE^–$ pins with a 33nF capacitor placed between the SENSE pins is recommended. Utilizing a good ground plane underneath the switching components will minimize interplane noise coupling. To dissipate the heat from the switching components, use a large area for the switching mode while keeping in mind that this negatively affects the radiated noise.

Table 6. Recommended Compensation Values

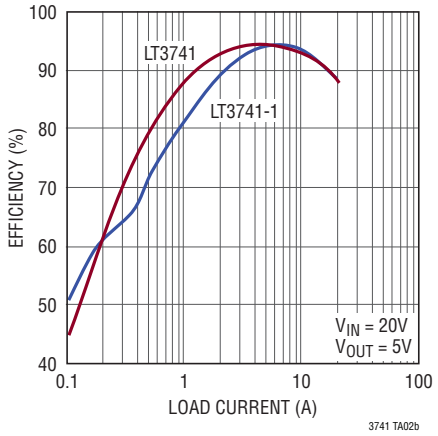
V_{IN} (V)	V_O (V)	I_L (A)	f_{SW} (MHz)	L (µH)	R_S (mΩ)	R_C (kΩ)	C_C (nF)
12	4	5	0.5	1.5	5	47.5	4.7
12	4	10	0.5	1.5	5	47.5	4.7
12	5	20	0.25	1.8	2.5	38.3	8.2
24	4	2	0.5	1.0	2.5	52.3	4.7
24	4	20	0.5	1.0	2.5	52.3	4.7

TYPICAL APPLICATIONS

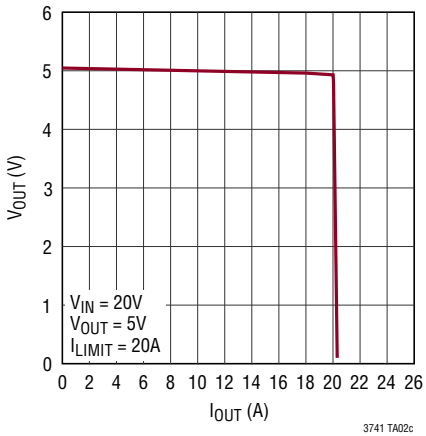
20A Super Capacitor Charger with 5V Regulated Output



Efficiency and Power Loss vs Load Current

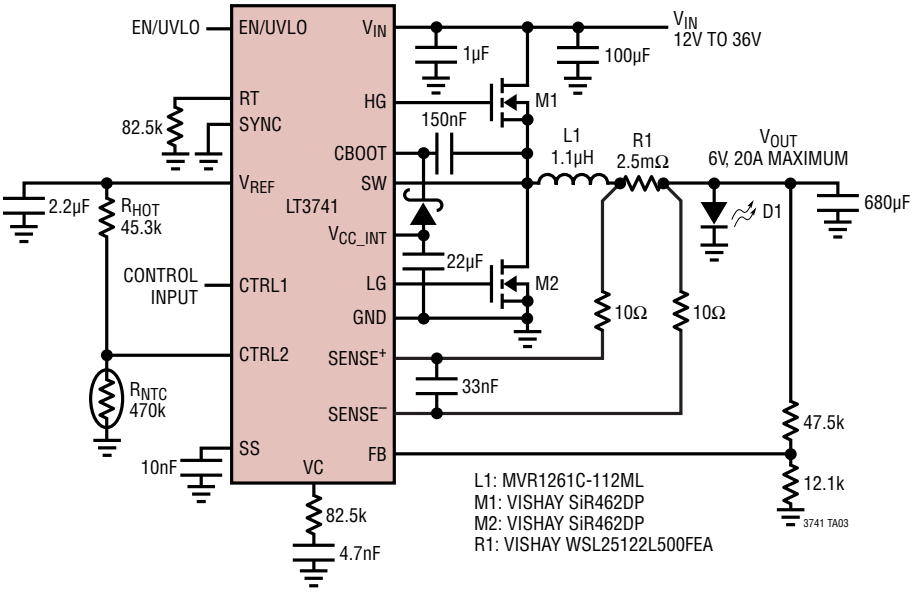


VOUT vs IOUT

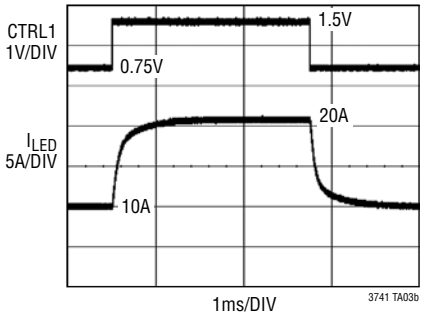


TYPICAL APPLICATIONS

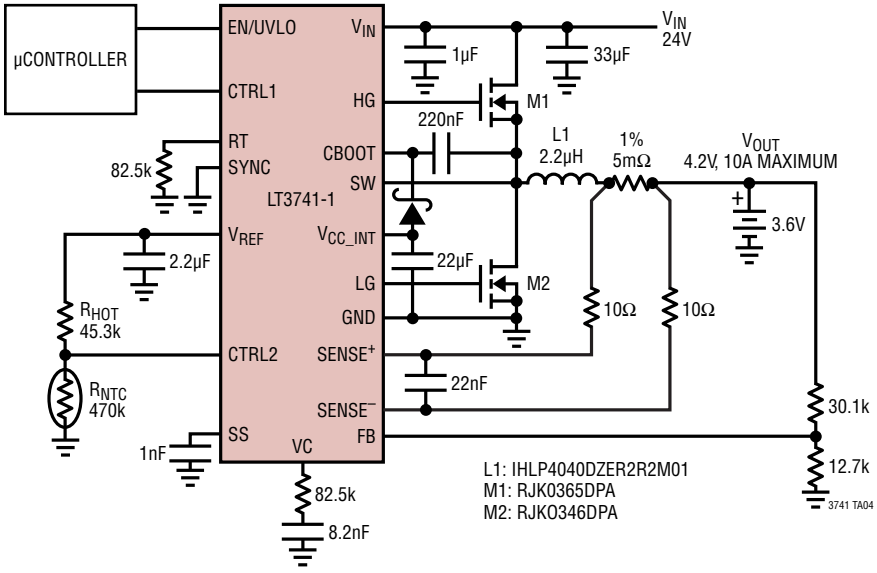
20A LED Driver



LED Current Waveforms 10A to 20A Current Step



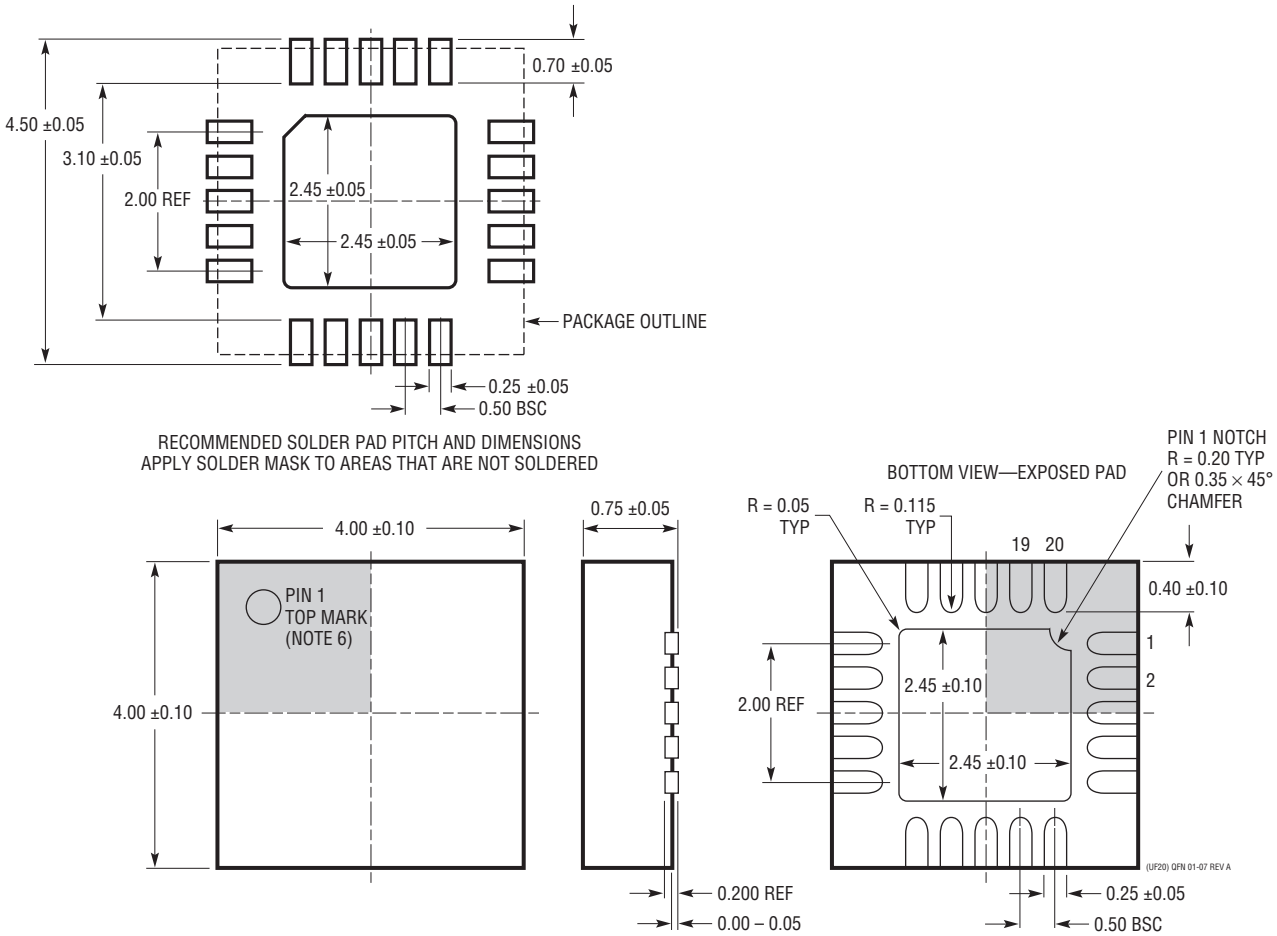
10A Single-Cell Lithium-Ion Battery Charger



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT3741#packaging for the most recent package drawings.

UF Package
20-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1710 Rev A)

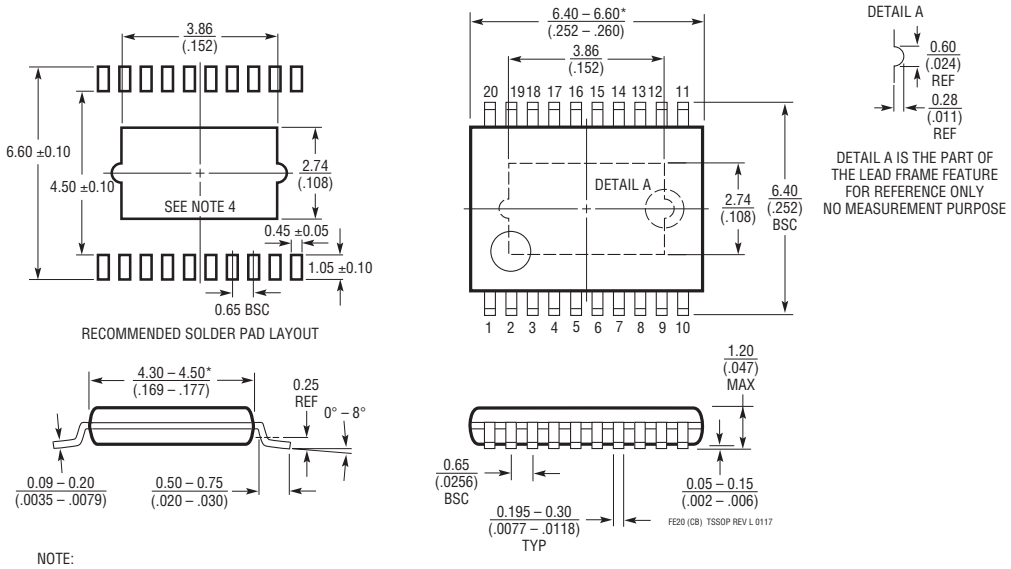


NOTE:
1. DRAWING IS PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-1)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT3741#packaging for the most recent package drawings.

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev L)
Exposed Pad Variation CB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

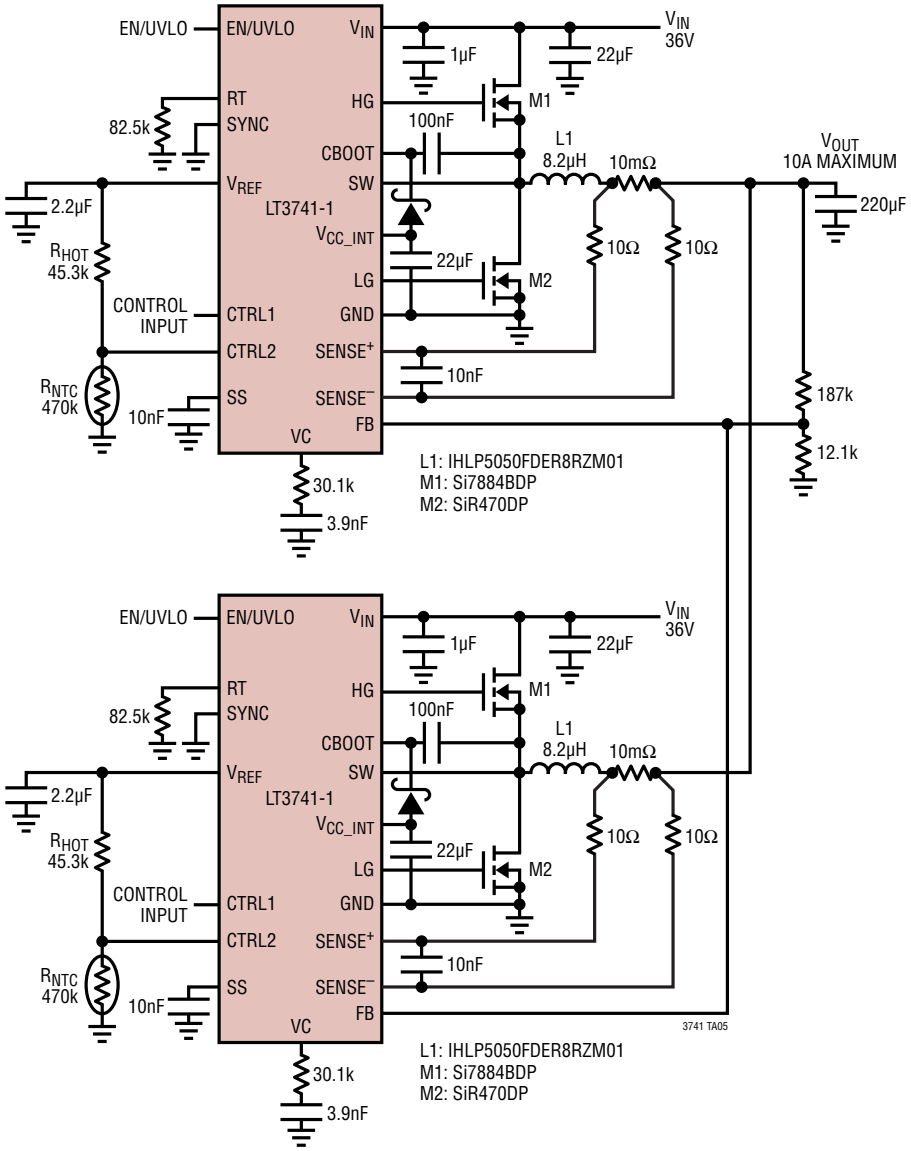
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	8/10	Revised to ±1.5% Voltage Regulation Accuracy in Features section	1
		Revised Absolute Maximum Ratings to delete CBOOT-SW Voltage	2
		Updated Electrical Characteristics section	3, 4
		Updated RT, HG and LG pin descriptions	10
		Updated Block Diagram	11
		Revised text, added a paragraph and revised equations in Applications Information section	13, 14
		Revised Table 4 and Switching Frequency Synchronization paragraph in the Applications Information section	16, 17
		Revised Typical Applications drawings and added vendor part numbers	19, 20, 24
		Updated Related Parts	24
B	9/10	Revised Voltage Regulator Amp value to g_m = 800µA/V on Figure 1 Block Diagram	11
C	5/13	Added LT3741-1 Option	All
		Added LT3741-1 Option to Order Information	2
		Clarified Non-Overlap and CTRL Current Specifications	3
		Clarified Regulated Current vs V_{FB} Graph	6
		Clarified Efficiency Graphs	8
		Clarified Common Mode Lockout Graph	9
		Added LT3741-1 Block Diagram	11
		Clarified Efficiency Graph	19
		Clarified Part Number on Schematic	20
D	9/13	Corrected package descriptions in Order Information section	2
E	1/14	Corrected package in Block Diagram	11
F	10/15	Revised UVLO Hysteresis Equation	17
G	11/17	Revised VC cap value Figures 1 and 2	10, 11
		Changed pin name to VC, 20A LED Driver circuit	20

TYPICAL APPLICATION

20V Regulated Output with 5A Current Limit



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3743	Synchronous Step-Down LED Driver	92% Efficiency, I_{OUT} to 20A, V_{IN}: 5.5V to 36V, I_Q = 2mA, I_{SD} < 1µA, 4mm × 5mm QFN-28, TSSOP-28E

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