

# 1.3A Eight-Switch Matrix LED Dimmer with CRC-8

## FEATURES

- Eight Independent 15V/110mΩ NMOS Switches
- Controls LED Dimming of Strings Up to 54V
- I<sup>2</sup>C Serial Interface with Programmable Address
- I<sup>2</sup>C Packet Error Checking with CRC-8
- Programmable 256:1 (8-Bit) PWM Dimming
- 11-Bit Precision Exponential Fade with Programmable Time
- Independent On/Off Control for Each Switch
- Programmable Shorted/Open LED Threshold with Fault Reporting
- Internal PWM Signal Generator
- Programmable Watchdog Timer
- Accurate V<sub>IN</sub> Referred Enable Pin
- User Defined Power-Up/Reset State of Switches
- Thermally Enhanced TSSOP Package

## APPLICATIONS

- Automotive LED Headlight Clusters
- Large LED Displays
- RGBW Color Mixing Lighting

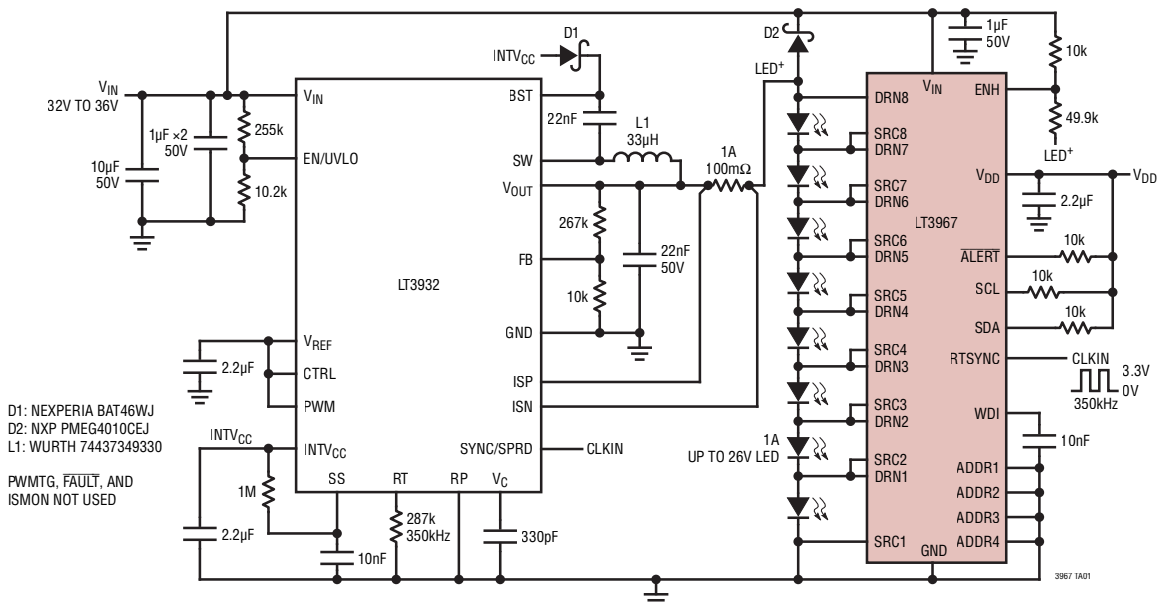
## DESCRIPTION

The **LT<sup>®</sup>3967** is an LED bypass switching device for dimming individual LEDs in a string using a common current source. It features eight individually controlled floating source 15V/110mΩ NMOS switches. The eight switches can be connected in parallel and/or in series to bypass current around LEDs in a string. The LT3967 uses the I<sup>2</sup>C serial interface to communicate with a microcontroller. Each of the eight channels can be independently programmed to bypass the LED string in constant on or off, or PWM dimming with or without fade transition. Using the programmable fade option provides 11-bit resolution exponential transition between PWM dimming states. The LT3967 provides an internal clock generator and also supports an external clock source for PWM dimming. The LT3967 reports fault conditions for each channel such as open LED and shorted LED. The four address pins allow 16 LT3967 devices to share the I<sup>2</sup>C bus and define the power-up state of the switches.

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## TYPICAL APPLICATION

1A Matrix LED Dimmer Powered by a Buck LED Driver



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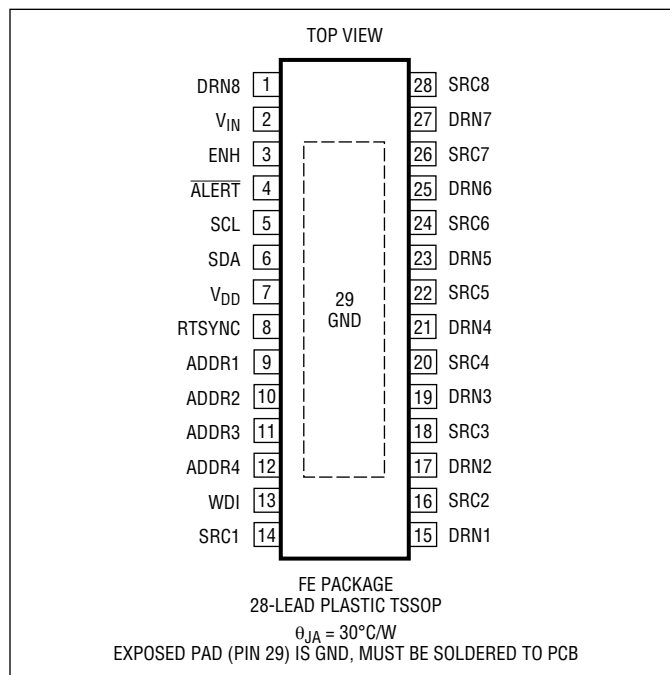
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## ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{IN}$ .....	60V
$V_{IN} - SRC[8:1]$ .....	-0.3V
ENH .....	60V
DRN[8:1] .....	60V
SRC[8:1] .....	60V
DRN[8:1] - SRC[8:1] (Each Channel) .....	-0.3V, 17V
$V_{DD}$ .....	6V
WDI .....	6V
SDA, SCL, ALERT .....	-0.3V to $V_{DD} + 0.3V$
RTSYNC .....	6V
ADDR[4:1] .....	6V
Operating Junction Temperature Range (Note 2)	
LT3967E .....	-40°C to 125°C
LT3967J .....	-40°C to 150°C
Storage Temperature Range .....	-65°C to 150°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3967EFE#PBF	LT3967EFE#TRPBF	LT3967FE	28-Lead Plastic TSSOP	-40°C to 125°C
LT3967JFE#PBF	LT3967JFE#TRPBF	LT3967FE	28-Lead Plastic TSSOP	-40°C to 150°C

Consult ADI Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container. [Tape and reel specifications](#). Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN} = 40\text{V}$ ,  $\text{ENH} = 38.5\text{V}$ ,  $V_{DD} = 5\text{V}$ ,  $\text{SRC}[8:1] = 0\text{V}$ ,  $\text{ADDR}[4:1]$  are tied to GND through a  $100\text{k}\Omega$  resistor respectively, SDA and SCL are pulled up to  $V_{DD}$  by a  $4.99\text{k}\Omega$  resistor respectively, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{DD}$ Input Supply Voltage		●	2.7		5.5	V
$V_{DD}$ Operating $I_Q$	I <sup>2</sup> C Bus Idle, $R_{\text{TSYNC}} = 28\text{k}$			1.5	2.2	mA
$V_{DD}$ Shutdown $I_Q$	$V_{IN} - \text{ENH} < 1.15\text{V}$ , All Channels LED ON $V_{IN} - \text{ENH} < 1.15\text{V}$ , All Channels LED OFF			0.5 0.6		mA mA
$V_{IN}$ Operating Voltage	All Channels $\text{VOTH} = \text{VSTH} = 0$ (Note 3)	●	8		60	V
$V_{IN}$ Operating $I_Q$ (Channel Not Switching)	All Channels $\text{VOTH} = \text{VSTH} = 0$ , LED ON			1.3	1.8	mA
	All Channels $\text{VOTH} = \text{VSTH} = 1$ , LED OFF			2.5	3.5	mA
	All Channels $\text{VOTH} = 1$ , $\text{VSTH} = 0$ , LED ON			1.8	2.5	mA
$V_{IN}$ Shutdown $I_Q$	$V_{IN} - \text{ENH} < 1.15\text{V}$ , All Channels LED ON			0.9		mA
	$V_{IN} - \text{ENH} < 1.15\text{V}$ , All Channels LED OFF			1.4		mA
DRN[8:1] Operating Voltage		●			$V_{IN} - 1\text{V}$	V
SRC[8:1] Operating Voltage		●			$V_{IN} - 6\text{V}$	V
Current Out of SRC[8:1] Pins (Each Channel)	Channel LED Is On (Channel Switch Is Off)	●		11	20	$\mu\text{A}$
	Channel LED Is Off (Channel Switch Is On)	●		45	75	$\mu\text{A}$
Switch On-Resistance				110		$\text{m}\Omega$
Switch Leakage Current	DRN = 8V, SRC = 0V, $\text{VOTH} = 1$				1	$\mu\text{A}$
Switch Transition Time ( $t_r/t_f$ )	DRN to 5V Through a $50\Omega$ Resistor, $\text{VOTH} = 1$		1.0	1.6	2.2	$\mu\text{s}$
DRN[8:1] to SRC[8:1] Overvoltage Protection Clamp Voltage	LED or Switch Bypass Current is 1.3A	●		15	17	V
Response Time from Switch Overvoltage Protection to Switch Turn On	LED or Switch Bypass Current is 1.3A	●		5.2	6.6	$\mu\text{s}$
Programmable Open LED Threshold ( $V_{\text{OTH}}$ )	SRC = 0V, $\text{VOTH} = 0$ (Note 3)	●	5.2	6.1	7.0	V
	SRC = 0V, $\text{VOTH} = 1$	●	10.4	11.4	12.4	V
	SRC = 2V, $\text{VOTH} = 0$	●	5.0	5.5	6.0	V
	SRC = 2V, $\text{VOTH} = 1$	●	10.1	10.8	11.5	V
Programmable Shorted LED Threshold ( $V_{\text{STH}}$ )	$\text{VSTH} = 0$ (Note 3)	●	0.85	1	1.15	V
	$\text{VSTH} = 1$	●	3.6	4	4.4	V
ENH Threshold Voltage Falling $\text{ENH}(V_{\text{TH}})$ ( $V_{IN} - \text{ENH}$ )		●	1.1	1.22	1.34	V
ENH Threshold Voltage Rising Hysteresis				50		mV
ENH Pin Input Bias Current	$V_{IN} - \text{ENH} = 1.5\text{V}$ , Current Out of ENH Pin			40	100	nA
<b>RTSYNC Programmable Internal Oscillator or External Clock Source</b>						
LED PWM Dimming Frequency (= RTSYNC Programmed Oscillator Frequency/2048 or External Clock Frequency/2048)	$R_{\text{TSYNC}} = 80.6\text{k}\Omega$	●	170	198	220	Hz
	$R_{\text{TSYNC}} = 28\text{k}\Omega$	●	450	500	550	Hz
	$R_{\text{TSYNC}} = 10\text{k}\Omega$	●	880	1010	1130	Hz
RTSYNC Output Voltage (Using Internal Oscillator)	$R_{\text{TSYNC}} = 28\text{k}\Omega$		0.83	0.88	0.93	V
Programmable LED PWM Dimming Frequency Range (Using Internal Oscillator)			100		1000	Hz
Standby Fixed LED PWM Dimming Frequency	$R_{\text{TSYNC}} = \text{Float}$		32	45	58	Hz

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RTSYNC Input Clock Frequency Range			200		2000	kHz
RTSYNC Input Low Threshold ( $RT_{VIL}$ )		●			0.4	V
RTSYNC Input High Threshold ( $RT_{VIH}$ )		●	1.5			V
RTSYNC Input Clock Pulse Width High ( $T_{RTH}$ )			100			ns
RTSYNC Input Clock Pulse Width Low ( $T_{RTL}$ )			100			ns
RTSYNC Input Clock Ramp Time Between $RT_{VIL}$ and $RT_{VIH}$ ( $T_{RTR}$ )	$T_{RTH} + T_{RTL} > T_{RTR}$				2.5	$\mu\text{s}$
<b>Watchdog Timer</b>						
Watchdog Upper Boundary (Timeout)	A 10nF Capacitor Between WDI and GND	●	15	17.5	20	ms
WDI Pin Pull-Up Current	WDI = 0.8V	●	9	10	11	$\mu\text{A}$
WDI Pin Pull-Down Current	WDI = 2.2V			200		$\mu\text{A}$
WDI Low Threshold Voltage				1		V
WDI High Threshold Voltage				2		V
<b>Address Select and ACMREG Register Power-On Reset</b>						
ADDR[4:1] Input Low Resistance to GND, ACMREG[M:N] = "00" at $V_{DD}$ Power-Up M:N=7:6 for ADDR[4], M:N=5:4 for ADDR[3], M:N=3:2 for ADDR[2], M:N=1:0 for ADDR[1]		●			5	$\text{k}\Omega$
ADDR[4:1] Input Low Resistance to GND, ACMREG[M:N] = "11" at $V_{DD}$ Power-Up M:N=7:6 for ADDR[4], M:N=5:4 for ADDR[3], M:N=3:2 for ADDR[2], M:N=1:0 for ADDR[1]		●	50		150	$\text{k}\Omega$
ADDR[4:1] Input High Resistance to $V_{DD}$ , ACMREG[M:N] = "11" at $V_{DD}$ Power-Up M:N=7:6 for ADDR[4], M:N=5:4 for ADDR[3], M:N=3:2 for ADDR[2], M:N=1:0 for ADDR[1]		●	50		150	$\text{k}\Omega$
ADDR[4:1] Input High Resistance to $V_{DD}$ , ACMREG[M:N] = "00" at $V_{DD}$ Power-Up M:N=7:6 for ADDR[4], M:N=5:4 for ADDR[3], M:N=3:2 for ADDR[2], M:N=1:0 for ADDR[1]		●			5	$\text{k}\Omega$
<b>Alert Status Output</b>						
$\overline{\text{ALERT}}$ Output Low Voltage	$I_{\overline{\text{ALERT}}} = 3\text{mA}$			0.3	0.4	V
$\overline{\text{ALERT}}$ Output High Leakage Current	$\overline{\text{ALERT}} = 5.5\text{V}$				0.1	$\mu\text{A}$
<b>I<sup>2</sup>C Port (See Note 5 for I<sup>2</sup>C Timing Diagram)</b>						
SDA and SCL Input Threshold Rising		●	$0.7V_{DD}$			V
SDA and SCL Input Threshold Falling		●			$0.25V_{DD}$	V
SDA and SCL Input Hysteresis		●	$0.05V_{DD}$			V
SDA and SCL Input Current	SDA = SCL = 0V to 5.5V		-250		250	nA
SDA Output Low Voltage	$I_{\text{SDA}} = 3\text{mA}$	●			0.4	V
SCL Clock Operating Frequency		●			400	kHz

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PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
(Repeated) Start Condition Hold Time ( $t_{HD\_STA}$ )		●	0.6		$\mu\text{s}$
Repeated Start Condition Set-Up Time ( $t_{SU\_STA}$ )		●	0.6		$\mu\text{s}$
Stop Condition Setup Time ( $t_{SU\_STO}$ )		●	0.6		$\mu\text{s}$
Data Hold Time Output ( $t_{HD\_DAT(O)}$ )		●	0	900	ns
Data Hold Time Input ( $t_{HD\_DAT(I)}$ )		●	0		ns
Data Set-Up Time ( $t_{SU\_DAT}$ )		●	100		ns
SCL Clock Low Period ( $t_{LOW}$ )		●	1.3		$\mu\text{s}$
SCL Clock High Period ( $t_{HIGH}$ )		●	0.6		$\mu\text{s}$
Data Rise Time ( $t_r$ )	$C_B = \text{Capacitance of One BUS Line (pF)}$ (Note 4)		$20+0.1C_B$	300	ns
Data Fall Time ( $t_f$ )	$C_B = \text{Capacitance of One BUS Line (pF)}$ (Note 4)		$20+0.1C_B$	300	ns
Input Spike Suppression Pulse Width ( $t_{SP}$ )				50	ns
Bus Free Time ( $t_{BUF}$ )		●		1.3	$\mu\text{s}$

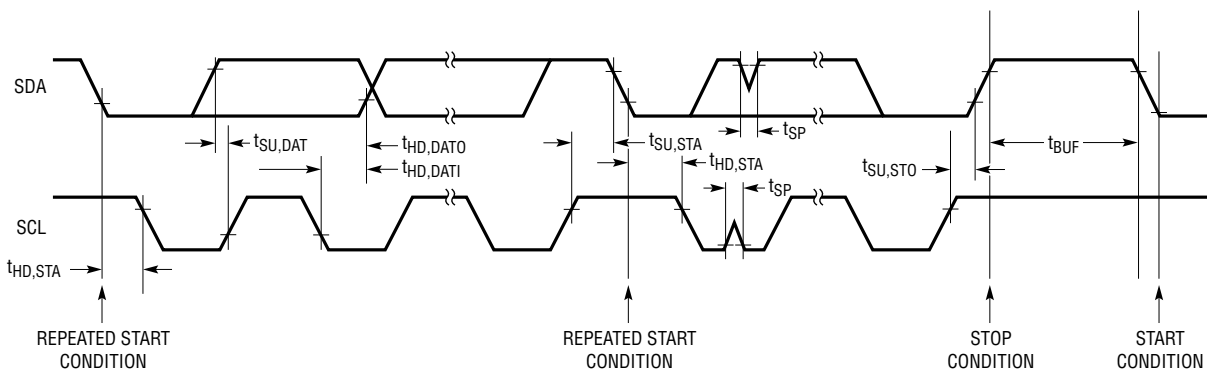
**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LT3967E is guaranteed to meet performance specifications from the  $0^\circ\text{C}$  to  $125^\circ\text{C}$  junction temperature. Specifications over the  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3967I is guaranteed over the full  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  operating junction temperature range. The LT3967H is guaranteed over the full  $-40^\circ\text{C}$  to  $150^\circ\text{C}$  operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than  $125^\circ\text{C}$ .

**Note 3:** VOTH and VSTH register bits are set by a LT3967 I<sup>2</sup>C command.  $V_{OTH}/V_{STH}$  programmed by VOTH/VSTH register bits refer to the open/shorted LED threshold between DRN and SRC of a channel. For a channel,  $V_{IN} > V_{SRC} + V_{OTH} + 1\text{V}$  is required for accurate open LED detection.

**Note 4:** Rise and fall times are measured at 30% and 70% levels.

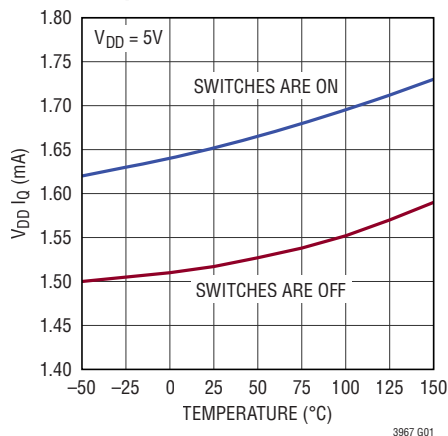
**Note 5:** I<sup>2</sup>C interface timing diagram (see below).



3967 TD

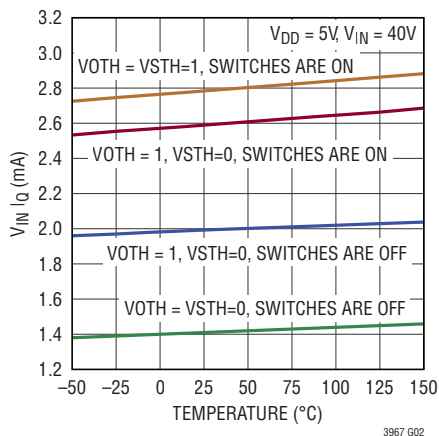
# TYPICAL PERFORMANCE CHARACTERISTICS

**V<sub>DD</sub> Quiescent Current vs Temperature**



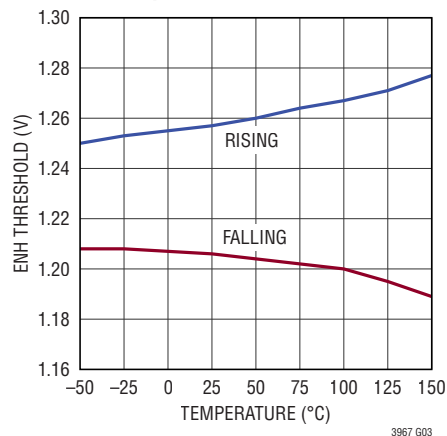
3967 G01

**V<sub>IN</sub> Quiescent Current vs Temperature**



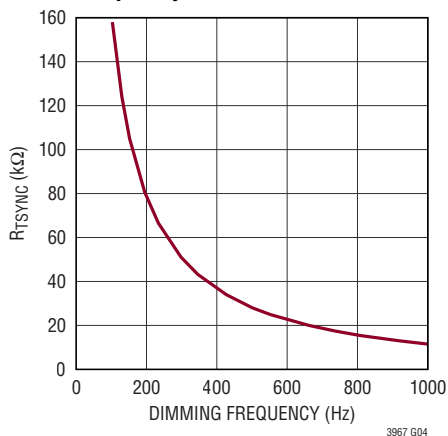
3967 G02

**Enable Threshold ENH(V<sub>TH</sub>) vs Temperature**



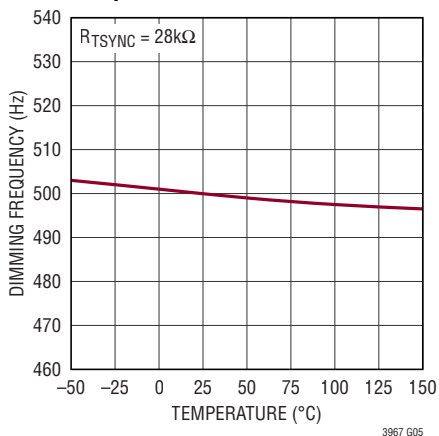
3967 G03

**R<sub>TSYNC</sub> vs PWM Dimming Frequency**



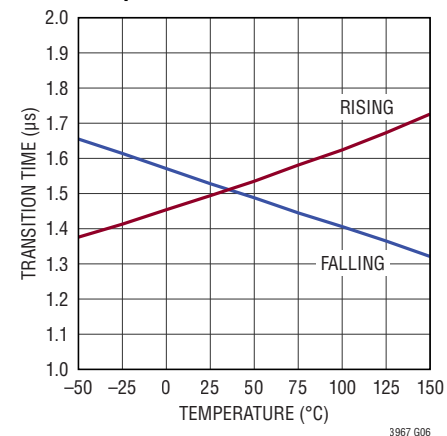
3967 G04

**PWM Dimming Frequency vs Temperature**



3967 G05

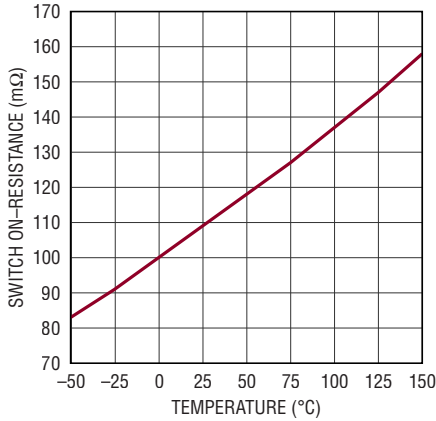
**Switching Transition Time vs Temperature**



3967 G06

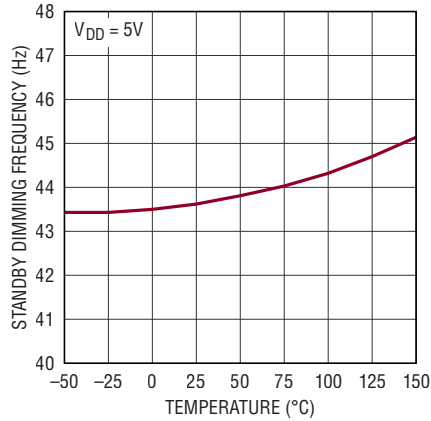
# TYPICAL PERFORMANCE CHARACTERISTICS

**Switch On-Resistance vs Temperature**



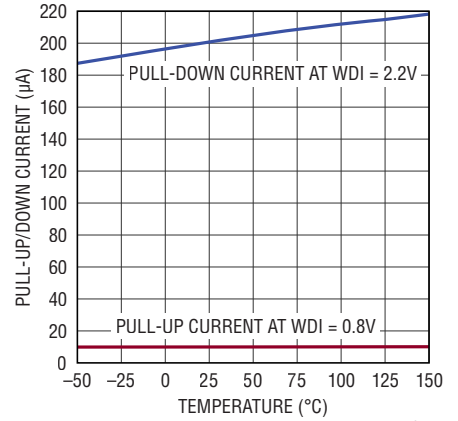
3967 G07

**Standby Dimming Frequency vs Temperature**



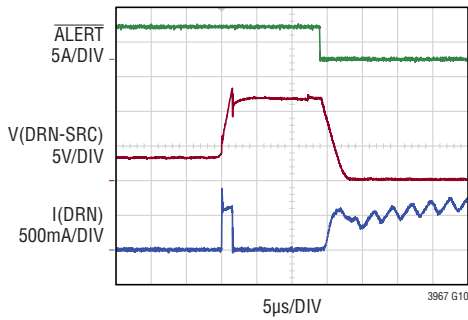
3967 G08

**WDI Pin Pull-Up/Pull-Down Current vs Temperature**



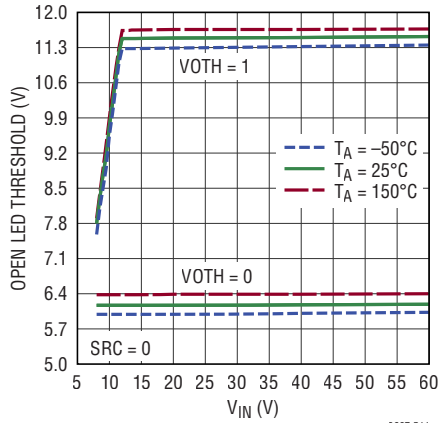
3967 G09

**Switch Open LED Protection Response Time Scope Photo**



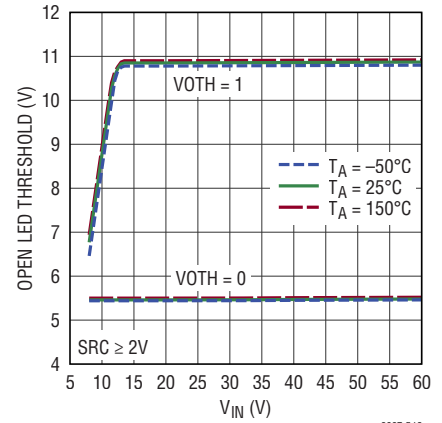
3967 G10

**Open LED Threshold vs  $V_{IN}$ , for SRC = 0V**



3967 G11

**Open LED Threshold vs  $V_{IN}$ , for SRC ≥ 2V**

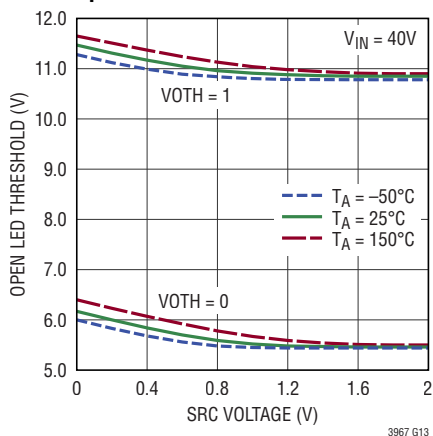


3967 G12

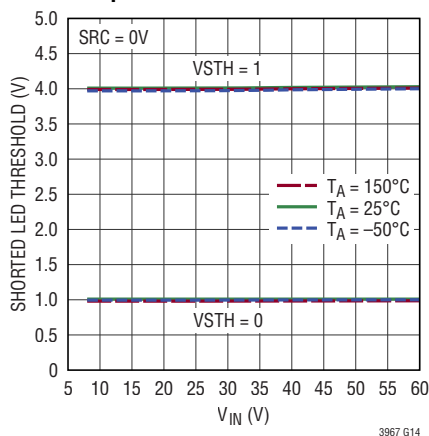


# TYPICAL PERFORMANCE CHARACTERISTICS

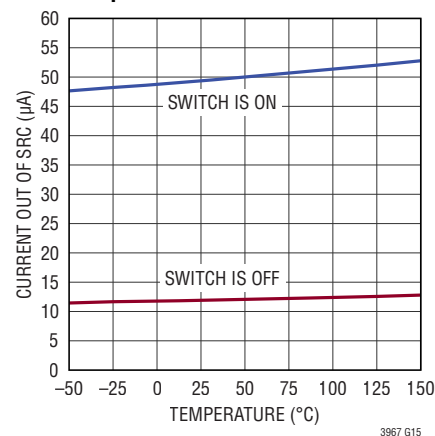
**Open LED Threshold vs SRC**



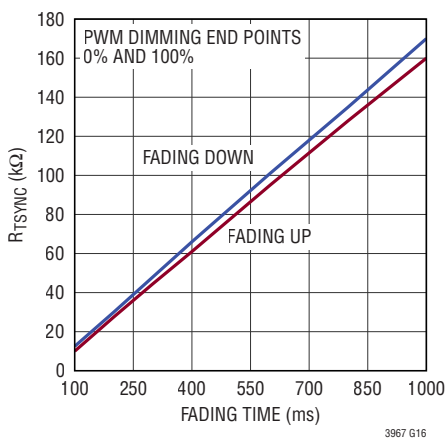
**Shorted LED Threshold vs VIN, Temperature**



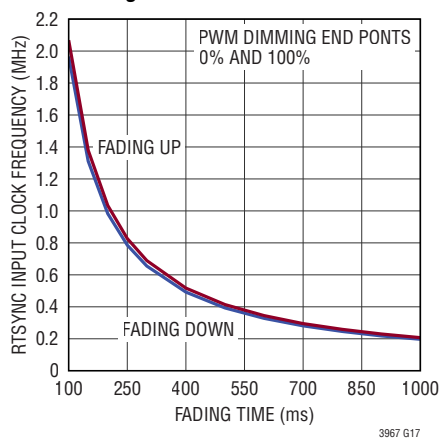
**Current Out of SRC Pin vs Temperature**



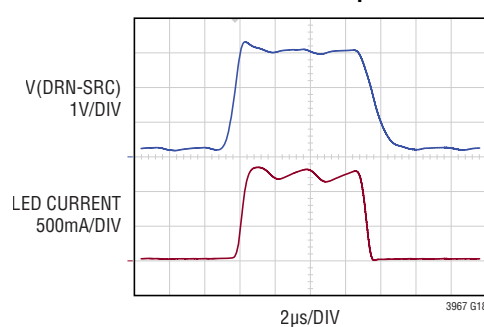
**RTSYNC vs Fading Time for FTM[2:0] = 001**



**RTSYNC Input Clock Frequency vs Fading Time for FTM[2:0] = 001**



**Switch Slew Rate Scope Photo**



## PIN FUNCTIONS

**ADDR[4:1]:** Programmable Address Select and Initial Switch State Set Pins. The device address is 010xxxx0 for all channel mode (ACMODE) write, 010xxxx1 for all channel mode (ACMODE) read, 101xxxx0 for single channel mode (SCMODE) write, and 101xxxx1 for single channel mode (SCMODE) read, where xxxx represents the input logic value from ADDR[4:1] pins. The input logic value is 0/1 if the pin is connected to GND/ $V_{DD}$  through a 150k $\Omega$  resistor or less. A total of 16 LT3967 devices can be connected to the same I<sup>2</sup>C bus. Resistor values at ADDR[4:1] pins are also used to determine the  $V_{DD}$  Power on Reset (POR) default value of ACMREG. A low value resistor ( $\leq 5k$ ) to GND or  $V_{DD}$  signals the LED should be off at start-up. A high value resistor ( $\geq 50k$ ) to GND or  $V_{DD}$  signals the LED should be on at start-up.

**ALERT:** Alert Output for Fault Condition Report.  $\overline{\text{ALERT}}$  pin is asserted (pulled low) to indicate any of the following fault conditions: an open LED, a shorted LED, overheat fault condition or a RTSYNC clock fault. The  $\overline{\text{ALERT}}$  pin is deasserted (released to high) after the part sends its alert response address successfully or the fault condition is cleared by an I<sup>2</sup>C write command. The alert function is disabled when ENH is undervoltage.

**DRN[8:1]:** Floating N-Channel FET Drain Side Pins. Tie to  $V_{DD}$  with a 100k $\Omega$  resistor if not used.

**ENH:** Shutdown and Undervoltage Detect Pin for  $V_{IN}$ . When ENH pin is 1.22V (nominal) lower than  $V_{IN}$  pin, PWM dimming and fault reporting are enabled. ENH undervoltage is reported through the I<sup>2</sup>C interface. Typically this pin is tied to a resistor divider to ensure the part is enabled only when  $V_{IN}$  is at least 6V higher than channel source voltage.

**GND:** Exposed Pad Pin. Solder the exposed pad directly to ground plane (GND).

**RTSYNC:** External PWM Clock Input and Internal Oscillator Frequency Programming Pin. Set the internal oscillator frequency using a resistor to GND if the internal oscillator is used for PWM dimming. An external clock source able to sink 500 $\mu$ A at 0.4V can be used for PWM dimming by driving RTSYNC above and below  $RT_{VIH}$  and  $RT_{VIL}$  respectively to override the internal oscillator. Do not leave the RTSYNC pin open. Place the resistor close to the IC if a resistor is used to set the internal oscillator frequency. LED PWM dimming frequency equals the programmed internal oscillator frequency divided by 2048 or the external clock frequency divided by 2048. If the programmed internal oscillator frequency or the external clock frequency becomes slower than 100kHz (nominal), the PWM clock setting LED dimming will switch to a 100kHz (nominal) internal standby clock. If the external clock connection is lost, the PWM clock setting LED dimming will switch to the  $R_{TSYNC}$  programmed internal oscillator frequency if a programming resistor  $R_{TSYNC}$  is connected between the RTSYNC pin and GND. Otherwise the PWM clock setting LED dimming will switch to the 100kHz (nominal) internal standby clock. This selection can be reset by  $V_{DD}$  POR, watchdog timeout or an I<sup>2</sup>C BCMODE write command.

**SCL:** Clock Input Pin for the I<sup>2</sup>C Serial Port. The I<sup>2</sup>C logic levels are scaled with respect to  $V_{DD}$ .

**SDA:** Data Input and Output Pin for the I<sup>2</sup>C Serial Port. The I<sup>2</sup>C logic levels are scaled with respect to  $V_{DD}$ .

## PIN FUNCTIONS

**SRC[8:1]:** Floating N-Channel FET Source Side Pins. The channel source voltage (SRC[8:1]) must be at least 6V lower than  $V_{IN}$  for proper channel switch bypass operation. Tie to GND if not used.

**$V_{IN}$ :** Input Supply Pin for LED Bypass Switches and Fault Detectors. Must be locally bypassed with a 1 $\mu$ F (or larger) capacitor placed close to this pin. For proper channel switch bypass operation,  $V_{IN}$  must be at least 6V higher than the channel source voltage.

**$V_{DD}$ :** Supply Voltage for I<sup>2</sup>C Serial Port and Input Supply Pin for Internal Bias and Logic. This pin sets the logic reference level of I<sup>2</sup>C SCL and SDA pins. SCL and SDA logic levels are scaled to  $V_{DD}$ . When the  $V_{DD}$  supply transitions above 2.5V (nominal), ACMREG and SCMREG are reset to the default value, and the I<sup>2</sup>C interface is active. The LT3967 will acknowledge communications to its address and data can be written to and read back from

the registers. This is true even if the part is disabled. The data in ACMREG and SCMREG will not change unless it is updated by an I<sup>2</sup>C command,  $V_{DD}$  POR or a watchdog timeout. Connect a 0.1 $\mu$ F (or larger) decoupling capacitor from this pin to ground.

**WDI:** Watchdog Timer Input Pin. This pin is used to set the watchdog upper boundary using a capacitor to GND. The watchdog starts monitoring I<sup>2</sup>C communications when  $V_{DD}$  transitions above 2.5V. A timeout occurs when the time between  $V_{DD}$  POR or START and STOP reaches the programmed watchdog upper boundary. The timeout resets all LT3967 registers to the default value, resets channel switches to the default state determined by resistor settings at ADDR[4:1] pins, and resets the PWM clock to the RTSYNC input clock. Do not leave this pin open. To disable the watchdog function, tie this pin to GND.

**BLOCK DIAGRAM**

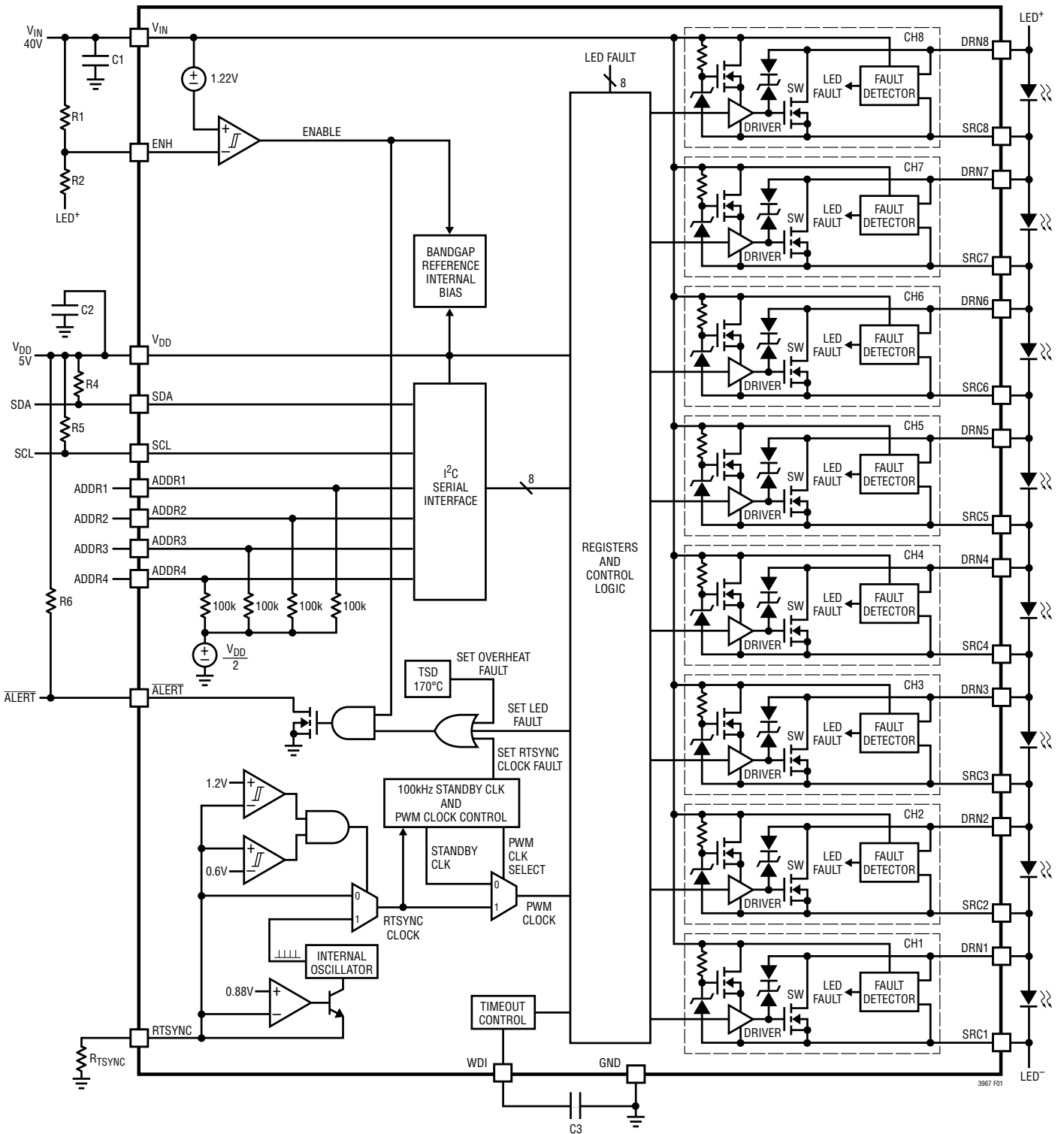


Figure 1. Block Diagram

## APPLICATIONS INFORMATION

### OVERVIEW

The LT3967 is an 8-channel LED bypass switching device with I<sup>2</sup>C serial interface, designed for dimming LED strings using a common current source. Each of the eight channels can be independently programmed to bypass the LED string in constant on or off, or dimming with or without fade transition. Operation can be best understood by referring to the Block Diagram in Figure 1.

The LT3967 operates over the V<sub>DD</sub> input supply range of 2.7V to 5.5V. The eight channel switches are powered by the V<sub>IN</sub> input supply and can be connected in parallel and/or in series. Each of the eight channel switches can bypass one or multiple series LEDs up to 10.1V.

Each channel has an LED fault detector which can be programmed to detect an open LED fault at one of the two threshold levels: 6.1V/5.5V and 11.4V/10.8V (default setting). When an open LED fault is detected in a channel, the channel switch will be turned on to bypass the faulty LED to maintain the continuity of the string and for self protection. The PWM dimming for this channel is interrupted until reset by the serial interface. Each channel LED fault detector can also be programmed to detect a shorted LED fault at one of the two threshold levels: 1V (default setting) and 4V. The 1V and 4V threshold levels may be used to differentiate a 2-short LED fault from a 1-short LED fault in a multi-LED segment. When a shorted LED fault is detected in a channel, the channel switch will continue with the programmed PWM dimming. Besides LED faults, the LT3967 also detects and reports an overheat fault condition ( $\geq 170^{\circ}\text{C}$ ) and a RTSYNC clock fault condition. The LT3967 asserts (pulls down) the  $\overline{\text{ALERT}}$  pin to interrupt the bus master when an LED fault and/or an overheat fault and/or a RTSYNC clock fault is detected. The master can use the alert response address (ARA) to determine which device is sending the alert.

The LT3967 I<sup>2</sup>C serial interface contains nine command registers for configuring channel switches and LED fault detectors and programming logarithmic fade time. It also contains two read-only fault status registers for reporting the LED and overheat faults.

The I<sup>2</sup>C serial interface supports random addressing of any register. The LT3967 address select pins ADDR4, ADDR3, ADDR2 and ADDR1 allow up to 16 LT3967 devices to share

the I<sup>2</sup>C bus. Resistor values at the address select pins are also used to determine the V<sub>DD</sub> POR default state of LEDs.

If a resistor is connected between the RTSYNC pin and the ground, the internal oscillator is chosen and the LED dimming frequency is set by the resistor. If the RTSYNC pin is driven by an external clock source, the external clock source is used to override the internal oscillator and the dimming frequency equals the external clock frequency divided by 2048.

Details of the LT3967 operation are found in the following sections.

### POWER-ON RESET AND DIMMING CYCLE INITIALIZATION

The channels are set in pairs with ADDR4 setting the two MSBs and ADDR1 setting the two LSBs. See Table 1 for an overview of the ACMREG register. When V<sub>DD</sub> transitions above 2.5V, an internal power-on reset (POR) signal is generated to reset all LT3967 registers to the default value. Resistor values at ADDR[4:1] pins are used to determine the POR default state of ACMREG register bits which set each channel switch state at start-up.

The POR also initializes each channel's PWM dimming counter with one-eighth dimming cycle shift, which can avoid simultaneous channel switching at the beginning of dimming cycle to reduce switching transients (see Figure 2). When using PWM dimming (with or without fade transition), the channel LED string is always turned on at the beginning of its dimming cycle. The channel LED string will be turned off if the value of the channel counter, which is clocked by the PWM clock, equals the dimming value stored in the channel SCMREG command register. Once the channel LED string is turned off, it remains off until its next dimming cycle starts.

### OPERATION IN SHUTDOWN CONDITION

The ENH pin is used to enable the IC. When ENH pin is undervoltage for the V<sub>IN</sub> supply, the part is in shutdown condition, in this mode PWM dimming,  $\overline{\text{ALERT}}$  pin asserting and fault reporting are disabled, and the IC does not respond to the broadcast read command. The LT3967 sets all OLFREG and SLFREG register bits high with

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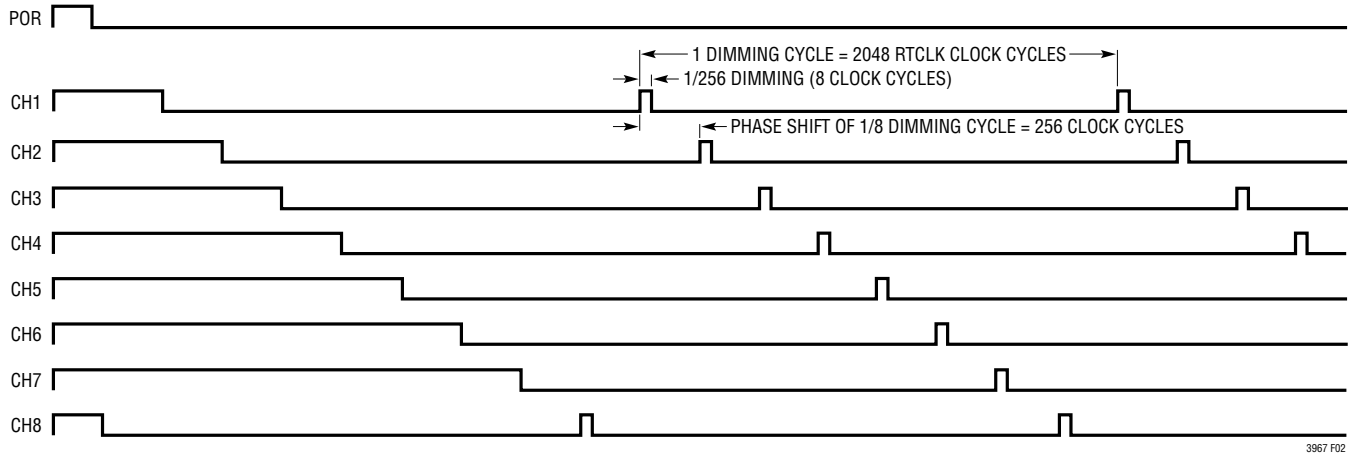


Figure 2. POR Dimming Cycle Initialization Diagram

$\overline{\text{ALERT}}$  pin deasserted to indicate that the IC is in shutdown condition. The channel switch state is controlled only by ACMREG register bits in shutdown condition.

When the IC is in shutdown or with  $V_{DD}$  less than 2.5V (nominal), the open LED detection programmed by VOTH bit is disabled. However the voltage between the channel DRN pin and the channel SRC pin starts clamping if it exceeds 13V (nominal). The clamping will trigger the channel switch to turn on to bypass the faulty LED. The switch will remain on unless it is reset by the power up of the digital logic.

Whether the IC is enabled or is in shutdown condition, as long as  $V_{DD}$  is applied, the serial interface is alive and any data written in the LT3967 command registers does not change unless updated by another I<sup>2</sup>C command. When ENH pin exits undervoltage to enable the IC, the LT3967 resets all OLFREG and SLFREG register bits low, and enables PWM dimming,  $\overline{\text{ALERT}}$  pin asserting and fault reporting.

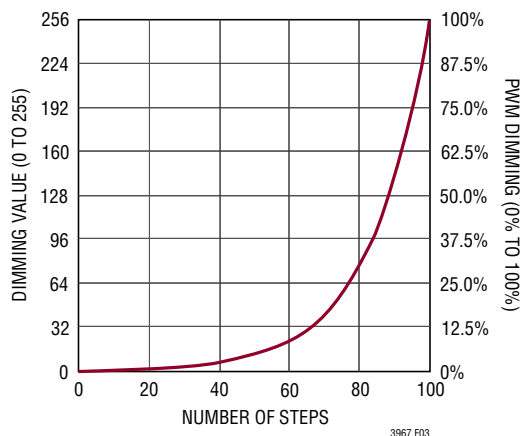
Because  $V_{IN}$  must be at least 6V higher than channel source voltage for proper channel switch bypass operation, it is recommended to enable the IC when  $V_{IN}$  is at least 6V higher than  $V_{LED+}$ . The resistor divider shown in Figure 1 can be used to generate ENH input signal.

### DIMMING WITHOUT FADE TRANSITION VS DIMMING WITH FADE TRANSITION

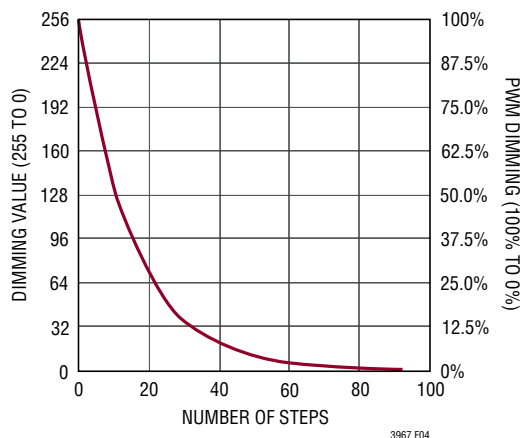
Each channel of the LT3967 can be independently programmed to perform dimming without fade transition or

dimming with fade transition. For dimming without fade transition, the dimming changes from the initial value to the target value in one dimming cycle. For dimming with fade transition, the dimming changes transitionally from the initial value to the target value step by step in multiple dimming cycles, following a predetermined exponential curve, which can favor the approximately logarithmic response of the human eye to brightness. The initial value is an existing 8-bit dimming value stored in channel SCMREG register. The target value comes from a SCMODE long format write command and will be stored in the register to replace the initial value when the STOP condition is received. For dimming with fade transition, each transitional step value is calculated using 11 bits according to the following formula:  $DV_{NEXT} = DV_{PRESENT} \cdot CF$ , where DV represents a transitional step dimming value, CF is a constant factor. CF is 1.0625 for up transition and 0.9375 for down transition. The transition process begins with the initial value served as the first  $DV_{PRESENT}$ , and ends with the target value when the last  $DV_{NEXT}$  is no less than the target value in up transition or no more than the target value in down transition. The number of the transitional steps depends on the distance between the initial value and the target value. The maximum number of transitional steps from LED constant off to constant on is 101 (see Figure 3) and the maximum number of transitional steps from LED constant on to constant off is 96 (see Figure 4). Each step can run various PWM dimming cycles (programmable), and each dimming cycle consists of 2048 RTSYNC clock cycles. Then  $T_{STEP} = T_{PWM} \cdot M =$

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**Figure 3. LT3967 Up Transition Dimming Curve from LED Constant Off to Constant On**



**Figure 4. LT3967 Down Transition Dimming Curve from LED Constant On to Constant Off**

$T_{RTSYN} \cdot M \cdot 2048$ , where M is the number of PWM dimming cycles running for each transitional step, which can be programmed to 1, 2, 4, 8, 16, 24 or 31 for dimming with fade transition. When M is programmed to 0, the channel LED dimming functions without fade transition.

### LT3967 I<sup>2</sup>C REGISTERS

The LT3967 has nine command registers (see Table 1 and Table 2) and two read-only fault status registers (see Table 3). The command registers are used to store the configuration bits sent by a master. The fault status registers are used to store the LED/overheat fault status bits. Both the command registers and the fault status registers can be read by the master.

### LT3967 COMMAND REGISTERS AND CHANNEL CONTROL

Upon the  $V_{DD}$  POR or an I<sup>2</sup>C bus timeout, each channel switch state is initialized according to the ACMREG register default value, which is determined by resistor settings at the address select pins. After data is received from a bus master, each channel switch is controlled either by the ACMODE register or by the channel SCMREG register, depending on which register has been last updated (see Figure 5). If SCMODE registers are dominant, the data in the ACMODE register is retained until it is overwritten or a POR/timeout occurs. Information about I<sup>2</sup>C bus timeout can be found in the Watchdog Timeout Reset section.

### I<sup>2</sup>C SERIAL INTERFACE

The LT3967 communicates through an I<sup>2</sup>C serial interface. The I<sup>2</sup>C serial interface is a 2-wire open-drain interface supporting multiple slaves and multiple masters on a single bus. Each device on the I<sup>2</sup>C bus is recognized by a unique address stored in the device and can only operate either as a transmitter or receiver, depending on the function of the device. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit the transfer. Devices addressed by the master are considered slaves. The LT3967 can only be addressed as a slave. Once addressed, it can receive configuration data

**Table 1. All Channel Mode (ACMODE) Command Register (8 Bits Long. See All Channel Mode (ACMODE) Command section for how to access this register)**

NAME	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	DEFAULT
ACMREG	Control Bit for CH8 1: LED On 0: LED Off	Control Bit for CH7 1: LED On 0: LED Off	Control Bit for CH6 1: LED On 0: LED Off	Control Bit for CH5 1: LED On 0: LED Off	Control Bit for CH4 1: LED On 0: LED Off	Control Bit for CH3 1: LED On 0: LED Off	Control Bit for CH2 1: LED On 0: LED Off	Control Bit for CH1 1: LED On 0: LED Off	AABCCDD (see Note at bottom of next page)

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**Table 2. Single Channel Mode (SCMODE) Command Registers (16 Bits Long. See Single Channel Mode (SCMODE) Command section for how to access these register bits)**

NAME	B[15] OPEN LED THRESHOLD PROGRAMMABLE BITS	B[14] SHORTED LED THRESHOLD PROGRAMMABLE BITS	B[13:11] FADE TIME MULTIPLIER PROGRAMMABLE BITS	B[10] FADING DONE INDICATOR (READ ONLY)	B[9] ASYNC. ON/OFF BIT	B[8] ASYNC. ENABLE BIT	B[7:0] DIMMING VALUE	DEFAULT
SCMREG1 (for CH1, the channel address: 000)	VOTH = 0: 6.1V/5.5V 1: 11.4V/10.8V	VSTH = 0: 1V 1: 4V	FTM[2:0] = 000: No Fade 001: 1x; 010:2x 011: 4x; 100:8x 101: 16x; 110:24x 111: 31x	FDI = 0: In Fading 1: Fading Done	AO = 0: LED Off 1: LED On	AE = 0: Async. Disabled 1: Async. Enabled	DV[7:0] = 00000000: LED Off 00000001: 1/256 Dimming 00000010: 2/256 Dimming ..... 11111110: 254/256 Dimming 11111111: LED Constant On	10000100 DDDDDDDD  (see Note)
SCMREG2 (for CH2, the channel address: 001)	VOTH = 0: 6.1V/5.5V 1: 11.4V/10.8V	VSTH = 0: 1V 1: 4V	FTM[2:0] = 000: No Fade 001: 1x; 010:2x 011: 4x; 100:8x 101: 16x; 110:24x 111: 31x	FDI = 0: In Fading 1: Fading Done	AO = 0: LED Off 1: LED On	AE = 0: Async. Disabled 1: Async. Enabled	DV[7:0] = 00000000: LED Off 00000001: 1/256 Dimming 00000010: 2/256 Dimming ..... 11111110: 254/256 Dimming 11111111: LED Constant On	10000100 DDDDDDDD  (see Note)
SCMREG3 (for CH3, the channel address: 010)	VOTH = 0: 6.1V/5.5V 1: 11.4V/10.8V	VSTH = 0: 1V 1: 4V	FTM[2:0] = 000: No Fade 001: 1x; 010:2x 011: 4x; 100:8x 101: 16x; 110:24x 111: 31x	FDI = 0: In Fading 1: Fading Done	AO = 0: LED Off 1: LED On	AE = 0: Async. Disabled 1: Async. Enabled	DV[7:0] = 00000000: LED Off 00000001: 1/256 Dimming 00000010: 2/256 Dimming ..... 11111110: 254/256 Dimming 11111111: LED Constant On	10000100 CCCCCCCC  (see Note)
SCMREG4 (for CH4, the channel address: 011)	VOTH = 0: 6.1V/5.5V 1: 11.4V/10.8V	VSTH = 0: 1V 1: 4V	FTM[2:0] = 000: No Fade 001: 1x; 010:2x 011: 4x; 100:8x 101: 16x; 110:24x 111: 31x	FDI = 0: In Fading 1: Fading Done	AO = 0: LED Off 1: LED On	AE = 0: Async. Disabled 1: Async. Enabled	DV[7:0] = 00000000: LED Off 00000001: 1/256 Dimming 00000010: 2/256 Dimming ..... 11111110: 254/256 Dimming 11111111: LED Constant On	10000100 CCCCCCCC  (see Note)
SCMREG5 (for CH5, the channel address: 100)	VOTH = 0: 6.1V/5.5V 1: 11.4V/10.8V	VSTH = 0: 1V 1: 4V	FTM[2:0] = 000: No Fade 001: 1x; 010:2x 011: 4x; 100:8x 101: 16x; 110:24x 111: 31x	FDI = 0: In Fading 1: Fading Done	AO = 0: LED Off 1: LED On	AE = 0: Async. Disabled 1: Async. Enabled	DV[7:0] = 00000000: LED Off 00000001: 1/256 Dimming 00000010: 2/256 Dimming ..... 11111110: 254/256 Dimming 11111111: LED Constant On	10000100 BBBBBBBB  (see Note)
SCMREG6 (for CH6, the channel address: 101)	VOTH = 0: 6.1V/5.5V 1: 11.4V/10.8V	VSTH = 0: 1V 1: 4V	FTM[2:0] = 000: No Fade 001: 1x; 010:2x 011: 4x; 100:8x 101: 16x; 110:24x 111: 31x	FDI = 0: In Fading 1: Fading Done	AO = 0: LED Off 1: LED On	AE = 0: Async. Disabled 1: Async. Enabled	DV[7:0] = 00000000: LED Off 00000001: 1/256 Dimming 00000010: 2/256 Dimming ..... 11111110: 254/256 Dimming 11111111: LED Constant On	10000100 BBBBBBBB  (see Note)
SCMREG7 (for CH7, the channel address: 110)	VOTH = 0: 6.1V/5.5V 1: 11.4V/10.8V	VSTH = 0: 1V 1: 4V	FTM[2:0] = 000: No Fade 001: 1x; 010:2x 011: 4x; 100:8x 101: 16x; 110:24x 111: 31x	FDI = 0: In Fading 1: Fading Done	AO = 0: LED Off 1: LED On	AE = 0: Async. Disabled 1: Async. Enabled	DV[7:0] = 00000000: LED Off 00000001: 1/256 Dimming 00000010: 2/256 Dimming ..... 11111110: 254/256 Dimming 11111111: LED Constant On	10000100 AAAAAAAA  (see Note)
SCMREG8 (for CH8, the channel address: 111)	VOTH = 0: 6.1V/5.5V 1: 11.4V/10.8V	VSTH = 0: 1V 1: 4V	FTM[2:0] = 000: No Fade 001: 1x; 010:2x 011: 4x; 100:8x 101: 16x; 110:24x 111: 31x	FDI = 0: In Fading 1: Fading Done	AO = 0: LED Off 1: LED On	AE = 0: Async. Disabled 1: Async. Enabled	DV[7:0] = 00000000: LED Off 00000001: 1/256 Dimming 00000010: 2/256 Dimming ..... 11111110: 254/256 Dimming 11111111: LED Constant On	10000100 AAAAAAAA  (see Note)

Note: Default values of A, B, C and D are determined by resistor at ADDR4, ADDR3, ADDR2 and ADDR1 pins respectively. A, B, C or D is set to 0 if the resistor to GND/VDD is 5kΩ or less, or is set to 1 if the values resistor to GND/VDD is between 50kΩ and 150kΩ.

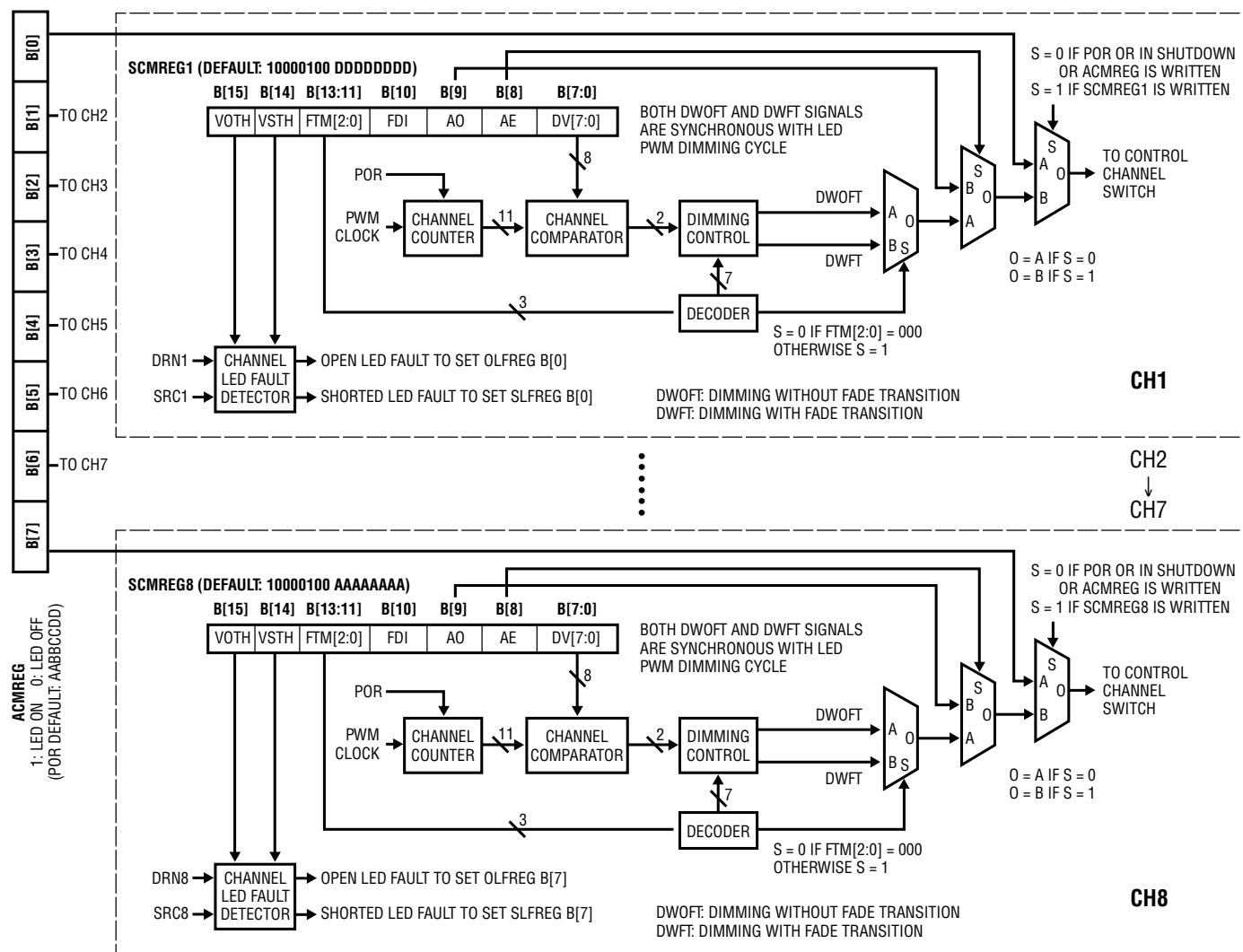


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**Table 3. Read-Only Fault Status Register (See All Channel Mode (ACMODE) Command section for how to access these register bits)**

NAME	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	DEFAULT
OLFREG	Open LED Status Bit for CH8 1: Fault 0: No Fault	Open LED Status Bit for CH7 1: Fault 0: No Fault	Open LED Status Bit for CH6 1: Fault 0: No Fault	Open LED Status Bit for CH5 1: Fault 0: No Fault	Open LED Status Bit for CH4 1: Fault 0: No Fault	Open LED Status Bit for CH3 1: Fault 0: No Fault	Open LED Status Bit for CH2 1: Fault 0: No Fault	Open LED Status Bit for CH1 1: Fault 0: No Fault	00000000
SLFREG	Shorted LED Status Bit for CH8 1: Fault 0: No Fault	Shorted LED Status Bit for CH7 1: Fault 0: No Fault	Shorted LED Status Bit for CH6 1: Fault 0: No Fault	Shorted LED Status Bit for CH5 1: Fault 0: No Fault	Shorted LED Status Bit for CH4 1: Fault 0: No Fault	Shorted LED Status Bit for CH3 1: Fault 0: No Fault	Shorted LED Status Bit for CH2 1: Fault 0: No Fault	Shorted LED Status Bit for CH1 1: Fault 0: No Fault	00000000

Note: The LT3967 sets all OLFREG and SLFREG register bits high, with ALERT pin asserted ( pulled low) to indicate the overheat fault condition ( $\geq 170^{\circ}\text{C}$ ) (See LED/Overheat Fault Detection and Reporting section for detail), with ALERT pin deasserted (pulled high) to indicate the IC is in shutdown condition (See Operation in Shutdown Condition section for detail). If the two conditions are concurrent, the shutdown condition dominates.



**Figure 5. LT3967 Command Registers and Channel Control Diagram**

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or transmit register contents. The serial clock line (SCL) is always an input to the LT3967 and the serial data line (SDA) is bidirectional. The LT3967 can only pull the serial data line (SDA) LOW and can never drive it HIGH. SCL and SDA are required to be externally connected to the  $V_{DD}$  supply through a pull-up resistor. When the data line is not being driven LOW, it is HIGH. Data on the I<sup>2</sup>C bus can be transferred at rates up to 100kbits/s in the standard mode and up to 400kbits/s in the fast mode.

### THE START AND STOP CONDITIONS

When the bus is idle, both SCL and SDA must be HIGH. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from HIGH to LOW while SCL is HIGH. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from LOW to HIGH while SCL is HIGH. The bus is then free for another transmission. However, if the master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address the same or another slave without first generating a STOP condition. When the bus is in use, it stays busy if a repeated START (Sr) is generated instead of a STOP condition. The repeated START (Sr) conditions are functionally identical to the START (S). Various combinations of read/write commands are then possible within such a transfer, except that the BCMODE write command for dimming cycle synchronization and the BCMODE read command for alert inquiry and the ACMODE write command for clearing the overheat fault bits must be self contained with a terminating STOP condition.

### I<sup>2</sup>C SERIAL PORT DATA TRANSFER

After the START condition, the I<sup>2</sup>C bus is busy and data transfer can begin between the master and the addressed LT3967 slave. Data is transferred over the bus in group of nine bits, one byte followed by one acknowledge (ACK) bit. The acknowledge signal is used for handshaking between the master and the slave.

A Packet Error Checking (PEC) mechanism is implemented in the LT3967 to improve I<sup>2</sup>C communication reliability. This mechanism requires that a PEC byte (or CRC-8 checksum), which is calculated over the entire

message frame including the address and read/write bit, is always appended at the end of each ACMODE or SCMODE command. The polynomial used for the PEC byte calculation is  $x^8 + x^2 + x + 1$  (initialized to zero). Both the transmitter and the receiver need to calculate a PEC byte. The transmitter sends its PEC byte derived from the read/write address and subsequent outgoing data bytes. The receiver calculates its own PEC byte from the read/write address and subsequent incoming data bytes, and compares it with the received one. A PEC-byte mismatch guarantees that an error has occurred during the transaction. A PEC-byte match suggests a reasonable likelihood of the command being received correctly, as long as the same polynomial is used. Example Linduino code for calculating CRC-8 PEC is provided (see next page).

When the LT3967 is written to, it acknowledges its device write address and subsequent data bytes. It acknowledges the PEC byte if the PEC bytes match. Otherwise it does not acknowledge it. The received data bytes are validated and transferred to internal holding latches upon the return of the acknowledgment of the PEC byte by the LT3967. The received data bytes are regarded as void by the LT3967 in case of mismatch. If desired, a repeated START (Sr) condition may be initiated by the master to address another device on the I<sup>2</sup>C bus or another register in the same device for data transfer. The LT3967 remembers the valid data it has received. Once selected channels of the devices on the I<sup>2</sup>C bus have been addressed and sent valid data, the master issues a STOP condition to finish the communication. The LT3967 will update its command registers with the data it has validated upon the STOP condition, except that the VOTH and VSTH bits are updated in the channel SCMREG command register upon the return of the acknowledgment of the PEC byte by the LT3967.

When reading from the LT3967, the master initiates the command by issuing a read address. The LT3967 acknowledges its device read address and responds with subsequent data bytes plus a PEC byte. The master is not required to acknowledge the data/PEC bytes.

The master can free the I<sup>2</sup>C bus by issuing a STOP condition after the data transfer. If desired the master can verify the data bytes written to the internal holding latches prior to updating them to the command registers by reading them back before sending a STOP condition.

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```
// Bytewise CRC-8 for LT3967 using X8 + X2 + X + 1
// Takes a running sum (or 0) as <in>, and current byte to CRC as <data>
// Returns the CRC-8 of <in> and <data> for sending or further CRC'ing
int8_t doCRC(int8_t in, int8_t data){
    int8_t crc;
    int8_t i;
    crc = in ^ data;           // XOR the incoming bytes
    for(i = 0; i < 8; i++){   // Step through each bit
        if (crc & 0x80) {     // If MSB is set
            crc <<= 1;        // Shift up, then
            crc ^= 0x07;      // XOR with the low byte of polynomial
        } else {              // If MSB is unset
            crc <<= 1;        // Simply shift up
        }
    }                          // Repeat for rest of bits
    return crc;               // Finally, send back the result
}
```

```
// Usage of ACMODE Write Protocol,
// where CHIPADDR and DATA are the bytes to send to LT3967
int8_t myCRC;
myCRC = doCRC(0, CHIPADDR);
myCRC = doCRC(myCRC, DATA);
// myCRC now holds the completed PEC byte for sending to LT3967
```

```
// Usage of SCMODE Write Short Format Protocol,
// where CHIPADDR and DATA are the bytes to send to LT3967
int8_t myCRC;
myCRC = doCRC(0, CHIPADDR);
myCRC = doCRC(myCRC, DATA);
// myCRC now holds the completed PEC byte for sending to LT3967
```

```
// Usage of SCMODE Write Long Format Protocol,
// where CHIPADDR, DATA1, and DATA2 are the bytes to send to LT3967
int8_t myCRC;
myCRC = doCRC(0, CHIPADDR);
myCRC = doCRC(myCRC, DATA1);
myCRC = doCRC(myCRC, DATA2);
// myCRC now holds the completed PEC byte for sending to LT3967
```

### Example Linduino® Code for Calculating CRC-8 PEC

## APPLICATIONS INFORMATION

### LT3967 I<sup>2</sup>C COMMANDS AND WRITE/READ PROTOCOLS

Only a master can issue an I<sup>2</sup>C command to start a write or read operation. The first command byte is always an I<sup>2</sup>C device address sent by a master. If the master issues a write command, all the remaining bytes of the command will be transmitted by the master. If the master issues a read command, all the remaining bytes of the command will be transmitted by the addressed LT3967 slave. The LT3967 I<sup>2</sup>C commands can be divided into three categories based on their purposes:

#### 1) All Channel Mode (ACMODE) Command

The ACMODE write command (see Figure 6) is used to set the ACMREG register bits (see Table 1) to control the eight channel switches together. The command is three bytes long including the PEC byte. The first byte is the ACMODE device write address and the second byte is the data byte to be written to the ACMREG register. Please note the ACMODE write command also updates DV[7:0] (B[7:0] in channel SCMREG register) accordingly for each channel for the purpose of dimming without flicker.

The ACMODE read command (see Figure 7) is used to read back the ACMREG register bits and to get the LED and overheat fault conditions. The command is five bytes long including the PEC byte. The first byte is the ACMODE device read address followed by three data bytes read respectively from the ACMREG register, the OLFREG register and the SLFREG register.

The LT3967 ACMODE device address is 010A<sub>4</sub>A<sub>3</sub>A<sub>2</sub>A<sub>1</sub> followed by an eighth bit which is a data direction bit (R/W) — a 0 indicates a write transmission (the master writes to the addressed LT3967), a 1 indicates a read transmission (the master reads from the addressed LT3967). A<sub>4</sub>A<sub>3</sub>A<sub>2</sub>A<sub>1</sub> is an input logic value from the programmable address select pins ADDR4, ADDR3, ADDR2 and ADDR1. The input logic value is 0/1 if the address select pin is connected to GND/V<sub>DD</sub> through a 150kΩ resistor or less.

#### ACMODE Write Command Latency

The ACMODE write command can be conveniently used for quick status control of the eight channel LEDs. Each ACMODE write command is three bytes long and takes about 70μs to transmit if 400kHz SCL clock is chosen. The command latency between the STOP condition and channel switching on (LED turning off) is about 1.2μs, and the command latency between the STOP condition and channel switching off (LED turning on) is about 2μs. Therefore, the minimum time from initiating to executing an ACMODE write command is about 73μs if 400kHz SCL clock is used.

#### ACMODE Write Command and Simultaneous Channel Switching

The ACMODE write command can control all 8 channels to switch together. It is possible to switch all LEDs from on/off to off/on simultaneously using a single ACMODE write command. A fast LED driver can respond well to a

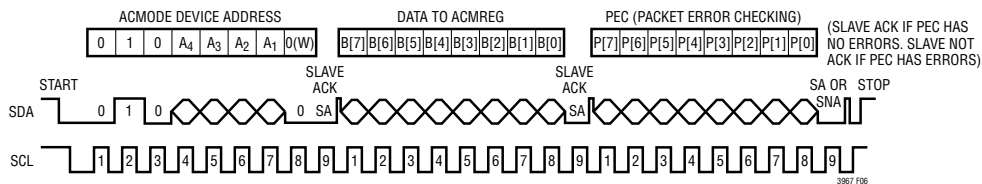


Figure 6. LT3967 I<sup>2</sup>C Serial Port ACMODE Write Protocol

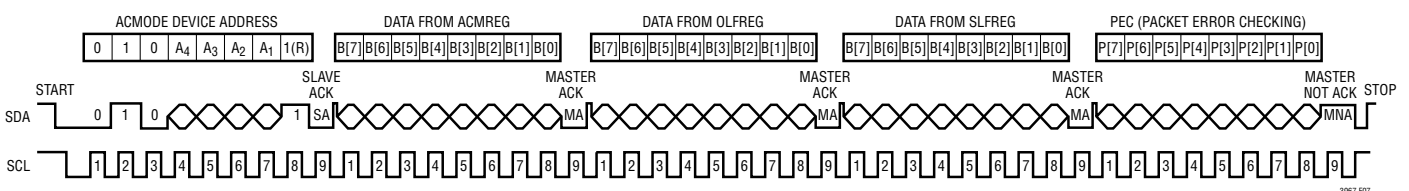


Figure 7. LT3967 I<sup>2</sup>C Serial Port ACMODE Read Protocol

## APPLICATIONS INFORMATION

sudden output voltage change caused by simultaneous channel switching. An LED driver with slower response may trigger false faults due to large transients in the string current. When working with a slow LED driver, you should avoid sending an ACMODE write command which can cause simultaneous channel switching. Instead you can use multiple ACMODE write commands, and each of them makes one channel switch at a time.

### 2) Single Channel Mode (SCMODE) Command

The SCMODE write command is used for setting the addressed channel SCMREG register bits to control the channel switch and to set the channel LED fault detecting thresholds.

The SCMODE write command has two formats: short format (see Figure 8) and long format (see Figure 9). Both the formats configure the channel SCMREG register. Choosing the short format or the long format depends on which bits of the channel SCMREG register you want to configure.

The SCMODE write command short format can program the channel open LED threshold by setting  $V_{OTH}$  (B[15]) and the channel shorted LED threshold by setting  $V_{STH}$  (B[14]). When asynchronous operation is enabled by setting AE (B[8]) to 1, the channel LED can be set to constant off or constant on immediately with AO (B[9]) set to 0 or 1.

Unlike the dimming operation, turning on and turning off of the channel LED are not synchronized with the channel dimming cycle for asynchronous operation. Please note the SCMODE write command short format with AE set to 1 will overwrite the channel's DV[7:0] (B[7:0]) with all ones or all zeros according to received AO value for the purpose of dimming without flicker. The SCMODE write command long format can program the fade time multiplier by setting FTM[2:0] (B[13:11]) and disable asynchronous operation by setting AE (B[8]) to 0 and set a new dimming value by updating DV[7:0] (B[7:0]).

The SCMODE write command short format is three bytes long including the PEC byte (see Figure 8). The first byte is the SCMODE device write address. The second byte consists of 3 sections—the first section (bit 7) must be 0 to indicate the short format, the second section (bit 6, bit 5 and bit 4) is the channel address indicating which channel SCMREG register is written to, the last section is the configuration data (bit 3 for VOTH, bit 2 for VSTH, bit 1 for AO and bit 0 for AE).

The SCMODE write command long format is four bytes long including the PEC byte (see Figure 9). The first byte is the SCMODE device write address. The second byte consists of 3 sections — the first section (bit 7) must be 1 to indicate the long format, the second section (bit 6, bit 5 and bit 4) is the channel address indicating which channel SCMREG register

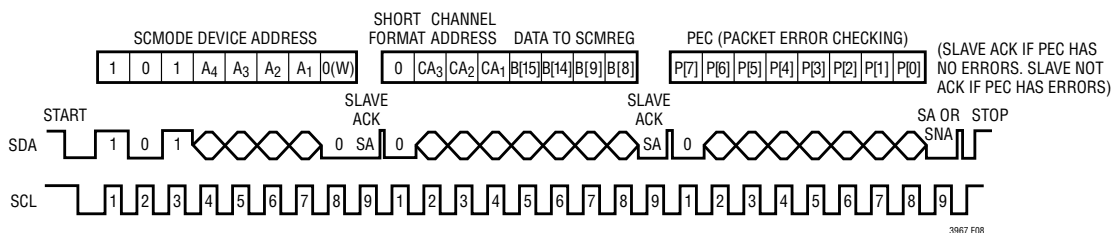


Figure 8. LT3967 I<sup>2</sup>C Serial Port SCMODE Write Short Format Protocol

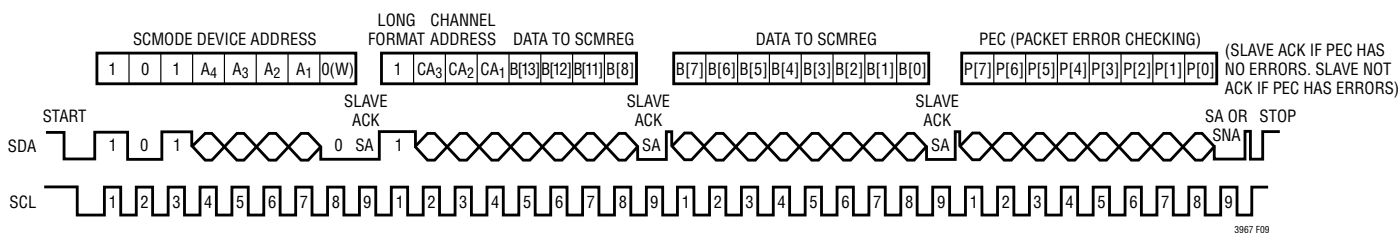


Figure 9. LT3967 I<sup>2</sup>C Serial Port SCMODE Write Long Format Protocol

## APPLICATIONS INFORMATION

is written to, the last section is the configuration data (bit 3, bit 2 and bit 1 for FTM[2:0] and bit 0 for AE). The third byte is the dimming value DV[7:0].

### Channel Open LED Threshold (V<sub>OTH</sub>) Programming

By using the SCMODE write command short format, you can program VOTH (B[15]) to 0 and 1 (default) to set the channel open LED threshold V<sub>OTH</sub> to 6.1V/5.5V and 11.4V/10.8V (default) respectively.

### Channel Shorted LED Threshold (V<sub>STH</sub>) Programming

By using the SCMODE write command short format, you can program VSTH (B[14]) to 0 (default) and 1 to set the channel shorted LED threshold V<sub>STH</sub> to 1V (default) and 4V respectively.

It is recommended to adjust the V<sub>OTH</sub> and V<sub>STH</sub> from their default values to the proper threshold levels based on LED-on voltage for each channel, once the application circuit is powered on.

### Channel PWM Dimming Fade Time Programming

By using the SCMODE write command long format, you can program FTM[2:0] (B[13:11]) to set the fade time multiplier. The fade time multiplier can be set to 0 (default), 1, 2, 4, 8, 16, 24 and 31 when FTM[2:0] bits are 000 (default), 001, 010, 011, 100, 101, 110 and 111 respectively (refer to Table 2, Figure 9 and Figure 5).

Fade time can be calculated using the formula:  $T_{FADE} = N \cdot T_{STEP} = N \cdot M \cdot T_{PWM} = N \cdot M \cdot T_{RTSYNC} \cdot 2048$ , where N is the number of transitional steps determined by the distance between the initial dimming value and the target dimming value. M is the programmed fade time multiplier which sets the number of PWM dimming cycles running for each transitional step. T<sub>STEP</sub>, T<sub>PWM</sub> and T<sub>RTSYNC</sub> represent the run time for one transitional step, one PWM dimming cycle and one RTSYNC input clock cycle respectively. When M is set to 0, the channel LED performs PWM dimming without fade transition.

The SCMODE read command (see Figure 10 and Figure 11) is used to read back the addressed channel SCMREG register bits. The SCMODE read command is four bytes long including the PEC byte. The first byte is the SCMODE device read address. The second byte comprises (from MSB to LSB) the open LED threshold bit V<sub>OTH</sub>, the shorted LED threshold bit V<sub>STH</sub>, the fade time multiplier FTM[2:0], the fading done indicator FDI which is a read-only bit used to indicate whether the fade process has ended or not, the asynchronous on/off bit AO and the asynchronous enable bit AE from the addressed SCMREG register. The third byte is the dimming value DV[7:0] from the addressed SCMREG register.

Unlike the SCMODE write command, the SCMODE read command does not contain the channel address. Actually the channel address received from the last SCMODE

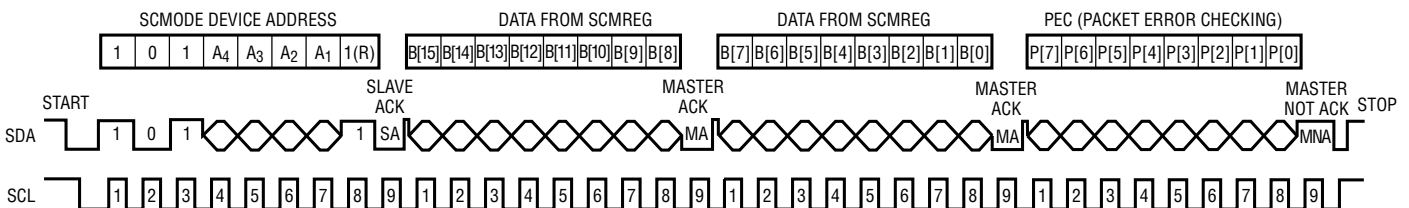


Figure 10. LT3967 I<sup>2</sup>C Serial Port SCMODE Read Protocol







## APPLICATIONS INFORMATION

if another device is sending an address at the same time using standard I<sup>2</sup>C bus arbitration. If the LT3967 is sending a 1 and reads a 0 on the SDA pin on the rising edge of SCL, it assumes another device with a lower address is sending and the LT3967 immediately aborts its transfer and waits for the next ARA cycle to try again. If transfer is successfully completed, the LT3967 will deassert its  $\overline{\text{ALERT}}$  pin and will not respond to further ARA requests until a new alert event occurs. Please note that the successfully completed ARA cycle deasserts the  $\overline{\text{ALERT}}$  pin only. It does not clear the fault status bit set in the OLFREG/SLFREG register.

### WATCHDOG TIMEOUT RESET

The LT3967 has a programmable watchdog timer designed to monitor I<sup>2</sup>C communications to make sure reliable connection between the master and the LT3967 slave. The WDI pin is used to set the watchdog upper boundary with a capacitor to GND. The watchdog starts monitoring the serial interface when  $V_{DD}$  transitions above 2.5V. A timeout occurs when the time between  $V_{DD}$  POR or START and STOP reaches the programmed watchdog upper boundary. Like the  $V_{DD}$  POR, the timeout event resets all LT3967 registers to the default value, and resets the PWM clock to the RTSYNC input clock. Each channel switch state is determined by resistor settings at ADDR[4:1] pins. In other words, watchdog timeout reset has the same initialization effect as  $V_{DD}$  POR reset.

For the customer who wants to know if the IC was reset by unexpected  $V_{DD}$  POR or watchdog timeout during normal operation, the following procedure is suggested: 1) Upon  $V_{DD}$  powered on, a unique data byte such as 10101010, which is different from the default determined by ADDR[4:1] resistor settings, should be immediately written to ACMREG register by using an ACMODE write command followed by 8 SCMODE write commands which configure channel dimming operation, and a STOP condition. 2) By reading ACMREG register periodically using an ACMODE read command at intervals less than the watchdog upper boundary (nominal 16ms with a 10nF capacitor), the customer is able to know if  $V_{DD}$  POR or watchdog timeout reset has unexpectedly occurred during normal

operation. ACMREG register reset to the default indicates  $V_{DD}$  POR or watchdog timeout has occurred. Otherwise it indicates the IC has been operating with neither  $V_{DD}$  POR nor watchdog timeout reset. Please note that the ACMODE write command mentioned in the procedure above should be used exclusively for detecting  $V_{DD}$  POR or watchdog timeout reset. It will not be used to set channel switch state in this case.

### RTSYNC INPUT CLOCK FAULT DETECTION AND ALERT ASSERTION

The PWM clock is required by the LT3967 to perform PWM dimming. The PWM clock is disabled as long as the LT3967 is disabled (ENH pin is undervoltage for  $V_{IN}$  supply). When the IC is being enabled, the PWM clock is set to the RTSYNC input clock coming either from the external clock source or from the  $R_{\text{TSYNC}}$  programmed internal oscillator. Besides the  $R_{\text{TSYNC}}$  programmed internal oscillator, the LT3967 provides an internal standby clock (100kHz nominal). When a RTSYNC clock fault is triggered upon the RTSYNC clock running slower than the internal standby clock, the PWM clock will be switched from the RTSYNC clock to the standby clock. If the external clock connection is lost, the PWM clock setting LED dimming will switch to the  $R_{\text{TSYNC}}$  programmed internal oscillator frequency without asserting  $\overline{\text{ALERT}}$  pin if a programming resistor  $R_{\text{TSYNC}}$  is connected between RTSYNC pin and GND. Otherwise the PWM clock will switch to the internal standby clock and  $\overline{\text{ALERT}}$  pin will be asserted. Once switched, the PWM clock remains with the standby clock until reset by  $V_{DD}$  POR, watchdog timeout or a BCMODE write command. The LT3967 asserts  $\overline{\text{ALERT}}$  pin to indicate the RTSYNC clock fault condition.  $\overline{\text{ALERT}}$  pin can be deasserted by  $V_{DD}$  POR, watchdog timeout, a BCMODE write command or a BCMODE read command which successfully sent the alert response address to the master.

### LED/OVERHEAT FAULT DETECTION AND REPORTING

The LT3967 detects and reports open LED, shorted LED and overheat fault conditions via  $\overline{\text{ALERT}}$  pin and I<sup>2</sup>C serial interface. (See the following sections for detail.)

## APPLICATIONS INFORMATION

### OPEN LED FAULT DETECTION AND ALERT ASSERTION

An open LED fault will be triggered when the voltage between the channel DRN pin and the channel SRC pin exceeds 13V (nominal) or when the voltage between the channel DRN pin and the channel SRC pin exceeds the programmed open LED threshold but less than 13V (nominal) for more than 15 $\mu$ s (nominal). Once an open LED fault is triggered in a channel, the fault status bit matching the channel will be set in the OLFREG status register, which will cause the  $\overline{\text{ALERT}}$  pin to be asserted (pulled down) and the channel switch to be turned on for the switch protection and to maintain continuity of the string for good LEDs. The switch can be turned off and PWM dimming reestablished by updating its registers with the serial interface.

### SHORTED LED FAULT DETECTION AND ALERT ASSERTION

A shorted LED fault will be triggered when the voltage between the channel DRN pin and the channel SRC pin falls below the programmed shorted LED threshold for more than 15 $\mu$ s (nominal). Once a shorted LED fault is triggered in a channel, the fault status bit matching the channel will be set in the SLFREG status register, which will cause the  $\overline{\text{ALERT}}$  pin to be asserted (pulled down). However, unlike the open LED fault, the channel switch will continue with the programmed PWM dimming.

### LED FAULT STATUS BIT CLEARANCE

The fault status bit set in the OLFREG/SLFREG register by an open/shorted LED fault can only be cleared by an ACMODE write command or a SCMODE write command accessing the channel. If the open/shorted LED fault no longer exists when the write command is updating the command register at the I<sup>2</sup>C STOP condition, the fault status bit matching the channel will be cleared and the  $\overline{\text{ALERT}}$  pin will be deasserted. Otherwise, the fault status bit will remain set, and the  $\overline{\text{ALERT}}$  pin will remain asserted or be asserted again if previously deasserted.

### OVERHEAT FAULT DETECTION AND ALERT ASSERTION

An overheat fault will be triggered when the IC temperature exceeds 170°C (nominal). Once an overheat fault is triggered, all status bits in both the OLFREG register and the SLFREG register will be set, which will cause the  $\overline{\text{ALERT}}$  pin to be asserted (pulled down) and all eight channel switches to be turned on (LEDs to be turned off) for cooling down the system.

### OVERHEAT STATUS BITS CLEARANCE

The fault status bits set in the OLFREG register and the SLFREG register by an overheat fault can only be cleared by an ACMODE write command with all 1s in its data byte. If the IC temperature is below 160°C (nominal) when the ACMODE write command is updating the ACMREG register at the I<sup>2</sup>C STOP condition, the fault status bits will be cleared and the  $\overline{\text{ALERT}}$  pin will be deasserted. Otherwise, the fault status bits will remain set, and the  $\overline{\text{ALERT}}$  pin will remain asserted or be asserted again if previously deasserted.

### ALERT DEASSERTION

The LT3967 deasserts the  $\overline{\text{ALERT}}$  pin in either of the following two situations:

- 1) The LT3967 has successfully completed the ARA procedure initiated by the master. Please note that the successfully completed ARA procedure does not clear fault status bits. It only deasserts the  $\overline{\text{ALERT}}$  pin.
- 2) The LT3967 has received an ACMODE or SCMODE command which cleared the fault status bits, resulting in the  $\overline{\text{ALERT}}$  pin deassertion.

### PRINTED CIRCUIT BOARD LAYOUT

When laying out the printed circuit board, the following checklist should be followed to ensure proper operation of the LT3967:

1. Connect the exposed pad of the package (Pin 29) directly to a large ground plane to minimize thermal and electrical impedance.

## APPLICATIONS INFORMATION

2. Keep the LED connection traces as short as possible.
3. Place power supply bypass capacitors as close as possible to the supply pins.
4. Place the  $R_{TSYNC}$  resistor as close as possible to the IC if a resistor is used to set LED dimming frequency.
5. Place the WDI capacitor as close as possible to the IC if the watchdog function is used.

### Long Wires or Cables Between LT3967 and LEDs

The best practice is to place the LT3967 and the LEDs it controls on the same PCB and to keep LED connection traces as short as possible. Long wires (>>10cm) between the LT3967 and the LEDs introduce parasitic inductance that leads to an underdamped RLC response (ringing) in the switching voltage when channel is switching on and off. A meter of 30-gage wire can introduce about  $1\mu\text{H}$  of parasitic inductance. The ringing can trigger open LED protection due to false open LED detection, and cause the channel to bypass good LEDs. In extreme cases, the ringing may exceed absolute maximum ratings and damage the part. The parasitic inductance also generates a step voltage waveform (relative to GND) at the switches at the frequency of the switching regulator. The magnitude of this step waveform depends upon the current ripple in the source and the parasitic inductance. The fast edges

of the step waveform can cause unintended toggling of the LT3967's switches.

RC snubber circuits (shown in Figure 14) can suppress the ringing and allow use of wires up to 1 meter with no false fault detection. The snubber should be placed close to the IC. Please note that an 8-LED string requires 9 snubbers: one snubber across each of the 8 switches and a snubber across all 8 switches (R9, C9). The 9th snubber (R9, C9) softens the stepped waveform edges. With the snubbers, the LT3967 can control the LEDs through a 1 meter ribbon cable (9 wires total) passing 1.3A with no false faults detected. The snubber value shown here is good for most applications.

### Schottky Clamping Diode for LT3967 Protection

For the boost-buck mode application titled Matrix LED Dimmer Powered by a Dual Buck Mode LED Driver with a Boost Pre-Regulator in the following Typical Applications section, where the voltage at the LED string bottom (LED1<sup>-</sup> node and LED2<sup>-</sup> node) may go below 0V, a Schottky clamping diode (D8 and D9) connecting the IC ground to the LED string bottom is required to keep  $\text{SRC} \geq -0.3\text{V}$ . A Schottky clamping diode (D6 and D7) connecting the top of the LED string (LED1<sup>+</sup> node and LED2<sup>+</sup> node) to the  $V_{\text{IN}}$  pin is required to guarantee that the absolute maximum rating  $V_{\text{IN}} - \text{SRC} \geq -0.3\text{V}$  is met.

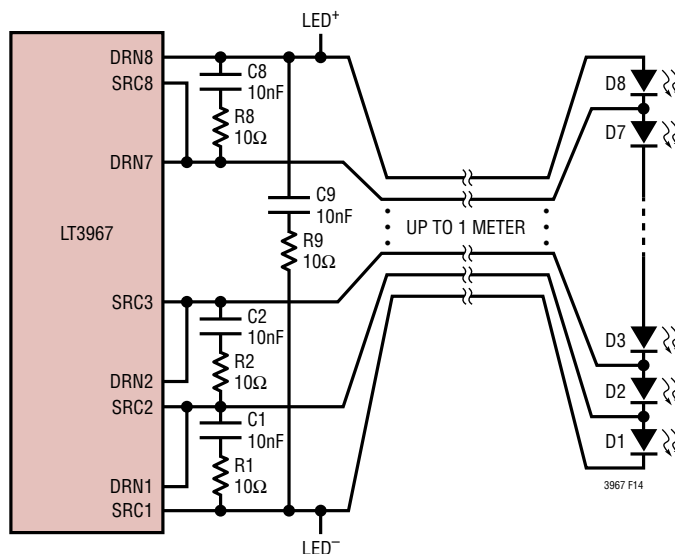
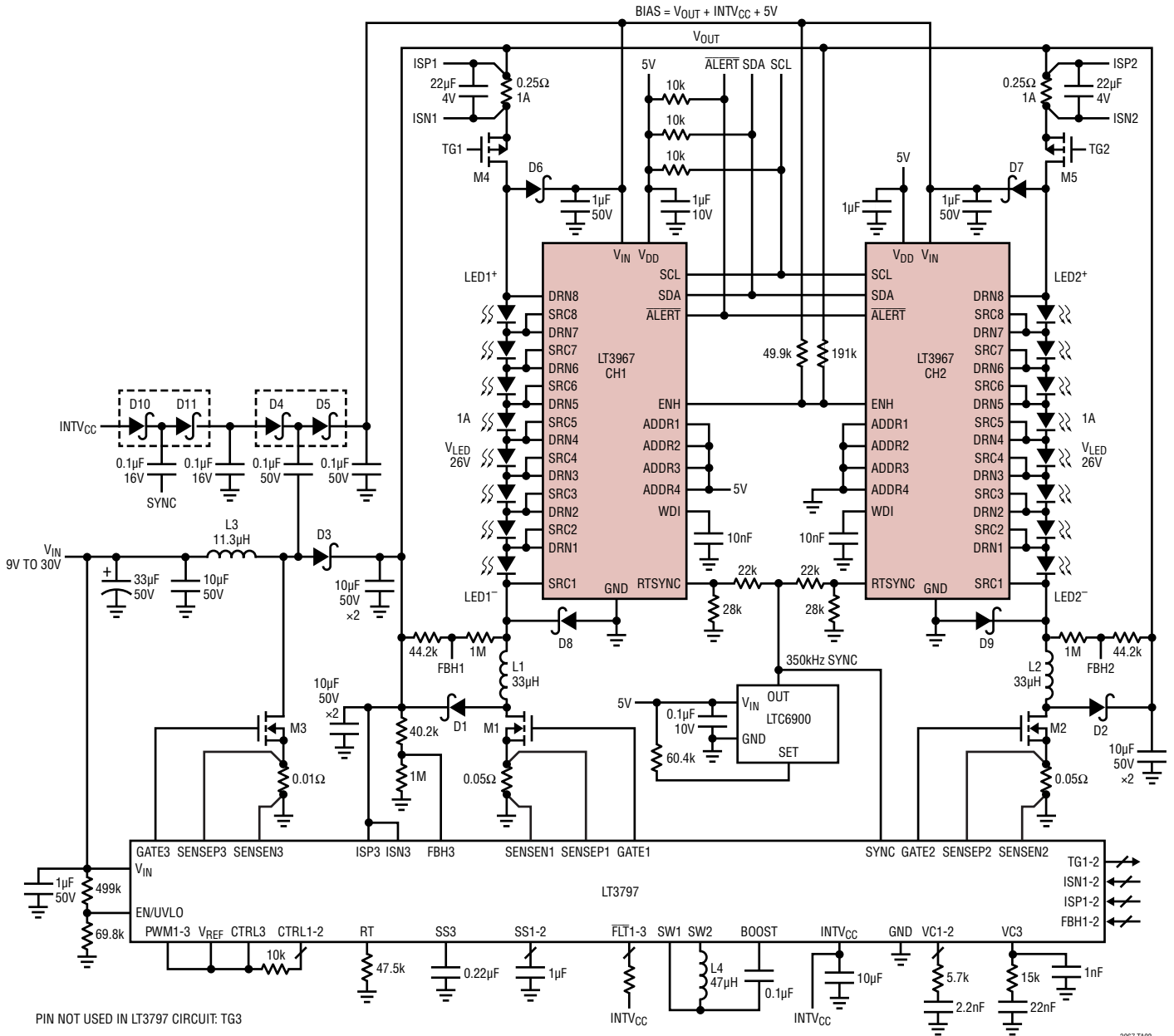


Figure 14. RC Snubbers in Long Wire Application

TYPICAL APPLICATIONS

Matrix LED Dimmer Powered by a Dual Buck Mode LED Driver with a Boost Pre-Regulator



PIN NOT USED IN LT3797 CIRCUIT: TG3

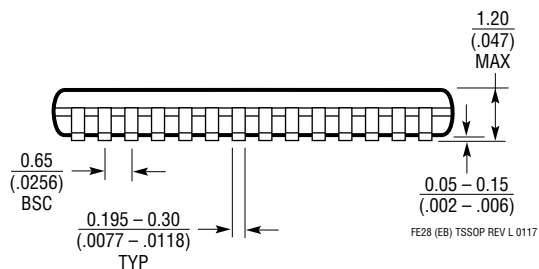
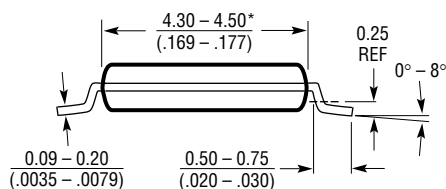
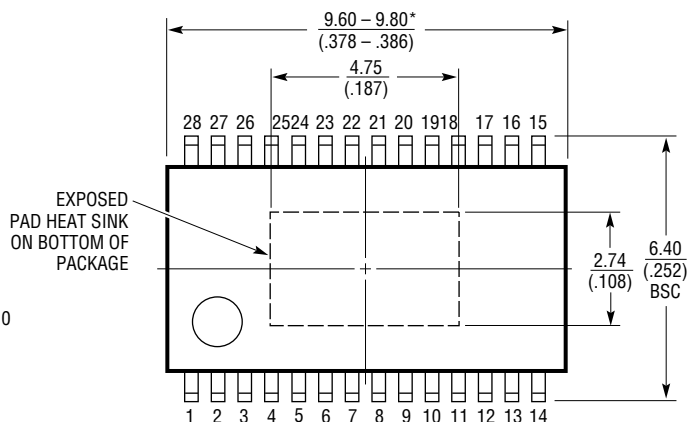
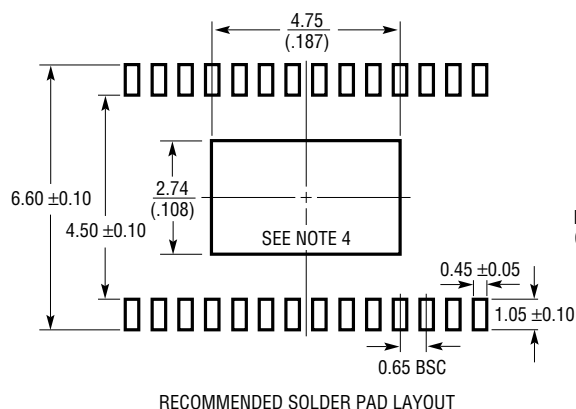
PIN NOT USED IN LTC6900 CIRCUIT: DIV

- L1, L2: WURTH ELECTRONICS 7447789133
- L3: WURTH ELECTRONICS 7443551111
- L4: COOPER BUSSMANN SD25-470-R
- D1, D2: DIODES DFLS260
- D3: DIODES PDS760
- D4, D5, D10, D11: CENTRAL SEMI CMPD6263S 2 IN 1 PACKAGE
- D6, D7: NXP SEMI PMEG6010CEH
- D8, D9: NXP SEMI PMEG4010CEH
- M1, M2: VISHAY Si7308DN
- M3: INFINEON BSC097N06
- M4, M5: VISHAY Si7309DN

3967 TA02

# PACKAGE DESCRIPTION

**FE Package**  
**28-Lead Plastic TSSOP (4.4mm)**  
 (Reference LTC DWG # 05-08-1663 Rev L)  
**Exposed Pad Variation EB**



- NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
  2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
  3. DRAWING NOT TO SCALE
  4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
- \*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE



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[NCL30086BDR2G](#) [CAT4004BHU2-GT3](#) [LV52207AXA-VH](#) [AP1694AS-13](#) [TLE4242EJ](#) [AS3688](#) [IS31LT3172-GRLS4-TR](#) [TLD2311EL](#)  
[KTD2694EDQ-TR](#) [KTZ8864EJAA-TR](#) [IS32LT3174-GRLA3-TR](#) [MP2488DN-LF-Z](#) [NLM0010XTSA1](#) [AL1676-20BS7-13](#)  
[ZXLD1370QESTTC](#) [MPQ7220GF-AEC1-P](#) [MPQ7220GR-AEC1-P](#) [MPQ4425BGJ-AEC1-P](#) [MPQ7220GF-AEC1-Z](#) [MPQ7220GR-AEC1-Z](#)  
[MPQ4425BGJ-AEC1-Z](#) [IS31FL3737B-QFLS4-TR](#) [IS31FL3239-QFLS4-TR](#) [KTD2058EUAC-TR](#) [KTD2037EWE-TR](#) [DIO5662ST6](#)  
[KTD2026BEWE-TR](#) [MAX20052CATC/V+](#) [MAX25606AUP/V+](#) [BD6586MUV-E2](#) [BD9206EFV-E2](#) [LYT4227E](#) [LYT6079C-TL](#)  
[MP3394SGF-P](#) [MP4689AGN-P](#) [MPQ4425AGQB-AEC1-Z](#)