LTPoE++/PoE+/PoE PD Forward/Flyback Controller

FEATURES

- **IEEE802.3af/at and LTPoE++™ 90W Powered Device (PD) with Forward/Flyback Controller**
- **LT4276A Supports All of the Following Standards:**
  - **LTPoE++ 38.7W, 52.7W, 70W and 90W**
  - **IEEE 802.3at 25.5W Compliant**
  - **IEEE 802.3af up to 13W Compliant**
- **LT4276B is IEEE 802.3at/af Compliant**
- **LT4276C is IEEE 802.3af Compliant**
- **Superior Surge Protection (100V Absolute Maximum)**
- **Wide Junction Temperature Range (–40°C to 125°C)**
- Auxiliary Power Support as Low as 9V
- No Opto-Isolator Required for Flyback Operation
- External Hot Swap™ N-Channel MOSFET for Lowest Power Dissipation and Highest System Efficiency
- >94% End-to-End Efficiency with LT4321 Ideal Bridge
- Available in a 28-Lead 4mm × 5mm QFN Package

APPLICATIONS

- High Power Wireless Data Systems
- Outdoor Security Camera Equipment
- Commercial and Public Information Displays
- High Temperature Applications

DESCRIPTION

The LT®4276 is a pin-for-pin compatible family of IEEE 802.3 and LTPoE++ Powered Device (PD) controllers. It includes an isolated switching regulator controller capable of synchronous operation in both forward and flyback topologies with auxiliary power support.

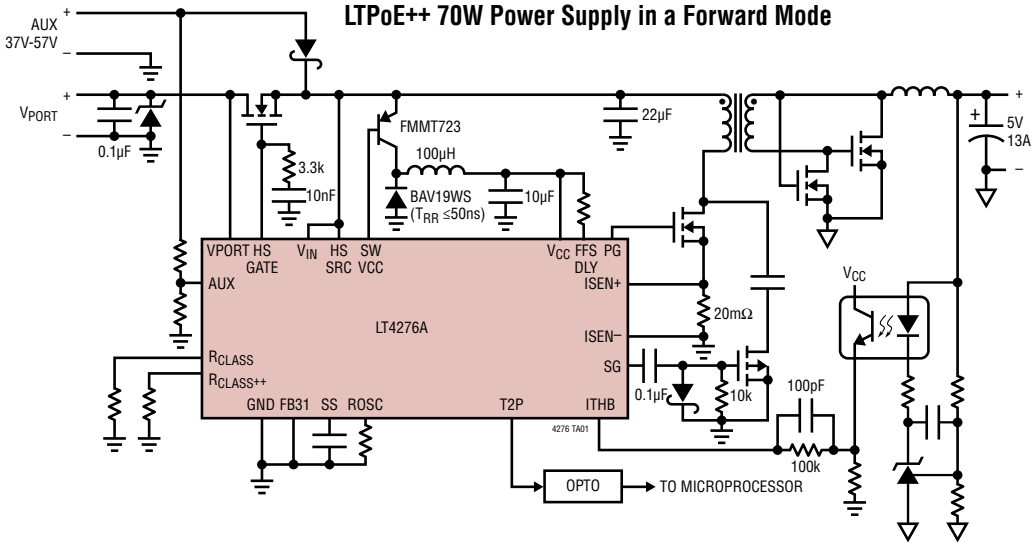
The LT4276A employs the LTPoE++ classification scheme, receiving 38.7W, 52.7W, 70W or 90W of power at the PD RJ45 connector, and is backwards compatible with IEEE 802.3. The LT4276B is a fully 802.3at compliant, 25.5W Type 2 (PoE+) PD. The LT4276C is a fully 802.3af compliant, 13W Type 1 (PoE) PD.

The LT4276 supports both forward and flyback power supply topologies, configurable for a wide range of PoE applications. The flyback topology supports No-Opto feedback. Auxiliary input voltage can be accurately sensed with just a resistor divider connected to the AUX pin.

The LT4276 utilizes an external, low $R_{DS(ON)}$ N-channel MOSFET for the Hot Swap function, maximizing power delivery and efficiency, reducing heat dissipation, and easing the thermal design.

TYPICAL APPLICATION

LTPoE++ 70W Power Supply in a Forward Mode



LT4276 Family

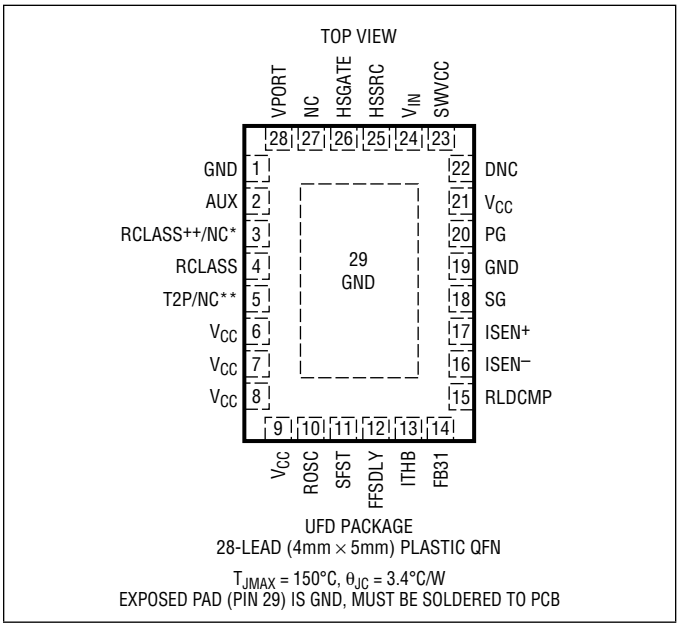
MAX DELIVERED POWER	LT4276 GRADE A	B	C
LTPoE++ 90W	●		
LTPoE++ 70W	●		
LTPoE++ 52.7W	●		
LTPoE++ 38.7W	●		
25.5W	●	●	
13W	●	●	●

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

VPORT, HSSRC, V_{IN} Voltages .....–0.3 to 100V
HSGATE Current..... ±20mA
V_{CC} Voltage..... –0.3 to 8V
RCLASS, RCLASS++
Voltages.....–0.3 to 8V (and ≤ VPORT)
SFST, FFSDLY, ITHB, T2P Voltages .....–0.3 to V_{CC}+0.3V
ISEN+, ISEN– Voltages.....±0.3V
FB31 Voltage.....+12V/–30V
RCLASS/RCLASS++ Current ..... –50mA
AUX Current.....±1.4mA
ROSC Current .....±100µA
RLDCMP Current .....±500µA
T2P Current.....–2.5mA
Operating Junction Temperature Range (Note 3)
LT4276AI/LT4276BI/LT4276CI.....–40°C to 85°C
LT4276AH/LT4276BH/LT4276CH ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JC} = 3.4°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

*RCLASS++ is not connected in the LT4276B and LT4276C
**T2P is not connected in the LT4276C

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	MAX PD POWER	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT4276AIUFD#PBF	LT4276AIUFD#TRPBF	4276A	90W	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C
LT4276AHUFD#PBF	LT4276AHUFD#TRPBF	4276A	90W	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT4276BIUFD#PBF	LT4276BIUFD#TRPBF	4276B	25.5W	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C
LT4276BHUFD#PBF	LT4276BHUFD#TRPBF	4276B	25.5W	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT4276CIUFD#PBF	LT4276CIUFD#TRPBF	4276C	13W	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C
LT4276CHUFD#PBF	LT4276CHUFD#TRPBF	4276C	13W	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{VPORT} = V_{HSSRC} = V_{VIN} = 40V, V_{VCC} = VCCREG, ROSC, PG, and SG Open, R_{FFSDLY} = 5.23kΩ to GND. AUX connected to GND unless otherwise specified. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	VPORT, HSSRC, V_{IN} Operating Voltage	At VPORT Pin	●			60	V
V_{SIG}	VPORT Signature Range	At VPORT Pin	●	1.5		10	V
V_{CLASS}	VPORT Classification Range	At VPORT Pin	●	12.5		21	V
V_{MARK}	VPORT Mark Range	At VPORT Pin, After 1st Classification Event	●	5.6		10	V
	VPORT AUX Range	At VPORT Pin, $V_{AUX} \geq$ 6.45V	●	8		60	V
	Signature/Class Hysteresis Window		●	1.0			V
	Reset Threshold		●	2.6		5.6	V
V_{HSON}	Hot Swap Turn-On Voltage		●		35	37	V
V_{HSOFF}	Hot Swap Turn-Off Voltage		●	30	31		V
	Hot Swap On/Off Hysteresis Window		●	3			V
Supply Current							
	VPORT, HSSRC & V_{IN} Supply Current	V_{VPORT} = V_{HSSRC} = V_{VIN} = 60V	●			2	mA
	VPORT Supply Current During Classification	V_{VPORT} = 17.5V, RCLASS, RCLASS++ Open	●	0.7	1.0	1.3	mA
	VPORT Supply Current During Mark Event	V_{VPORT} = V_{MARK} after 1st Classification Event	●	0.4		2.2	mA
Signature and Classification							
	Signature Resistance	V_{SIG} (Note 4)	●	23.6	24.4	25.5	kΩ
	Signature Resistance During Mark Event	V_{MARK} (Note 4)	●	5.2	8.3	11.4	kΩ
	RCLASS/RCLASS++ Voltage	–10mA ≥ I_{RCLASS} ≥ –36mA	●	1.36	1.40	1.43	V
	Classification Stability Time	V_{VPORT} Step to 17.5V, R_{CLS} = 35.7Ω	●			2	ms
Digital Interface							
V_{AUXT}	AUX Threshold	V_{PORT} = 17.5V, V_{IN} = V_{HSSRC} = 18.5V	●	6.05	6.25	6.45	V
I_{AUXH}	AUX Pin Current	V_{AUX} = 6.05V, V_{PORT} = 17.5V, V_{IN} = 9V, V_{CC} = 0V	●	3.3	5.3	7.3	µA
	T2P Output High	V_{VCC} - V_{T2P}, –1mA Load	●			0.3	V
	T2P Leakage	V_{T2P} = 0V	●	–1		1	µA
Hot Swap Control							
I_{GPU}	HSGATE Pull Up Current	V_{HSGATE} - V_{HSSRC} = 5V (Note 5)	●	–27	–22	–18	µA
	HSGATE Voltage	–10µA Load, with respect to HSSRC	●	10		14	V
	HSGATE Pull Down Current	V_{HSGATE} - V_{HSSRC} = 5V	●	400			µA
V_{CC} Supply							
VCCREG	V_{CC} Regulation Voltage		●	7.2	7.6	8.0	V
Feedback Amplifier							
V_{FB}	FB31 Regulation Voltage		●	3.11	3.17	3.23	V
	FB31 Pin Bias Current	RLDCMP Open			-0.1		µA
gm	Feedback Amplifier Average Trans-Conductance	Time Average, –2µA < I_{ITHB} < 2µA	●	–52	–40	–26	µA/V
I_{SINK}	ITHB Average Sink Current	Time Average, V_{FB31} = 0V	●	4.4	8.0	13.4	µA
Soft-Start							
I_{SFST}	Charging Current	V_{SFST} = 0.5V, 3.0V	●	–49	–42	–36	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{VPORT} = V_{HSSRC} = V_{VIN} = 40V, V_{VCC} = VCCREG, ROSC, PG, and SG Open, R_{FFSDLY} = 5.23kΩ to GND. AUX connected to GND unless otherwise specified. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gate Outputs							
	PG, SG Output High Level	I = –1mA	●	V_{CC} –0.1			V
	PG, SG Output Low Level	I = 1mA	●			1	V
	PG Rise Time, Fall Time	PG = 1000pF			15		ns
	SG Rise Time, Fall Time	SG = 400pF			15		ns
Current Sense/Overcurrent							
V_{FAULT}	Overcurrent Fault Threshold	V_{ISEN}+ - V_{ISEN}–	●	125	140	155	mV
$\Delta V_{SENSE}/\Delta V_{ITHB}$	Current Sense Comparator Threshold with Respect to V_{ITHB}		●	–130	–111	–98	mV/V
$V_{ITHB(OS)}$	V_{ITHB} Offset		●	3.03	3.17	3.33	V
Timing							
f_{OSC}	Default Switching Frequency	ROSC Pin Open	●	200	214	223	kHz
	Switching Frequency	R_{OSC} = 45.3kΩ to GND	●	280	300	320	kHz
f_{T2P}	LTPoE++ Signal Frequency				f_{SW}/256		
t_{MIN}	Minimum PG On Time		●	175	250	330	ns
D_{MAX}	Maximum PG Duty Cycle		●	63	66	70	%
$t_{PGDELAY}$	PG Turn-On Delay-Flyback PG Turn-On Delay-Forward	5.23kΩ from FFSDLY to GND 52.3kΩ from FFSDLY to GND 10.5kΩ from FFSDLY to V_{CC} 52.3kΩ from FFSDLY to V_{CC}			45 171 92 391		ns ns ns ns
t_{FBDLY}	Feedback Amp Enable Delay Time				350		ns
t_{FB}	Feedback Amp Sense Interval				550		ns
t_{PGSG}	PG Falling to SG Rising Delay Time-Flyback PG Falling to SG Falling Delay Time-Forward	Resistor from FFSDLY to GND 10.5kΩ from FFSDLY to V_{CC} 52.3kΩ from FFSDLY to V_{CC}			20 67 301		ns ns ns
t_{START}	Start Timer (Note 6)	Delay After Power Good	●	80	86	93	ms
t_{FAULT}	Fault Timer (Note 6)	Delay After Overcurrent Fault	●	80	86	93	ms
I_{MPS}	MPS Current		●	10	12	14	mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. All voltages with respect to GND unless otherwise noted. Positive currents are into pins; negative currents are out of pins unless otherwise noted.

Note 3. This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature can exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

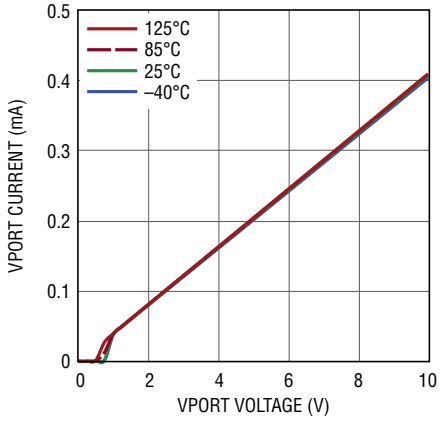
Note 4. Signature resistance specifications do not include resistance added by the external diode bridge which can add as much as 1.1kΩ to the port resistance.

Note 5. I_{GPU} available in PoE powered operation. That is, available after V(VPORT) > V_{HSON} and V(AUX) < V_{AUXT}, over the range where V(VPORT) is between V_{HSOFF} and 60V.

Note 6. Guaranteed by design, not subject to test.

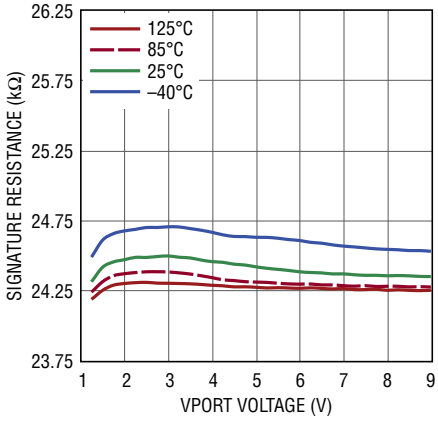
TYPICAL PERFORMANCE CHARACTERISTICS

Input Current vs Input Voltage 25k Detection Range



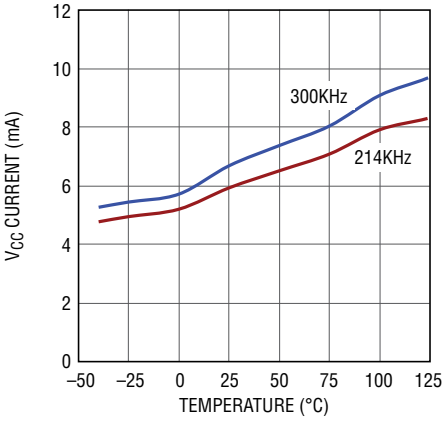
4276 G01

Signature Resistance vs Input Voltage



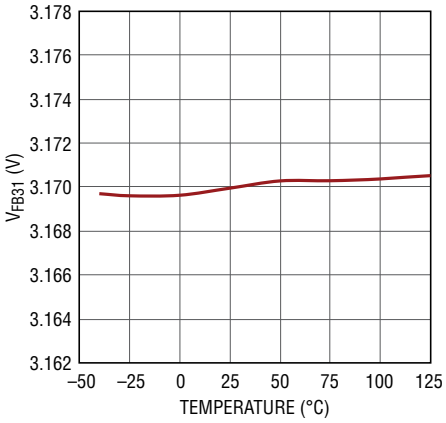
4276 G02

V_{CC} Current vs Temperature



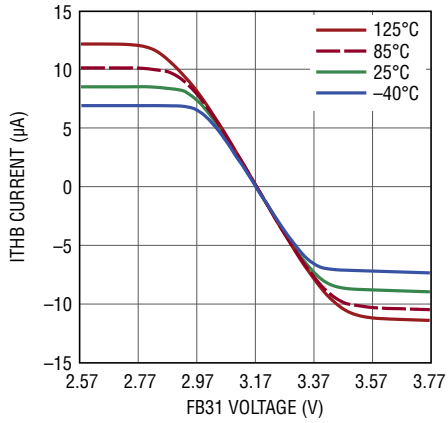
4276 G03

V_{FB31} vs Temperature



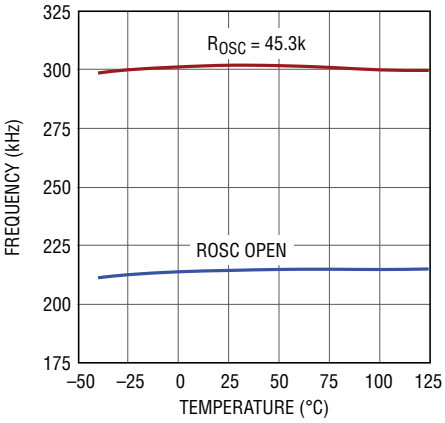
4276 G04

Feedback Amplifier Output Current vs V_{FB31}



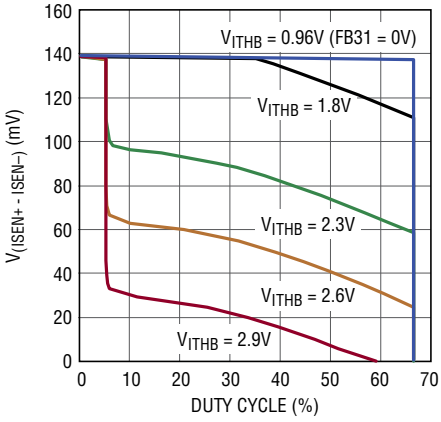
4276 G05

Switching Frequency vs Temperature



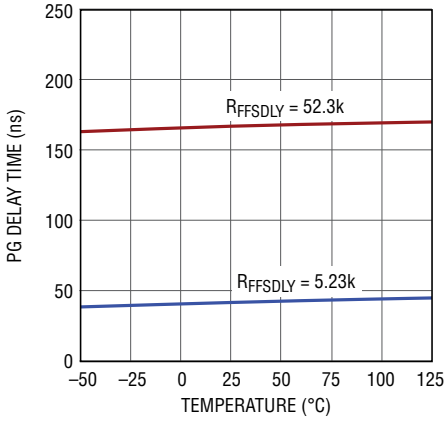
4276 G06

Current Sense Voltage vs Duty Cycle, I_{THB}



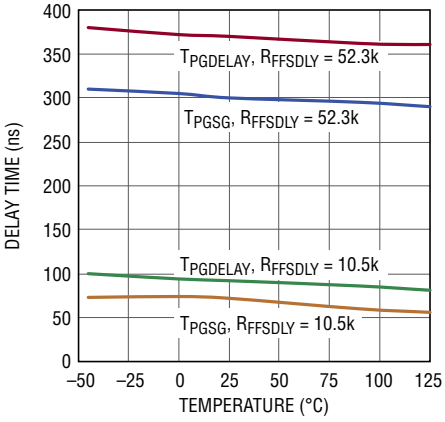
4276 G07

PG Delay Time vs Temperature in Flyback Mode



4276 G08

PG Delay Time vs Temperature in Forward Mode



4276 G09

PIN FUNCTIONS

GND(Pins 1, 19, Exposed Pad Pin 29): Device Ground. Exposed Pad must be electrically and thermally connected to PCB GND and Pin 19.

RCLASS++ (Pin 3, LT4276A Only): LTPoE++ Class Select Input. Connect a resistor between RCLASS++ to GND per Table 1.

AUX (Pin 2): Auxiliary Sense. Assert AUX via a resistive divider from the auxiliary power input to set the voltage at which the auxiliary supply takes over. Asserting AUX pulls down HSGATE, disconnects the signature resistor and disables classification. The AUX pin sinks I_{AUXH} when below its threshold voltage of V_{AUXT} to provide hysteresis. Connect to GND if not used.

RCLASS (Pin 4): Class Select Input. Connect a resistor between RCLASS to GND per Table 1.

T2P (Pin 5, LT4276A and LT4276B only): PSE Type Indicator. Low impedance to V_{CC} indicates 2-event classification. Alternating low/high impedance indicates LTPoE++ classification (LT4276A only, see Applications Information). High impedance indicates 1-event classification. This pin is not connected on the LT4276C. See the Applications Information Section for pin behavior when using the AUX pin.

DNC (Pin 22): Do Not Connect. Leave pin open.

ROSC (Pin 10): Programmable Frequency Adjustment. Resistor to GND programs operating frequency. Leave open for default frequency of 214kHz.

SFST (Pin 11): Soft-Start. Capacitor to GND sets soft-start timing.

FFSDLY (Pin 12): Forward/Flyback Select and Primary Gate Delay Adjustment. Resistor to GND adjusts gate drive delay for a flyback topology. Resistor to V_{CC} adjusts gate drive delay for a forward topology.

ITHB (Pin 13): Current Threshold Control. The voltage on this pin corresponds to the peak current of the external FET. Note that the voltage gain from ITHB to the input of the current sense comparator (V_{SENSE}) is negative.

FB31 (Pin 14): Feedback Input. In flyback mode, connect external resistive divider from the third winding feedback. Reference voltage is 3.17V. Connect to GND in forward mode.

RLDCMP (Pin 15): Load Compensation Adjustment. Optional resistor to GND controls output voltage set point as a function of peak switching current. Leave RLDCMP open if load compensation is not needed.

ISEN– (Pin 16): Current Sense, Negative Input. Route as a dedicated trace to the current sense resistor.

ISEN+ (Pin 17): Current Sense, Positive Input. Route as a dedicated trace to the current sense resistor.

SG (Pin 18): Secondary (Synchronous) Gate Drive, Output.

PG (Pin 20): Primary Gate Drive, Output.

V_{CC} (Pins 6, 7, 8, 9, 21): Switching Regulator Controller Supply Voltage. Connect a local 1µF ceramic capacitor from V_{CC} pin 21 to GND pin 19 as close as possible to LT4276 as shown in Table 2.

SWVCC(Pin 23): Switch Driver for V_{CC}'s Buck Regulator. This pin drives the base of a PNP in a buck regulator to generate V_{CC}.

V_{IN} (Pin 24): Buck Regulator Supply Voltage. Usually separated from HSSRC by a pi filter.

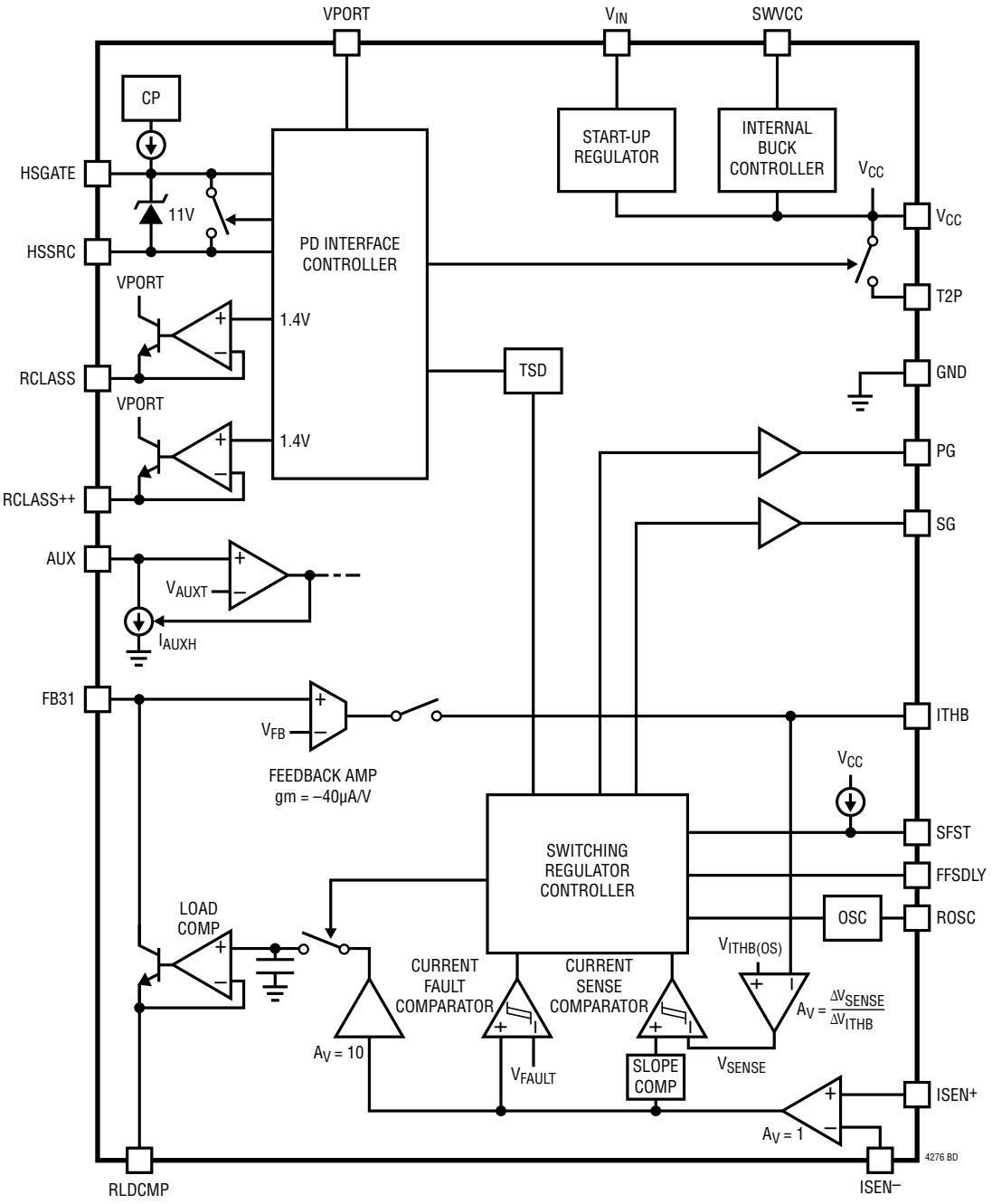
HSSRC (Pin 25): External Hot Swap MOSFET Source. Connect to source of the external MOSFET.

HSGATE (Pin 26): External Hot Swap MOSFET Gate Control, Output. Capacitance to GND determines inrush time.

NC (Pin 27): No Connection. Not internally connected.

VPORT (Pin 28): PD Interface Supply Voltage and External Hot Swap MOSFET Drain Connection.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

OVERVIEW

Power over Ethernet (PoE) continues to gain popularity as products take advantage of DC power and high speed data available from a single RJ45 connector. The LT4276A allows higher power while maintaining backwards compatibility with existing PSE systems. The LT4276 combines a PoE PD controller and a switching regulator controller capable of either flyback or forward isolated power supply operation.

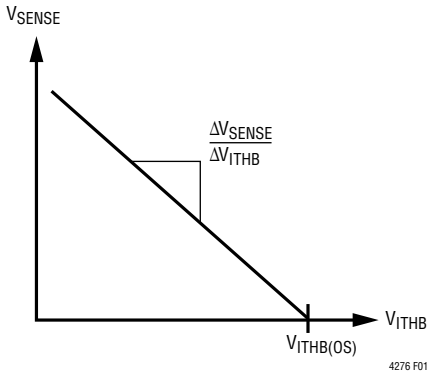


Figure 1. V_{SENSE} vs. V_{ITHB}

SIGNIFICANT DIFFERENCES FROM PREVIOUS PRODUCTS

The LT4276 has several significant differences from previous Linear Technology products. These differences are briefly summarized below. See Applications Information for more detail.

ITHB Is Inverted from the Usual ITH pin

The ITHB pin voltage has an inverse relationship to the current sense comparator threshold, V_{SENSE}. Furthermore, the ITHB pin offset voltage, $V_{ITHB(OS)}$, is 3.17V. See Figure 1.

Duty-Cycle Based Soft-Start

The LT4276 uses a duty cycle ramp soft-start that injects charge into ITHB. This allows startup without appreciable overshoot and with inexpensive external components.

The Feedback Pin (FB31) is 3.17V rather than 1.25V

The error amp feedback voltage (V_{FB}) is 3.17V.

Flyback/Forward Mode Is Pin Selectable

The LT4276 operates in flyback mode if FFSDLY is pulled down by a resistor to GND. It operates in forward mode if FFSDLY is pulled up by a resistor to V_{CC}. The value of this resistor determines the $t_{PGDELAY}$ and t_{PGSG}.

T2P Pin Polarity Is Reversed

The T2P pin pulls up to V_{CC} when active rather than pulling down to GND.

V_{CC} Is Powered by Internally Driven Buck Regulator

The LT4276 includes a buck regulator controller that must be used to generate the V_{CC} supply voltage.

PoE MODES OF OPERATION

The LT4276 has several modes of operation, depending on the input voltage sequence applied to the VPORT pin.

Table 1. Classification Codes, Power Levels and Resistor Selection

CLASS	PD POWER AVAILABLE	PD TYPE	NOMINAL CLASS CURRENT	LT4276 GRADE CAPABILITY			RESISTOR (1%)	
				A	B	C	R_{CLS}	R_{CLS}++
0	13W	Type 1	0.7mA	√	√	√	Open	Open
1	3.84W	Type 1	10.5mA	√	√	√	150Ω	Open
2	6.49W	Type 1	18.5mA	√	√	√	80.6Ω	Open
3	13W	Type 1	28mA	√	√	√	52.3Ω	Open
4	25.5W	Type 2	40mA	√	√		35.7Ω	Open
4*	38.7W	LTPoE++	40mA	√			Open	35.7Ω
4*	52.7W	LTPoE++	40mA	√			150Ω	47.5Ω
4*	70W	LTPoE++	40mA	√			80.6Ω	64.9Ω
4*	90W	LTPoE++	40mA	√			52.3Ω	118Ω

*An LTPoE++ PD classifies as class 4 by an IEEE 802.3 compliant PSE.

APPLICATIONS INFORMATION

Detection

During detection, the PSE looks for a 25kΩ signature resistor which identifies the device as a PD. The LT4276 signature resistor is smaller than 25k to compensate for the additional series resistance introduced by the IEEE required bridge.

Classification

The detection/classification process varies depending on whether the PSE is Type 1, Type 2, or LTPoE++. A Type 1 PSE, after a successful detection, may apply a classification probe voltage of 15.5V to 20.5V and measure current.

In 2-event classification, a Type 2 PSE probes for power classification twice as shown in Figure 3. The LT4276A or LT4276B recognizes this and pulls the T2P pin up to V_{CC} to signal the load that Type 2 power is available. Otherwise it does not pull up on the T2P pin, indicating that only Type 1 power is available. If an LT4276A senses an LTPoE++ PSE it alternates between pulling T2P up and floating T2P at a rate of f_{T2P} to indicate the LTPoE++ power is available.

LTPoE++ Classification

The LT4276A allows higher power allocation while maintaining backwards compatibility with existing PSE systems by extending the classification signaling of IEEE 802.3. Linear Technology PSE controllers capable of LTPoE++ are listed in the Related Parts section. IEEE PSEs classify an LTPoE++ PD as a Type 2 PD.

Classification Resistors (R_{CLS} and R_{CLS++})

The R_{CLS} and R_{CLS++} resistors set the classification current corresponding to the PD power classification. Select the value of R_{CLS} from Table 1 and connect the resistor between the RCLASS pin and GND. For LTPoE++, use the LT4276A and select the value of R_{CLS++} from Table 1 in addition to R_{CLS}. The resistor tolerance must be 1% or better to avoid degrading the overall accuracy of the classification circuit.

Signature Corrupt During Mark

During the mark state, the LT4276 presents <11kΩ to the port as required by the IEEE specification.

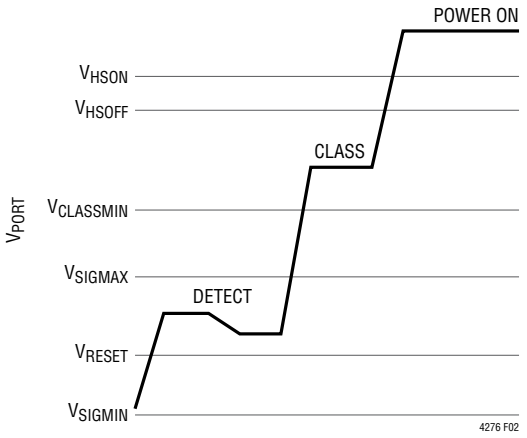


Figure 2. Type 1 Detect/Class Signaling Waveform

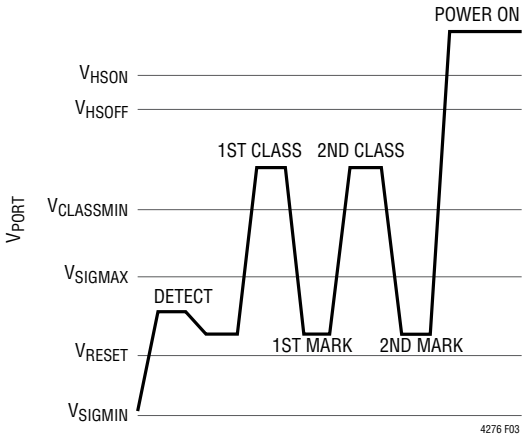


Figure 3. Type 2 Detect/Class Signaling Waveform

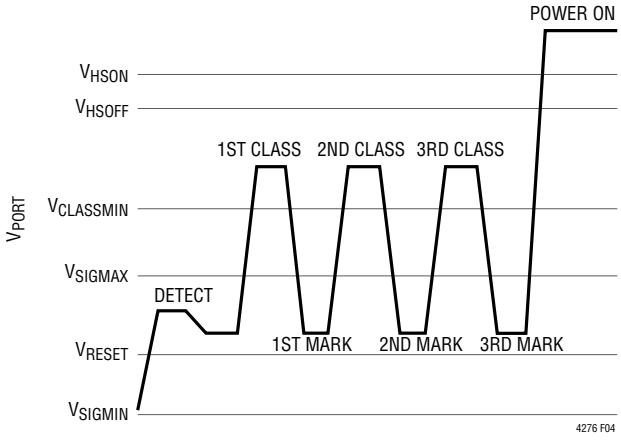


Figure 4. LTPoE++ Detect/Class Signaling Waveform

APPLICATIONS INFORMATION

Inrush and Powered On

Once the PSE detects and optionally classifies the PD, the PSE then powers on the PD. When the port voltage rises above the V_{HSON} threshold, it begins to source I_{GPU} out of the HSGATE pin. This current flows into an external capacitor (C_{GATE} in Figure 5) that causes a voltage to ramp up the gate of the external MOSFET. The external MOSFET acts as a source follower and ramps the voltage up on the output bulk capacitor (C_{PORT} in Figure 5), thereby determining the inrush current (I_{INRUSH} in Figure 5). To meet IEEE requirements, design I_{INRUSH} to be ~100mA.

The LT4276 internal charge pump provides an N-channel MOSFET solution, eliminating a larger and more costly P-channel FET. The low $R_{DS(ON)}$ MOSFET also maximizes power delivery and efficiency, reduces power and heat dissipation, and eases thermal design.

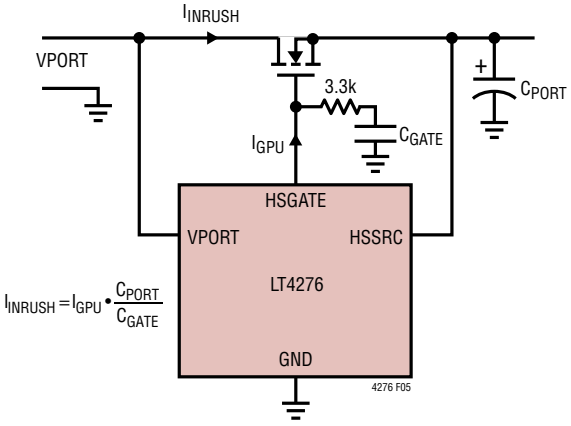


Figure 5. Programming I_{INRUSH}

DELAY START

After the HSGATE charges up to approximately 7V above HSSRC, fully enhancing the external Hot Swap MOSFET, the switching regulator controller operates after a delay of t_{START}. During this delay, the LT4276 draws I_{MPS} from VPORT to ensure that the PSE does not DC disconnect the PD due to Maintain Power Signature requirements.

EXTERNAL V_{CC} SUPPLY

The external V_{CC} supply must be configured as a buck regulator shown in Figure 6. To optimize the buck regulator, use the external component values in Table 2 corresponding to the V_{IN} operating range. This buck regulator runs in discontinuous mode with the inductor peak current considerably higher than average load current on V_{CC}. Thus, the saturation current rating of the inductor must exceed the values shown in Table 2. Place the capacitor, C, as close as possible to V_{CC} pin 21 and GND pin 19. For optimal performance, place the external components as close as possible to the LT4276.

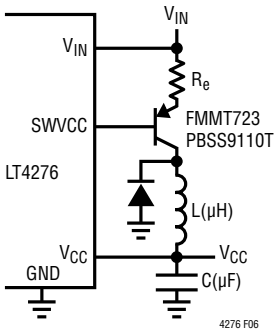


Figure 6. V_{CC} Buck Regulator

Table 2 . Buck Regulator Component Selection

V_{IN}	C	L	I_{SAT}	R_e
9V-57V	22µF	22µH	≥1.2A	1Ω
PoE	10µF	100µH	≥300mA	20Ω

AUXILIARY SUPPLY OVERRIDE

If the AUX pin is held above V_{AUXT}, the LT4276 enters auxiliary power supply override mode. In this mode the signature resistor is disconnected, classification is disabled, and HSGATE is pulled down. The T2P pin pulls up to V_{CC} on the LT4276B (or the LT4276A when no R_{CLS}++ resistor is present). The T2P pin alternates between pulling up and floating at f_{T2P} on the LT4276A when the R_{CLS}++ resistor is present.

The AUX pin allows for setting the auxiliary supply turn on (V_{AUXON}) and turn off (V_{AUXOFF}) voltage thresholds. The auxiliary supply hysteresis voltage (V_{AUXHYS}) is set by sinking current (I_{AUXH}) only when the AUX pin voltage is

APPLICATIONS INFORMATION

less than V_{AUXT}. Use the following equations to set V_{AUXON} and V_{AUXOFF} via R1 and R2 in Figure 7. A capacitor up to 1000pF may be placed between the AUX pin and GND to improve noise immunity.

V_{AUXON} must be lower than V_{HSOFF}.

$$R1 = \frac{V_{AUXON} - V_{AUXOFF}}{I_{AUXH}} = \frac{V_{AUXHYS}}{I_{AUXH}}$$

$$R2 = \frac{R1}{\left(\frac{V_{AUXOFF}}{V_{AUXT}} - 1\right)}$$

$$R1 \geq \frac{V_{AUX(MAX)} - V_{AUXT}}{1.4mA}$$

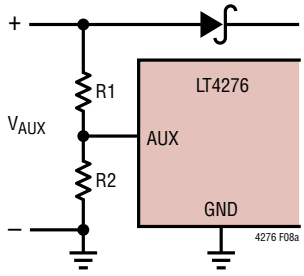


Figure 7. AUX Threshold and Hysteresis Calculation

SWITCHING REGULATOR CONTROLLER OPERATION

The switching regulator controller portion of the LT4276 is a current mode controller capable of implementing either a flyback or a forward power supply. When used in flyback mode, no opto-isolator is required for feedback because the output voltage is sensed via the transformer's third winding.

Flyback Mode

The LT4276 is programmed into flyback mode by placing a resistor R_{FFSDLY} from the FFSDLY pin to GND. This resistor must be in the range of 5.23kΩ to 52.3kΩ. If using a potentiometer to adjust R_{FFSDLY}, ensure the adjustment of the potentiometer does not exceed 52.3kΩ.The value of R_{FFSDLY} determines $t_{PGDELAY}$ according to the following equations:

$$t_{PGDELAY} \approx 2.69ns/k\Omega \bullet R_{FFSDLY} + 30ns$$

$$t_{PGSG} \approx 20ns$$

The PG and SG relationships in flyback mode are shown in Figure 8.

The SG pin must be connected to the secondary side MOSFET through a gate drive transformer as shown in Figure 9. Add a Schottky diode from PG to GND as shown in Figure 9 to prevent PG from going negative.

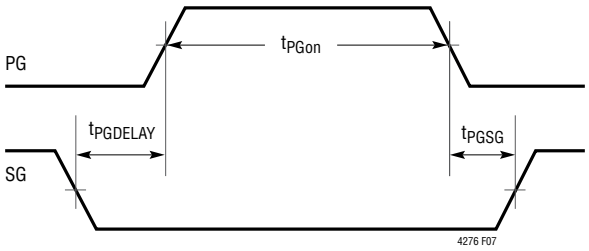


Figure 8: PG and SG Relationship in Flyback Mode

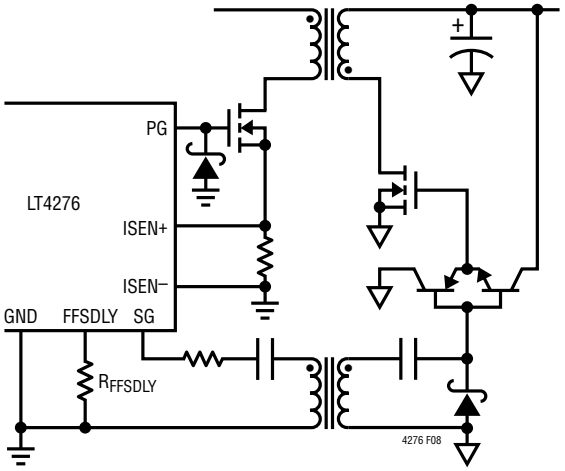


Figure 9: Example PG and SG Connections in Flyback Mode

Forward Mode

The LT4276 is programmed into forward mode by placing a resistor R_{FFSDLY} from the FFSDLY pin to V_{CC}. The R_{FFSDLY} resistor must be in the range of 10.5kΩ to 52.3kΩ. If using a potentiometer to adjust R_{FFSDLY} ensure the adjustment of the potentiometer does not exceed 52.3kΩ.

The value of R_{FFSDLY} determines $t_{PGDELAY}$ and t_{PGSG} according to the following equations:

$$t_{PGDELAY} \approx 7.16ns/k\Omega \bullet R_{FFSDLY} + 17ns$$

$$t_{PGSG} \approx 5.60ns/k\Omega \bullet R_{FFSDLY} + 7.9ns$$

The PG and SG relationships in forward mode are shown in Figure 10.

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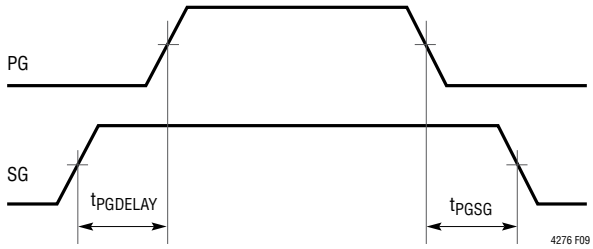

Figure 10: PG and SG relationship in Forward Mode

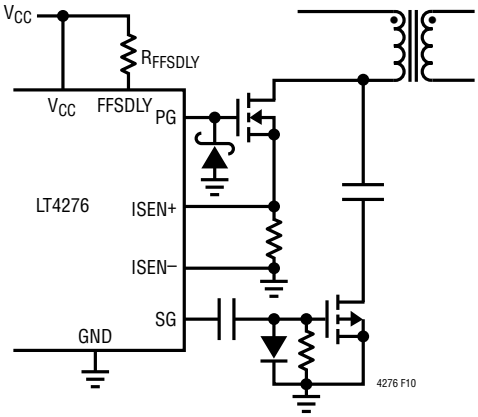

Figure 11: Example PG and SG Connections in Forward Mode

In forward mode, the SG pin has the correct polarity to drive the active clamp P-channel MOSFET through a simple level shifter as shown in Figure 11. Add a Schottky diode from the PG to GND as shown in Figure 11 to prevent PG from going negative.

FEEDBACK AMPLIFIER

In the flyback mode, the feedback amplifier senses the output voltage through the transformer's third winding as shown in Figure 12. The amplifier is enabled only during the fixed interval, t_{FB}, as shown in Figure 13. This eliminates the opto-isolator in isolated designs, thus greatly improving the dynamic response and stability over lifetime. Since t_{FB} is a fixed interval, the time-averaged transconductance, gm, varies as a function of the user-selected switching frequency.

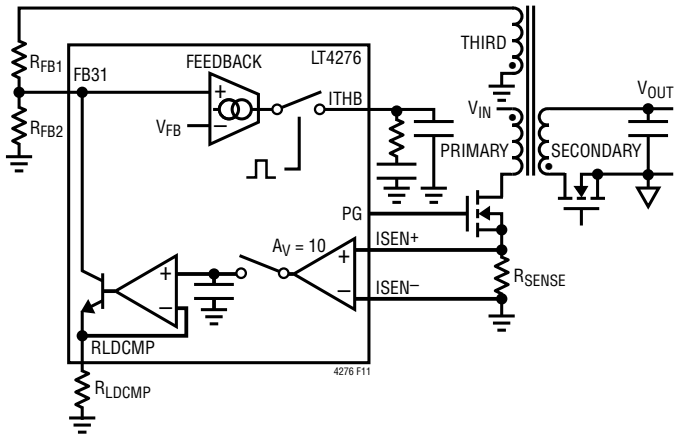

Figure 12: Feedback and Load Compensation Connection

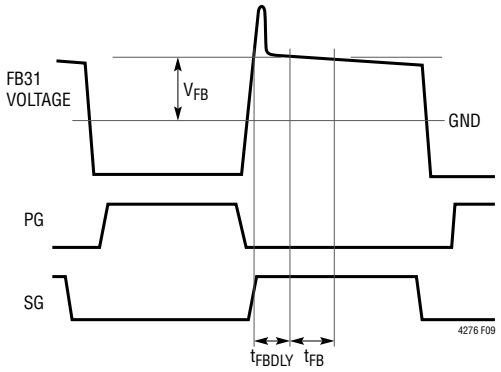

Figure 13: Feedback Amplifier Timing Diagram

FEEDBACK AMPLIFIER OUTPUT, ITHB

As shown in the Block Diagram, V_{SENSE} is the input of the Current Sense Comparator. V_{SENSE} is derived from the output of a linear amplifier whose input is the voltage on the ITHB pin, V_{ITHB}.

This linear amplifier inverts its input, V_{ITHB}, with a gain, $\Delta V_{SENSE}/\Delta V_{ITHB}$, and with an offset voltage of $V_{ITHB(OS)}$ to yield its output, V_{SENSE}. This relationship is shown graphically in Figure 1. Note the slope $\Delta V_{SENSE}/\Delta V_{ITHB}$ is a negative number and is provided in the electrical characteristics table.

$$V_{ITHB} = V_{ITHB(OS)} + V_{SENSE} \bullet \left(\frac{\Delta V_{SENSE}}{\Delta V_{ITHB}} \right)^{-1}$$

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The block diagram shows V_{SENSE} is compared against the voltage across the current sense resistor, V(ISEN+)-V(ISEN–) modified by the internal slope compensation voltage discussed subsequently.

LOAD COMPENSATION

As can be seen in Figure 13, the voltage on the FB31 pin droops slightly during the flyback period. This is mostly caused by resistances of components of the secondary side such as: the secondary winding, $R_{DS(ON)}$ of the synchronous MOSFET, ESR of the output capacitor, etc. These resistances cause a feedback error that is proportional to the current in the secondary loop at the time of feedback sample window. To compensate for this error, the LT4276 places a voltage proportional to the peak current in the primary winding on the RLDCMP pin.

Determining Feedback and Load Compensation Resistors

Because the resistances of components on the secondary side are generally not well known, an empirical method must be used to determine the feedback and load compensation resistor values.

$$\text{INITIALLY SET } R_{FB2} = 2k\Omega$$

$$R_{FB1} \approx R_{FB2} \frac{V_{OUT}}{V_{FB}} \frac{N_{THIRD}}{N_{SECONDARY}} - R_{FB2}$$

Connect the resistor R_{LDCMP} between the RLDCMP pin and GND. R_{LDCMP} must be at least 10kΩ. Adjust R_{LDCMP} for minimum change of V_{OUT} over the full input and output load range. A potentiometer in series with 10kΩ may be initially used for R_{LDCMP} and adjusted. The potentiometer+10kΩ may then be removed, measured, and replaced with the equivalent fixed resistor. The resulting V_{OUT} differs from the desired V_{OUT} due to offset injected by load compensation. The change to R_{FB2} to correct this is predicted by:

$$\Delta R_{FB2} = \frac{\Delta V_{OUT}}{V_{FB}} \frac{N_{THIRD}}{N_{SECONDARY}} \frac{R_{FB2}^2}{R_{FB1}}$$

Where: ΔV_{OUT} is the desired change to V_{OUT}
ΔR_{FB2} is the required change to R_{FB2}

$N_{THIRD}/N_{SECONDARY}$ is the transformer third winding to secondary winding

OPTO-ISOLATOR FEEDBACK

For forward mode operation, the flyback voltage cannot be sensed across the transformer. Thus, opto-isolator feedback must be used. When using opto-isolator feedback, connect the FB31 pin to GND and leave the RLDCMP pin open. In this condition, the feedback amplifier sinks an average current of I_{SINK} into the ITHB pin. An example for feedback connections is shown in Figure 14. Note that since I_{SINK} is time-averaged over the switching period, the sink current varies as a function of the user-selected switching frequency.

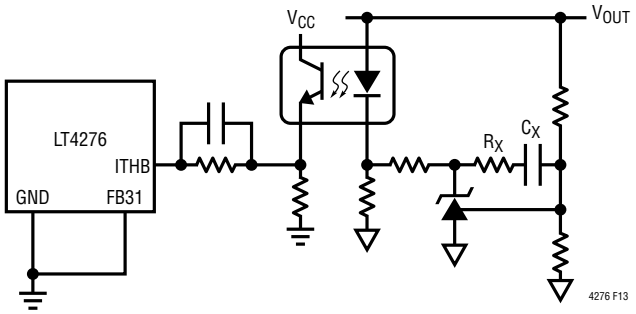

Figure 14: Opto-isolator Feedback Connections in the Forward Mode

SOFT-START

In PoE applications, a proper soft-start design is required to prevent the PD from drawing more current than the PSE can provide.

The soft-start time, t_{SFST}, is approximately the time in which the power supply output voltage, V_{OUT}, is charging its output capacitance, C_{OUT}. This results in an inrush current at the port of the PD, Iport_inrush. Care must be taken in selecting t_{SFST} to prevent the PD from drawing more current than the PSE can provide.

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In the absence of an output load current, the Iport_inrush, is approximated by the following equation:

$$Iport\_inrush \approx (C_{OUT} \bullet V_{OUT}^2)/(\eta \bullet t_{SFST} \bullet V_{IN})$$

where η is the power supply efficiency,

V_{IN} is the input voltage of the PD

Iport_inrush plus the port current due to the load current must be below the current the PSE can provide. Note that the PSE current capability depends on the PSE operating standard.

The LT4276 contains a soft-start function that controls t_{SFST} by connecting an external capacitor, C_{SFST}, between the SFST pin and GND. The SFST pin is pulled up with I_{SFST} when the LT4276 begins switching. The voltage ramp on the SFST pin is proportional to the duty cycle ramp for PG.

For flyback mode, the soft-start time is:

$$t_{SFST} = \frac{600\mu A}{nF}\left(\frac{C_{SFST}}{I_{SFST}}\right)\left(t_{PGon} + t_{PGDELAY} - t_{MIN}\right)$$

where t_{PGon} is the time when PG is high as shown in Figure 8 once the power supply is in steady-state.

In forward mode, each of the back page applications schematics provides a chart with t_{SFST} vs. C_{SFST}. Select the application and choose a value of C_{SFST} that corresponds to the desired soft-start time.

CURRENT SENSE COMPARATOR

The LT4276 uses a differential current sense comparator to reduce the effects of stray resistance and inductance on the measurement of the primary current. ISEN+ and ISEN– must be Kelvin connected to the sense resistor pads.

Like most switching regulator controllers, the current sense comparator begins sensing the current t_{MIN} after PG turns on. Then, the comparator turns PG off after the voltage across ISEN+ and ISEN– exceeds the current sense comparator threshold, V_{SENSE}. Note that the voltage across ISEN+ and ISEN– is modified by LT4276's internal slope compensation.

SLOPE COMPENSATION

The LT4276 incorporates current slope compensation. Slope compensation is required to ensure current loop stability when the duty cycle is greater than or near 50%. The slope compensation of the LT4276 does not reduce the maximum peak current at higher duty cycles.

CONTROL LOOP COMPENSATION

In flyback mode, loop frequency compensation is performed by connecting a resistor/capacitor network from the output of the feedback amplifier (ITHB pin) to GND as shown in Figure 12. In forward mode, loop compensation is performed by varying R_X and C_X in Figure 14.

ADJUSTABLE SWITCHING FREQUENCY

The LT4276 has a default switching frequency, f_{OSC}, of 214 kHz when the ROSC pin is left open. If a higher switching frequency, f_{SW}, is desired (up to 300 kHz), a resistor no smaller than 45.3kΩ may be added between the ROSC pin to GND. The resistor can be calculated below:

$$R_{OSC} = \frac{3900k\Omega \bullet kHz}{\left(f_{SW} - f_{OSC}\right)}(k\Omega)$$

SHORT CIRCUIT RESPONSE

If the power supply output voltage is shorted, overloaded, or if the soft-start capacitor is too small, an overcurrent fault event occurs when the voltage across the sense pins exceeds V_{FAULT} (after the blanking period of t_{MIN}). This begins the internal fault timer t_{FAULT}. For the duration of t_{FAULT}, the LT4276 turns off PG and SG and pulls the SFST pin to GND. After t_{FAULT} expires, the LT4276 initiates soft-start.

The fault and soft-start sequence repeats as long as the short circuit or overload conditions persist. This condition is recognized by the PG waveform shown in Figure 15 repeating at an interval of t_{FAULT}.

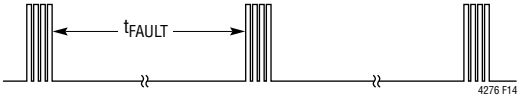


Figure 15: PG Waveform with Output Shorted

APPLICATIONS INFORMATION

OVERTEMPERATURE PROTECTION

The IEEE 802.3 specification requires a PD to withstand any applied voltage from 0V to 57V indefinitely. During classification, however, the power dissipation in the LT4276 may be as high as 1.5W. The LT4276 can easily tolerate this power for the maximum IEEE classification timing but overheats if this condition persists abnormally.

The LT4276 includes an over-temperature protection feature which is intended to protect the device during momentary overload conditions. If the junction temperature exceeds the over-temperature threshold, the LT4276 pulls down HSGATE pin, disables classification, and disables the switching regulator operation.

MAXIMUM DUTY CYCLE

The maximum duty cycle of the PG pin is modified by the chosen $t_{PGDELAY}$ and f_{SW}. It is calculated below:

$$\text{MAX POWER SUPPLY DUTY CYCLE} = D_{MAX} - t_{PGDELAY} \bullet f_{SW}$$

For an appropriate margin during transient operation, the forward or flyback power supply should be designed so that its maximum steady-state duty cycle should be about 10% lower than the LT4276 Maximum Power Supply Duty Cycle calculated above.

EXTERNAL INTERFACE AND COMPONENT SELECTION

PoE Input Diode Bridge

PDs are required to polarity-correct its input voltage. When diode bridges are used, the diode forward voltage drops affect the voltage at the VPORT pin. The LT4276 is designed to tolerate these voltage drops. The voltage parameters shown in the Electrical Characteristics are specified at the LT4276 package pins.

For high efficiency applications, the LT4276 supports an LT4321-based PoE ideal diode bridge that reduces the forward voltage drop from 0.7V to nearly 20mV per diode in normal operation, while maintaining IEEE 802.3 compliance.

Auxiliary Input Diode Bridge

Some PDs are required to receive AC or DC power from an auxiliary power source. A diode bridge is typically required to handle the voltage rectification and polarity correction.

In high efficiency applications, the voltage drop across the rectifier cannot be tolerated. The LT4276 can be configured with an LT4320-based ideal diode bridge to recover the diode voltage drop and ease thermal design.

Input Capacitor

A 0.1µF capacitor is needed from VPORT to GND to meet the input impedance requirement in IEEE 802.3 and to properly bypass the LT4276. This capacitor must be placed as close as possible to the VPORT and GND pins.

Transient Voltage Suppressor

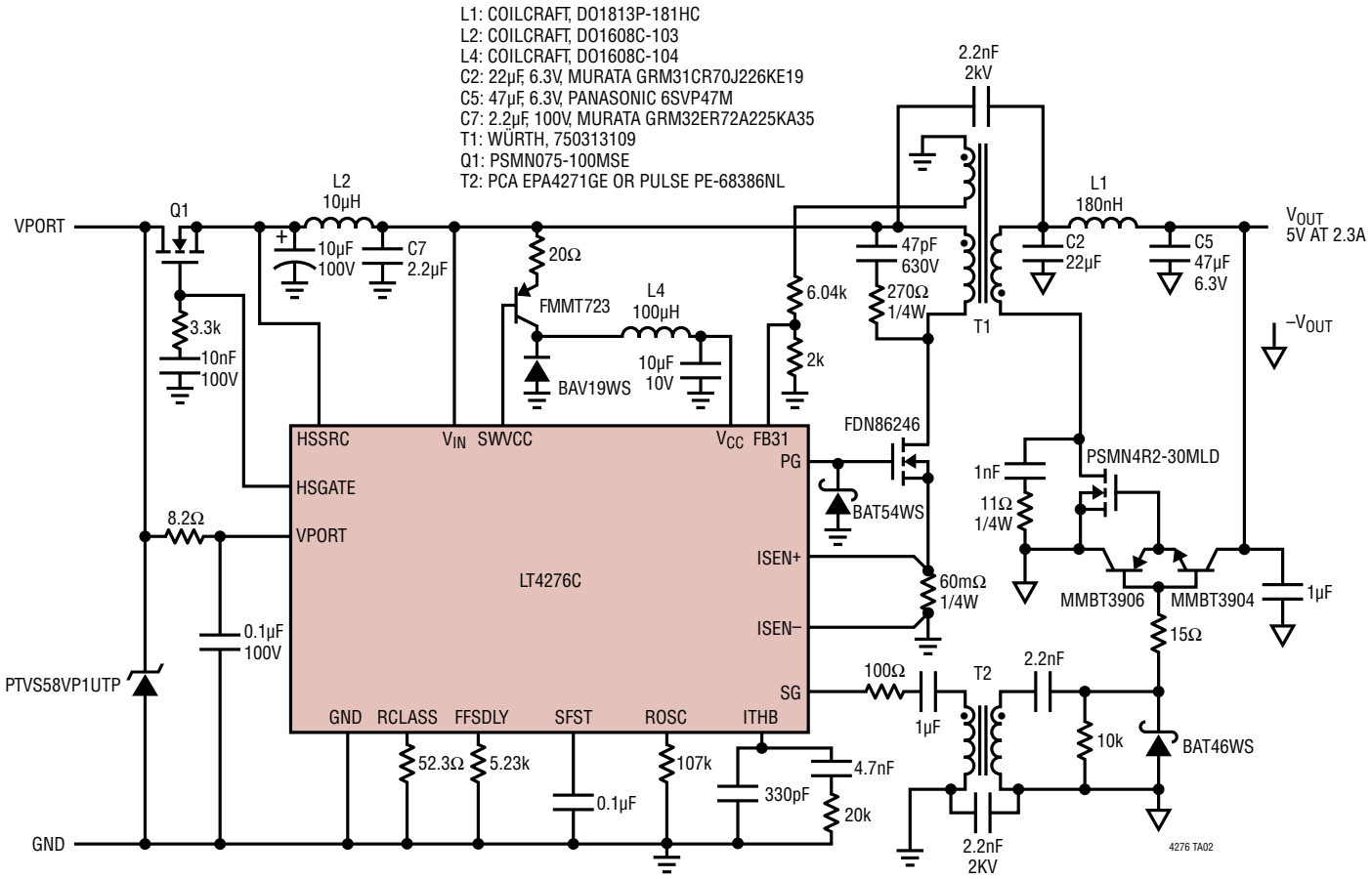
The LT4276 specifies an absolute maximum voltage of 100V and is designed to tolerate brief overvoltage events due to Ethernet cable surges.

To protect the LT4276, install a unidirectional transient voltage suppressor (TVS) such as an SMAJ58A between the VPORT and GND pins. This TVS must be placed as close as possible to the VPORT and GND pins of the LT4276. For PD applications that require an auxiliary power input, install a TVS between V_{IN} and GND as close as possible to the LT4276.

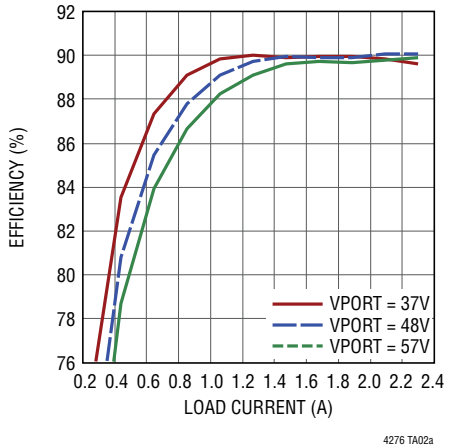
For extremely high cable discharge and surge protection contact Linear Technology Applications.

TYPICAL APPLICATIONS

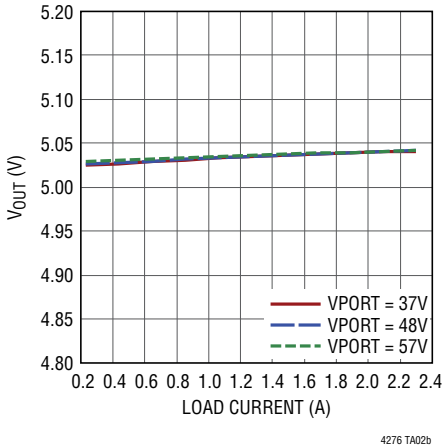
13W (TYPE 1) PoE Power Supply in Flyback Mode with 5V, 2.3A Output



Efficiency vs Load Current

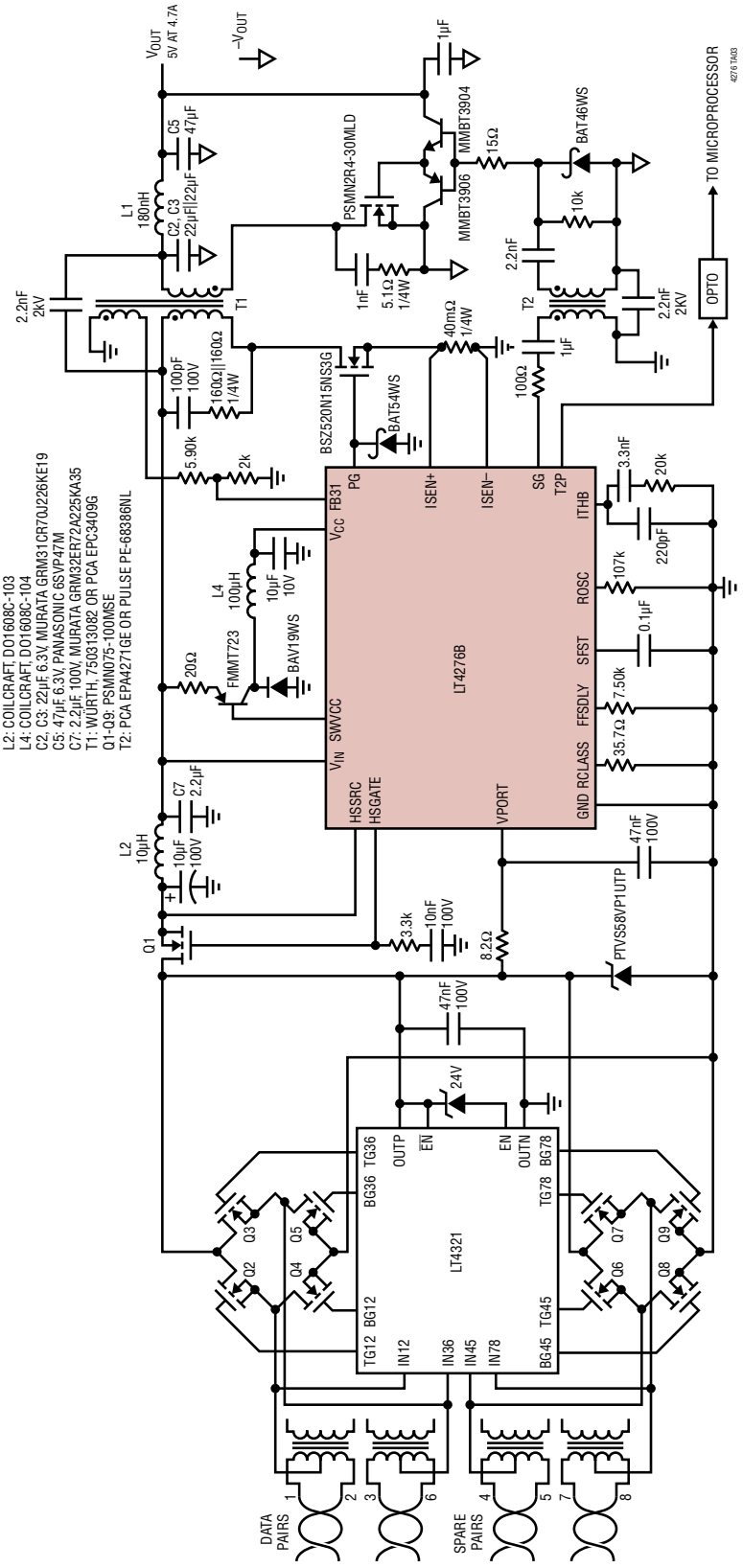


Output Regulation vs Load Current

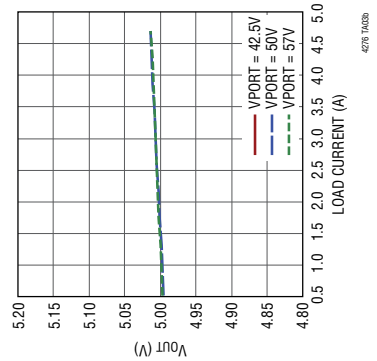


TYPICAL APPLICATIONS

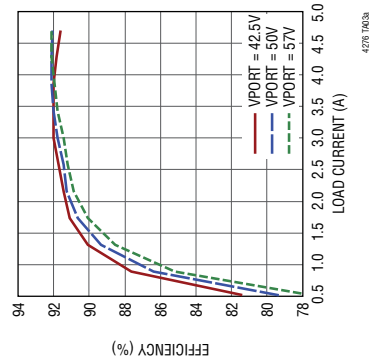
25.5W (Type 2) PoE+ Power Supply in Flyback Mode with 5V, 4.7A Output



VOUT vs Load Current

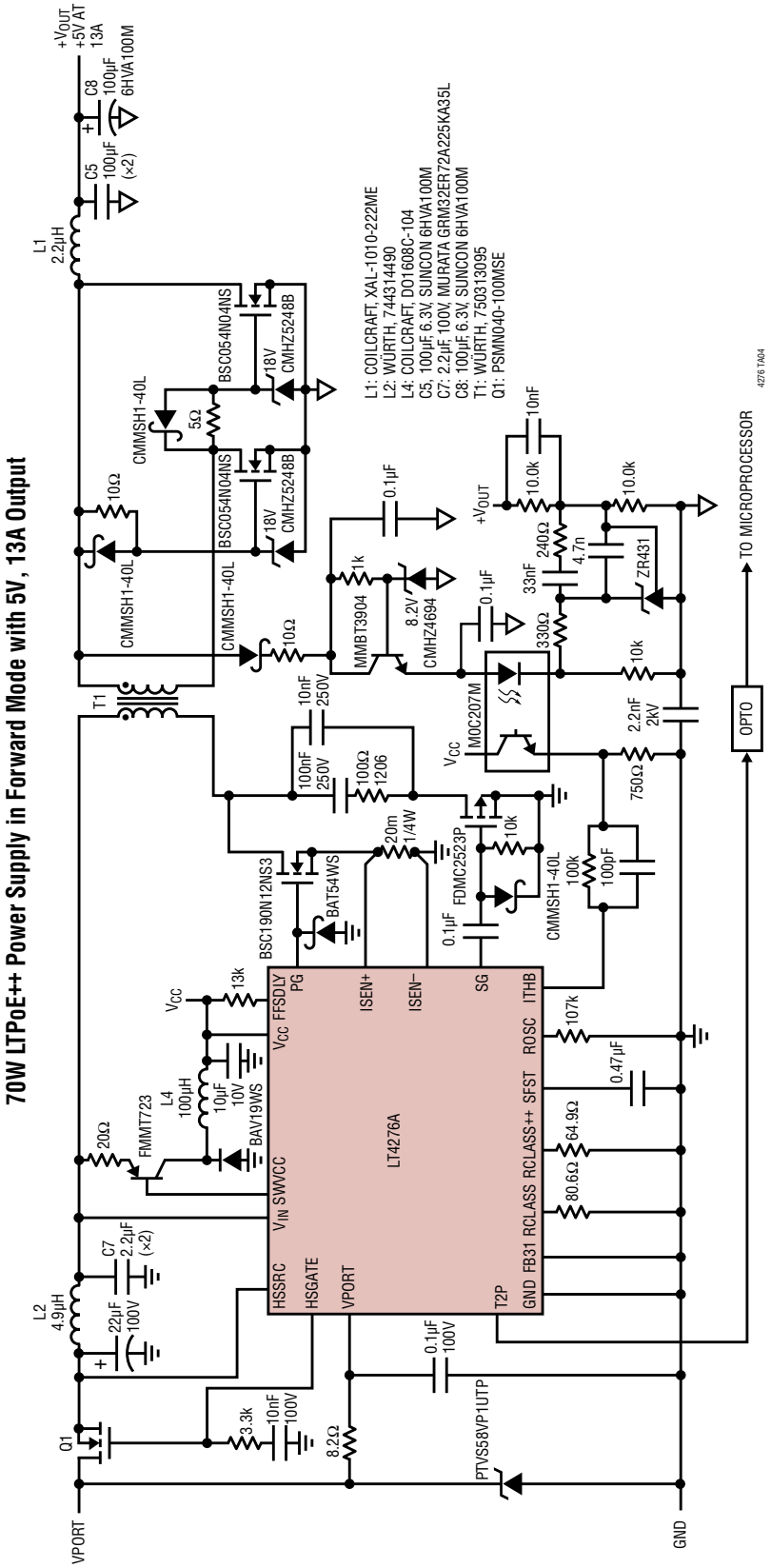


Efficiency vs Load Current



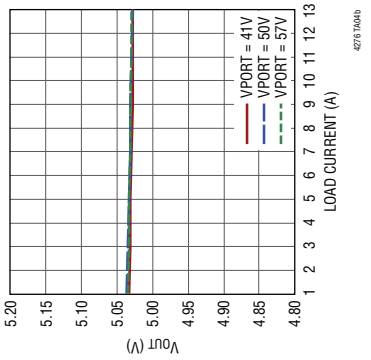
TYPICAL APPLICATIONS

70W LTPoE++ Power Supply in Forward Mode with 5V, 13A Output

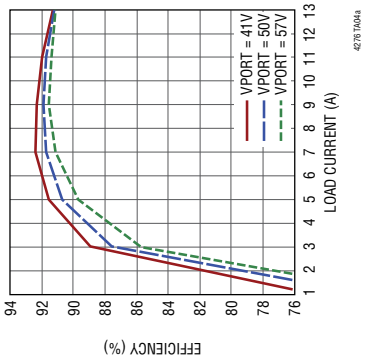


C_{SFST} (µF)	t_{SFST} (ms)
0.10	1.2
0.33	3.8
1.0	12
3.3	38

V_{OUT} vs Load Current

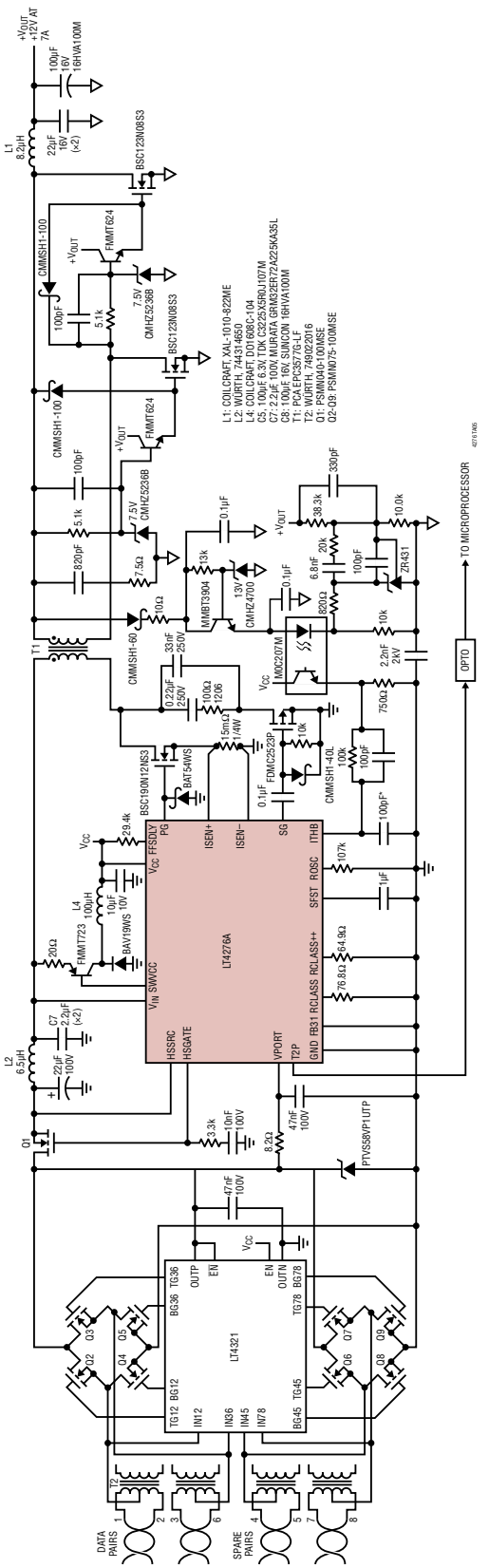


Efficiency vs Load Current

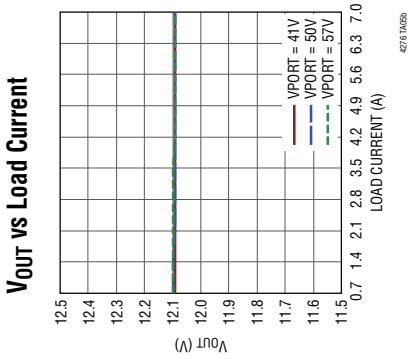


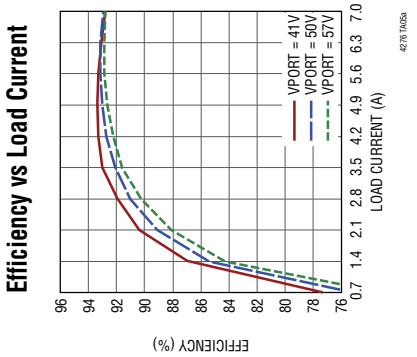
TYPICAL APPLICATIONS

90W LTPoE++ Power Supply in Forward Mode with 12V, 7A Output



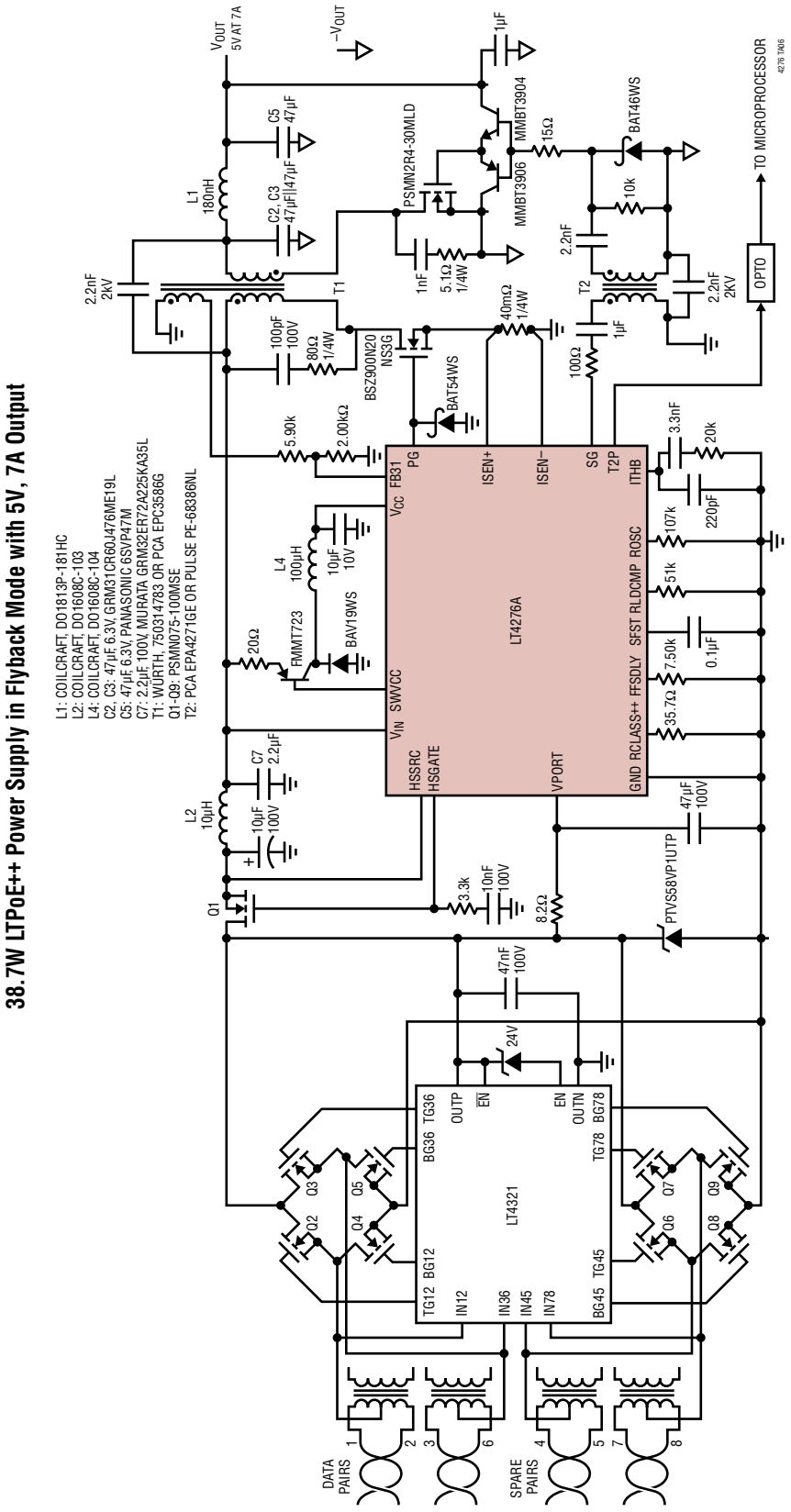
C_{SFST} (µF)	t_{SFST} (ms)
0.10	1.5
0.33	4.9
1.0	15
3.3	48



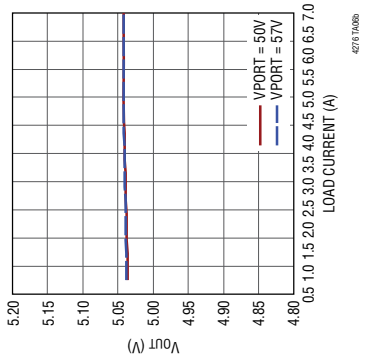


TYPICAL APPLICATIONS

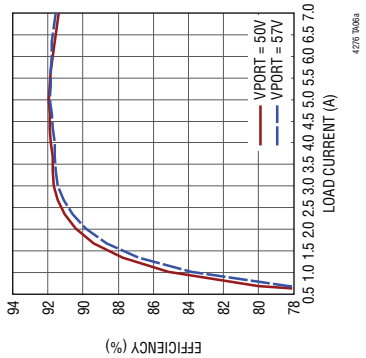
38.7W LTPoE++ Power Supply in Flyback Mode with 5V, 7A Output



Output Regulation vs Load Current

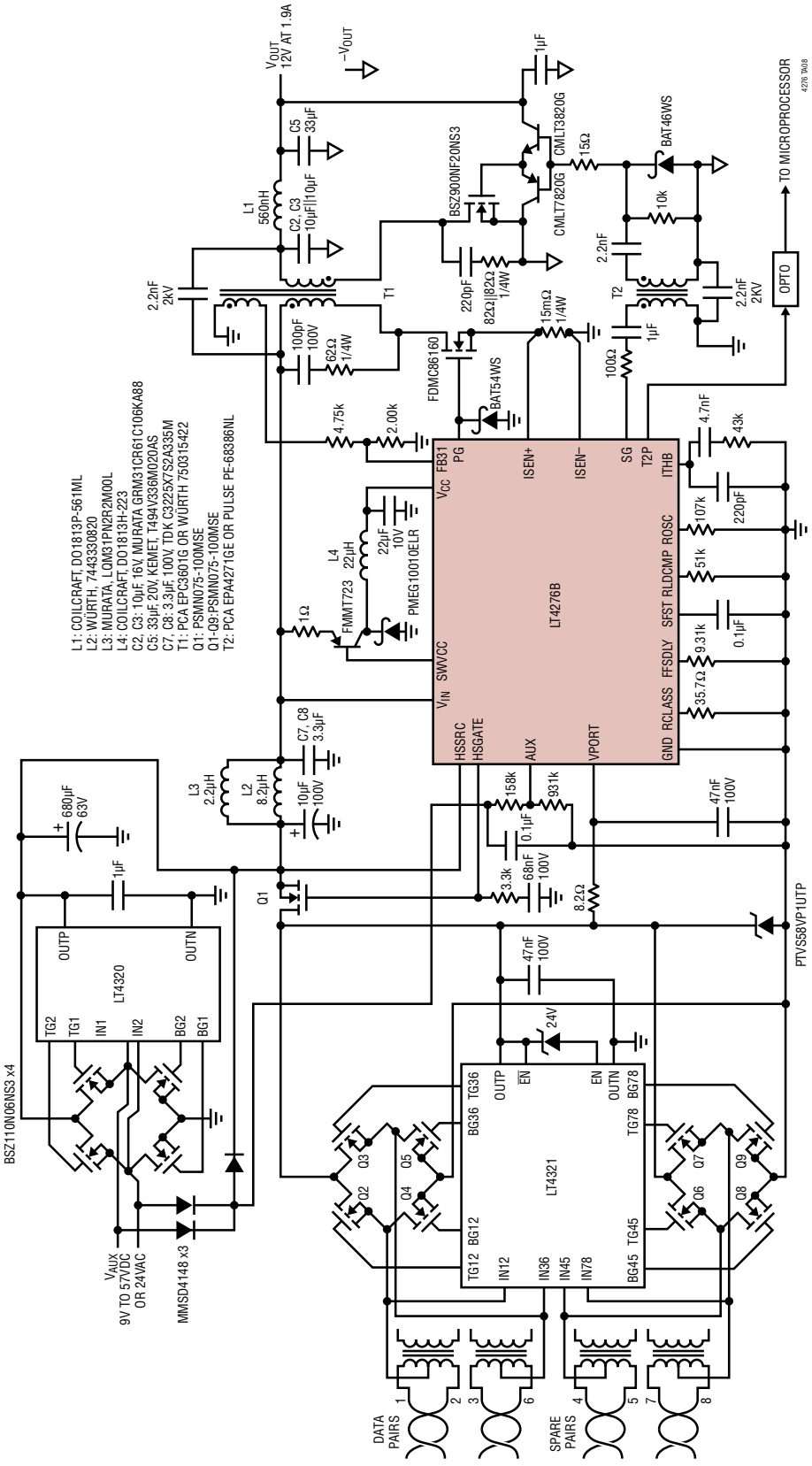


Efficiency vs Load Current

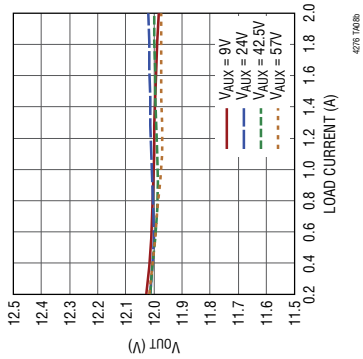


TYPICAL APPLICATIONS

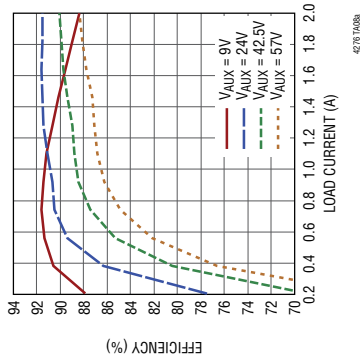
25.5W (Type 2) PoE+ and 9V-57V Auxiliary Input Power Supply in Flyback Mode with 12V, 1.9A Output



Output Regulation vs Load Current

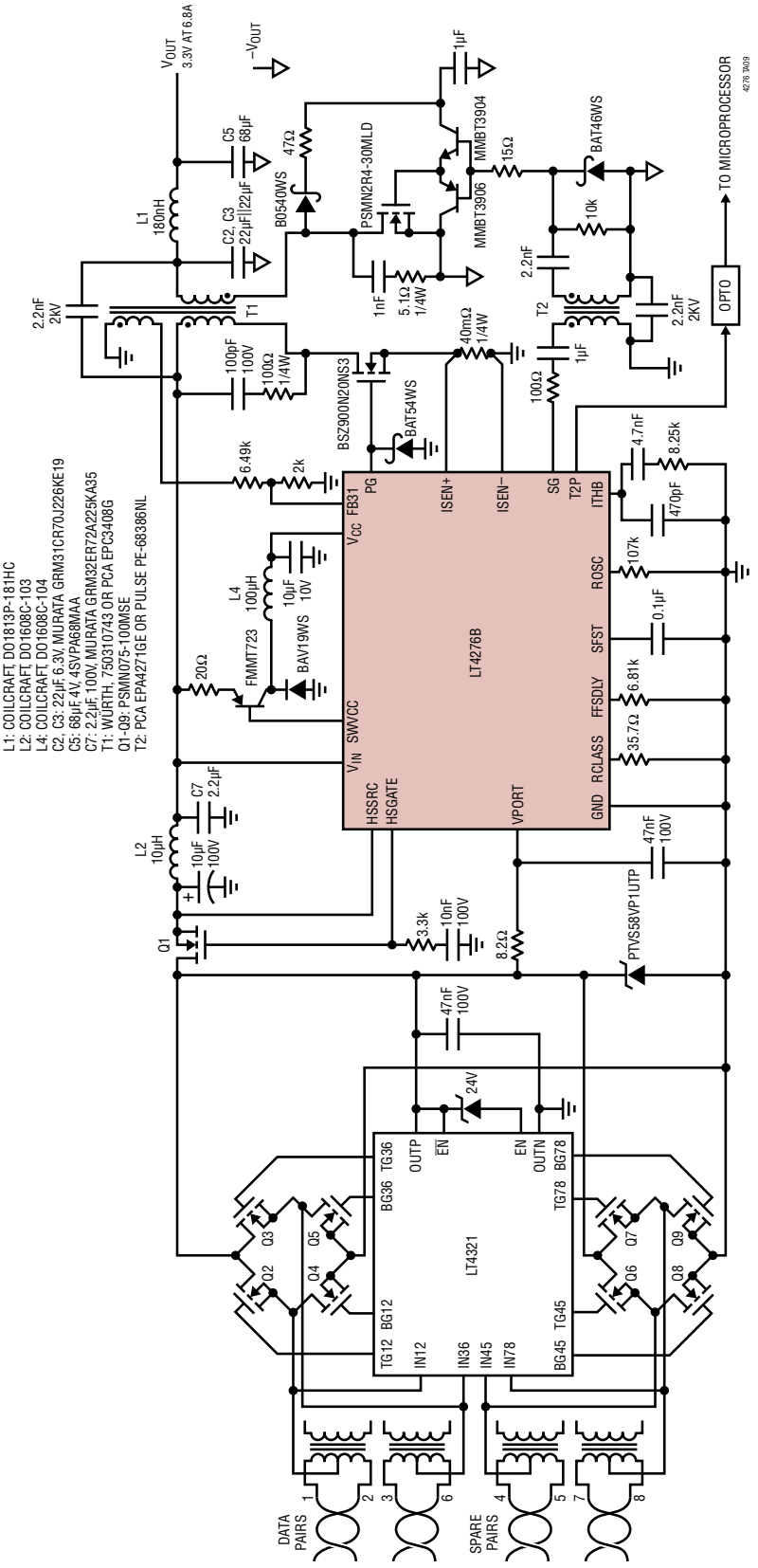


Efficiency vs Load Current

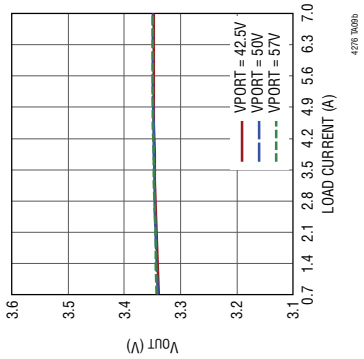


TYPICAL APPLICATIONS

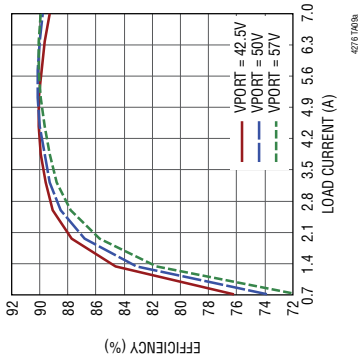
25.5W (Type 2) PoE+ Power Supply in Flyback Mode with 3.3V, 6.8A Output



Output Regulation vs Load Current

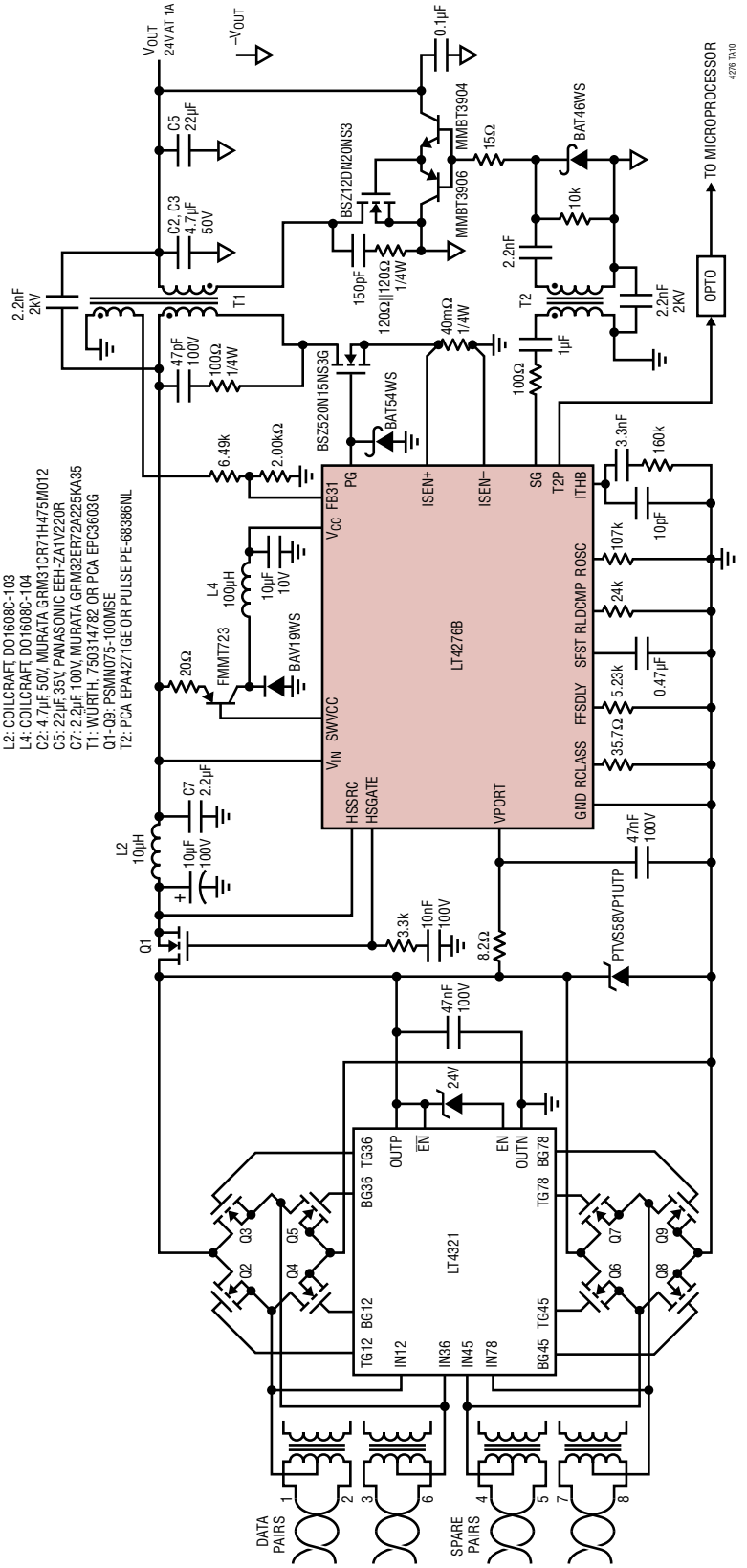


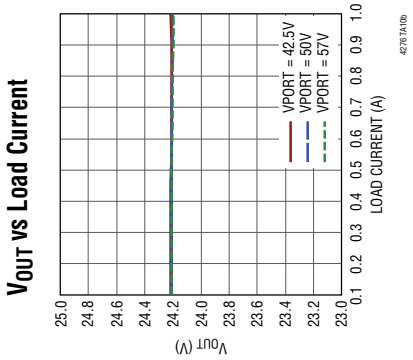
Efficiency vs Load Current

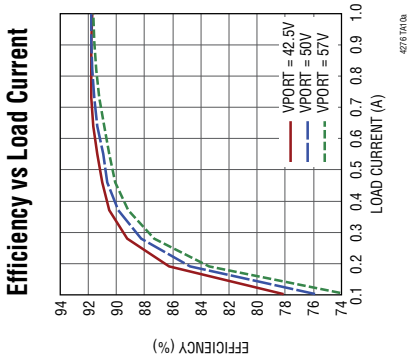


TYPICAL APPLICATIONS

25.5W (Type 2) PoE+ Power Supply in Flyback Mode with 24V, 1A Output



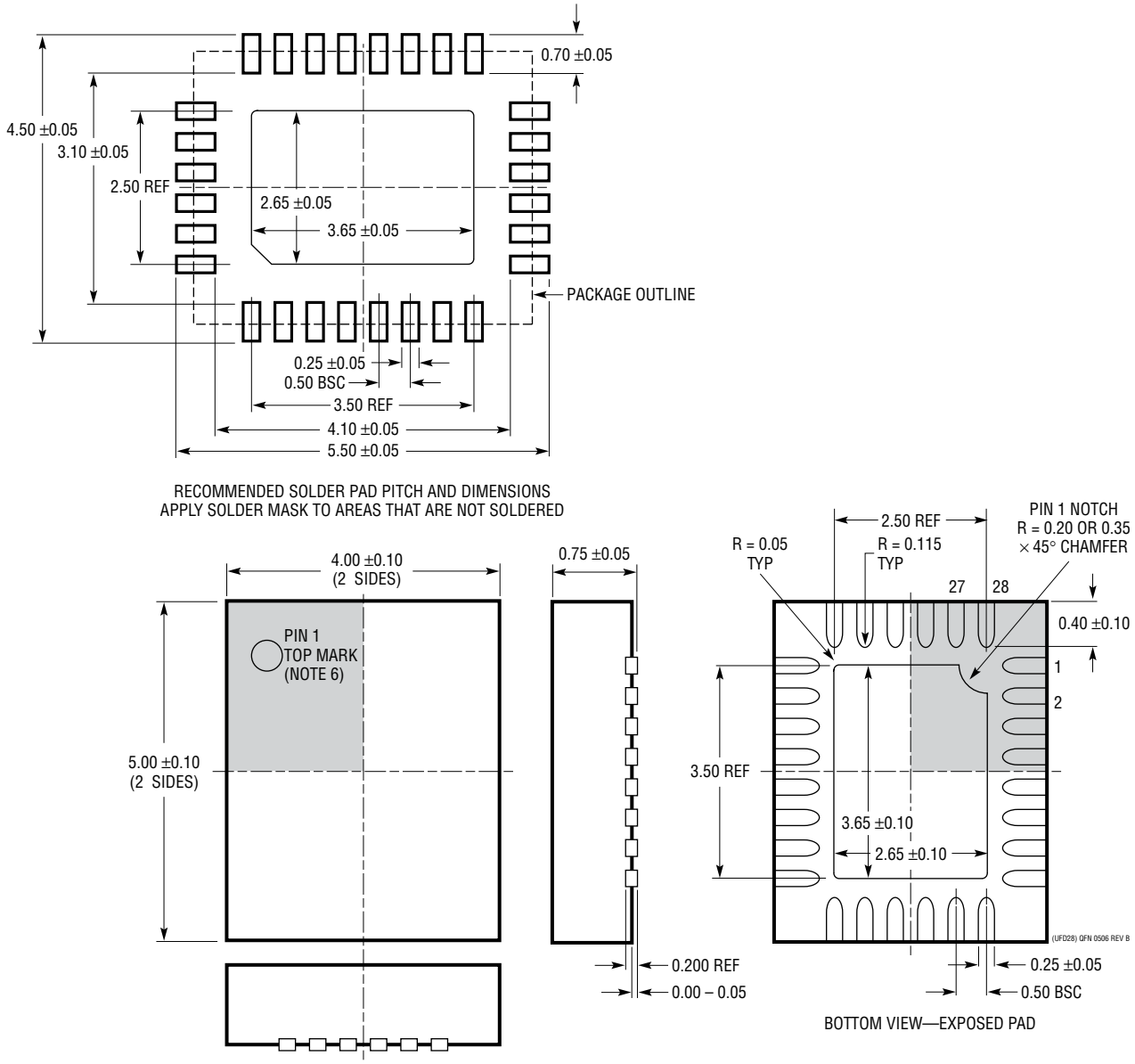




PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT4276#packaging for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev B)



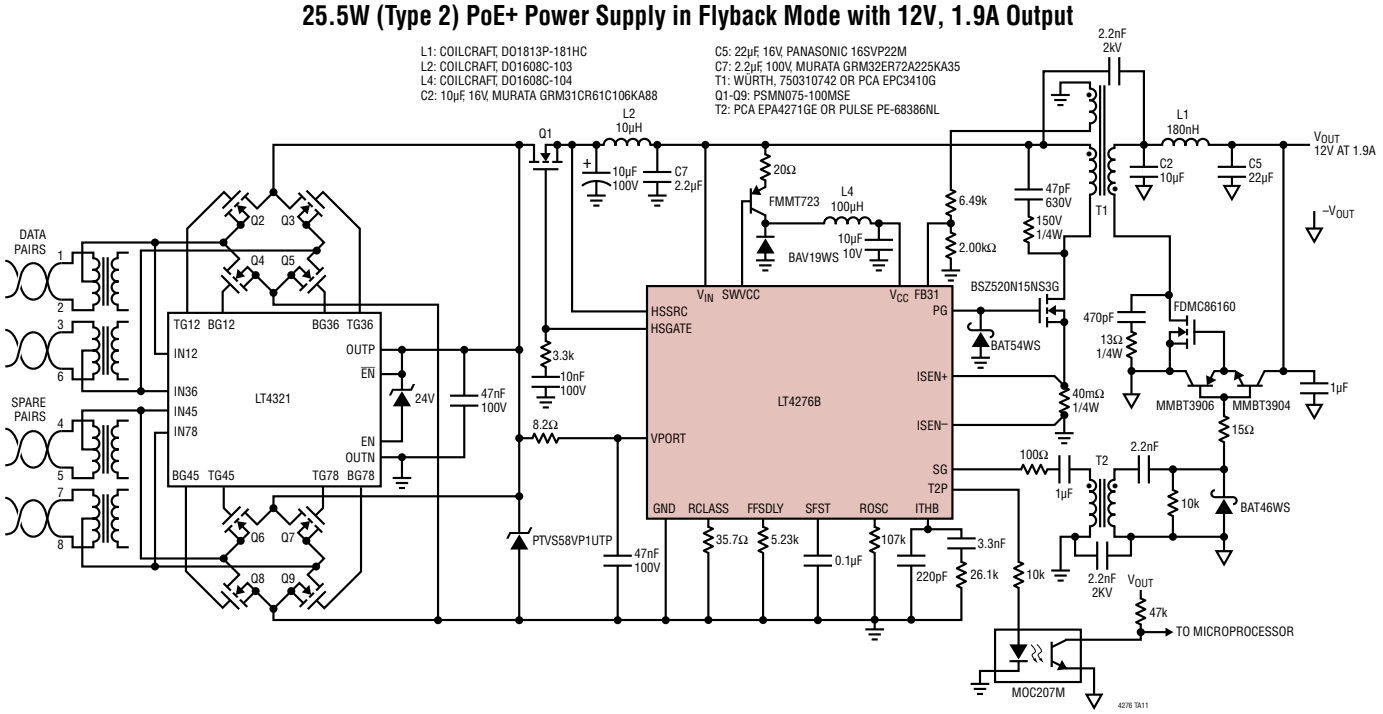
NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

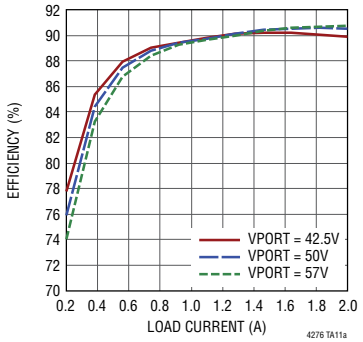
REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/15	Changed diode type of diode between SWVCC and V_{CC} from Schottky to regular (BAV19WS) on all applicable schematics.	1, 10, 16-20, 22, 23
		Added additional conditions to V_{AUXT} and I_{AUXH} parameters.	3
		Revised graph: PG Delay Time vs Temperature in Flyback Mode.	5
		Added T2 transformer part number recommendation to all flyback schematics.	16, 17, 19-23, 26
		Updated parts list for 25.5W (12V/1.9A) flyback schematic.	21

TYPICAL APPLICATION

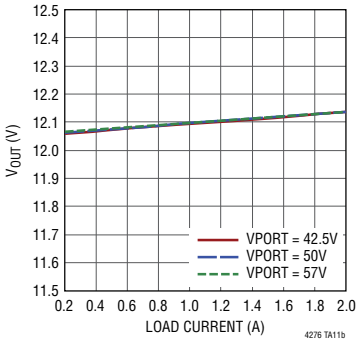
25.5W (Type 2) PoE+ Power Supply in Flyback Mode with 12V, 1.9A Output



Efficiency vs Load Current



Output Regulation vs Load Current



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4267/ LTC4267-1/ LTC4267-3	IEEE 802.3af PD Interface With Integrated Switching Regulator	Internal 100V, 400mA Switch, Programmable Class, 200/300kHz Constant Frequency PWM
LTC4269-1	IEEE 802.3af PD Interface With Integrated Flyback Switching Regulator	2-Event Classification, Programmable Class, Synchronous No-Opto Flyback Controller, 50kHz to 250kHz, Aux Support
LTC4269-2	IEEE 802.3af PD Interface With Integrated Forward Switching Regulator	2-Event Classification, Programmable Class, Synchronous Forward Controller, 100kHz to 500kHz, Aux Support
LT4275A/B/C	LTPoE++/PoE+/PoE PD Controller	External Switch, LTPoE++ Support
LTC4278	IEEE 802.3af PD Interface With Integrated Flyback Switching Regulator	2-Event Classification, Programmable Class, Synchronous No-Opto Flyback Controller, 50kHz to 250kHz, 12V Aux Support
LTC4290/LTC4271	8-Port PoE/PoE+/LTPoE++ PSE Controller	Transformer Isolation, Supports IEEE 802.3af, IEEE 802.3at and LTPoE++ PDs
LT4320/LT4320-1	Ideal Diode Bridge Controller	9V-72V ,DC to 600Hz Input. Controls 4-NMOSFETs, Voltage Rectification without Diode Drops
LT4321	PoE Ideal Diode Bridge Controller	Controls 8-NMOSFETs for IEEE-required PD Voltage Rectification without Diode Drops

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