3.3V Single Supply Video Difference Amplifier

FEATURES

- **Differential or Single-Ended Gain Block**
- **Wide Supply Range 3V to 12.6V**
- **Output Swings Rail-to-Rail**
- **Input Common Mode Range Includes Ground**
- **600V/µs Slew Rate**
- **–3dB Bandwidth = 75MHz, A_V = ±2**
- CMRR at 10MHz: >60dB
- Specified on 3.3V, 5V and ±5V Supplies
- High Output Drive: ±70mA
- Power Shutdown to 300µA
- Operating Temperature Range: –40°C to 85°C
- Available in 8-Lead SO and Tiny 3mm x 3mm x 0.8mm DFN Packages

APPLICATIONS

- Differential to Single-Ended Conversion
- Video Line Driver
- Automotive Displays
- RGB Amplifiers
- Coaxial Cable Drivers
- Low Voltage High Speed Signal Processing

DESCRIPTION

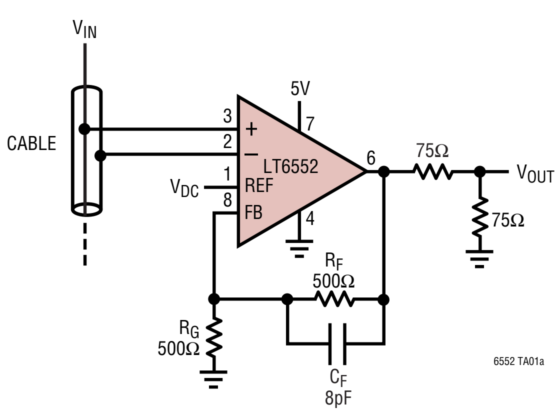
The LT®6552 is a video difference amplifier optimized for low voltage single supply operation. This versatile amplifier features uncommitted high input impedance (+) and (–) inputs and can be used in differential or single-ended configurations. A second set of inputs gives gain adjustment and DC control to the differential amplifier.

On a single 3.3V supply, the input voltage range extends from ground to 1.3V and the output swings from ground to 2.9V while driving a 150Ω load. The LT6552 features 75MHz – 3dB bandwidth, 600V/µs slew rate, and ±70mA output current making it ideal for driving cables directly. The LT6552 maintains its performance for supplies from 3V to 12.6V and is fully specified at 3.3V, 5V and ±5V supplies. The shutdown feature reduces power dissipation to less than 1mW and allows multiple amplifiers to drive the same cable.

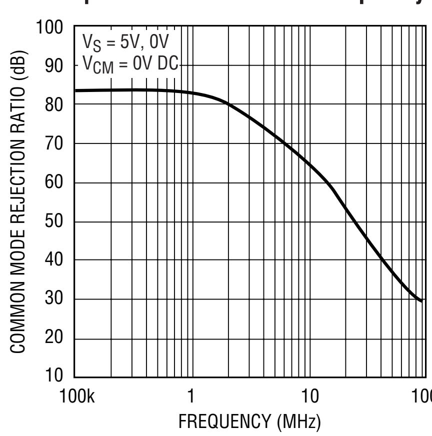
The LT6552 is available in the 8-lead SO package as well as a tiny, dual fine pitch leadless package (DFN). The device is specified over the commercial and industrial temperature ranges.

TYPICAL APPLICATION

Cable Sense Amplifier for Loop Through Connections with DC Adjust



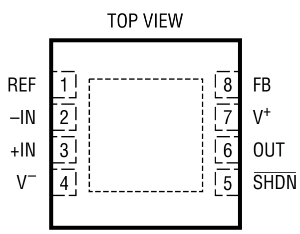
Input Referred CMRR vs Frequency



ABSOLUTE MAXIMUM RATINGS (Note 1)

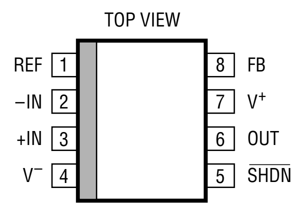
Supply Voltage (V^+ to V^-) 12.6V
Input Current (Note 2) .... ±10mA
Input Voltage Range .... V^- to V^+
Differential Input Voltage
+Input (Pin 3) to –Input (Pin 2) .... $\pm V_S$
Output Short-Circuit Duration (Note 3) .... Indefinite
Operating Temperature Range (Note 4) ...–40°C to 85°C
Specified Temperature Range (Note 5) ....–40°C to 85°C
Maximum Junction Temperature .... 150°C
(DD Package) .... 125°C
Storage Temperature Range ....–65°C to 150°C
(DD Package) ....–65°C to 125°C
Lead Temperature
(Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 160°C/W
UNDERSIDE METAL CONNECTED TO V–
(PCB CONNECTION OPTIONAL)

ORDER PART NUMBER
LT6552CDD LT6552IDD
DD PART MARKING*
LADR



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LT6552CS8 LT6552IS8
S8 PART MARKING
6552 6552I

*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for parts specified with wider operating temperature ranges.

3.3V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 3.3V, 0V. Figure 1 shows the DC test circuit, $V_{REF} = V_{CM}$ = 1V, V_{DIFF} = 0V, $V_{\overline{SHDN}} = V^+$, unless otherwise noted. $R_L = R_F + R_G$ = 1k. (Note 6)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Both Inputs (Note 7)			5	20	mV
			●			25	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift		●		40		µV/°C
I_B	Input Bias Current	Any Input	●		20	50	µA
I_{OS}	Input Offset Current	Either Input Pair	●		1	5	µA

3.3V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 3.3V, 0V. Figure 1 shows the DC test circuit, V_{REF} = V_{CM} = 1V, V_{DIFF} = 0V, $V_{\overline{SHDN}}$ = V^+, unless otherwise noted. R_L = R_F + R_G = 1k. (Note 6)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
e_n	Input Noise Voltage Density	f = 10kHz			55		nV/√Hz
i_n	Input Noise Current Density	f = 10kHz			0.7		pA/√Hz
R_{IN}	Input Resistance	Common Mode, V_{CM} = 0V to 1.3V			300		kΩ
CMRR	Common Mode Rejection Ratio	V_{CM} = 0V to 1.3V	●	58	83		dB
	Input Range		●	0		1.3	V
PSRR	Power Supply Rejection	V_S = 3V to 12V	●	48	54		dB
	Minimum Supply (Note 8)		●	3			V
G_E	Gain Error	V_O = 0.5V to 2V, R_L = 1k R_L = 150Ω	● ●		1 1	3 3	% %
V_{OH}	Swing High	(V_{DIFF} = 0.4V), V_{REF} (Pin 1) = 0V, A_V = 10 R_L = 1k R_L = 150Ω R_L = 75Ω	 ● ● 	 3.1 2.5 2	 3.2 2.9 2.5		 V V V
V_{OL}	Swing Low	(V_{DIFF} = –0.1V), V_{REF}(Pin 1) = 0V, A_V = 10 R_L = 1k I_{SINK} = 5mA I_{SINK} = 10mA	 ● ● ●		 8 65 40	 50 120 200	 mV mV mV
SR	Slew Rate	V_{OUT} = 0.5V to 2.5V Measure from 1V to 2V, R_L = 150Ω, A_V = 2			350		V/µs
FPBW	Full-Power Bandwidth (Note 9)	V_O = $2V_{P-P}$			55		MHz
BW	Small-Signal –3dB Bandwidth	A_V = 2, R_L = 150Ω			65		MHz
t_r, t_f	Rise Time, Fall Time (Note 10)	A_V =50, V_O = 0.5V to 2.5V, 20% to 80%, R_L = 150Ω			125	175	ns
t_S	Settling Time to 3% Settling Time to 1%	A_V = 2, ΔV_{OUT} = 2V, Positive Step R_L = 150Ω			20 30		ns ns
	Differential Gain	A_V = 2, R_L = 150Ω, Output Black Level = 0.6V			0.4		%
	Differential Phase	A_V = 2, R_L = 150Ω, Output Black Level = 0.6V			0.15		Deg
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{DIFF} = 1V	 ●	35 25	50		mA mA
I_S	Supply Current		 ●		12.5	13.5 15	mA mA
	Supply Current, Shutdown	$V_{\overline{SHDN}}$ = 0.5V	●		300	750	µA
V_L	Shutdown Pin Input Low Voltage		●			0.5	V
V_H	Shutdown Pin Input High Voltage		●	3			V
	Shutdown Pin Current	$V_{\overline{SHDN}}$ = 0.5V $V_{\overline{SHDN}}$ = 3V	● ●		40 3	150 10	µA µA
t_{ON}	Turn On-Time	$V_{\overline{SHDN}}$ from 0.5V to 3V			250		ns
t_{OFF}	Turn Off-Time	$V_{\overline{SHDN}}$ from 3V to 0.5V			450		ns
	Shutdown Output Leakage Current	$V_{\overline{SHDN}}$ = 0.5V, 0V ≤ V_{OUT} ≤ V^+	●		0.25		µA

5V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, 0V; Figure 1 shows the DC test circuit, V_{REF} = V_{CM} = 1V, V_{DIFF} = 0V, $V_{\overline{SHDN}}$ = V^+, unless otherwise noted. R_L = R_F + R_G = 1k. (Note 6)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Both Inputs (Note 7)	 ●		5	20 25	mV mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift		●		40		µV/°C
I_B	Input Bias Current	Any Input	●		20	50	uA
I_{OS}	Input Offset Current	Either Input Pair	●		1	5	uA
e_n	Input Noise Voltage Density	f = 10kHz			55		nV/√Hz
i_n	Input Noise Current Density	f = 10kHz			0.7		pA/√Hz
R_{IN}	Input Resistance	Common Mode, V_{CM} = 0V to 3V			300		kΩ
CMRR	Common Mode Rejection Ratio	V_{CM} = 0V to 3V	●	58	83		dB
	Input Range		●	0		3	V
PSRR	Power Supply Rejection	V_S = 3V to 12V	●	48	54		dB
	Minimum Supply (Note 8)		●	3			V
G_E	Gain Error	V_O = 0.5V to 3.5V, R_L = 1k R_L = 150Ω	● ●		1 1	3 3	% %
V_{OH}	Swing High	(V_{DIFF} = 0.6V), V_{REF}(Pin 1) = 0V, A_V = 10 R_L = 1k R_L = 150Ω R_L = 75Ω, 0°C ≤ T_A ≤ 70°C (Only)	 ● ● ●	 4.8 3.6 2.75	 4.875 4.3 3.4		 V V V
V_{OL}	Swing Low	(V_{DIFF} = –0.1V), V_{REF} (Pin 1) = 0V, A_V = 10 R_L = 1k I_{SINK} = 5mA I_{SINK} = 10mA	 ● ● ●		 8 65 110	 50 120 200	 mV mV mV
SR	Slew Rate	V_{OUT} = 0.5V to 3.5V Measure from 1V to 3V, R_L = 150Ω, A_V = 2			 450		 V/µs
FPBW	Full-Power Bandwidth (Note 9)	V_O = $2V_{P-P}$			70		MHz
BW	Small-Signal –3dB Bandwidth	A_V = 2, R_L = 150Ω			70		MHz
t_r, t_f	Rise Time, Fall Time	5V, 0V; A_V = 50, V_O = 0.5V to 3.5V, 20% to 80%, R_L = 1k			125	175	ns
t_S	Settling Time to 3% Settling Time to 1%	A_V = 2, ΔV_{OUT} = 2V, Positive Step R_L = 150Ω			20 30		ns ns
	Differential Gain	A_V = 2, R_L = 150Ω, Output Black Level = 1V			0.25		%
	Differential Phase	A_V = 2, R_L = 150Ω, Output Black Level = 1V			0.04		Deg
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{DIFF} = 1V 0°C ≤ T_A ≤ 70°C –40°C ≤ T_A ≤ 85°C	 ● ●	50 45 35	70		mA mA mA
I_S	Supply Current		 ●		13.5	14.5 16	mA mA
	Supply Current Shutdown	$V_{\overline{SHDN}}$ = 0.5V	●		400	900	µA
V_L	Shutdown Pin Input Low Voltage		●			0.5	V
V_H	Shutdown Pin Input High Voltage		●	4.7			V
	Shutdown Pin Current	$V_{\overline{SHDN}}$ = 0.5V $V_{\overline{SHDN}}$ = 4.7V	● ●		60 4	200 10	µA µA

5V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, 0V. Figure 1 shows the DC test circuit, V_{REF} = V_{CM} = 1V, V_{DIFF} = 0V, $V_{\overline{SHDN}}$ = V^+, unless otherwise noted. R_L = R_F + R_G = 1k. (Note 6)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ from 0.5V to 4.7V			250		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ from 4.7V to 0.5V			450		ns
	Shutdown Output Leakage Current	$V_{\overline{SHDN}}$ = 0.5V, 0V ≤ V_{OUT} ≤ V^+	●		0.25		µA

±5V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V. Figure 2 shows the DC test circuit, V_{REF} = V_{CM} = 0V, V_{DIFF} = 0V, $V_{\overline{SHDN}}$ = V^+, unless otherwise noted. R_L = R_F + R_G = 1k. (Note 6)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Both Inputs (Note 7)	 ●		10	25 30	mV mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift		●		50		µV/°C
I_B	Input Bias Current	Any Input	●		25	50	µA
I_{OS}	Input Offset Current	Either Input Pair	●		1	5	µA
e_n	Input Noise Voltage Density	f = 10kHz			55		nV/√Hz
i_n	Input Noise Current Density	f = 10kHz			0.7		pA/√Hz
R_{IN}	Input Resistance	Common Mode, V_{CM} = –5V to 3V			300		kΩ
CMRR	Common Mode Rejection Ratio	V_{CM} = –5V to 3V	●	58	75		dB
	Input Range		●	–5		3	V
PSRR	Power Supply Rejection	V_S = ±2V to ±6V, V_{CM} = 0V	●	48	54		dB
G_E	Gain Error	V_O = –3V to 3V, R_L = 1k R_L = 150Ω	● ●		1 1	3 3	% %
	Output Voltage Swing	(V_{DIFF} = ± 0.6V), V_{REF} (Pin 1) = 0V, A_V = 10 R_L = 1k R_L = 150Ω R_L = 75Ω, 0°C ≤ T_A ≤ 70°C (Only)	 ● ● ●	 ±4.8 ±3.6 ±2.75	 ±4.875 ±4.3 ±3.4		 V V V
SR	Slew Rate	V_{CM} = 0V, V_{DIFF} = –1.5V to +1.5V, V_O = –5V to 5V Measure from –2V to 2V, R_L = 150Ω		400	600		V/µs
FPBW	Full-Power Bandwidth	V_O = $6V_{P-P}$ (Note 9)			30		MHz
BW	Small-Signal –3dB Bandwidth	A_V = 2, R_L = 150Ω			75		MHz
t_r, t_f	Rise Time, Fall Time	A_V = 50, V_O = –3V to 3V, 20% to 80%			125	175	ns
t_S	Settling Time to 3% Settling Time to 1%	A_V = 2, ΔV_{OUT} = 6V, Positive Step R_L = 150Ω			25 35		ns ns
	Differential Gain	A_V = 2, R_L = 150Ω, Output Black Level = 0V			0.2		%
	Differential Phase	A_V = 2, R_L = 150Ω, Output Black Level = 0V			0.15		Deg
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{DIFF} = ±1V 0°C ≤ T_A ≤ 70°C –40°C ≤ T_A ≤ 85°C	 ● ●	50 45 35	70		mA mA mA
	Supply Current Shutdown	$V_{\overline{SHDN}}$ = –4.5V	●		650	1400	µA
I_S	Supply Current		 ●		14	16.5 18.5	mA mA
V_L	Shutdown Pin Input Low Voltage		●			–4.5	V
V_H	Shutdown Pin Input High Voltage		●	4.7			V

±5V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V. Figure 2 shows the DC test circuit, V_{REF} = V_{CM} = 0V, V_{DIFF} = 0V, $V_{\overline{SHDN}}$ = V^+, unless otherwise noted. R_L = R_F + R_G = 1k. (Note 6)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Shutdown Pin Current	$V_{\overline{SHDN}}$ = –4.5V $V_{\overline{SHDN}}$ = 4.7V	● ●		85 3	250 10	μA μA
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ from –4.5V to 4.7V			200		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ from 4.7V to –4.5V			400		ns
	Shutdown Output Leakage Current	$V_{\overline{SHDN}}$ = –4.5V, $V^- \le V_{OUT} \le V^+$	●		0.25		μA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The inputs are protected from ESD with diodes to the supplies.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum.

Note 4: The LT6552C/LT6552I are guaranteed functional over the temperature range of –40°C to 85°C.

Note 5: The LT6552C is guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet specified performance from –40°C to 85°C, but is not tested or QA sampled at these temperatures. The LT6552I is guaranteed to meet specified performance from –40°C to 85°C.

Note 6: When R_L = 1k is specified, the load resistor is R_F + R_G, but when R_L = 150Ω or R_L = 75Ω is specified, then an additional resistor of that value is added to the output.

Note 7: V_{OS} measured at the output (Pin 6) is the contribution from both input pairs and is input referred.

Note 8: Minimum supply is guaranteed by the PSRR test.

Note 9: Full power bandwidth is calculated from the slew rate.

FPBW = SR/2πVp

Note 10: V_S = 3.3V, t_r and t_f limits are guaranteed by correlation to V_S = 5V and ±5V tests.

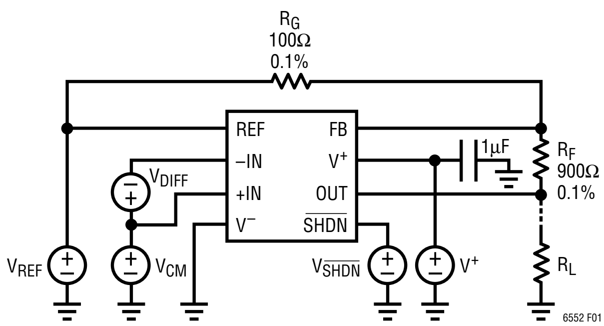


Figure 1. 3.3V, 5V DC Test Circuit

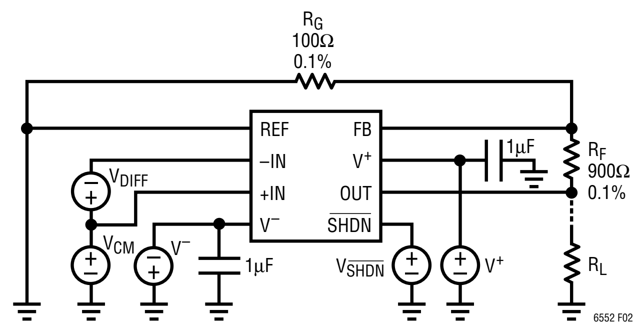
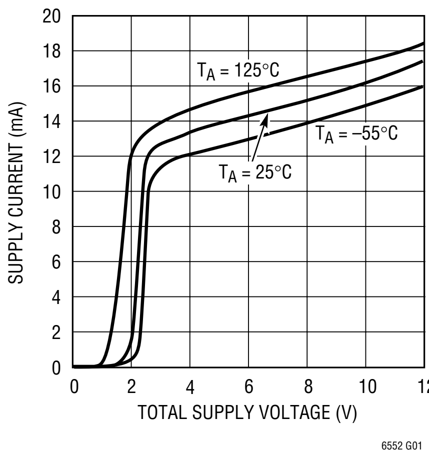


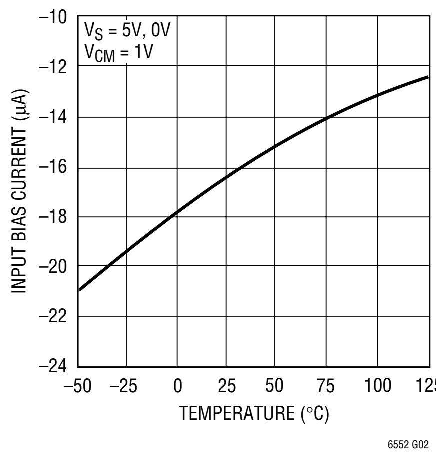
Figure 2. ±5V DC Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

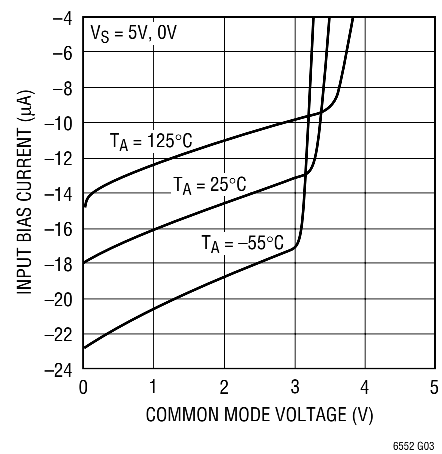
Supply Current vs Supply Voltage



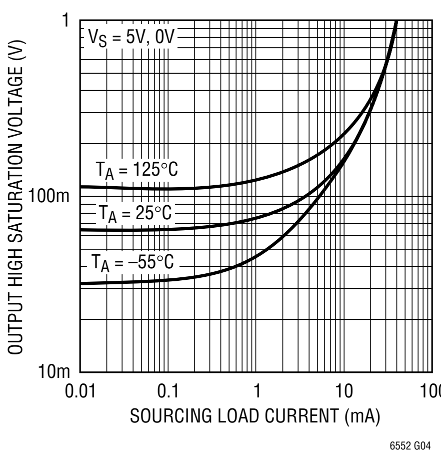
Input Bias Current vs Temperature



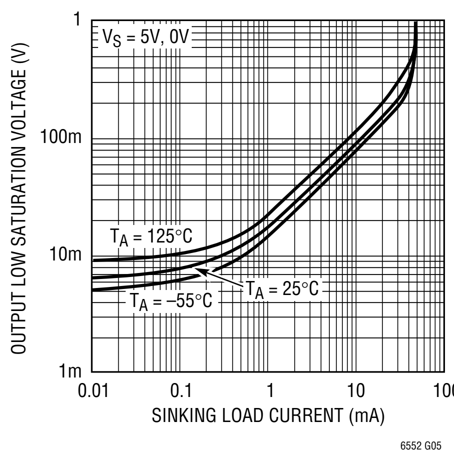
Input Bias Current vs Common Mode Voltage



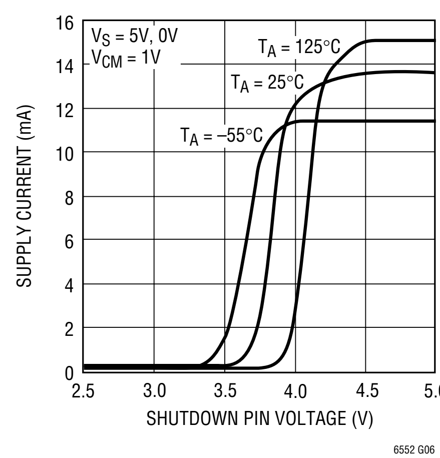
Output Saturation Voltage vs Load Current (Output High)



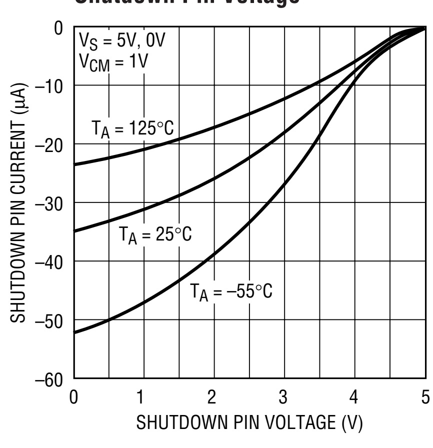
Output Saturation Voltage vs Load Current (Output Low)



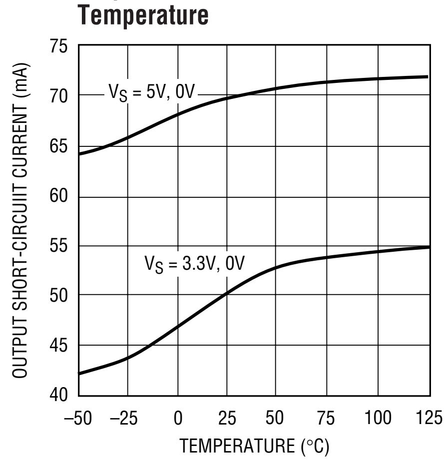
Supply Current vs Shutdown Pin Voltage



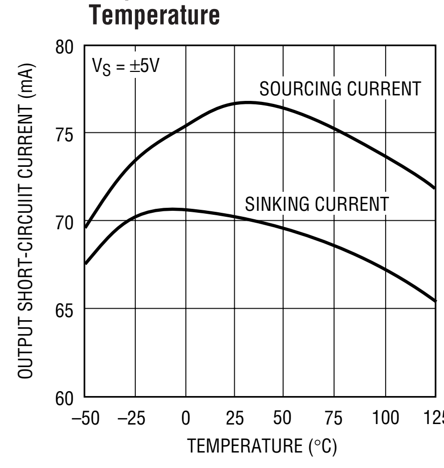
Shutdown Pin Current vs Shutdown Pin Voltage



Output Short-Circuit Current vs Temperature

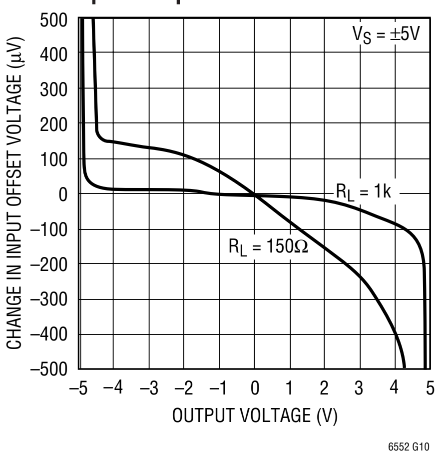


Output Short-Circuit Current vs Temperature

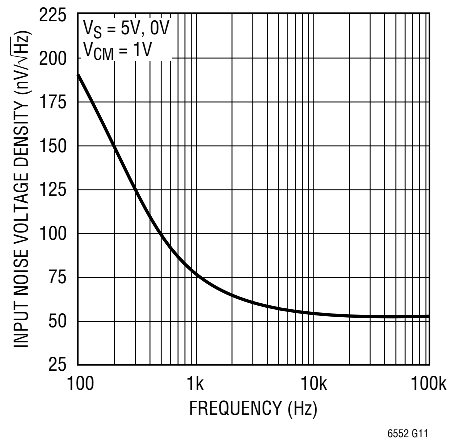


TYPICAL PERFORMANCE CHARACTERISTICS

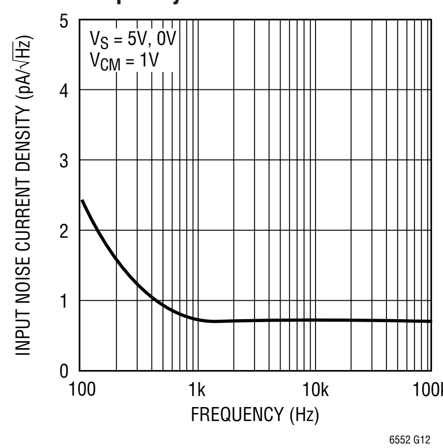
Open-Loop Gain



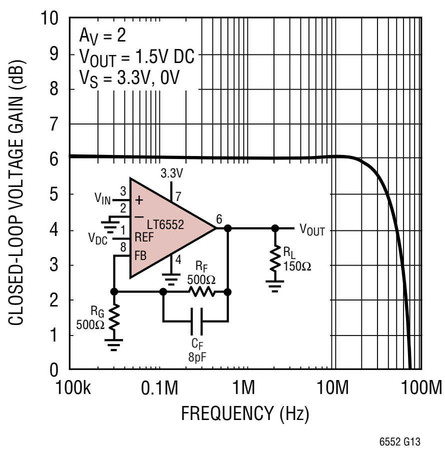
Input Noise Voltage Density vs Frequency



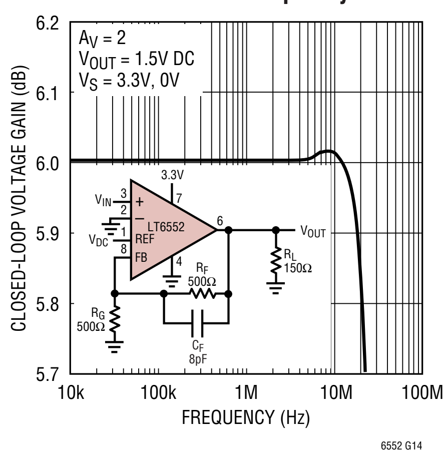
Input Noise Current Density vs Frequency



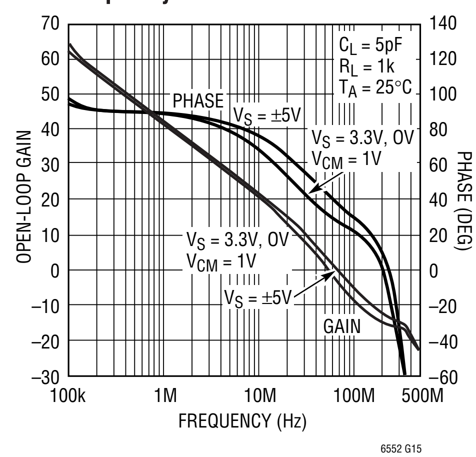
Closed-Loop Voltage Gain vs Frequency



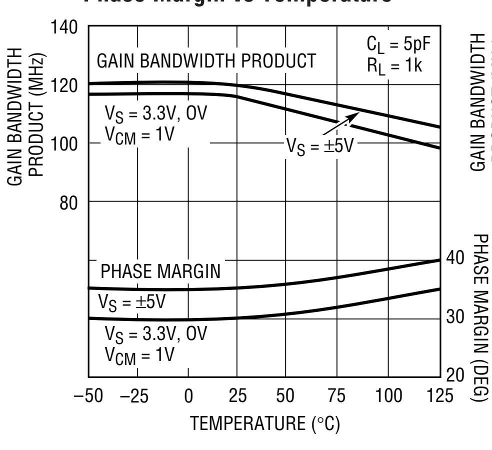
Gain Flatness vs Frequency



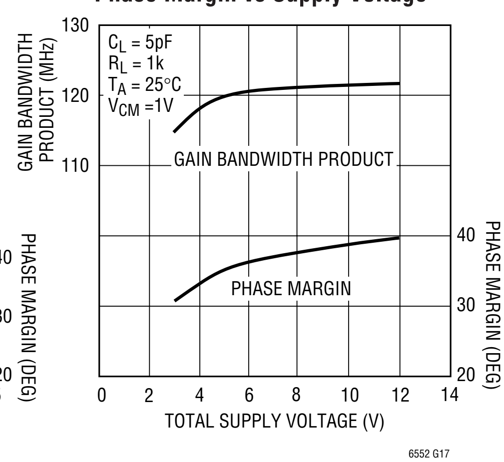
Open-Loop Gain and Phase vs Frequency



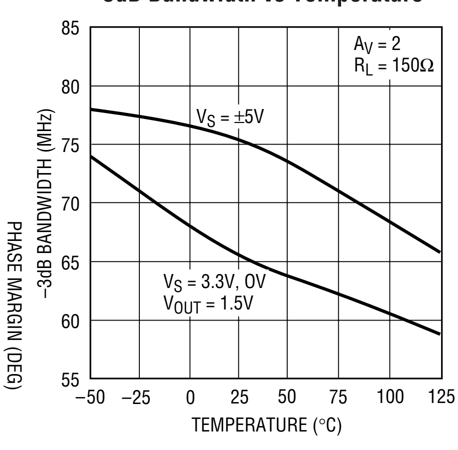
Gain Bandwidth Product and Phase Margin vs Temperature



Gain Bandwidth Product and Phase Margin vs Supply Voltage

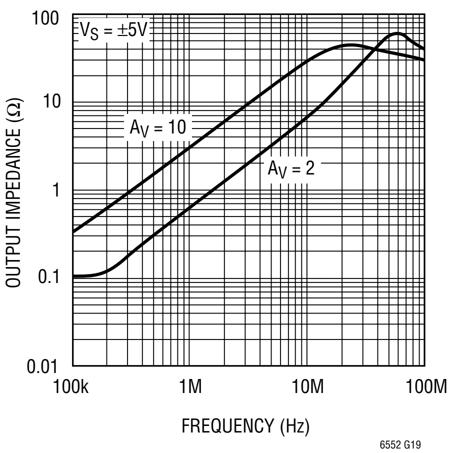


–3dB Bandwidth vs Temperature

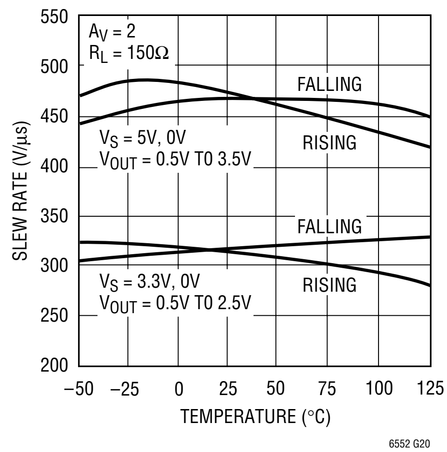


TYPICAL PERFORMANCE CHARACTERISTICS

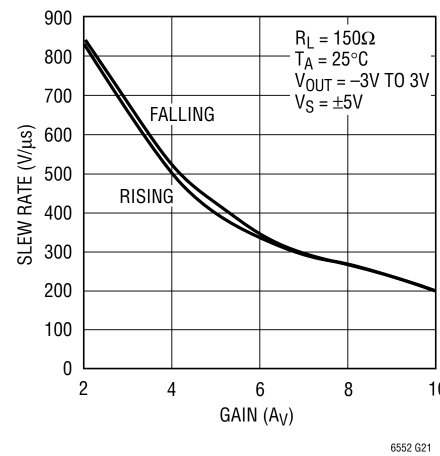
Output Impedance vs Frequency



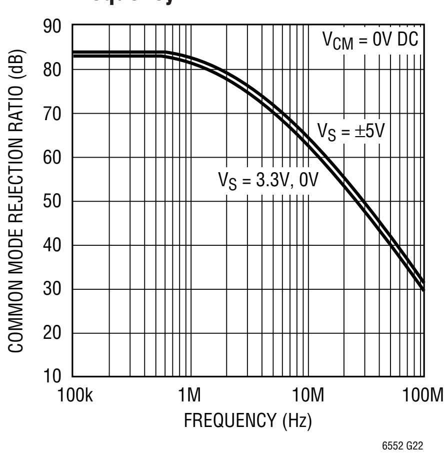
Slew Rate vs Temperature



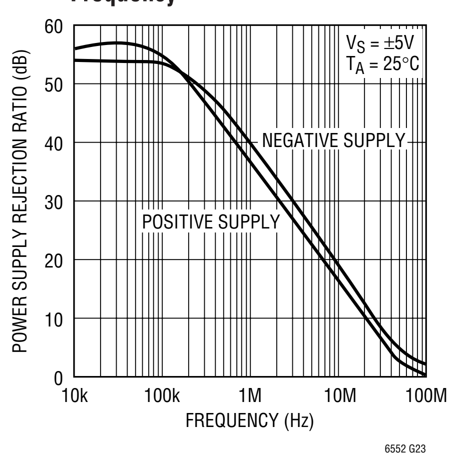
Slew Rate vs Closed-Loop Gain



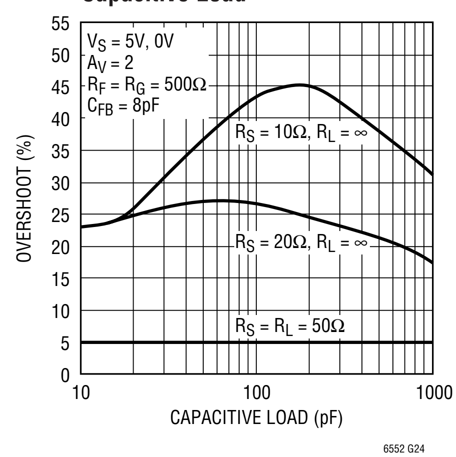
Common Mode Rejection Ratio vs Frequency



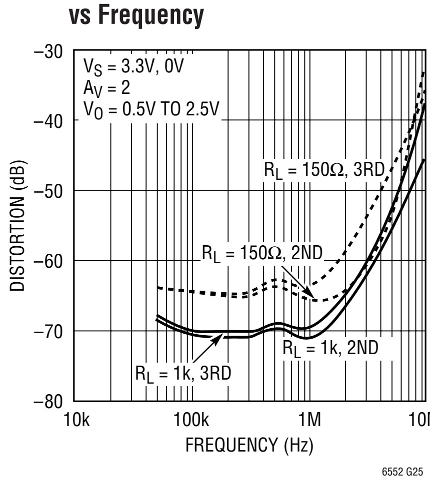
Power Supply Rejection Ratio vs Frequency



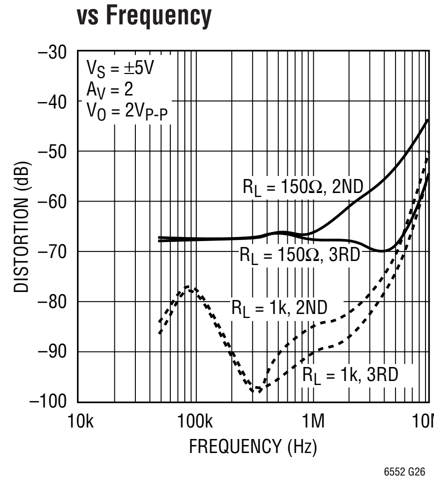
Series Output Resistor vs Capacitive Load



2nd and 3rd Harmonic Distortion vs Frequency

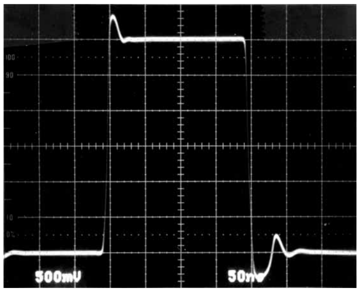


2nd and 3rd Harmonic Distortion vs Frequency



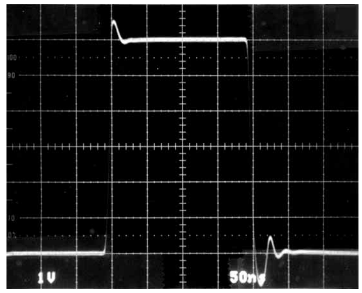
TYPICAL PERFORMANCE CHARACTERISTICS

Large Signal Response, V_S = 5V, 0V



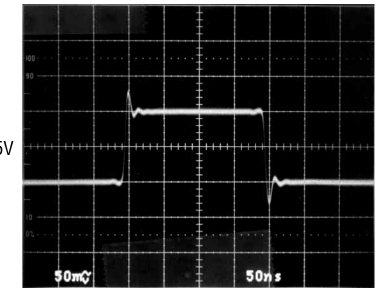
A_V = 2
C_F = 5pF
C_L = 10pF
$R_F = R_G$ = 500Ω
R_L = 150Ω

Large Signal Response, V_S = ±5V



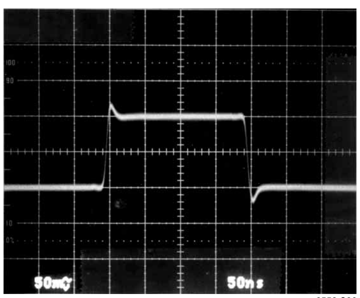
A_V = 2
C_F = 5pF
C_L = 10pF
$R_F = R_G$ = 500Ω
R_L = 150Ω

Small Signal Response, V_S = 5V, 0V



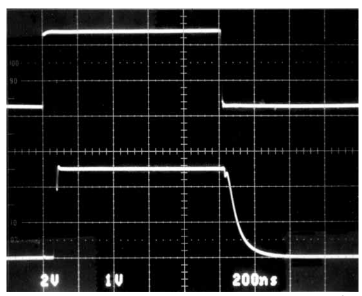
A_V = 1
C_L = 10pF
R_L = 150Ω

Small Signal Response, V_S = 5V, 0V



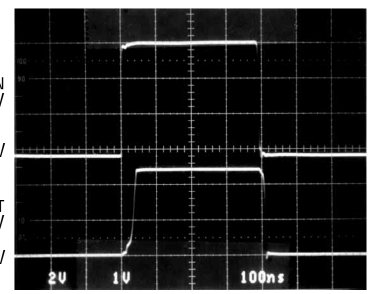
A_V = 2
C_F = 5pF
C_L = 10pF
$R_F = R_G$ = 500Ω
R_L = 150Ω

Shutdown Response



A_V = 2
R_L = 150Ω
V_{IN} = 1.25V
V_S = 5V, 0V

Output Overdrive Recovery



A_V = 2
V_S = 5V, 0V

APPLICATIONS INFORMATION

The LT6552 is a video difference amplifier with two pairs of high impedance inputs. The primary purpose of the LT6552 is to convert high frequency differential signals into a single-ended output, while rejecting any common mode noise. In the simplest configuration, one pair of inputs is connected to the incoming differential signal, while the other pair of inputs is used to set amplifier gain and DC level. The device will operate on either single or dual supplies and has an input common mode range which includes the negative supply. The common mode rejection ratio is greater than 60dB at 10MHz. Feedback is applied to Pin 8 and the LT6552's transient response is optimized for gains of 2 or greater.

Figure 3 shows the single supply connection. The amplifier gain is set by a feedback network from the output to Pin 8 (FB). A DC signal applied to Pin 1 (REF) establishes the output quiescent voltage and the differential signal is applied to Pins 2 and 3.

Figure 4 shows several other connections using dual supplies. In each case, the amplifier gain is set by a feedback network from the output to Pin 8 (FB).

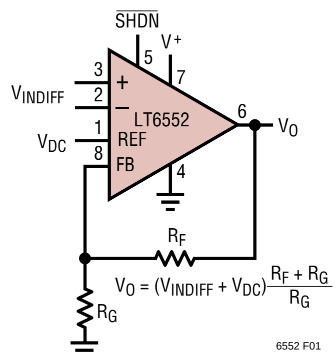


Figure 3

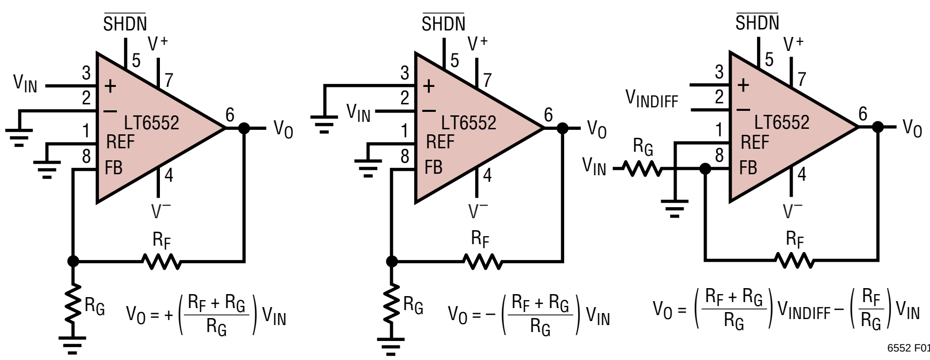


Figure 4

APPLICATIONS INFORMATION

Amplifier Characteristics

Figure 5 shows a simplified schematic of the LT6552. There are two input stages; the first one consists of transistors Q1 to Q8 for the (+) and (–) inputs while the second input stage consists of transistors Q9 to Q16 for the reference and feedback inputs. This topology provides high slew rates at low supply voltages. The input common mode range extends from ground to typically 1.75V from V_{CC}, and is limited by $2V_{BE}$'s plus a saturation voltage of current sources I1-I4. Each input stage drives the degeneration resistors of PNP and NPN current mirrors, Q17 to Q20, that convert the differential signals into a single-ended output. The complementary drive generator supplies current to the output transistors that swing from rail-to-rail.

The current generated through R1 or R2, divided by the capacitor CM, determines the slew rate. Note that this current, and hence the slew rate, are proportional to the magnitude of the input step. The input step equals the output step divided by the closed-loop gain. The highest slew rates are therefore obtained in the lowest gain configurations. The Typical Performance Characteristic Curve of Slew Rate vs Closed-Loop Gain shows the details.

ESD

The LT6552 has reverse-biased ESD protection diodes on all inputs and outputs, as shown in Figure 5. If these pins are forced beyond either supply, unlimited current will flow through these diodes. If the current is transient in nature and limited to 100mA or less, no damage to the device will occur.

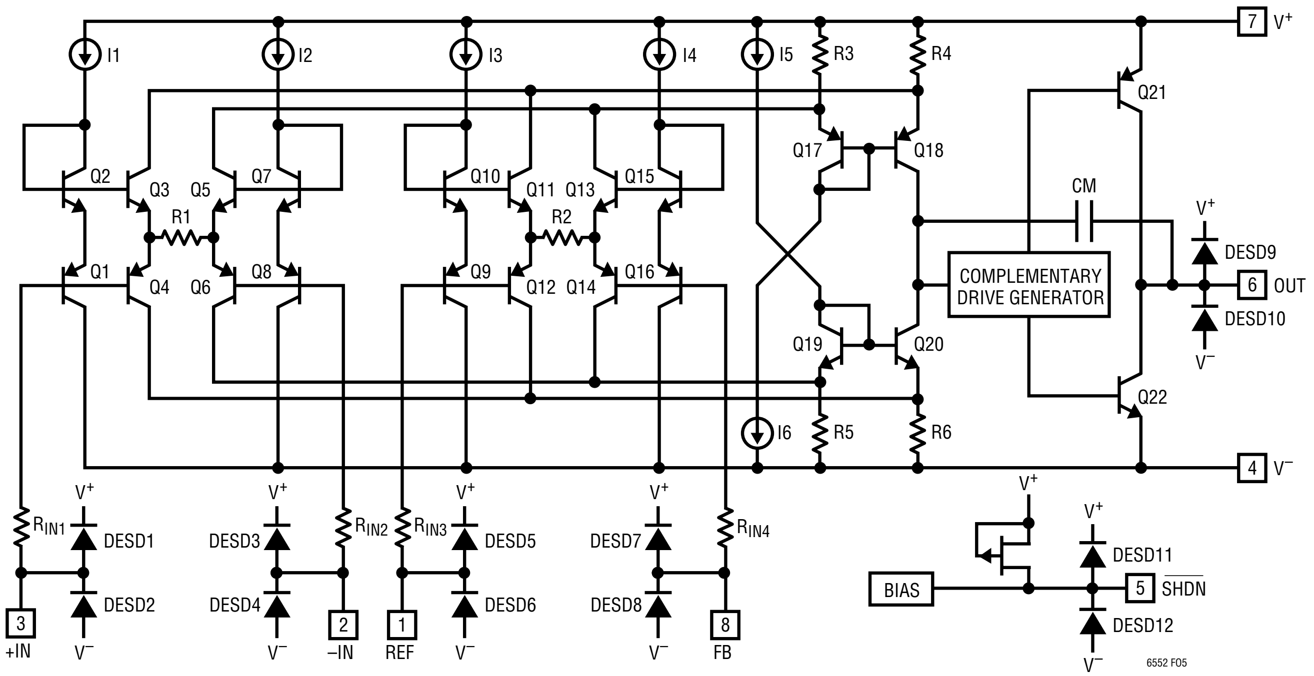


Figure 5. Simplified Schematic

APPLICATIONS INFORMATION

Layout and Passive Components

With a bandwidth of 75MHz and a slew rate of 600V/µs, the LT6552 requires special attention to board layout and supply bypassing. Use a ground plane, short lead lengths and RF quality low ESR supply bypass capacitors. The positive supply pin should be bypassed with a small capacitor (typically 0.1µF) within 1 inch of the pin. When driving loads greater than 10mA, an additional 4.7µF electrolytic capacitor should be used. When using split supplies, the same is true for the negative supply pin. The parallel combination of the feedback resistor and gain setting resistor on Pin 8 (FB) can combine with the input capacitance to form a pole which can degrade stability. In general, use feedback resistors of 1k or less.

Operating with Low Closed-Loop Gains

The LT6552 has been optimized for closed-loop gains of 2 or greater. For a closed-loop gain of 2 the response peaks about 3dB. Peaking can be reduced by using low value feedback resistors, and can be eliminated by placing a capacitor across the feedback resistor (feedback zero). Figure 6 shows the closed-loop gain of 2 frequency response with various values of the feedback capacitor. This peaking shows up as a time domain overshoot of 40%; with an 8pF feedback capacitor the overshoot is eliminated. Figures 7A and 7B show the Small Signal Response of the LT6552 with and without an 8pF feedback capacitor.

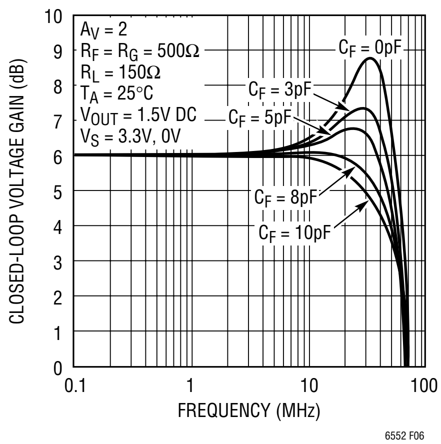


Figure 6. Closed-Loop Gain vs Frequency

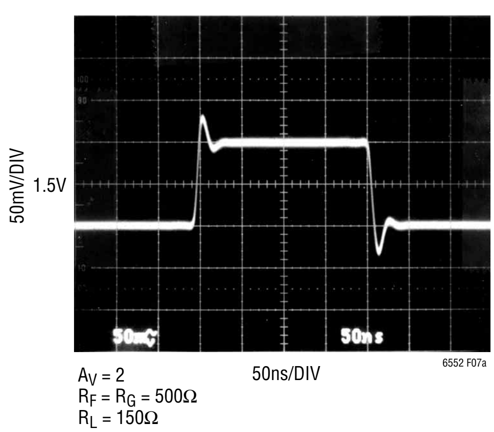


Figure 7A. Small Signal Transient Response, V_S = 3.3V, 0V

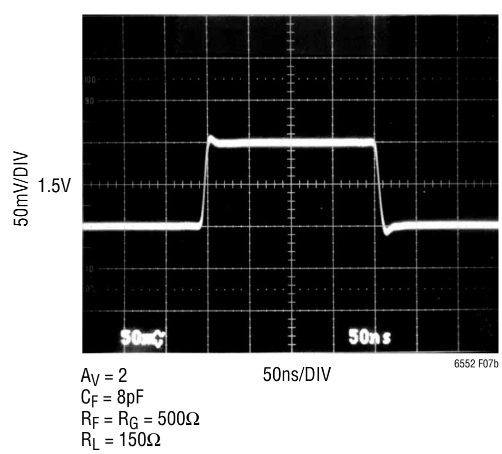


Figure 7B. Small Signal Transient Response, V_S = 3.3V, 0V with 8pF Feedback Capacitor

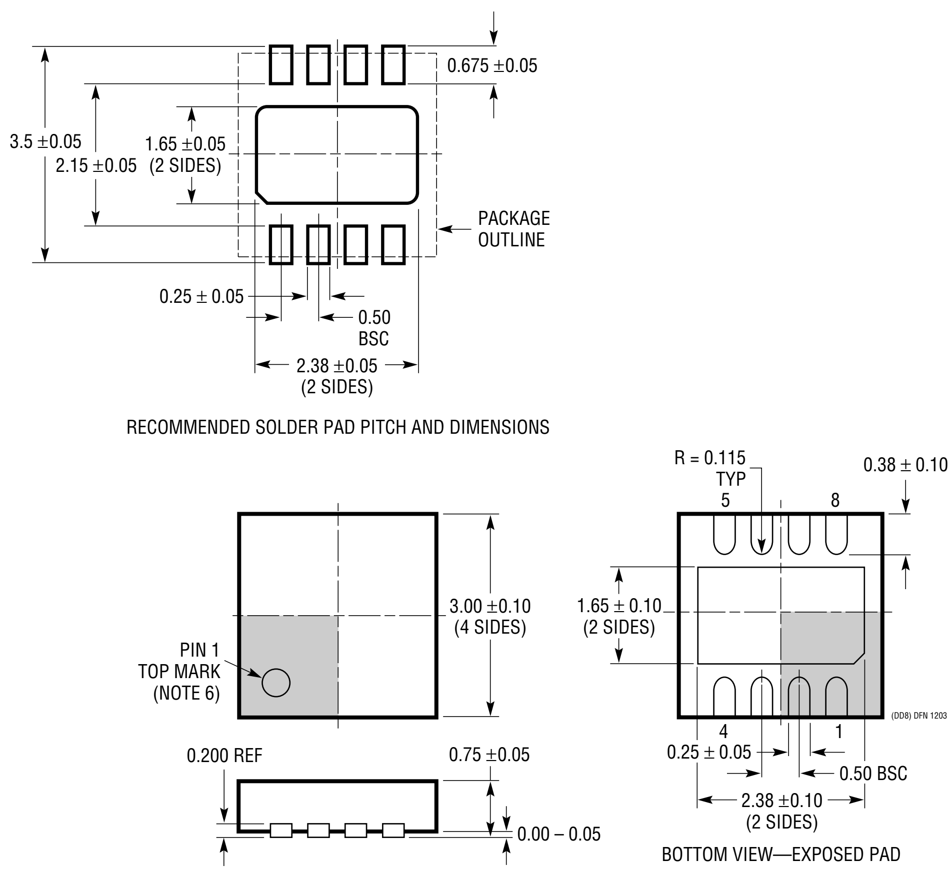
APPLICATIONS INFORMATION

$\overline{\text{SHDN}}$ Pin

The LT6552 includes a shutdown feature that disables the part, reducing quiescent current and making the output high impedance. The part can be shutdown by bringing the $\overline{\text{SHDN}}$ pin within 0.5V of V^-. When shutdown the supply current is typically 400µA and the output leakage current is 0.25µA ($V^- \leq V_{OUT} \leq V^+$). In normal operation the $\overline{\text{SHDN}}$ can be tied to V^+ or left floating; if the pin is left unconnected, an internal FET pull-up will keep the LT6552 fully operational.

PACKAGE DESCRIPTION

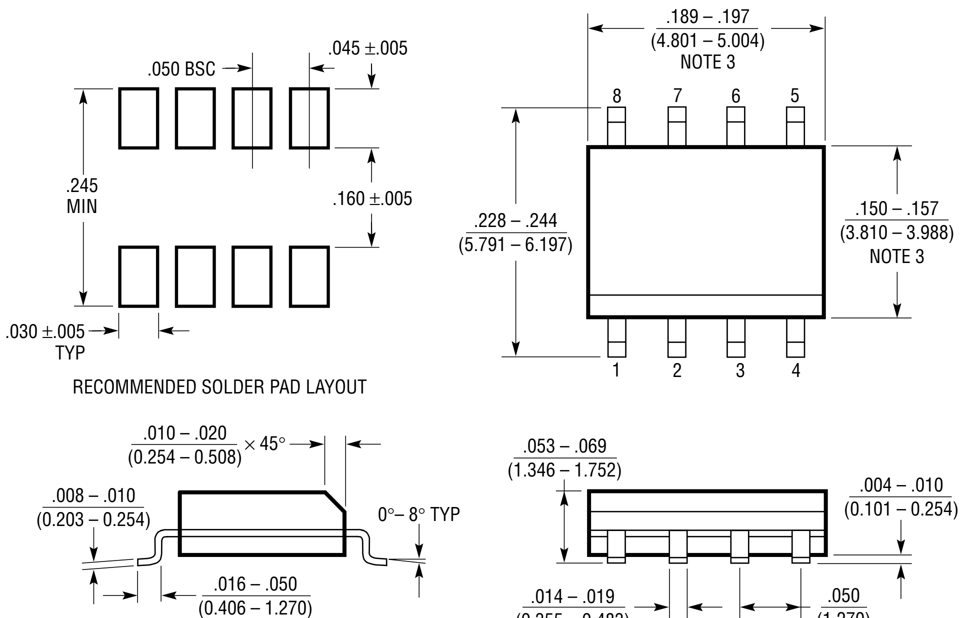
DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)

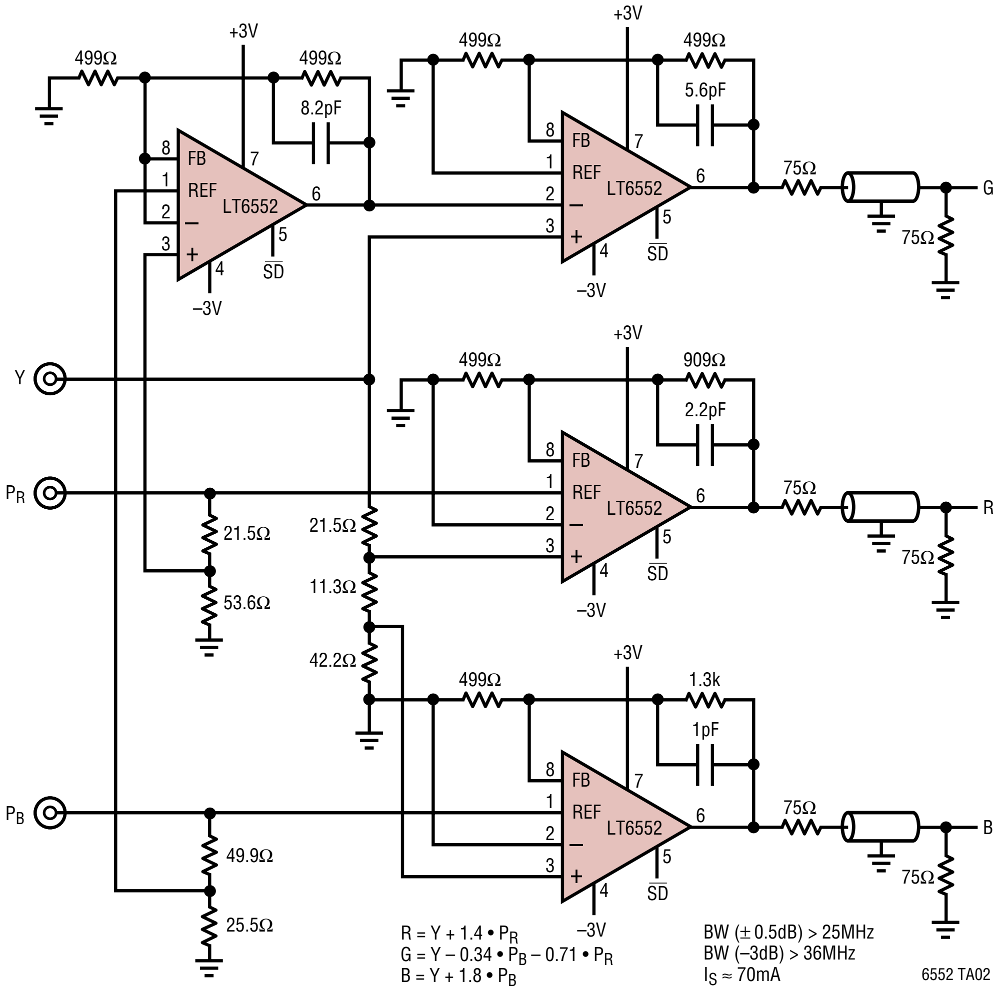


NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

TYPICAL APPLICATION

YP_BP_R to RGB Video Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1193	A_V = 2 Video Difference Amp	80MHz BW, 500V/µs Slew Rate, Shutdown
LT1675	RGB Multiplexer with Current Feedback Amplifiers	–3dB Bandwidth = 250MHz, 100MHz Pixel Switching
LT6205/LT6206/LT6207	Single/Dual/Quad Single Supply 3V, 100MHz Video Op Amps	450V/µs Slew Rate, Rail-to-Rail Output, Input Common Modes to Ground
LT6550/LT6551	3.3V Triple and Quad Video Amplifiers	Internal Gain of 2, 110MHz –3dB Bandwidth, Input Common Modes to Ground

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