Bidirectional Synchronous 100V Buck/Boost Controller with Reverse Supply, Reverse Current and Fault Protection

FEATURES

- **Bidirectional Voltage or Current Regulation**
- **Bidirectional Reverse Current Protection**
- **Input and Output Negative Voltage Protection to –60V**
- **Bidirectional Inrush Current Limit and Boost Output Short Protection**
- **Switching MOSFET Short Detection and Protection**
- **10V Gate Drive**
- Wide Input and Output Voltage Range Up to 100V
- Feedback Voltage Tolerance: ±1.0% Over Temperature
- Bidirectional Programmable Current Regulation and Monitoring
- Extensive Self-Test, Diagnostics and Fault Reporting
- Programmable Fixed or Synchronizable Switching Frequency: 80kHz to 600kHz
- Programmable Soft-Start and Dynamic Current Limit
- Masterless, Fault Tolerant Current Sharing

APPLICATIONS

- Dual Battery Automotive and Industrial Systems
- High Power System Backup and Supply Stabilization
- "N+1" Redundant, High Reliability Power Supplies
- Power Interrupt Protection System

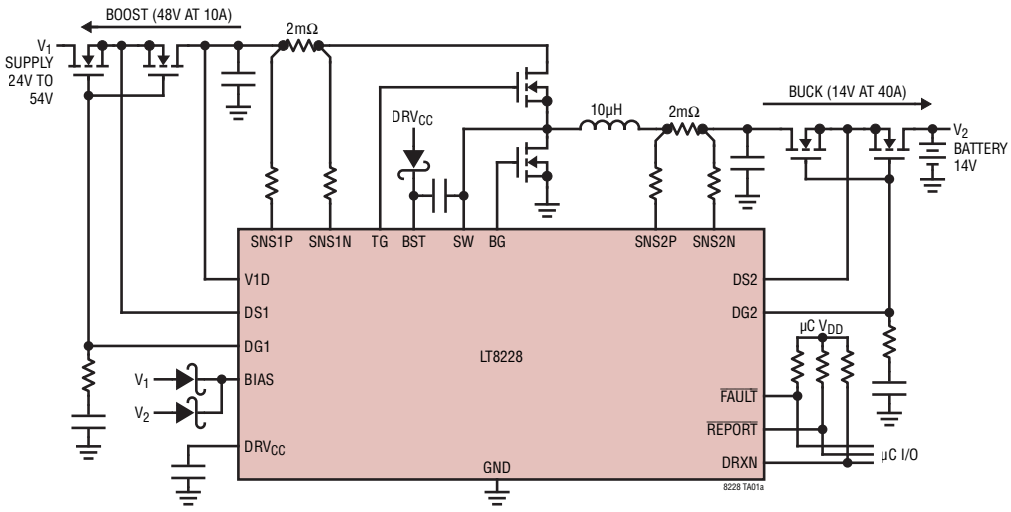
DESCRIPTION

The LT®8228 is a 100V bidirectional constant-current or constant-voltage synchronous buck or boost controller with independent compensation network. The direction of the power flow is automatically determined by the LT8228 or externally controlled. The input and output protection MOSFETs protect against negative voltages, control inrush currents and provide isolation between terminals under fault conditions such as switching MOSFET shorts. In buck mode, the protection MOSFETs at the V_1 terminal prevents reverse current. In boost mode, the same MOSFETs regulate the output inrush current and protects itself with an adjustable timer circuit breaker.

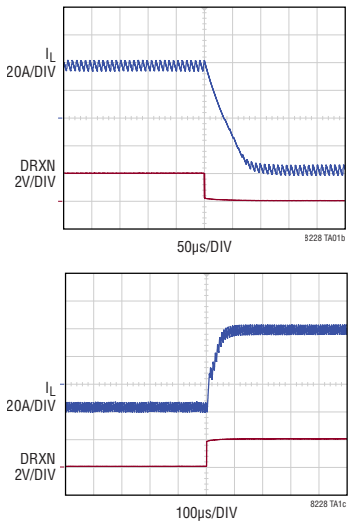
The LT8228 offers bidirectional input and output current limit as well as independent current monitoring. Masterless, fault tolerant current sharing allows any LT8228 in parallel to be added or subtracted while maintaining current sharing accuracy. Internal and external fault diagnostics and reporting are available via the $\overline{\text{FAULT}}$ and $\overline{\text{REPORT}}$ pins. The LT8228 is available in a 38-lead TSSOP package.

TYPICAL APPLICATION

Simplified Bidirectional Battery Backup System



Buck and Boost Mode Transitions



Rev. 0

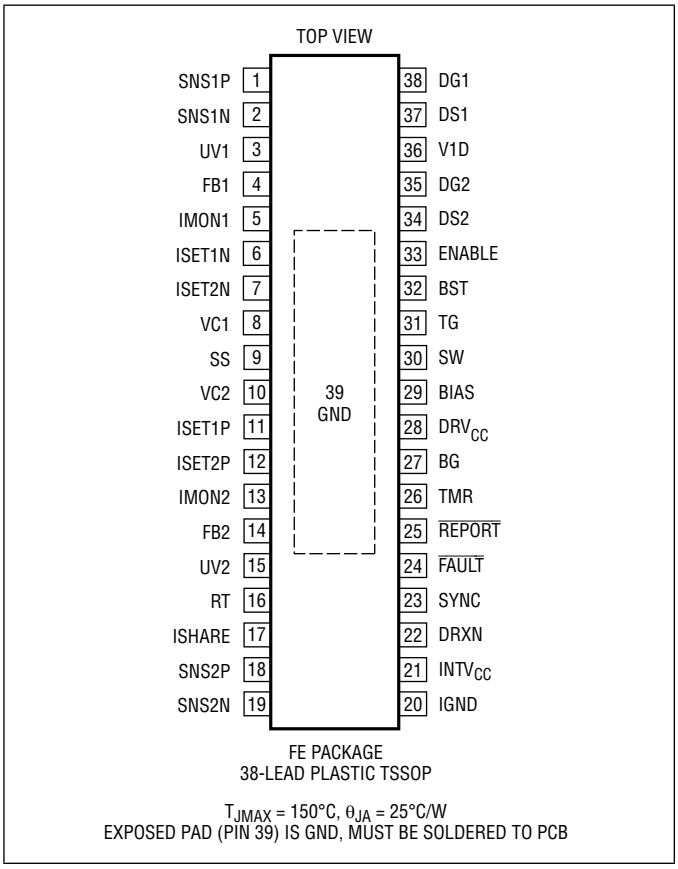
TABLE OF CONTENTS

ABSOLUTE MAXIMUM RATINGS

(Note 1)

DS1, DS2 ..... –60V to 100V
DG1 (Note 2) ..... DS1 –0.3V to DS1 + 15V
DG2 (Note 3) ..... DS2 –0.3V to DS2 + 15V
ENABLE, V1D, BIAS 100V
SNS1P, SNS2P, SNS1N, SNS2N 100V
SNS1P – SNS1N, SNS2P – SNS2N ..... ±0.3V
SW (Note 4) ..... –5V to 100V
DRV_{CC} (Note 5), BST – SW 15V
TG, BG ..... (Note 6)
$INTV_{CC}$ (Note 7) 4V
ISET1P, ISET1N, ISHARE ..... $INTV_{CC}$
ISET2P, ISET2N ..... $INTV_{CC}$
VC1, VC2, RT, SS, IMON1, IMON2 ..... $INTV_{CC}$
FB1, UV1, FB2, UV2 ..... 5.5V
DRXN, SYNC, IGND, $\overline{FAULT}$, $\overline{REPORT}$ 5.5V
Operating Junction Temperature Range
LT8228E, I (Notes 8, 9) ..... –40°C to 125°C
LT8228H J (Notes 8, 9) ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 175°C

PIN CONFIGURATION



FE PACKAGE
38-LEAD PLASTIC TSSOP

T_{JMAX} = 150°C, θ_{JA} = 25°C/W
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8228EFE#PBF	LT8228EFE#TRPBF	LT8228FE	38-Lead Plastic TSSOP	–40°C to 125°C
LT8228IFE#PBF	LT8228IFE#TRPBF	LT8228FE	38-Lead Plastic TSSOP	–40°C to 125°C
LT8228HFE#PBF	LT8228HFE#TRPBF	LT8228FE	38-Lead Plastic TSSOP	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. DS1 = V1D = 48V, DS2 = BIAS = 14V, R_{IN1} = 1k, R_{IN2} = 1k, and ISHARE = $INTV_{CC}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_1	Buck Mode Input Voltage		●	6		100	V
V_2	Boost Mode Input Voltage		●	6		100	V
V_{BIAS}	BIAS Operating Voltage Range		●	8		100	V
I_{QV1}	DS1 Quiescent Current (Shutdown) DS1 Quiescent Current (Not Switching)	ENABLE = 0V ENABLE = 2V, V_{UV1} = V_{UV2} = 0V	●		10 200	45 350	µA µA
I_{QV2}	DS2 Quiescent Current (Shutdown) DS2 Quiescent Current (Not Switching)	ENABLE = 0V ENABLE = 2V, V_{UV1} = V_{UV2} = 0V	●		10 10	40 20	µA µA
I_{QBIAS}	BIAS Quiescent Current (Shutdown) BIAS Quiescent Current (Not Switching)	ENABLE = 0V ENABLE = 2V, V_{UV1} = V_{UV2} = 0V	●		4 3.7	10 5	µA mA
I_{SS}	Soft-Start Current (Note 10)	SS = 0V	●	9.5	10	10.5	µA
Threshold Voltages							
EN_{THRESH}	ENABLE Threshold (Falling) ENABLE Hysteresis		●	1.16	1.20 100	1.24	V mV
UV_{V1}	UV1 Voltage Threshold (Falling) UV1 Hysteresis		●	1.18	1.20 100	1.22	V mV
UV_{V2}	UV2 Voltage Threshold (Falling) UV2 Hysteresis		●	1.18	1.20 100	1.22	V mV
OV_{V1}	FB1 Over Voltage Threshold (Rising) FB1 Over Voltage Hysteresis		●	1.28	1.30 100	1.32	V mV
OV_{V2}	FB2 Over Voltage Threshold (Rising) FB2 Over Voltage Hysteresis		●	1.28	1.30 100	1.32	V mV
DRXN	DRXN Logic Threshold (Rising) DRXN Logic Threshold (Falling)		● ●	1.05 0.75	1.10 0.80	1.15 0.85	V V
SYNC	SYNC Logic Threshold (Rising) SYNC Logic Threshold (Falling)		● ●	 0.65	0.95 0.80	1.10	V V
$I_{SHARETHRESH}$	ISHARE Disable Threshold (Rising) ISHARE Disable Hysteresis		●	2.45	2.49 0.40	2.53	V V
V_{CC} Regulator							
V_{DRVCC}	DRV_{CC} Regulation Voltage	12V < V_{BIAS} < 100V	●	9.7	10	10.5	V
ΔV_{DRVCC}	DRV_{CC} Load Regulation	I_{DRVCC} = 0mA to 100mA			1.0	2.5	%
$I_{DRVCCMAX}$	DRV_{CC} Current Limit (Note 10)	V_{BIAS} = 14V, V_{DRVCC} = 8V	●	100	160		mA
DRV_{CCUV}	DRV_{CC} Undervoltage Threshold (Falling) DRV_{CC} Undervoltage Hysteresis		●	6.1	6.35 300	6.6	V mV
DRV_{CCOV}	DRV_{CC} Overvoltage Threshold (Rising) DRV_{CC} Overvoltage Hysteresis		●	14.6	15.1 1.0	15.6	V V
$V_{BIAS} - V_{DRVCC}$	DRV_{CC} Dropout Voltage	V_{BIAS} = 10V, I_{DRVCC} = 100mA	●		1.0	3.5	V
V_{INTVCC}	$INTV_{CC}$ Regulation Voltage		●	3.8	4.0	4.3	V
$INTV_{CCUV}$	$INTV_{CC}$ Undervoltage Threshold (Falling) $INTV_{CC}$ Undervoltage Hysteresis		●	3.45	3.6 0.2	3.75	V V
$INTV_{CCOV}$	$INTV_{CC}$ Overvoltage Threshold (Rising) $INTV_{CC}$ Overvoltage Hysteresis		●	4.50	4.7 0.5	4.85	V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. DS1 = V1D = 48V, DS2 = BIAS = 14V, R_{IN1} = 1k, R_{IN2} = 1k, and ISHARE = $INTV_{CC}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Protection MOSFET at V_1 Terminal Controller							
ΔV_{DG1}	DG1 Gate Drive (DG1 – DS1)	 V_{DS1} = 6V, V_{DS2} = 0V, BIAS = 8V V_{DS1} = 0V, V_{DS2} = 0V, BIAS = 8V	● ● ●	8.0 8.0 8.0	10	12.5	V V V
I_{DG1UP}	DG1 Pull-Up Current (Note 10)	V_{DG1} = V_{DS1} = 48V, V_{DG2} = V_{DS2} =14V	●	7	10	13	µA
$I_{DG1DOWN}$	DG1 Pull-Down Current (Note 10)	V_{DG1} – V_{DS1} = 5V	●	–110	–80	–60	mA
$V_{1NEGATIVE}$	Negative DS1 Voltage Threshold for DG1 Off	V_{DG1} = 0V, I_{DG1} = –1mA	●	–2.2	–1.7		V
$I_{REVERSEV1}$	DS1 Reverse Leakage Current	V_{DS1} = –55V				0.6	mA
$V_{SET1NMAX}$	ISET1N Boost Output Inrush limit in Boost Mode (Note 11)	V_{DS1} = 8V, V_{DG1} – V_{DS1} = 2.5V, I_{DG1} = 0, DRXN = 0V, SS > 1.5V (Boost)	●	1.35	1.40	1.45	V
$V_{SNS1P,1N(RCUR)}$	Buck Mode Reverse Current Threshold for DG1 Off ($V_{SNS1P,SNSN1N}$)	V_{DS2} = 14V, DRXN = 2V (Buck)	●	–5.0	–3.0	–1.0	mV
V_{DG1UV}	DG1 Undervoltage Threshold (Falling) DG1 Undervoltage Hysteresis		●	3.8	4.5 0.5	5.0	V V
Protection MOSFET at V_2 Terminal Controller							
ΔV_{DG2}	DG2 Gate Drive (DG2 – DS2)	 V_{DS1} = 0V, V_{DS2} = 6V, BIAS = 8V V_{DS1} = 0V, V_{DS2} = 0V, BIAS = 8V	● ● ●	8.0 8.0 8.0	10	12.5	V V V
I_{DG2UP}	DG2 Pull-Up Current (Note 10)	V_{DG1} = V_{DS1} = 48V, V_{DG2} = V_{DS2} = 14V	●	7	10	13	µA
$I_{DG2DOWN}$	DG2 Pull-Down Current (Note 10)	V_{DG2} – V_{DS2} = 5V	●	–110	–80	–60	mA
$V_{2NEGATIVE}$	Negative DS2 Voltage Threshold for DG2 Off	V_{DG2} = 0V, I_{DG2} = –1mA	●	–2.2	–1.7		V
$I_{REVERSEV2}$	DS2 Reverse Leakage Current	V_{DS2} = –55V				0.6	mA
V_{DG2UV}	DG2 Undervoltage Threshold (Falling) DG2 Undervoltage Hysteresis		●	3.8	4.4 0.5	5.0	V V
Current Sense Amplifiers (Note 12)							
I_{B1}	SNS1P, SNS1N Bias Current	2.5V < V_{CM1} < 100V V_{CM1} = 0V	● ●	–105 35	–90 50	–70 70	µA µA
I_{ISET1P}	ISET1P Output Current 2.5V < V_{CM1} < 100V	V_{RSNS1} = 1mV V_{RSNS1} = 25mV V_{RSNS1} = 50mV V_{RSNS1} = 80mV	● ● ● ●	0.0 24.0 48.5 78.0	1.0 25.0 50.0 80.0	2.2 26.0 51.5 82.0	µA µA µA µA
I_{ISET1N}	ISET1N Output Current 2.5V < V_{CM1} < 100V	V_{RSNS1} = –1mV V_{RSNS1} = –25mV V_{RSNS1} = –50mV V_{RSNS1} = –80mV	● ● ● ●	0.0 24.0 48.5 78.0	1.0 25.0 50.0 80.0	2.2 26.0 51.5 82.0	µA µA µA µA
I_{IMON1}	IMON1 Output Current 2.5V < V_{CM1} < 100V	V_{RSNS1} = –80mV V_{RSNS1} = –50mV V_{RSNS1} = –25mV V_{RSNS1} = –1mV V_{RSNS1} = 1mV V_{RSNS1} = 25mV V_{RSNS1} = 50mV V_{RSNS1} = 80mV	● ● ● ● ● ● ● ●	78.0 48.5 24.0 0.0 0.0 24.0 48.5 78.0	80 50.0 25.0 1.0 1.0 25.0 50.0 80.0	82.0 51.5 26.0 2.2 2.2 26.0 51.5 82.0	µA µA µA µA µA µA µA µA
I_{ISET1P}, I_{ISET1N}, I_{IMON1}	Output Current, V_{CM1} < 2.5V	$\lvert V_{RSNS1}\rvert$ = 1mV $\lvert V_{RSNS1}\rvert$ = 25mV $\lvert V_{RSNS1}\rvert$ = 50mV $\lvert V_{RSNS1}\rvert$ = 80mV	● ● ● ●	0.0 22.5 47.5 76.0	1.0 25.0 50.0 80.0	3.0 27.5 52.5 84.0	µA µA µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. DS1 = V1D = 48V, DS2 = BIAS = 14V, R_{IN1} = 1k, R_{IN2} = 1k, and ISHARE = $INTV_{CC}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{B2}	SNS2P, SNS2N Bias Current	2.5V < V_{CM2} < 100V	●	–105	–90	–70	µA
		V_{CM2} = 0V	●	35	50	70	µA
I_{ISET2P}	ISET2P Output Current 2.5V < V_{CM2} < 100V	V_{RSNS2} = 1mV	●	0.0	1.0	2.2	µA
		V_{RSNS2} = 25mV	●	24.0	25.0	26.0	µA
		V_{RSNS2} = 50mV	●	48.5	50.0	51.5	µA
		V_{RSNS2} = 80mV	●	78.0	80.0	82.0	µA
I_{ISET2N}	ISET2N Output Current 2.5V < V_{CM2} < 100V	V_{RSNS2} = –1mV	●	0.0	1.0	2.2	µA
		V_{RSNS2} = –25mV	●	24.0	25.0	26.0	µA
		V_{RSNS2} = –50mV	●	48.5	50.0	51.5	µA
		V_{RSNS2} = –80mV	●	78.0	80.0	82.0	µA
I_{IMON2}	IMON2 Output Current 2.5V < V_{CM2} < 100V	V_{RSNS2} = –80mV	●	78.0	80.0	82.0	µA
		V_{RSNS2} = –50mV	●	48.5	50.0	51.5	µA
		V_{RSNS2} = –25mV	●	24.0	25.0	26.0	µA
		V_{RSNS2} = –1mV	●	0.0	1.0	2.2	µA
		V_{RSNS2} = 1mV	●	0.0	1.0	2.2	µA
		V_{RSNS2} = 25mV	●	24.0	25.0	26.0	µA
		V_{RSNS2} = 50mV	●	48.5	50.0	51.5	µA
		V_{RSNS2} = 80mV	●	78.0	80.0	82.0	µA
I_{ISET2P}, I_{ISET2N}, I_{IMON2},	Output Current, V_{CM1} < 2.5V	$\lvert V_{RSNS1}\rvert$ = 1mV	●	0.0	1.0	3.0	µA
		$\lvert V_{RSNS1}\rvert$ = 25mV	●	22.5	25.0	27.5	µA
		$\lvert V_{RSNS1}\rvert$ = 50mV	●	47.5	50.0	52.5	µA
		$\lvert V_{RSNS1}\rvert$ = 80mV	●	76.0	80.0	84.0	µA
I_{ISHARE}	ISHARE Output Current, ISHARE = 0V DRXN = 0V (Boost Mode), 2.5V < V_{CM1} < 100V	V_{RSNS1} = –1mV	●	0.0	1.0	2.2	µA
		V_{RSNS1} = –25mV	●	24.0	25.0	26.0	µA
		V_{RSNS1} = –50mV	●	48.5	50.0	51.0	µA
		V_{RSNS1} = –80mV	●	78.0	80.0	82.0	µA
	ISHARE Output Current, ISHARE = 0V DRXN = 2V (Buck Mode), 2.5V < V_{CM1} < 100V	V_{RSNS2} = 1mV	●	0.0	1.0	2.2	µA
		V_{RSNS2} = 25mV	●	24.0	25.0	26.0	µA
		V_{RSNS2} = 50mV	●	48.5	50.0	51.0	µA
		V_{RSNS2} = 80mV	●	78.0	80.0	82.0	µA
	ISHARE Output Current, ISHARE = 0V DRXN = 0V (Boost Mode), V_{CM1} < 2.5V	V_{RSNS1} = –1mV	●	0.0	1.0	3.0	µA
		V_{RSNS1} = –25mV	●	22.5	25.0	27.5	µA
		V_{RSNS1} = –50mV	●	47.5	50.0	52.5	µA
		V_{RSNS1} = –80mV	●	76.0	80.0	84.0	µA
	ISHARE Output Current, ISHARE = 0V DRXN = 2V (Buck Mode), V_{CM2} < 2.5V	V_{RSNS2} = 1mV	●	0.0	1.0	3.0	µA
		V_{RSNS2} = 25mV	●	22.5	25.0	27.5	µA
		V_{RSNS2} = 50mV	●	47.5	50.0	52.5	µA
		V_{RSNS2} = 80mV	●	76.0	80.0	84.0	µA
Buck Voltage and Current Regulation							
V_{FB2}	FB2 Regulation Voltage (Note 13)		●	1.198	1.210	1.222	V
I_{FB2}	FB2 Pin Bias Current		●		10	50	nA
g_{mFB1}	V_2 Error Amplifier Transconductance				0.8		ms
V_{ISET1P}	ISET1P Regulation Voltage (Note 14)		●	1.198	1.210	1.222	V
$g_{mISET1P}$	ISET1P Error Amplifier Transconductance				0.8		ms
V_{ISET2P}	ISET2P Regulation Voltage (Note 14)		●	1.198	1.210	1.222	V
$g_{mISET2P}$	ISET2P Error Amplifier Transconductance				0.8		ms
R_{VC2}	VC2 Output Impedance				1000		kΩ
ΔI_{ISET1P}	Buck Mode Input Current (ISET1P) Regulation Error (Note 15)	R_{SNS1} = 5Ω, R_{SET1P} = 24.3k, V_{CM1} = 48V, DRXN = 2V (Buck Mode)	●		0	±2.5	%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. DS1 = V1D = 48V, DS2 = BIAS = 14V, R_{IN1} = 1k, R_{IN2} = 1k, and ISHARE = $INTV_{CC}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ΔI_{SET2P}	Buck Mode Output Current (ISET2P) Regulation Error (Note 15)	R_{SNS2} = 5Ω, R_{SET2P} = 24.3k, V_{CM2} = 14V, DRXN = 2V (Buck Mode)	●		0	±2.5	%
$\Delta I_{SHAREBUCK}$	Buck Mode Output Current Sharing Error (Note 16)	R_{SNS2} = 5Ω, R_{SET2P} = 24.3K, V_{CM2} = 14V, DRXN = 2V (Buck Mode), I_{SHARE} = 0.605V	●		0	±4	%
Boost Voltage and Current Regulation							
V_{FB1}	FB1 Regulation Voltage (Note 13)		●	1.198	1.210	1.222	V
I_{FB1}	FB1 Pin Bias Current		●		10	50	nA
g_{mFB1}	V1 Error Amplifier Transconductance				0.8		ms
V_{ISET1N}	ISET1N Regulation Voltage (Note 14)		●	1.198	1.210	1.222	V
$g_{mISET1N}$	ISET1N Error Amplifier Transconductance				0.8		ms
V_{ISET2N}	ISET2N Regulation Voltage (Note 14)		●	1.198	1.210	1.222	V
$g_{mISET2N}$	ISET2N Error Amplifier Transconductance				0.8		ms
R_{VC1}	VC1 Output Impedance				1000		kΩ
ΔI_{SET1N}	Boost Mode Output Current (ISET1N) Regulation Error (Note 15)	R_{SNS1} = 5Ω, R_{SET1N} = 24.3k, V_{CM1} = 48V, DRXN = 2V (Buck Mode)	●		0	±2.5	%
ΔI_{SET2N}	Boost Mode Input Current (ISET2N) Regulation Error (Note 15)	R_{SNS2} = 5Ω, R_{SET2N} = 24.3k, V_{CM2} = 14V, DRXN = 2V (Buck Mode)	●		0	±2.5	%
$\Delta I_{SHAREBOOST}$	Boost Mode Output Current Sharing Error (Note 16)	R_{SNS1} = 5Ω, R_{SET1N} = 24.3k, V_{CM1} = 14V, DRXN = 2V (Buck Mode), IS_{HARE} = 0.605V	●		0	±4	%
Switching MOSFET Driver							
RTG	Pull-Up On-Resistance Pull-Down On-Resistance				2.5 1.0		Ω Ω
RBG	Pull-Up On-Resistance Pull-Down On-Resistance				2.5 1.0		Ω Ω
t_{RTG}	TG Rise Time	C_{LOAD} = 6800pF (10% to 90%)			50		ns
t_{FTG}	TG Fall Time	C_{LOAD} = 6800pF (10% to 90%)			20		ns
t_{RBG}	BG Rise Time	C_{LOAD} = 6800pF (10% to 90%)			50		ns
t_{FBG}	BG Fall Time	C_{LOAD} = 6800pF (10% to 90%)			20		ns
t_{DTGBG}	TG Off to BG On Delay	C_{LOAD} = 6800pF Each Driver (50% to 50%)			50		ns
t_{DBGTG}	BG Off to TG On Delay	C_{LOAD} = 6800pF Each Driver (50% to 50%)			50		ns
t_{ONBUCK}	Min TG On-Time in Buck Mode	DRXN = 2V			150		ns
$t_{ONBOOST}$	Min BG On-Time in Boost Mode	DRXN = 0V			150		ns
$t_{OFFBOOST}$	Min BG Off-Time in Boost Mode	DRXN = 0V			200		ns
$t_{DTGBG,V1D\ =\ 48V}$	TG Off to BG On Delay, V_{1D} = 48V (Note 17)				60		ns
$t_{DTGBG,V1D\ =100V}$	TG Off to BG On Delay, V_{1D} = 100V (Note 17)				60		ns
PLL and Oscillator							
f_{PROG}	Programmable Frequency	R_{RT} = 124k R_{RT} = 100k R_{RT} = 14k	● ● ●	75 95 540	80 100 600	85 105 660	kHz kHz kHz
f_{SYNC}	Synchronizable Frequency		●	82		700	kHz
$f_{SPSC,MAX}$	Spread Spectrum Maximum Frequency	R_{RT} = 100k, f_{PROG} = 100kHz	●		130	145	kHz
$f_{SPSC,MIN}$	Spread Spectrum Maximum Frequency	R_{RT} = 100k, f_{PROG} = 100kHz	●	65	80		kHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. DS1 = V1D = 48V, DS2 = BIAS = 14V, R_{IN1} = 1k, R_{IN2} = 1k, and ISHARE = $INTV_{CC}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logic							
$V_{\overline{FAULT}}$	$\overline{FAULT}$ Low Voltage	$I_{\overline{FAULT}}$ = 2mA (Fault Condition)	●		0.2	0.35	V
$I_{LKG\overline{FAULT}}$	$\overline{FAULT}$ Pin Leakage Current		●			1	µA
$V_{\overline{REPORT}}$	$\overline{REPORT}$ Low Voltage	$I_{\overline{REPORT}}$ = 2mA	●		0.2	0.35	V
$I_{LKG\overline{REPORT}}$	$\overline{REPORT}$ Pin Leakage Current		●			1	µA
$I_{PULLDRXN}$	DRXN Pin Pull-Down Current (Boost Mode)	UV1 = 0V	●		100	120	µA
$I_{LKGDRXN}$	DRXN Pin Leakage Current (Buck Mode)		●			1	µA
R_{IGND}	IGND Pin Resistance to GND (Sharing Enabled)		●		120	200	Ω

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for an extended period may affect device reliability and lifetime.

Note 2: An internal clamp limits the DG1 pin to a minimum of 10V above DS1. Driving this pin to voltages beyond this clamp may damage the device.

Note 3: An internal clamp limits the DG2 pin to a minimum of 10V above DS2. Driving this pin to voltages beyond this clamp may damage the device.

Note 4: Negative voltages on the SW pin are limited in an application by the body diodes of the external NMOS device M3, or parallel Schottky diodes when present. The SW pin is tolerant to these negative voltages in excess of one diode drop below ground down to –5V, guaranteed by design.

Note 5: No external loading is allowed on this pin other than for charging the boost capacitor, C_{BST}.

Note 6: Do not apply a voltage or current sources to these pins. They must be connected to capacitive loads only, otherwise permanent damage may occur.

Note 7: $INTV_{CC}$ cannot be externally driven. No external loading is allowed on this pin other than connecting to the ISHARE pin and the pull-up resistor for DRXN whose value should not be less than 50k.

Note 8: The LT8228 is tested and specified under pulse load conditions such that $T_J \cong T_A$. The LT8228E is 100% production tested at T_A = 25°C and performance is guaranteed from 0°C to 125°C. Performance at –40°C to 125°C is assured by design, characterization and correlation with statistical process controls. The LT8228I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT8228H is guaranteed over the full –40°C to 150°C operating junction temperature range.

Note 9: The LT8228 includes over-temperature protection that is intended to protect the device during overload conditions. When the junction temperature exceeds 150°C, overtemperature protection is activated. Continuous operation above the specified maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 10: Current convention. Positive current is defined as current flowing out of the pin.

Note 11: There is a direct conduction path from V_2 to V_{1D} through V_2 protection MOSFET M4 and the body diode of TG MOSFET M2. In Boost mode, this specification limits the current into V_1 from V1D through DG1.

Note 12: I_{B1} is defined as the average of the input bias current to the SNS1P and SNS1N pins. Likewise, I_{B2} is defined as the average of the input bias current to the SNS2P and SNS2N pins. The LT8228 is tested and specified for these conditions with the voltages at the SNS1P, SNS1N, SNS2P and SNS2N pins applied through 1k input gain resistors. V_{RSNS1} represents the voltage between the input gain resistors for the SNS1P and SNS1N pins. Likewise, V_{RSNS2} represents the voltage between the input gain resistors for the SNS2P and SNS2N pins. V_{CM1} and V_{CM2} are the common mode voltages at the input gain resistors R_{IN1} and R_{IN2}.

Note 13: The LT8228 is tested in a feedback loop that servos the output of the error amplifier, VC, to the internal reference voltage by tying the FB pin to the VC pin with all ISET pins tied to ground.

Note 14: The LT8228 is tested in a feedback loop that servos the output of the error amplifier VC to the internal reference voltage by tying the ISET pin under test to the VC pin with the FB and other ISET pins tied to ground.

Note 15: Current regulation error is the difference between the measured current through the sense resistor and the programmed current set by: (1) the sense resistor R_{SNS}, (2) the input gain resistors R_{IN} and (3) the ISET resistor R_{SET}. The LT8228 is tested in a feedback loop that regulates a current through R_{SNS} by tying the VC pin to the gate of a grounded N-channel MOSFET whose drain is connected to R_{SNS}. The error due to the SNS pin bias current across R_{SNS} is subtracted from this specification. This specification is tested with no ripple voltage on R_{SNS}.

Note 16: Current sharing error is the difference between the current through the sense resistor R_{SNS} and the average current defined by the ISHARE pin. The voltage on ISHARE represents the average ISHARE currents of multiple ideal LT8228s in parallel. The LT8228 is tested in a feedback loop that regulates a current through R_{SNS} by tying the VC pin to the gate of a grounded N-channel MOSFET whose drain is connected to R_{SNS}. The current sharing loop servos the ISET1N pin voltage in boost mode or the ISET2P pin voltage in buck mode to the ISHARE pin voltage of 600mV. The error due to the SNS pin bias current across R_{SNS} is subtracted from this specification. This specification is tested with no ripple voltage on R_{SNS}.

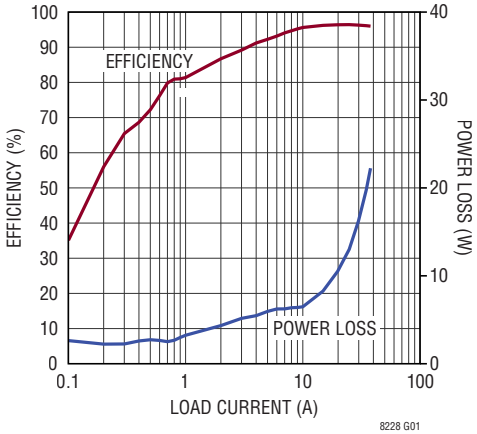
Note 17: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels. Rise and fall times are assured by design, characterization and correlation with statistical process controls.

TYPICAL PERFORMANCE CHARACTERISTICS

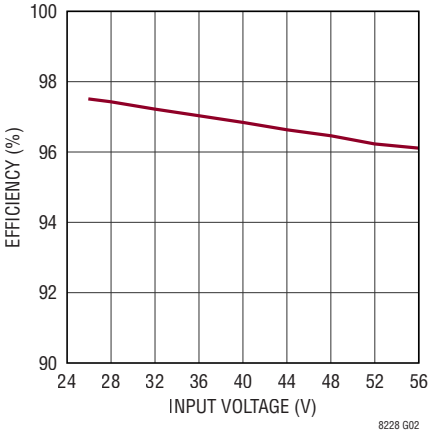
T_A = 25°C, unless otherwise noted.

BUCK EFFICIENCY AND OPERATION

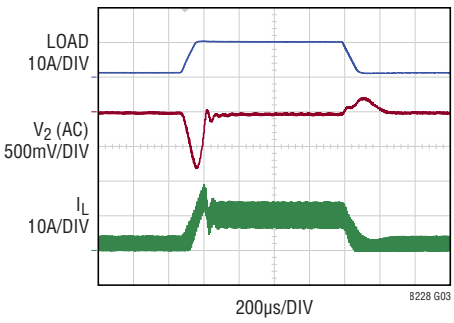
Efficiency vs V_2 Current (Buck) (V_1 = 48V, V_2 = 14V)



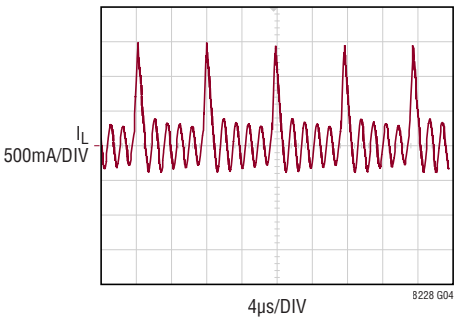
Efficiency vs V_1 (Buck) (V_2 = 14V, I_{V2} = 20A)



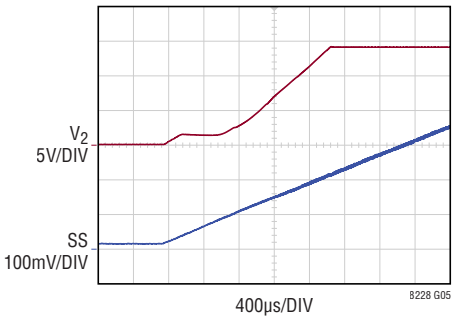
Load Step (Buck)



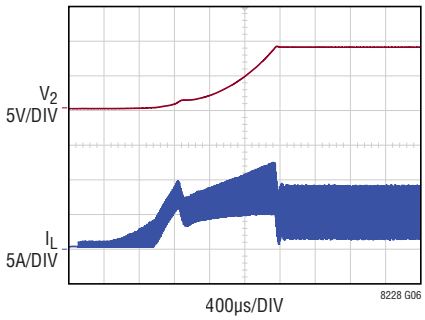
Inductor Current at Light Load (Buck)



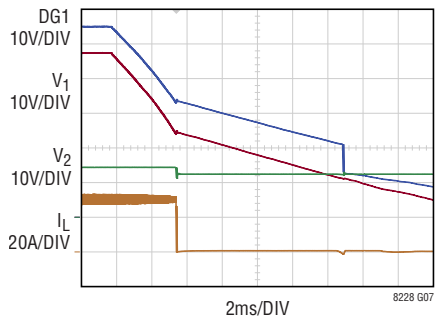
Soft Start-Up (Buck)



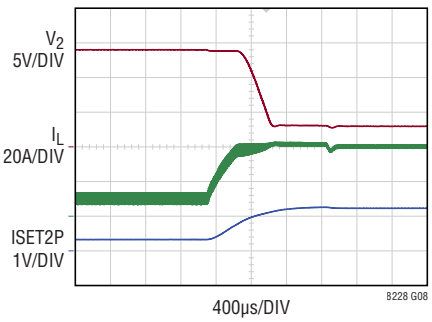
Start-Up at Prebiased Load (Buck)



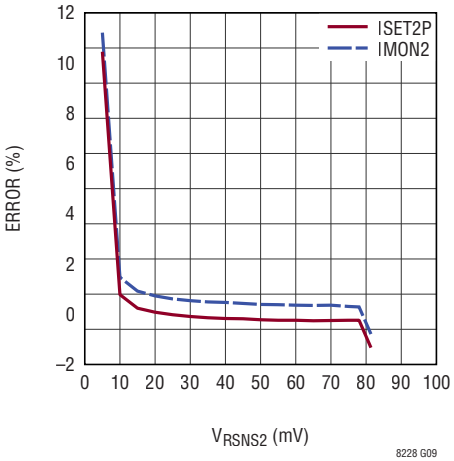
Output Higher Than Input, $V_2 > V_1$ (Reverse Current Protection, Buck)



Short-Circuit/Voltage and Current Regulation Transition (Buck)



ISET2P and IMON2 Measurement Accuracy

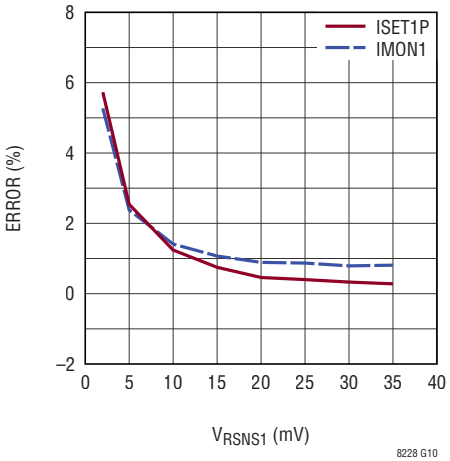


TYPICAL PERFORMANCE CHARACTERISTICS

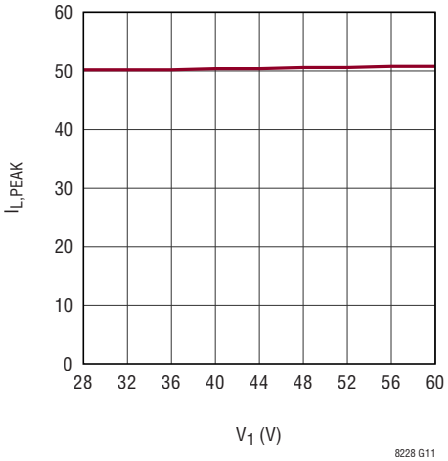
T_A = 25°C, unless otherwise noted.

BUCK EFFICIENCY AND OPERATION

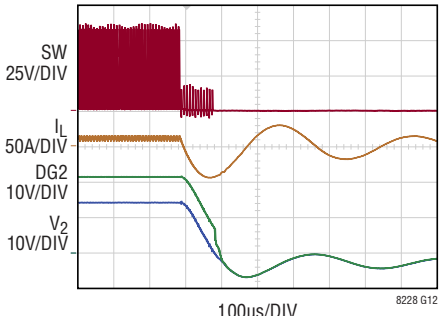
ISET1P and IMON1 Measurement Accuracy



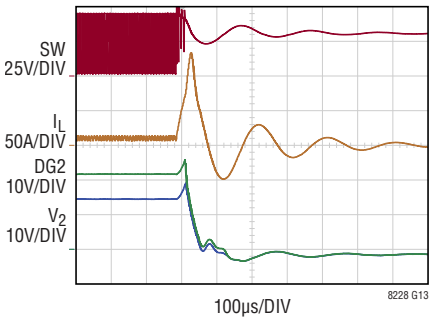
Peak Inductor Current vs V_1 (Buck)



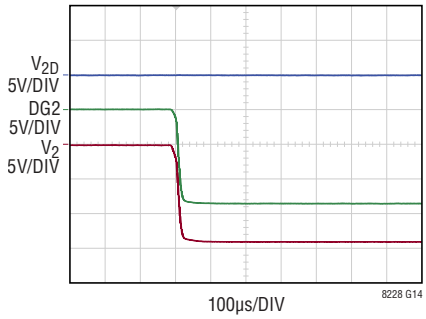
BG MOSFET Short in Regulation (Buck)



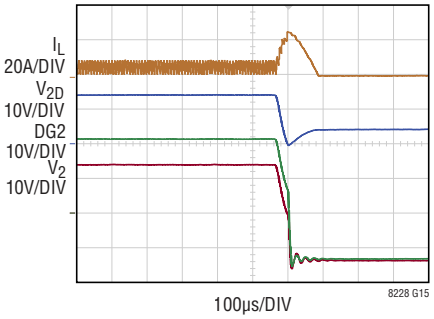
TG MOSFET Short in Regulation (Buck)



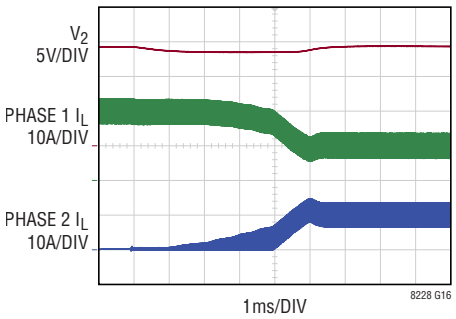
Reverse Battery Insertion at V_2 (LT8228 Disabled)



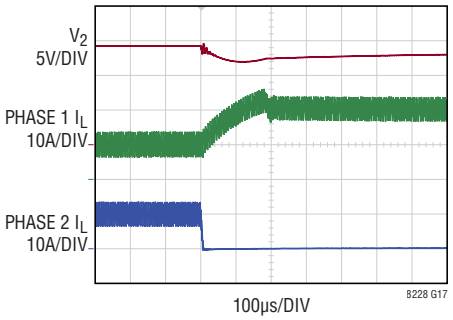
Reverse Battery Insertion at V_2 in Regulation



Multiphase Operation (Buck) Phase Turn-On



Multiphase Operation (Buck) Phase Turn-Off

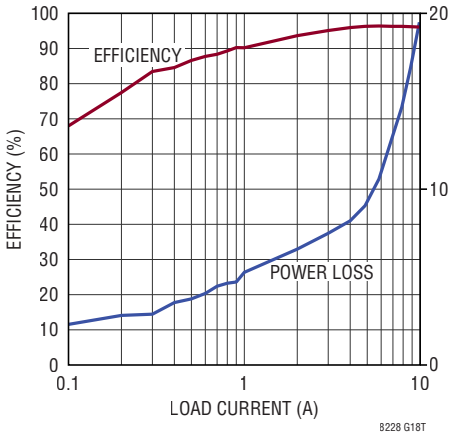


TYPICAL PERFORMANCE CHARACTERISTICS

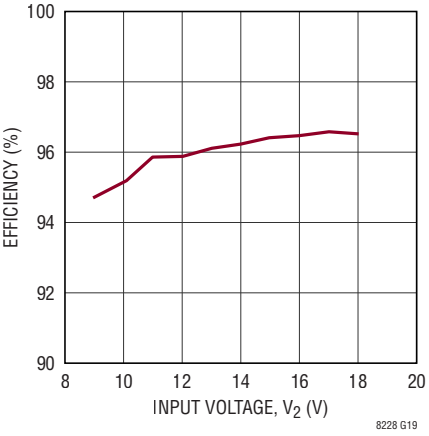
T_A = 25°C, unless otherwise noted.

BOOST EFFICIENCY AND OPERATION

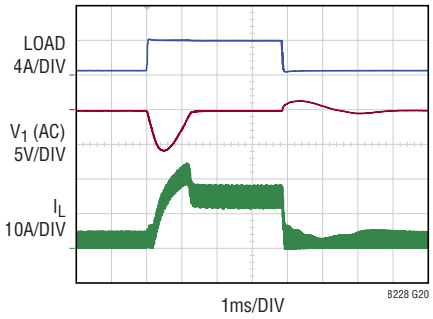
Efficiency vs V_1 Current (Boost) (V_1 = 48V, V_2 = 14V)



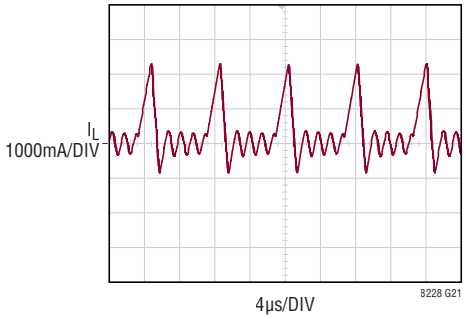
Efficiency vs V2 (Boost) (V_1 = 48V, I_{V1} = 5A)



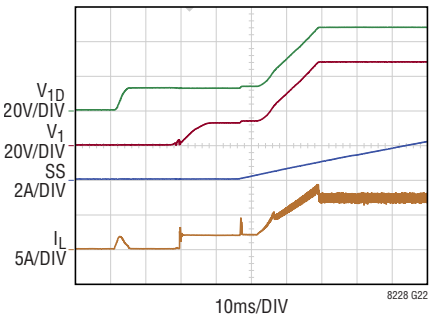
Load Step (Boost)



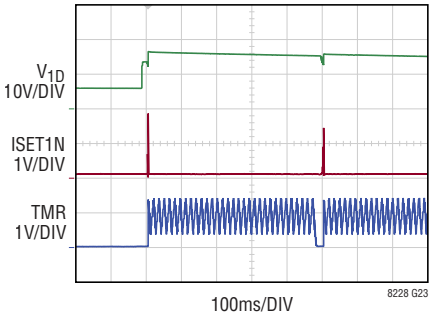
Inductor Current at Light Load (Boost)



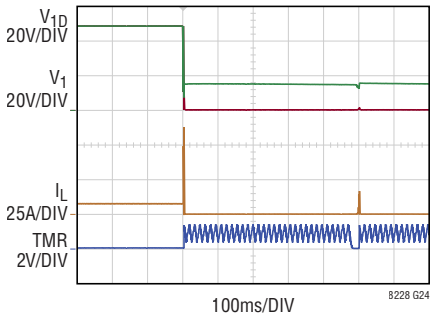
Soft Start-Up (Boost)



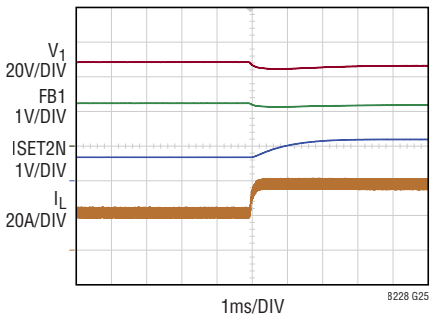
Output Short (Boost, Start-Up)



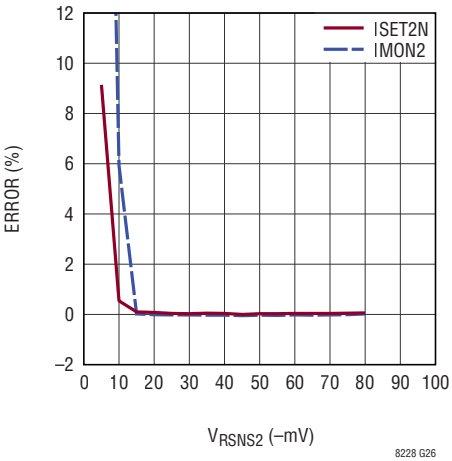
Output Short-Circuit Transient (Boost)/TMR Pin Operation



Voltage and Current Regulation Transition (Boost)



ISET2N and IMON2 Measurement Accuracy

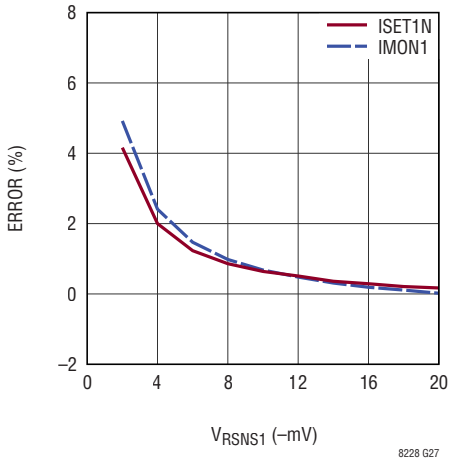


TYPICAL PERFORMANCE CHARACTERISTICS

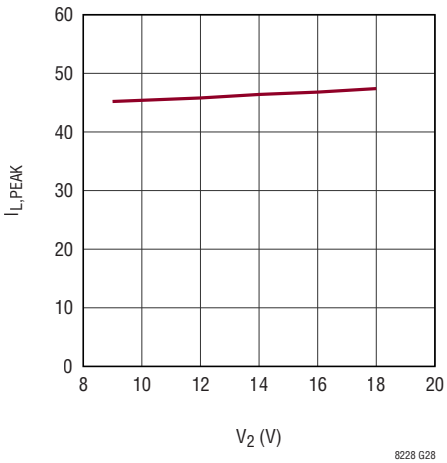
T_A = 25°C, unless otherwise noted.

BOOST EFFICIENCY AND OPERATION

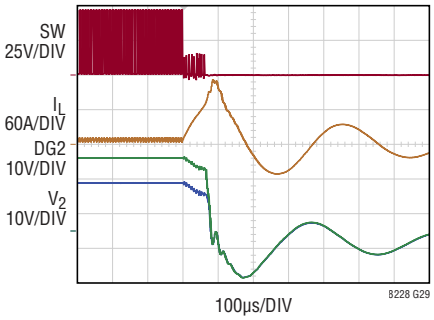
ISET1N and IMON1 Measurement Accuracy



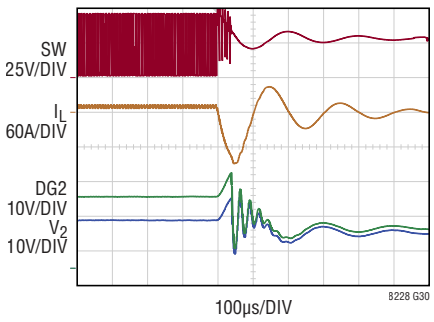
Maximum Inductor Current vs V_2 (Boost)



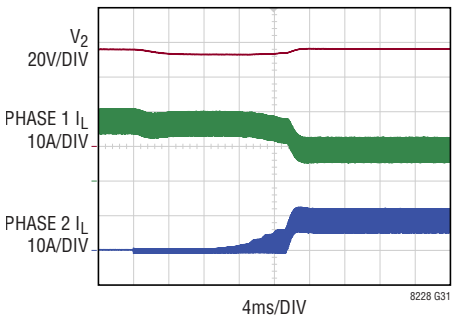
BG MOSFET Short in Regulation (Boost)



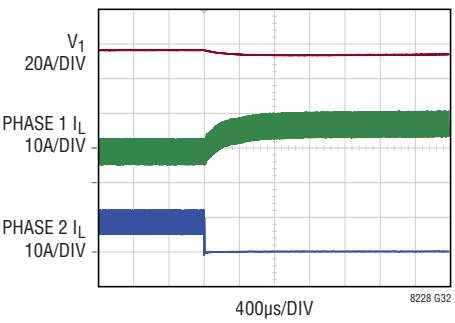
TG MOSFET Short in Regulation (Boost)



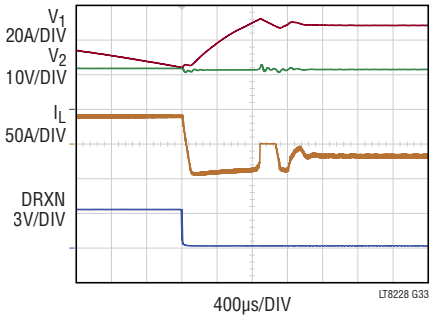
Multiphase Operation Boost Phase Turn-On



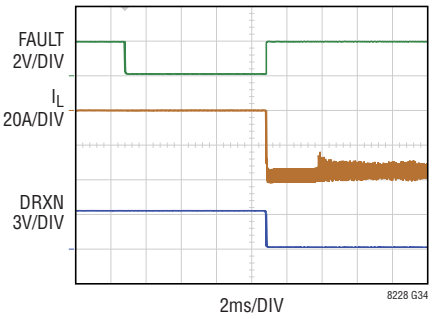
Multiphase Operation Boost Phase Turn-Off



Auto DRXN: Buck to Boost Transition (Input Undervoltage)



Auto DRXN: Buck to Boost Transition (Output Overvoltage)

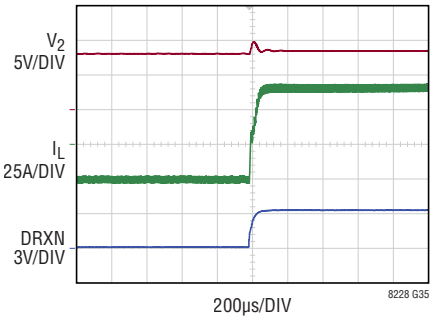


TYPICAL PERFORMANCE CHARACTERISTICS

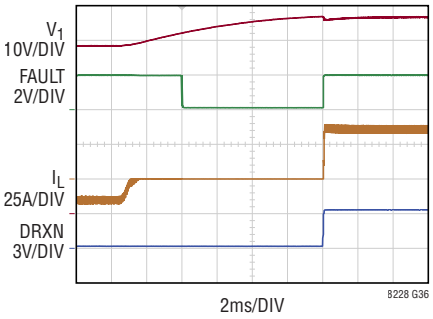
T_A = 25°C, unless otherwise noted.

BOOST EFFICIENCY AND OPERATION

Auto DRXN: Boost to Buck Transition (Input Undervoltage)

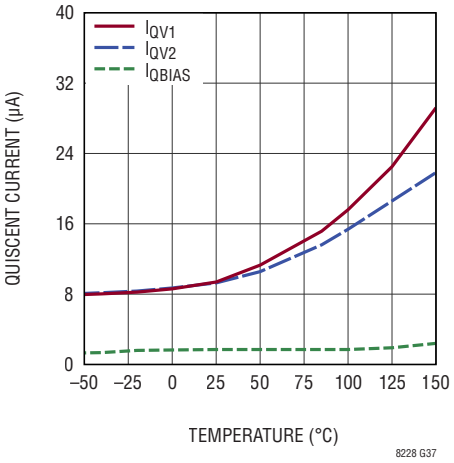


Auto DRXN: Boost to Buck Transition (Output Overvoltage)

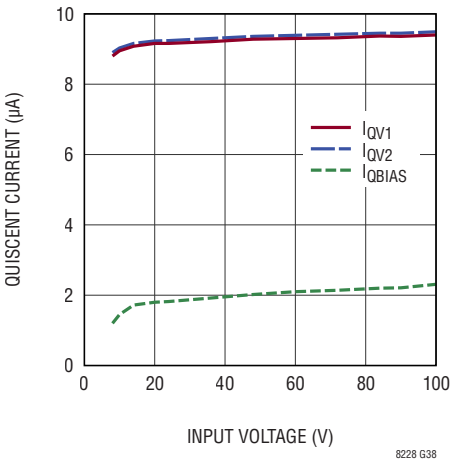


ENABLE, SUPPLY CURRENT AND V_{CC}

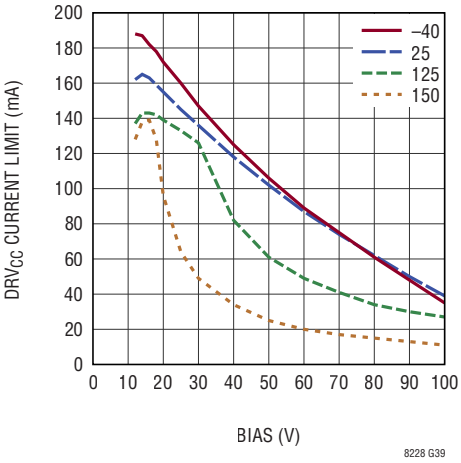
Shutdown Current vs Temperature (V_1 = 48V, V_2 = 14V, BIAS = 14V)



Shutdown Current vs Input Voltage (Input = V_1, V_2, BIAS)



DRV_{CC} Current Limit vs BIAS (Temperature = –40°C, 25°C, 150°C)

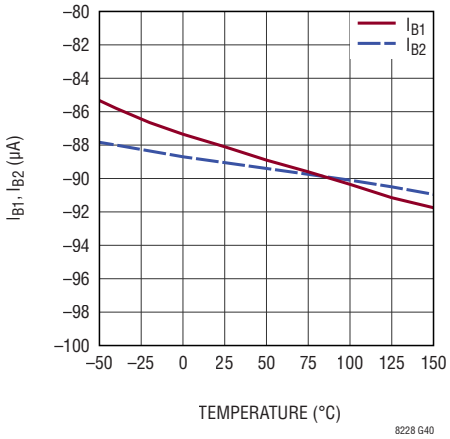


TYPICAL PERFORMANCE CHARACTERISTICS

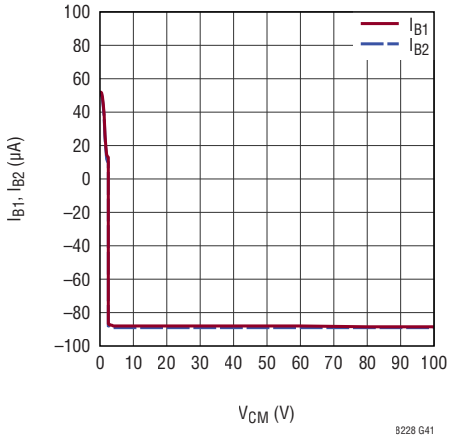
T_A = 25°C, unless otherwise noted.

REGULATION AND CURRENT SENSE

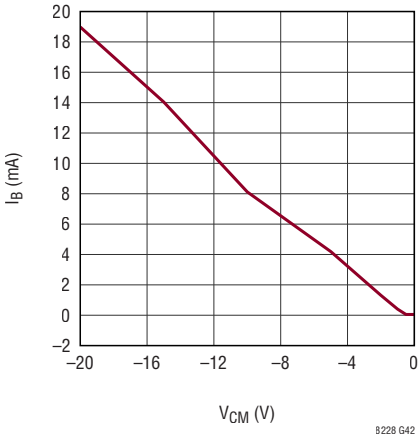
CSA1/CSA2 Input Bias Current vs Temperature



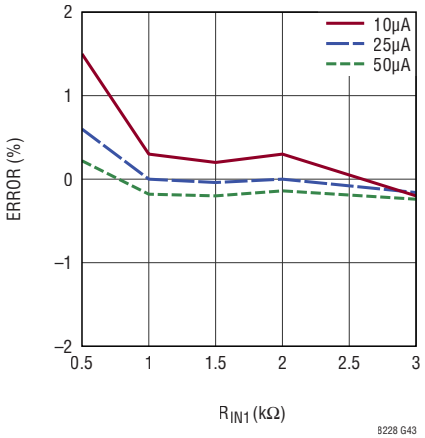
CSA1/CSA2 Input Bias Current vs V_{CM}



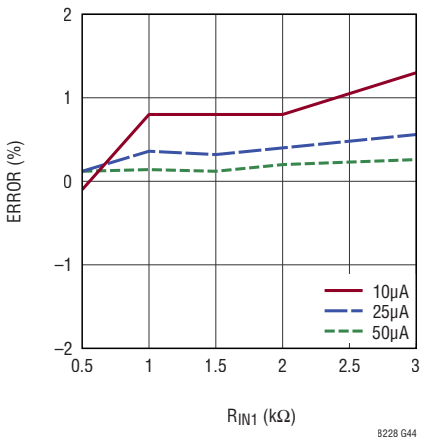
CSA1/CSA2 Input Bias Current vs V_{CM} (Reverse Battery Fault)



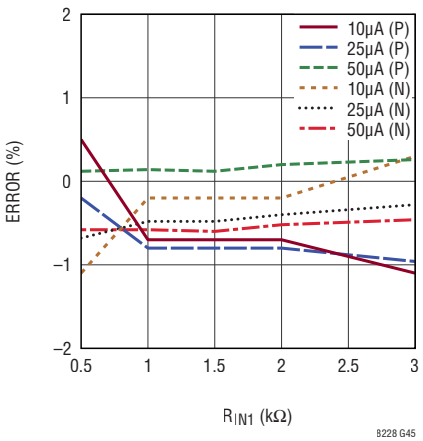
ISET1P Gain Error vs R_{IN1} (V_{CM1} > 2.5V, Output: 10µA, 25µA and 50µA)



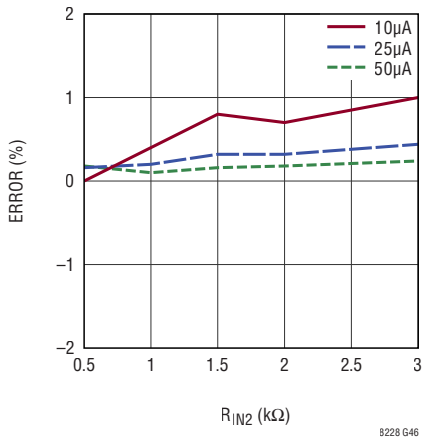
ISET1N Gain Error vs RI_{N1} (V_{CM1} > 2.5V, Output: 10µA, 25µA and 50µA)



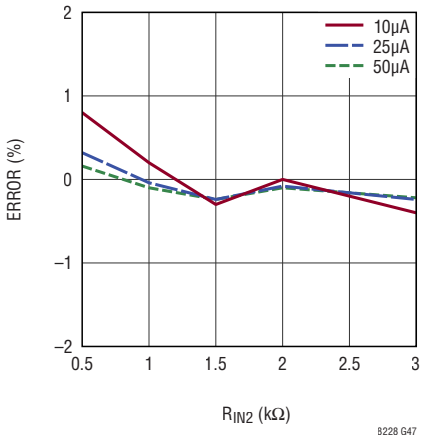
IMON1 Gain Error vs R_{IN1} (V_{CM1} > 2.5V, Output: 10µA, 25µA and 50µA)



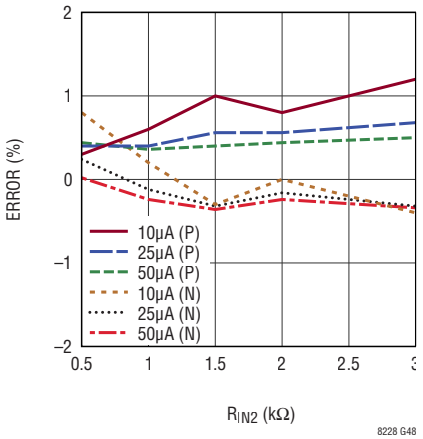
ISET2P Gain Error vs R_{IN2} (V_{CM2} > 2.5V, Output: 10µA, 25µA and 50µA)



ISET2N Gain Error vs R_{IN2} (V_{CM2} > 2.5V, Output: 10µA, 25µA and 50µA)



IMON2 Gain Error vs R_{IN2} (V_{CM2} > 2.5V, Output: 10µA, 25µA and 50µA)

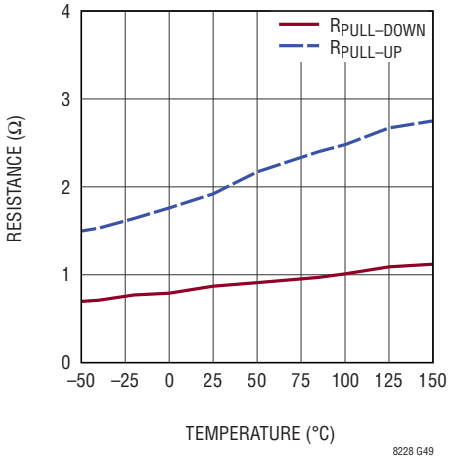


TYPICAL PERFORMANCE CHARACTERISTICS

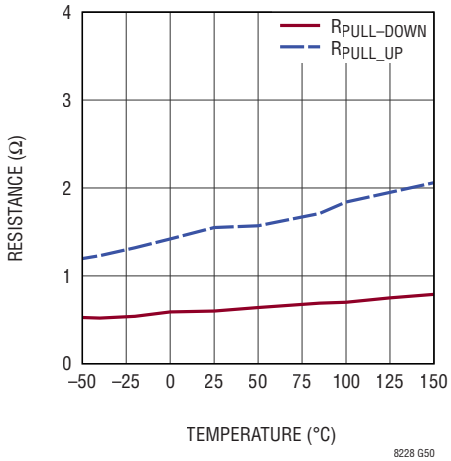
T_A = 25°C, unless otherwise noted.

SS CURRENT, FREQUENCY, THRESHOLDS AND DRIVER

TG Pull-Up/Down Resistance vs Temperature

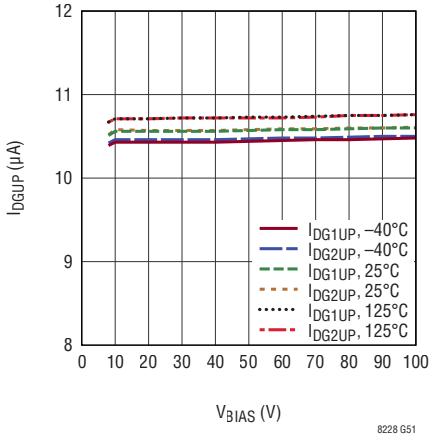


BG Pull-Up/Down Resistance vs Temperature

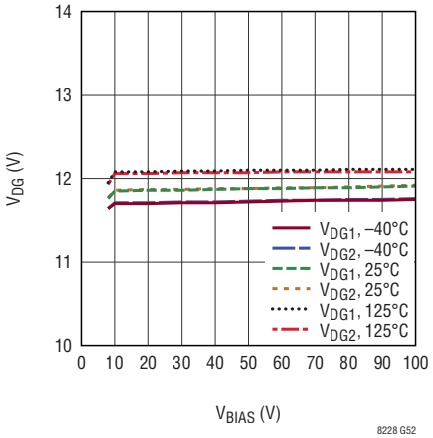


PROTECTION MOSFET CONTROLLER

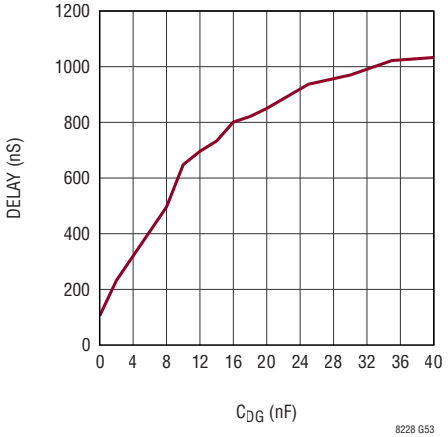
DG1/DG2 Pull-Up Current vs BIAS (DS1 = 0V, DS2 = 0V)



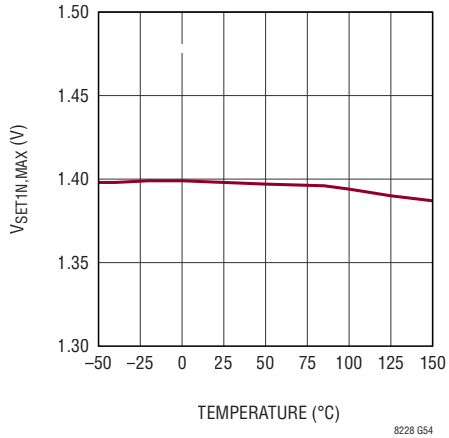
DG1/DG2 vs BIAS (DS1 = 0V, DS2 = 0V)



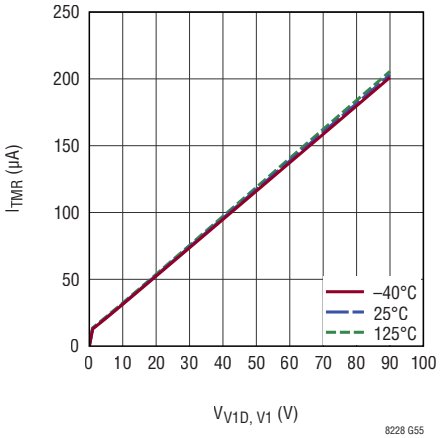
DG1/DG2 Turn-Off Delay vs Capacitance



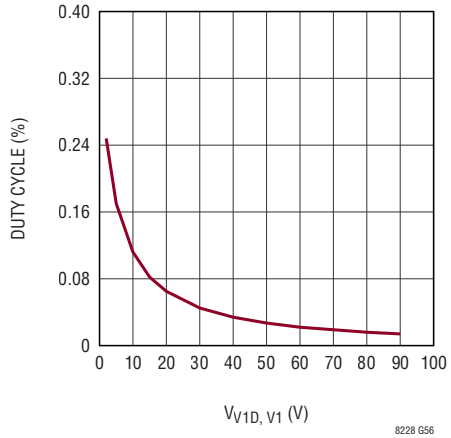
ISET1N Inrush Regulation vs Temperature



TMR Current vs V (V1D, DS1)



DG1 Retry Duty Cycle vs V (V1D, DS1)



PIN FUNCTIONS

SNS1P, SNS1N (Pins 1, 2): Positive and Negative Input Terminals of the V_1 Bidirectional Current Sense Amplifier (CSA1 in the Block Diagram section). The pins allow current monitoring and regulation of the V_1 input current in buck mode and V_1 output current in boost mode. Current sense polarity is positive for current flowing out of V_1 into V_2. Place input gain resistors R_{IN1} between the current sense resistor R_{SNS1} and these pins. Typical bias current into these pins is 90µA for common mode voltage above 2.5V. As common mode voltage decreases below 2.5V, bias current decreases and reverses direction. Refer to the curve of I_{B1} over V_{CM1} in the Typical Performance Characteristics section.

CSA1 is connected in a negative feedback loop to make SNS1N and SNS1P pin voltages equal. The voltage across the current sense resistor and the input gain resistors generates a difference in current flowing into the SNS1N and SNS1P pins, I_{SNS1N} and I_{SNS1P}. The current flowing through R_{SNS1}, I_{SNS1}, includes the V_1 current, the input bias current of CSA1's negative feedback terminal and the differential current given by Equation 1.

$$I_{SNS1N} - I_{SNS1P} = \frac{I_{SNS1} \bullet R_{SNS1}}{R_{IN1}} \quad (1)$$

In buck mode, this current difference is generated out of the ISET1P and IMON1 pins. In boost mode, it is generated out of the ISET1N, ISHARE and IMON1 pins. Limit the difference between SNS1N and SNS1P pin currents to ±100µA by choosing the values of R_{SNS1} and R_{IN1} appropriately. Refer to the R_{SNS1} and R_{IN1} Selection in Applications Information section for more details.

UV1 (Pin 3): Undervoltage Detection Input for V_1. It is a high impedance pin with the undervoltage detection threshold set at 1.2V typically. The undervoltage level is set using a resistor divider connected between V_1 node and ground. If V_1 needs reverse voltage protection, connect the resistor divider in series with a diode whose anode is connected to V_1. The status of the UV1 pin is reported at the $\overline{\text{REPORT}}$ pin in buck mode.

If the DRXN pin is externally set high for buck mode operation and the UV1 pin voltage falls below its threshold voltage, the $\overline{\text{FAULT}}$ and SS pins pull low and the LT8228 stops switching. If the DRXN pin is high but not externally controlled, and the UV1 pin voltage falls below the threshold voltage, the regulation mode changes from buck to boost and the DRXN pin is internally driven low. See the Operation section for more information. Tie the pin to $INTV_{CC}$ if not used.

FB1 (Pin 4): V_{1D} Feedback Voltage and Overvoltage Detection Input. This pin is one of the boost mode error amplifier's (EA1 in the Block Diagram section) inverting terminals. It is a high impedance pin and senses the V_{1D} voltage through an external resistor divider network. The pin is regulated to the typical internal reference voltage of 1.21V in boost mode.

V1D overvoltage detection threshold is set at 1.3V typically. The status of V_{1D} overvoltage is reported at the $\overline{\text{REPORT}}$ pin in boost mode. If the DRXN pin is externally set low for boost mode operation and the FB1 pin voltage rises above its overvoltage threshold voltage, the $\overline{\text{FAULT}}$ pin pulls low. If the DRXN pin is low but not externally controlled, and the FB1 pin voltage rises above the overvoltage threshold voltage for a duration of 1024 switching clock cycle, the regulation mode changes from boost to buck and the DRXN pin is pulled high by the external pull-up resistor. Tie the pin to ground if not used.

IMON1 (Pin 5): V_1 Current Monitor Output. The current out of this pin is equal to the absolute voltage across the current sense resistor R_{SNS1} divided by the value of the input sense resistor R_{IN1}. This current represents V_1 input current in buck mode and V_1 output current in boost mode. Connecting a resistor R_{MON1}, from IMON1 to ground generates a voltage V_{MON1} for monitoring by an external ADC. The maximum dynamic range for IMON1 is 2.5V. To set R_{MON1}, first determine the maximum monitor voltage $V_{MON1MAX}$ based on ADC input dynamic range. Next, calculate the value of R_{MON1} with Equation 2.

$$R_{MON1} = \frac{R_{IN1}}{I_{SNS1MAX} \bullet R_{SNS1}} \bullet V_{MON1MAX} \quad (2)$$

where $I_{SNS1MAX}$ is the maximum of the programmed V_1 output current limit $I_{V1N(LIM)}$ in boost mode or the programmed V_1 input current limit $I_{V1P(LIM)}$ in buck mode. A filtering capacitor can be added to read the average current at the ADC input. Refer to the R_{MON1} Selection for V_1 Current Monitoring in Applications Information section

PIN FUNCTIONS

for more detail on resistor and capacitor selection. Tie the pin to ground if not used.

ISET1N (Pin 6): Boost Mode Output Current Limit Programming. This pin sets the V_1 output current limit in boost mode by connecting a resistor R_{SET1N} from ISET1N to ground. The pin outputs a current equal to the negative voltage across the current sense resistor R_{SNS1} divided by the value of the input sense resistor R_{IN1}. The voltage at ISET1N is regulated to the lower of the SS pin voltage and the typical internal reference voltage of 1.21V. Calculate the value of R_{SET1N} with Equation 3.

$$R_{ISET1N} = \frac{R_{IN1}}{R_{SNS1} \bullet I_{V1N(LIM)}} \bullet 1.21V \quad (3)$$

where $I_{V1N(LIM)}$ is the maximum programmed V_1 output current limit in boost mode.

In boost mode, at start-up when V_1 is lower than V_2 or V_1 is shorted to GND, the output current cannot be limited by the boost regulation loop. Under such conditions, the LT8228 controls the output current by controlling M1, the V_1 protection MOSFET. The LT8228 controls DG1, the gate of M1 by regulating ISET1N to 1.4V.

Current at this pin is discontinuous during switching. Connect a filtering capacitor at this pin to regulate the average current limit. The value of the filtering capacitor affects the current regulation loop stability. Refer to the R_{SET1N} Selection for V_1 Output Current Limit (Boost Mode) in Applications Information section for resistor and capacitor selection. Tie the pin to ground if not used.

ISET2N (Pin 7): Boost Mode Input Current Limit Programming. This pin sets the V_2 input current limit in boost mode by connecting a resistor R_{SET2N} from ISET2N to ground. The pin outputs a current equal to the negative voltage across the current sense resistor R_{SNS2} divided by the value of the input sense resistor R_{IN2}. The voltage at ISET2N is regulated to the lower of the SS pin voltage and the typical internal reference voltage of 1.21V. Calculate the value of R_{SET2N} with Equation 4.

$$R_{ISET2N} = \frac{R_{IN2}}{R_{SNS2} \bullet I_{V2N(LIM)}} \bullet 1.21V \quad (4)$$

where $I_{V2N(LIM)}$ is the maximum programmed V_2 input current limit in boost mode. Connect a filtering capacitor at this pin to regulate the average current limit. The value of the filtering capacitor affects the current regulation loop stability. Refer to the R_{SET2N} Selection for V2 Input Current Limit (Boost Mode) in Applications Information section for resistor and capacitor selection. Tie the pin to ground if not used.

VC1 (Pin 8): Boost Mode Error Amplifier (EA1 in the Block Diagram section) Compensation. VC1 is the compensation pin for boost mode regulation of the V_{1D} voltage, the V_1 output current and the V_2 input current. EA1 servos the higher of the FB1, ISET1N and ISET2N pin voltages to the typical internal reference voltage of 1.21V. If the SS pin voltage is lower than the typical internal reference of 1.21V, EA1 regulates the current programming pins ISET1N and ISET2N voltages to the SS pin voltage. Leave the pin open if not used.

SS (Pin 9): Soft-Start Input. The LT8228 limits all the ISET pin voltages to the SS pin voltage when the pin voltage is lower than the typical internal reference voltage of 1.21V. Connect a soft-start capacitor C_{SS} between the SS pin and ground. When the LT8228 is disabled, or a fault is detected (refer to the Soft-Start in Applications Information section for all the fault conditions), the SS pin is actively pulled low by an internal MOSFET to reset the soft-start. Select C_{SS} for a soft-start time t_{SS} according to Equation 5.

$$C_{SS} = \frac{10\mu A}{1.21V} \bullet \frac{1}{t_{SS}} \quad (5)$$

Leave the pin open if not used.

VC2 (Pin 10): Buck Mode Error Amplifier (EA2 in the Block Diagram section) Compensation. VC2 is the compensation pin for buck mode regulation of the V_{2D} voltage, the V_2 output current and the V_1 input current. EA2 servos the higher of the FB2, ISET1P and ISET2P pin voltages to the typical internal reference voltage of 1.21V. If the SS pin voltage is lower than the typical internal reference of 1.21V, EA2 regulates the current programming pins

PIN FUNCTIONS

ISET1P and ISET2P voltages to the SS pin voltage. Leave the pin open if not used.

ISET1P (Pin 11): Buck Mode Input Current Limit Programming. This pin sets the V_1 input current limit in buck mode by connecting a resistor R_{SET1P} from ISET1P to ground. The pin outputs a current equal to the positive voltage across the current sense resistor R_{SNS1} divided by the value of the input sense resistor R_{IN1}. The voltage at ISET1P is regulated to the lower of the SS pin voltage and the typical internal reference voltage of 1.21V. Calculate the value of R_{SET1P} with Equation 6.

$$R_{ISET1P} = \frac{R_{IN1}}{R_{SNS1} \bullet I_{V1P(LIM)}} \bullet 1.21V \quad (6)$$

where $I_{V1P(LIM)}$ is the maximum programmed V_1 input current limit in buck mode. Connect a filtering capacitor at this pin to regulate the average current limit. The value of the filtering capacitor affects the current regulation loop stability. Refer to the R_{SET1P} Selection for V_1 Input Current Limit (Buck Mode) in Applications Information section for resistor and capacitor selection. Tie the pin to ground if not used.

ISET2P (Pin 12): Buck Mode Output Current Limit Programming. This pin sets the V_2 output current limit in buck mode by connecting a resistor R_{SET2P} from ISET2P to ground. The pin outputs a current equal to the positive voltage across the current sense resistor R_{SNS2} divided by the value of the input sense resistor R_{IN2}. The voltage at ISET2P is regulated to the lower of the SS pin voltage and the typical internal reference voltage of 1.21V. Calculate the value of R_{SET2P} with Equation 7.

$$R_{ISET2P} = \frac{R_{IN2}}{R_{SNS2} \bullet I_{V2P(LIM)}} \bullet 1.21V \quad (7)$$

where $I_{V2P(LIM)}$ is the maximum programmed V_2 output current limit in buck mode. Connect a filtering capacitor at this pin to regulate the average current limit. The value of the filtering capacitor affects the current regulation loop stability. Refer to the R_{SET2P} Selection for V_2 Output Current Limit (Buck Mode) in Applications Information section for resistor and capacitor selection. Tie the pin to ground if not used.

IMON2 (Pins 13): V_2 Current Monitor Output. The current out of this pin is equal to the absolute voltage across the current sense resistor R_{SNS2} divided by the value of the input sense resistor R_{IN2}. This current represents V_2 input current in boost mode and V_2 output current in buck mode. Connecting a resistor R_{MON2}, from IMON2 to ground generates a voltage V_{MON2} for monitoring by an external ADC. The maximum dynamic range for IMON2 is 2.5V. To set R_{MON2}, first determine the maximum monitor voltage $V_{MON2MAX}$ based on ADC input dynamic range. Next, calculate the value of R_{MON2} with Equation 8.

$$R_{MON2} = \frac{R_{IN2}}{I_{SNS2MAX} \bullet R_{SNS2}} \bullet V_{MON2MAX} \quad (8)$$

where $I_{SNS2MAX}$ is the maximum of the $I_{V2N(LIM)}$, programmed V_2 input current limit in boost mode or $I_{V2P(LIM)}$, the programmed V_2 output current limit in buck mode. A filtering capacitor can be added to read the average current at the ADC input. Refer to the R_{MON2} Selection for V_2 Current Monitoring in Applications Information section for more detail on resistor and capacitor selection. Tie the pin to ground if not used.

FB2 (Pin 14): V_{2D} Feedback Voltage and Overvoltage Detection Input. This pin is one of the buck mode error amplifier's (EA2 in the Block Diagram section) inverting terminals. It is a high impedance pin and senses the V_{2D} voltage through an external resistor divider network. The pin is regulated to the typical internal reference voltage of 1.21V in buck mode.

V2D overvoltage detection threshold is set at 1.3V typically. The status of V_{2D} overvoltage is reported at the $\overline{\text{REPORT}}$ pin in boost mode. If the DRXN pin is externally set high for buck mode operation and the FB2 pin voltage rises above its overvoltage threshold voltage, the $\overline{\text{FAULT}}$ pin pulls low. If the DRXN pin is high but not externally controlled, and the FB2 pin voltage rises above the overvoltage threshold voltage for a duration of 1024 switching

PIN FUNCTIONS

clock cycle, the regulation mode changes from buck to boost and the DRXN pin is actively pulled-low. Tie the pin to ground if not used.

UV2 (Pin 15): Undervoltage Detection Input for V_2 . It is a high impedance pin with the undervoltage detection threshold set at 1.2V typically. The undervoltage level is set using a resistor divider connected between V_2 node and ground. If V_2 needs reverse voltage protection, connect the resistor divider in series with a diode whose anode is connected to V_2 . The status of the UV2 pin is reported at the $\overline{\text{REPORT}}$ pin in boost mode.

If the DRXN pin is externally set low for boost mode operation and the UV2 pin voltage falls below its threshold voltage, the $\overline{\text{FAULT}}$ and SS pin pulls low and the LT8228 stops switching. If the DRXN pin is low but not externally controlled, and the UV2 pin voltage falls below the threshold voltage, the regulation mode changes from boost to buck and the DRXN pin is pulled high by the external pull-up resistor. See the Operation section for more information. Tie the pin to $INTV_{CC}$ if not used.

RT (Pin 16): Switching Frequency Set Input. Place a resistor R_{RT} from RT to ground to set the internal frequency. The range of frequency is 80kHz to 600kHz. Set the R_{RT} resistance for a fixed frequency f_{PROG} according to the R_{RT} resistance vs frequency curve in Typical Performance Characteristics section. See the Programming the Switching Frequency in Applications Information section for more details on resistor selection. Do not tie this pin to ground or leave it open.

ISHARE (Pin 17): Masterless Current Sharing Input for Paralleling. Together with the IGND pin, this pin allows equal output current sharing among multiple LT8228s in parallel, enabling higher total load current, better heat management and redundancy. Each LT8228 regulates to the average output current eliminating the need for a master controller. When paralleling, tie the ISHARE pins of all the LT8228s together. For each LT8228, connect a local resistor R_{SHARE} from the ISHARE pin to its own IGND pin.

In buck mode when DRXN is high, the ISHARE pin outputs a current equal to the current out of the ISET2P pin which represents V_2 output current. In boost mode when DRXN is low, the ISHARE pin outputs a current equal to the current out of the ISET1N pin which represents V_1 output current. Each LT8228 contributes this current into the common ISHARE node. When all the R_{SHARE} resistors are equal, voltage at the ISHARE node represents the average output current. When a controller is disabled or has a fault condition, the ISHARE pin does not output any current.

In buck mode, V_2 output current is regulated so that ISET2P pin voltage is equal to the voltage on the ISHARE pin. To regulate each LT8228's V_2 output current to the average output current, make R_{SET2P} and R_{SHARE} equal. In boost mode, V_1 output current is regulated so that ISET1N pin voltage is equal to the voltage on the ISHARE pin. To regulate each LT8228's V_1 output current to the average output current, make R_{SET1N} and R_{SHARE} equal. In order to set different output current limits in buck and boost modes, R_{SET2P} and R_{SET1N} can be set at different values as long as the value of R_{SHARE} is changed based on the mode of operation defined by the DRXN pin.

Connect a filtering capacitor between the ISHARE pin and ground for average current regulation. See the Paralleling Multiple LT8228s in Applications Information section for more details. Refer to the IGND pin function description for fault tolerance and redundancy design. Tie the ISHARE pin to $INTV_{CC}$ if not used.

SNS2P, SNS2N (Pins 18, 19): Positive and Negative Input Terminals of the V_2 Bidirectional Current Sense Amplifier (CSA2 in the Block Diagram section) for current monitoring and regulation of the input current in boost mode and output current in buck mode. Current sense polarity is positive for current flowing out of V_1 into V_2 . Place input gain resistors R_{IN2} between the current sense resistor R_{SNS2} and these pins. Typical bias current into these pins is 90µA for common mode voltage above 2.5V. As common mode voltage decreases below 2.5V, bias current decreases and reverses direction. See the curve of I_{B2} over V_{CM2} in the Typical Performance Characteristics section.

PIN FUNCTIONS

CSA2 is connected in a negative feedback loop to make SNS2N and SNS2P pin voltages equal. The voltage across the current sense resistor and the input gain resistors generate a difference in current flowing into the SNS2N and SNS2P pins, ISNS2N and ISNS2P. The current flowing through R_{SNS2} , ISNS2, includes the V_2 current, the input bias current of CSA2's negative feedback terminal and the differential current given by Equation 9.

$$I_{SNS2N} - I_{SNS2P} = \frac{I_{SNS2} \bullet R_{SNS2}}{R_{IN2}} \quad (9)$$

In buck mode, this current difference is generated out of the ISET2P, ISHARE and IMON2 pins. In boost mode, it is generated out of the ISET2N and IMON2 pins. Limit the difference between SNS2N and SNS2P pin currents to ±100µA by choosing the values of R_{SNS2} and R_{IN2} appropriately. Refer to the R_{SNS2} and R_{IN2} Selection for Peak Inductor Current in Applications Information section for more details.

IGND (Pin 20): Current Sharing Ground. Connect a local resistor R_{SHARE} from the ISHARE pin to the IGND pin. When the LT8228 is enabled and the internal diagnostic routine is passed, the IGND pin connects R_{SHARE} to ground through a 120Ω switch. During shutdown or a faulted condition, ISHARE stops generating current and the switch at the IGND pin is opened so that no current flows through the current sharing resistor. This disconnects the R_{SHARE} resistor from the common ISHARE node so that the ISHARE node continues to represent the average output current of the remaining active LT8228's in parallel. With this scheme, any paralleled LT8228 can be added or subtracted without affecting current sharing accuracy. The IGND pin along with the ISHARE pin provides a current sharing that is masterless as well as fault tolerant. Refer to the Paralleling Multiple LT8228s in Applications Information section for more information. Tie the pin to ground if not used.

$INTV_{CC}$ (Pin 21): Internal 4V V_{CC} Supply. $INTV_{CC}$ is powered from DRV_{CC}. Connect a minimum bypass capacitor of 1µF from $INTVC_C$ to ground. Do not load this pin except for pulling up the DRXN and $\overline{FAULT}$ pins.

DRXN (Pin 22): Buck or Boost Regulation Mode Select. Pulling the pin high selects buck regulation mode and pulling the pin low selects boost regulation mode. Drive the DRXN pin with logic level input or with a pull-up resistor. Driving the DRXN pin higher than 1.1V selects buck mode and lower than 0.8V selects boost mode. The pull-up resistor allows the LT8228 to auto-select the regulation mode based on the UV1, UV2, FB1 and FB2 pin voltages. The DRXN pin is high impedance when the LT8228 is in buck mode which pulls the DRXN pin high through the pull-up resistor. A 100µA pull-down is enabled when the LT8228 is in boost mode which pulls the DRXN pin low. The typical value of the pull-up resistor is 100k and should not be less than 40k when connected to $INTV_{CC}$ to guarantee a low logic level.

When the LT8228 is enabled and the UV1 pin voltage is higher than 1.2V, the part starts regulation in buck mode. If the UV1 pin voltage is lower than 1.2V when enabled, the LT8228 starts regulation in boost mode. If both UV1 and UV2 pin voltages are lower than 1.2V, the part is in buck mode, the $\overline{FAULT}$ and SS pins pull low and the LT8228 does not switch. If the LT8228 is in buck mode and the UV1 pin voltage drops lower than 1.2V or the FB2 pin voltage rises higher than 1.3V for 1024 switching clock cycles, the controller transitions to boost mode. When in boost mode, if the UV2 pin voltage drops lower than 1.2V or the FB1 pin voltage rises higher than 1.3V for 1024 switching clock cycles, the controller transitions to buck mode. If both the FB1 and FB2 pin voltages are higher than 1.3V for 1024 switching clock cycles, the part is in buck mode, the $\overline{FAULT}$ and SS pins pull low and the LT8228 does not switch. Anytime DRV_{CC} or $INTV_{CC}$ pin voltages fall below their respective undervoltage threshold, the part goes to buck mode, the $\overline{FAULT}$ and SS pins pull low and the LT8228 does not switch.

When multiple LT8228s are in parallel, tie all the DRXN pins together to operate all LT8228s in the same regulation mode. Connect a single pull-up resistor between the common DRXN node and an external voltage source. If the external voltage source is not available, each LT8228

PIN FUNCTIONS

needs its own pull-up resistor in series with a diode whose anode is connected to its $INTV_{CC}$ pin. This diode prevents unintentional boost mode selection when one or more channels are disabled. Refer to the Paralleling Multiple LT8228s in Applications Information section for more information. Do not leave this pin open.

SYNC (Pin 23): Synchronization or Spread Spectrum Input. Synchronize to an external clock with pulses that have duty cycles between 5% and 95% from 80kHz to 600kHz. The high level of the clock voltage needs to be above 1V and the low level needs to be below 0.5V. To enable spread spectrum of the internal frequency generator, connect this pin to $INTV_{CC}$. Connect this pin to ground to disable spread spectrum. Do not leave this pin open.

$\overline{FAULT}$ (Pin 24): Fault Status Indicator. $\overline{FAULT}$ is an open-drain logic pin which flags fault conditions (refer to the $\overline{FAULT}$ Conditions in Applications Information section for more information). When the $\overline{FAULT}$ pin asserts, the LT8228 stops switching and the SS pin pulls low. Pull-up the pin with an LED in series with a resistor to a voltage source to provide a visual status indicator. For a sink current of 2mA, the maximum voltage overtemperature at the $\overline{FAULT}$ pin is 0.5V. Tie the pin to ground if not used.

$\overline{REPORT}$ (Pin 25): Diagnostic Status. This pin is an open-drain active low output that reports the state of the internal diagnostic monitors of critical safety features through a digital logic bit stream synchronized to the frequency of the SYNC pin. See the Report Feature in Applications Information section for more details on the report function. Pull-up the pin with a series resistor to a microcontroller input logic voltage source. For a sink current of 2mA, the maximum voltage overtemperature at the $\overline{REPORT}$ pin is 0.5V. Tie the pin to ground if not used.

TMR (Pin 26): Timer Input for SOA Management of V_1 Protection MOSFET (M1). Connect a capacitor between this pin and ground to set the M1 turn-off and cool down periods at excess power dissipation during output inrush current in boost mode. In boost mode, when current regulation at ISET1N is 1.4V and voltage across M1 (V1D, DS1) exceeds 500mV, the TMR pin voltage starts to increase. The current charging up this pin increases with the voltage difference between V1D and DS1 pins (see Applications Information). When the TMR reaches 1.4V, the LT8228 shorts DG1 to DS1 to turn-off M1. Upon M1 gate off, a cool down interval commences while the TMR pin cycles 32 times between 0.4V and 1.4V with 2µA charge and discharge currents. When TMR crosses 0.4V the 32nd time, the DG1 pin pulls high, turning on M1.

BG (Pin 27): Bottom Gate Drive. The BG pin drives the gate of the low side N-channel synchronous switch MOSFET M3. The BG voltage transitions between DRV_{CC} and ground.

DRV_{CC} (Pin 28): 10V Gate Drive V_{CC} Supply. DRV_{CC} is powered from BIAS. It provides power to the top gate (TG) and bottom gate (BG) MOSFET drivers. Connect a minimum bypass capacitor of 2.2µF from DRV_{CC} to ground.

BIAS (Pin 29): DRV_{CC} and Control Circuitry Supply. This pin supplies the DRV_{CC} regulator as well as the internal control circuitry. BIAS can be connected to V_1 or V_2 or an external supply. No negative voltage is allowed at the BIAS pin. Refer to the BIAS, DRV_{CC}, $INTV_{CC}$ and Power Dissipation in Applications Information section for more details. Connect a minimum bypass capacitor of 10µF from BIAS to ground.

SW (Pin 30): Switch Node. This pin connects to the source of the top side MOSFET M2 and to the drain of the bottom side MOSFET M3. This pin also connects to the inductor and the bootstrap capacitor C_{BST}.

TG (Pin 31): Top Gate Drive. The TG pin drives the gate of the high side N-channel MOSFET M2. TG draws power from the BST pin and returns to the SW pin, providing true floating gate drive to the high side MOSFETs.

BST (Pin 32): Top Gate Driver Boosted Supply. The BST pin supplies power to the floating TG driver for the high side MOSFET (M2). Connect a low ESR capacitor from the BST pin to the SW pin. Connect a fast recovery diode from DRV_{CC} to BST to supply this pin. The pin voltage swings from a diode below DRV_{CC} up to $DRV_{CC} + V_{1D}$.

ENABLE (PIN 33): Enable Input. Pull this pin above 1.3V typically to enable the LT8228. When this pin is pulled below the typical threshold voltage of 1.2V, the controller stops switching, the protection MOSFETs are turned off, and the DRV_{CC} and $INTV_{CC}$ regulators are disabled. When

PIN FUNCTIONS

the ENABLE pin is pulled below 0.7V typically, the LT8228 turns off internal references and enters a low quiescent current state of 10µA typically.

DS2 (Pin 34): Source Input of the V_2 N-channel Protection MOSFET and DG2 Drive Return. Connect the pin to the sources of the V_2 N-channel protection MOSFETs M4A and M4B. If a single MOSFET M4 is used as the V_2 protection MOSFET, DS2 pin connects to both the source of M4 and the V_2 terminal. Voltage sensed at the DS2 pin is used for M4's gate control. DS2 can sustain voltages down to –40V. The LT8228 protects itself and the load at V_1 by turning off M4 when a supply is connected in reverse at V_2.

DG2 (Pin 35): V_2 Protection MOSFET M4A and M4B's Gate. The DG2 pin controls the gate of the N-channel MOSFETs M4A and M4B. After the LT8228 is enabled, The DG2 pin pulls high with a 10µA pull-up current to a typical value of 10V above DS2 to enhance M4A and M4B. When the LT8228 is disabled, or in a fault condition, or if the V_2 voltage goes negative, the LT8228 shorts DG2 to DS2, turning off M4A and M4B (refer to the $\overline{\text{FAULT}}$ Conditions in the Applications Information section). This pin is designed for capacitive load only. Connect a series capacitor C_{DG2} and a resistor R_{DG2} for inrush current control. Refer to the Inrush Current Control in Applications Information section for more details. Keep the pin open if not in use.

V1D (Pin 36): The Drain of V_1 Protection MOSFET M1A. The voltage sensed at this pin is used to control the DG1 voltage in boost mode. V_{1D} is the regulated output in boost mode. Connect a minimum bypass capacitor of 10µF from V1D to ground.

DS1 (Pin 37): Source Input of the V_1 N-channel Protection MOSFET and DG1 Drive Return. Connect the pin to the sources of the V_1 N-channel protection MOSFETs M1A and M1B. If a single MOSFET M1 is used as the V_1 protection MOSFET, DS1 pin connects to both the source of M1 and the V_1 terminal. Voltage sensed at the DS1 pin is used for M1's gate control. DS1 can sustain voltages down to –40V. The LT8228 protects itself and the load at V_2 by turning off M1 when a supply is connected in reverse at V_1.

DG1 (Pin 38): V_1 Protection MOSFET M1A and M1B's Gate. The DG1 pin controls the gate of the N-channel MOSFETs M1A and M1B. After the LT8228 is enabled, The DG1 pin pulls high with a 10µA pull-up current to a typical value of 10V above DS1 to enhance M1A and M1B. When the LT8228 is disabled, or in a fault condition, or if the V_1 voltage goes negative, the LT8228 shorts DG1 to DS1, turning off M1A and M1B (refer to the $\overline{\text{FAULT}}$ Conditions in the Applications Information section). Connect a series capacitor C_{DG1} and a resistor R_{DG1} for inrush current control and boost output short current regulation. Refer to the Inrush Current Control and boost short output current in Applications Information section for more details. This pin is designed for capacitive load only. Keep the pin open if not in use.

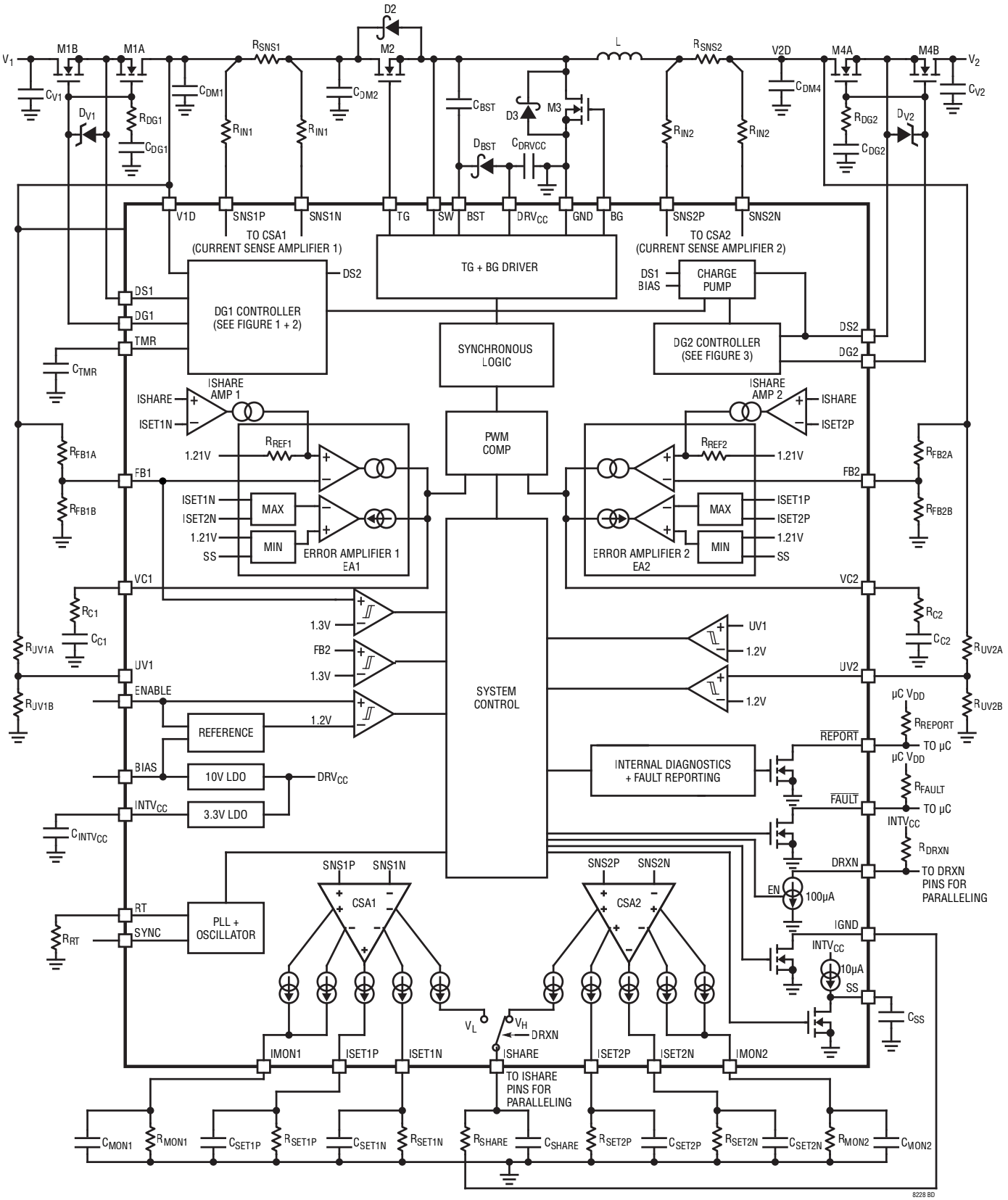
In buck mode, when V_1 falls within 500mV of V_2 and R_{SNS1} current passes negative threshold, the LT8228 detects reverse current and shorts DG1 to DS1, turning off M1. Negative threshold for reverse current detection in buck mode is given by Equation 10.

$$I_{RCUR,BUCK} = \frac{R_{IN}}{R_{SNS2}} \bullet 3\mu A \quad (10)$$

In boost mode, at start-up when V_1 is lower than V_2 or V_1 is shorted to GND, the output current cannot be limited by the boost regulation loop. Under such conditions, the LT8228 controls the output current by controlling M1A, the V_1 protection MOSFET. The LT8228 controls DG1, the gate of M1 by regulating ISET1N to 1.4V. Current regulation at ISET1N and voltage across M1 (V1D, DS1) exceeding 500mV triggers current at the TMR pin. The current is proportional to the voltage across the drain and source of M1. If the voltage at the TMR pin reaches 1.4V, the LT8228 turns of M1 and initiates a cool down period. Programming the TMR pin with a capacitor (see Application Information) keeps M1 always within its safe operating area (SOA).

GND (Exposed Pad Pin 39): Ground. The exposed pad of the TSSOP is an electrical connection to GND. Tie the exposed pad directly to the other GND pin and the PCB ground to ensure proper electrical and thermal performance.

BLOCK DIAGRAM



OPERATION

Refer to the Block Diagram section when reading the following sections about the operation of the LT8228.

OVERVIEW

The LT8228 is a 100V bidirectional peak current mode synchronous controller with protection MOSFETs. The controller provides a step-down output voltage V_2 from an input voltage V_1 when in buck mode or a step-up output voltage V_1 from an input voltage V_2 when in boost mode. The input and output voltage can be set as high as 100V. The mode of operation is externally controlled through the DRXN pin or automatically selected. In addition, the LT8228 has protection MOSFETs for the V_1 and the V_2 terminals. The protection MOSFETs provide negative voltage protection, isolation between the input and output terminals during an internal or external fault, reverse current protection and inrush current control. In applications such as battery backup systems, the bidirectional feature allows the battery to be charged from either a higher or lower voltage supply. When the supply is unavailable, the battery boosts or bucks power back to the supply. To optimize transient response, the LT8228 has two error amplifiers: EA1 in boost mode and EA2 in buck mode with separate compensation pins VC1 and VC2 respectively. The controller operates in discontinuous conduction mode when reverse inductor current is detected for conditions such as light load operation.

The LT8228 provides input and output current limit programming in buck and boost mode operation using four pins, ISET1P, ISET1N, ISET2P and ISET2N. The controller also provides independent input and output current monitoring using the IMON1 and IMON2 pins. Current limit programming and monitoring is functional for the entire input and output voltage range of 0V to 100V. Dynamic control of the input and output current limits is achieved by modulating the ISET pins. These features allow maximum design flexibility for applications such as maintaining battery charging profiles. The LT8228 employs a masterless fault-tolerant current sharing scheme using the ISHARE and the IGND pins allowing higher load current, better heat management and redundancy.

The LT8228's control circuitry and the 10V gate drive are supplied from the BIAS pin. The BIAS pin is tied to either V_1 or V_2 or to an independent source. Managing the voltage at the BIAS pin lowers thermal dissipation. The 10V gate drive feature complements high voltage high current switching MOSFETs, which tend to have higher threshold tvoltages.

The LT8228 provides fixed switching frequency operation from 80kHz to 600kHz programmed through the RT pin. The SYNC pin is used to synchronize to an external clock or enable the spread spectrum of the switching frequency set by the RT pin.

The LT8228 has undervoltage protection for the input and overvoltage protection for the output, over temperature protection and switching MOSFET fault detection and protection that are all reported via the $\overline{\text{FAULT}}$ and the $\overline{\text{REPORT}}$ pins. When the controller is enabled, an internal diagnostic routine checks for functionality of critical circuits before switching starts. If any error is found, the controller remains disabled and the error can be read through the $\overline{\text{REPORT}}$ pin. Fault reporting and internal diagnostics improve the reliability of the LT8228 from a safety perspective.

BUCK MODE OPERATION

In buck mode, the LT8228 is a peak current mode step-down controller where V_1 is the input supply and V_2 is the output load. Two back-to-back N-channel MOSFETs M1A and M1B are placed between the V_1 terminal and the input of the buck regulator V_{1D} as shown in the Block Diagram section. DS1 is the source and DG1 is the gate of both M1A and M1B. V_{1D} is the drain of M1A and V_1 is the drain of M1B. M1A is used by the LT8228 V_1 protection MOSFET controller to protect the regulator from reverse current from V_2 to V_1 and negative voltages on V_1. M1B is used to control the inrush current from V_1 to V_{1D} and to isolate V_1 and V_2 during fault conditions. Depending on the application requirement, either M1A or M1B or both M1A and M1B are optional. In normal operation when M1A and M1B are enhanced, the voltage difference between V_1 and V_{1D} is equal to the total on-resistance multiplied by the V_1 input current.

OPERATION

Two back-to-back N-channel MOSFETs M4A and M4B are placed between the V_2 terminal and the output of the buck regulator, V_{2D} as shown in the Block Diagram section. M4A is used by the LT8228's V_2 protection MOSFET controller to protect the regulator from negative voltages on V_2. M4B is used to control inrush current from V_2 to V_{2D} and to isolate V_1 and V_2 completely during fault conditions. DS2 is the source and DG2 is the gate of both M4A and M4B. V_{2D} is the drain of M4A and V_2 is the drain of M4B. Depending on the application requirement, either M4A or M4B or both M4A and M4B are optional. In normal operation when M4A and M4B are enhanced, the voltage difference between V_2 and V_{2D} is equal to the total on-resistance multiplied by the V_2 output current.

V_{2D} is the node to be regulated by the buck regulator through a resistor divider from V_{2D} to the FB2 feedback pin. The error amplifier regulates the FB2 pin to the typical internal reference voltage of 1.21V. The compensation of the buck regulator error amplifier output is at the VC2 pin. The VC2 pin sets the inductor current which is modulated to regulate the V_{2D} voltage.

In a general implementation where V_{2D} is regulated to a constant voltage, EA2 senses the output voltage through the FB2 pin and compares the signal to the typical internal reference voltage of 1.21V. Low V_{2D} voltage creates a higher VC2 voltage to increase the current flow into the V_{2D} node and raises V_{2D} to the steady state regulation target value. Conversely, higher V_{2D} voltage creates a lower VC2 voltage to reduce the current flow into the V_{2D} node and lowers V_{2D} to the steady state target value.

In buck mode, the LT8228 provides input and output current limiting using the ISET1P and the ISET2P pins respectively. The controller additionally provides input and output current monitoring using the IMON1 and IMON2 pins respectively. The input current is measured by the V_1 current sense amplifier CSA1 which senses the voltage across the current sense resistor R_{SNS1} and generates a current proportional to the sensed voltage. CSA1 outputs the current out of the IMON1 and ISET1P pins. Similarly, the output current is measured by the V_2 current sense amplifier CSA2 which senses the voltage difference across the current sense resistor R_{SNS2} and generates a current proportional to the sensed voltage. CSA2 outputs the current out of the IMON2 and ISET2P pins.

The voltages at the IMON1, IMON2, ISET1P and ISET2P pins are set by connecting resistors from these pins to ground. The buck regulator limits current when either ISET1P or ISET2P reaches the typical internal reference voltage of 1.21V. This current regulation feature is ideal for many battery charging applications. During start-up when the SS pin voltage is lower than the typical internal reference voltage, ISET1P and ISET2P are regulated to the SS pin voltage.

BOOST MODE OPERATION

In boost mode, the LT8228 is a peak current mode step-up controller where V_2 is the input supply and V_1 is the output load. Two back-to-back N-channel MOSFETs M1A and M1B are placed between the V_1 terminal and the output of the boost regulator, V1D as shown in the Block Diagram section. DS1 is the source and DG1 is the gate of both M1A and M1B. V1D is the drain of M1A and V_1 is the drain of M1B. M1A is used by the LT8228 V_1 protection MOSFET controller to protect the regulator from negative voltages on V_1 and to control the outrush current from V1D to V_1. M1B is used to control the inrush current from V_1 to V1D and to isolate V_1 and V_2 during fault conditions. Depending on the application requirement, either M1A or M1B or both M1A and M1B are optional. In normal operation when M1A and M1B are enhanced, the voltage difference between V_1 and V1D is equal to the total on-resistance multiplied by the V_1 output current.

Two back-to-back N-channel MOSFETs M4A and M4B are placed between the V_2 terminal and the output of the buck regulator V_{2D} as shown in the Block Diagram section. M4A is used by the LT8228 V_2 protection MOSFET controller to protect the regulator from negative voltages on V_2. M4B is used to control the inrush current from V_2 to V_{2D} and to isolate V_1 and V_2 during fault conditions. DS2 is the source and DG2 is the gate of both M4A and M4B. V_{2D} is the drain of M4A and V_2 is the drain of M4B. Depending on the application requirement, either M4A or M4B or both M4A and M4B are optional. In normal operation when M4A and M4B are enhanced, the voltage difference between V_2 and V_{2D} is equal to the total on-resistance multiplied by the V_2 output current.

OPERATION

V1D is the node to be regulated by the boost regulator through a resistor divider from V1D to the FB1 feedback pin. The error amplifier regulates the FB1 pin to the typical internal reference voltage of 1.21V. The compensation of the boost regulator error amplifier output is at the VC1 pin. The VC1 pin sets the inductor current which is modulated to regulate the V1D voltage.

In a general implementation where V1D is regulated to a constant voltage, EA1 senses the output voltage through the FB1 pin and compares the signal to the typical internal reference voltage of 1.21V. Low V1D voltage would create a higher VC1 voltage, and more current would flow into the V1D node, raising V1D to the steady state regulation target value. Conversely, higher V1D voltage would create a lower VC1 voltage, thus reducing the current flowing into the V1D node, lowering the V1D voltage closer to the steady state target value.

In boost mode, the LT8228 provides input and output current limiting using the ISET2N and the ISET1N pins respectively. The controller additionally provides input and output current monitoring using the IMON2 and IMON1 pins respectively. The input current is measured by the V_2 current sense amplifier CSA2 which senses the voltage across the current sense resistor R_{SNS2} and generates a current proportional to the sensed voltage. CSA2 outputs the current out of the IMON2 and ISET2P pins. Similarly, the output current is measured by the V_1 current sense amplifier CSA1 which senses the voltage difference across the current sense resistor R_{SNS1} and generates a current proportional to the sensed voltage. CSA1 outputs the current out of the IMON1 and ISET1N pins.

The voltages at the IMON1, IMON2, ISET1N and ISET2N pins are set by connecting resistors from these pins to ground. The boost regulator limits current when either ISET1N or ISET2N reaches the typical internal reference voltage of 1.21V. This current regulation feature is ideal for many battery charging applications. During start-up when the SS pin voltage is lower than the typical internal reference voltage, ISET1P and ISET2P are regulated to the SS pin voltage.

V_1 PROTECTION MOSFET CONTROLLER OPERATION

The LT8228 provides protection functionality at the V_1 terminal using two N-channel MOSFETs M1A and M1B connected back-to-back in series or a single N-channel MOSFET M1 as shown in Figure 1. In dual MOSFET back-to-back configuration, DS1 is the source and DG1 is the gate of both M1A and M1B. V1D is the drain of M1A and V_1 is the drain of M1B. In single MOSFET configuration, the source of M1 is connected to DS1 and the V_1 terminal, DG1 is the gate and V1D is the drain. The advantages of the dual MOSFET configuration are inrush current control and complete isolation of the V_1 terminal in a fault condition. In normal operation, the controller drives DG1 high with a typical 10µA pull-up current that enhances the V_1 protection MOSFETs to provide a low loss conduction path between V_1 and V1D. The DG1 voltage is clamped at a typical value of 10V above DS1. The DG1 controller shorts DG1 to DS1 thereby isolating V_1 from the rest of the circuit when (1) the LT8228 is disabled or

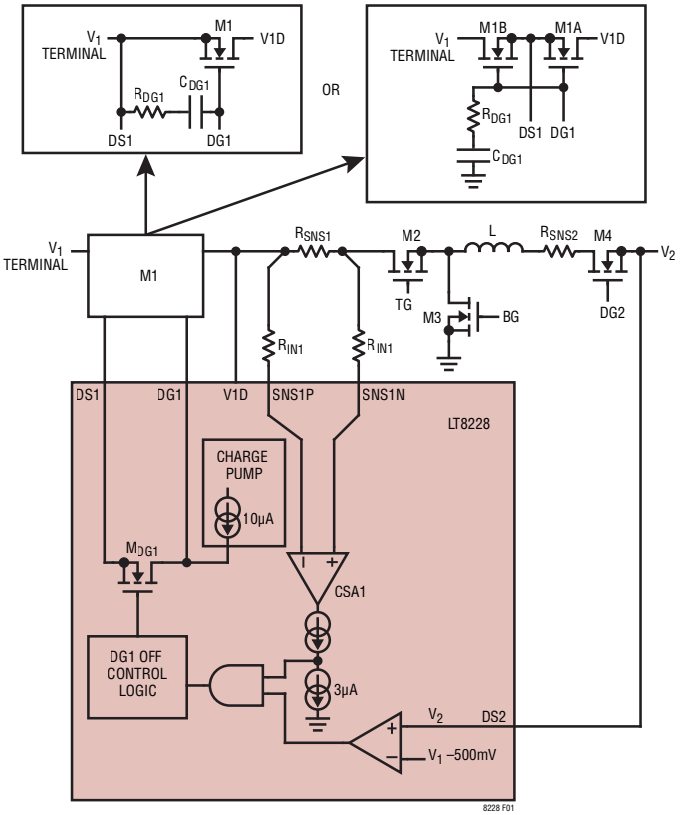


Figure 1. M1 Control in Buck Mode

OPERATION

(2) DS1 drops below –1.7V typically or (3) the internal temperature rises above the overtemperature threshold or (4) Any of the switching MOSFET short conditions is detected or (5) DRV_{CC} pin voltage drops below its undervoltage threshold or rises above its overvoltage threshold or (6) $INTV_{CC}$ pin voltage drops below its undervoltage threshold or rises above its overvoltage threshold or (7) the part fails the internal diagnostic tests. When M1 is not enhanced in single MOSFET configuration, V1D is a forward diode voltage away from V_1 due to the M1 body diode. In dual MOSFET configuration, V1D is fully isolated from V_1 when M1A and M1B are not enhanced.

The buck mode operation circuitry of the V_1 protection MOSFET controller is shown in Figure 1. Without protection MOSFETs, there is a direct conduction path from V_2 to V_1 through the body diode of the top MOSFET M2. If V_2 is higher than V_1 by a forward diode voltage, uncontrolled reverse current flows from V_2 to V_1. Unlike other buck controllers, the LT8228 provides protection from this reverse current condition using the V_1 protection MOSFET. If V_1 falls within 500mV of V_2 and R_{SNS1} current passes negative threshold, the LT8228 detects reverse current. A fast pull-down circuit shorts DG1 and DS1, turning off M1. This isolates V_1 from V1D and stops any reverse current. The reverse current detect threshold is set by Equation 11.

$$I_{RCUR,BUCK} = \frac{R_{IN}}{R_{SNS2}} \bullet 3\mu A \quad (11)$$

This protection feature is useful for applications where V_2 is prebiased with a load such as a battery.

In dual MOSFET configuration, inrush current to C_{DM1} and C_{DM2} in buck mode is limited by controlling the DG1 pin voltage slew rate. In this configuration, the compensation resistor R_{DG1} and capacitor C_{DG1} are ground referenced as shown in Figure 1. At start-up, a 10µA pull-up current charges DG1, pulling up both MOSFET gates. M1B operates as a source follower (see Equation 12).

$$I_{INRUSH,BUCK} = \frac{10\mu A \bullet (C_{DM1} + C_{DM2})}{C_{DG1}} \quad (12)$$

This feature is not available with single MOSFET due to the M1 body diode connecting V1D to V_1.

The boost mode operation circuitry of the protection MOSFET controller at V_1 is shown in Figure 2. Without protection MOSFETs, there is a direct conduction path from V_2 to V_1 through the body diode of the top MOSFET M2. If V_2 is higher than V_1 by a forward diode voltage, uncontrolled current flows from V_2 to V_1. This condition is common to most boost start-up events. Unlike other boost controllers, the LT8228 provides protection from this uncontrolled output current condition using the V_1 protection MOSFET M1A (M1 in single MOSFET configuration). This current is limited in boost mode through DG1 by regulating the ISET1N pin voltage to 1.4V. Further reduction in V_2 output current is possible by increasing the R_{SET1N} resistance or injecting current into the ISET1N pin.

In addition to output current control in boost mode, the LT8228 includes an adjustable fault timer to protect M1A (M1 in single MOSFET configuration) from excessive power dissipation damage. If V1D is higher than V_1 by

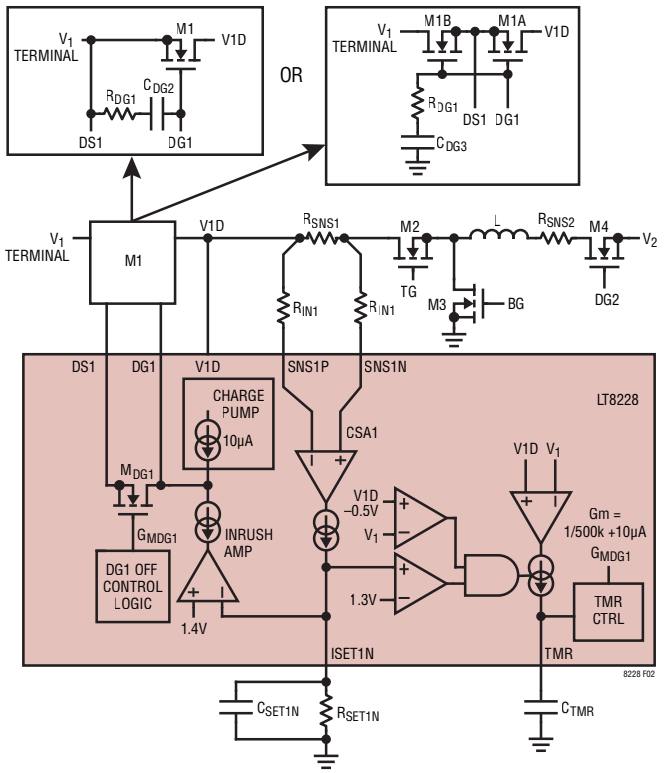


Figure 2. M1 Control in Boost Mode

OPERATION

500mV and ISET1N is regulated to 1.4V, a current source starts charging up the capacitor connected at the TMR pin to ground. When TMR reaches 1.4V, the DG1 controller shorts DG1 to DS1 and turns off M1. The timer allows the LT8228 to increase the voltage at V_1 while protecting the MOSFET from being damaged by long period of high power dissipation. The TMR charging current varies depending on the voltage drop between V1D and V_1, corresponding to the MOSFET V_{DS}. The on time is inversely proportional to the voltage drop across the MOSFET. This helps to keep the MOSFET within its safe operating area (SOA). After a cool down timer cycle, the LT8228 allows M1 to turn back on and resume its operation.

V_2 PROTECTION MOSFET CONTROLLER OPERATION

The LT8228 provides protection functionality at the V_2 terminal using two N-channel MOSFETs M4A and M4B connected back-to-back in series or a single N-channel MOSFET M4 as shown in Figure 3. In dual MOSFET back-to-back configuration, DS2 is the source and DG2 is the gate of both M4A and M4B. V_{2D} is the drain of M4A and V_2 is the drain of M4B. In single MOSFET configuration, the source of M4 is connected to DS2 and the V_2 terminal, DG2 is the gate and V_{2D} is the drain. The advantages of dual MOSFET configuration are inrush current control in boost mode and complete isolation of the V_2 terminal in a fault condition. In a BG MOSFET M3 short fault, dual MOSFET configuration is necessary to isolate V_2 from ground. In normal operation, the controller drives DG2 high with a typical 10µA pull-up current that enhances the V_2 protection MOSFETs to provide a low loss conduction path between V_2 and V_{2D}. The DG2 voltage is clamped at a typical value of 10V above DS2. The DG2 controller shorts DG2 to DS2 thereby isolating V_2 from the rest of the circuit when (1) the LT8228 is disabled or (2) DS2 drops below –1.7V typically or (3) the internal temperature rises above the overtemperature threshold or (4) any of the switching MOSFET short conditions is detected or (5) DRV_{CC} pin voltage drops below its undervoltage threshold or rises above its overvoltage threshold or (6) $INTV_{CC}$ pin voltage drops below its undervoltage threshold or rises above its overvoltage threshold or (7) the part fails the internal diagnostic tests. When M4 is not enhanced in single MOSFET configuration, V_{2D} is a forward diode voltage away from V_2 due to the M1 body diode. In dual MOSFET configuration, V_{2D} is fully isolated from V_2 when M4 is not enhanced.

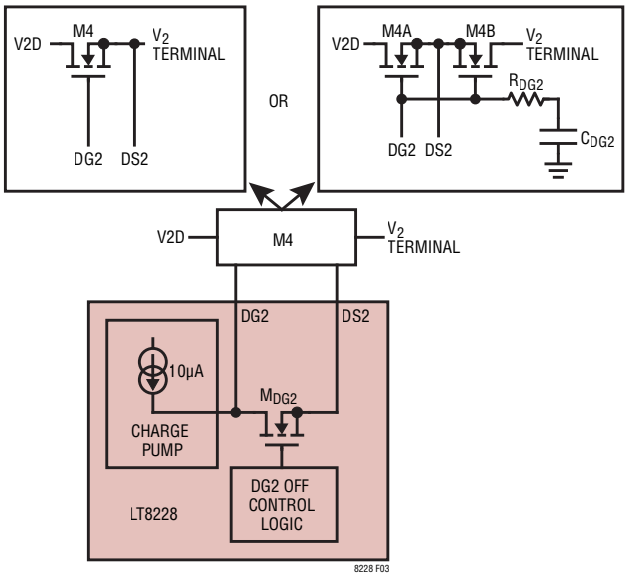


Figure 3. M4 Control in Buck and Boost Mode

In dual MOSFET configuration, inrush current to C_{DM4}, C_{DM2} and C_{DM1} in boost mode is limited by controlling the DG2 pin voltage slew rate. In this configuration, the resistor R_{DG2} and capacitor C_{DG2} are ground referenced as shown in Figure 3. At start-up, a 10µA pull-up current charges DG2, pulling up both MOSFET gates. M2B operates as a source follower (see Equation 13).

$$I_{INRUSH,BUCK} = \frac{10\mu A \bullet (C_{DM1} + C_{DM2} + C_{DM4})}{C_{DG2}} \quad (13)$$

This feature is not available with single MOSFET due to the M4 body diode connecting V_2 to V_{2D}.

MODE OF OPERATION (DRXN)

The DRXN pin selects the LT8228 mode of operation. Pulling the pin high selects buck regulation mode and pulling the pin low selects boost regulation mode. Drive the DRXN pin with either external logic for manual control or connect a pull-up resistor to $INTV_{CC}$ or an external supply for auto-selection. The LT8228 auto-selects the

OPERATION

regulation mode based on the UV1, UV2, FB1 and FB2 pin voltages. When external logic is used, include the pull-up resistor for cases where the external logic is accidently disconnected for increased system reliability. This allows the LT8228's auto-selection of the operation mode to take over. In buck mode, the DRXN pin goes high impedance which externally pulls the pin voltage high through the pull-up resistor. In boost mode, a typically 100µA pull-down is enabled which pulls the DRXN pin low.

When the LT8228 is enabled, and the DRXN pin is configured for auto-selection for the mode of operation, the DRXN pin is high impedance until the internal regulators are functional. The LT8228 then selects the mode of operation based on the logic shown in Figure 4. If the UV1 pin voltage is higher than 1.2V, the controller is in buck mode operation. If the UV1 pin voltage is lower than 1.2V, the controller goes into boost mode. During buck mode operation, if the UV1 pin voltage drops lower than 1.2V or FB2 pin voltage stays higher than 1.3V for 1024 switching cycles, the LT8228 changes mode of operation from buck to boost. Additional time requirement for the FB2 overvoltage ensures no mode hopping during transients at the load. In boost mode operation if the UV2 pin voltage drops lower than 1.2V or FB1 pin voltage stays higher than 1.3V for 1024 switching cycles, the LT8228 changes mode of operation from boost to buck. Anytime both UV1 and UV2 pin voltage drops below 1.2V or both FB1 and FB2 pin voltage stays higher than 1.3V for 1024 switching cycles, the controller goes to buck mode operation, stops switching, pulls down on the $\overline{\text{FAULT}}$ pin and report the fault at the $\overline{\text{REPORT}}$ pin. For input undervoltage fault, the SS pin is also pulled low. Anytime DRV_{CC} or $INTV_{CC}$ pin voltages fall below their respective undervoltage threshold, the part goes to buck mode, the $\overline{\text{FAULT}}$ and SS pin pulls low and the LT8228 does not switch.

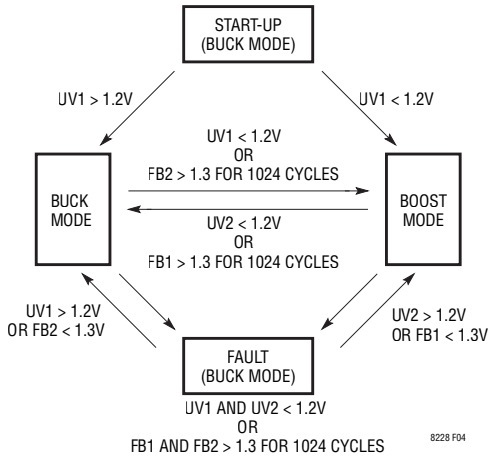


Figure 4. Automatic Mode of Operation

During startup or fast transient, output overshoot higher than 10% is possible at light load. If the overshoot condition last more than 1024-clock cycle, the DRXN will change state. Ensure minimum loading to avoid unintended DRXN change.

When the DRXN pin is driven high with external logic for buck mode operation, and the UV1 pin voltage drops lower than 1.2V or FB2 pin voltage stays higher than 1.3V for 1024 switching cycles, the LT8228 stops switching, pulls down on the $\overline{\text{FAULT}}$ and report the fault at the $\overline{\text{REPORT}}$ pin. When the DRXN pin is driven low with external logic for boost mode operation, and the UV2 pin voltage drops lower than 1.2V or FB1 pin voltage stays higher than 1.3V for 1024 switching cycles, the LT8228 stops switching, pulls down on the $\overline{\text{FAULT}}$ and report the fault at the $\overline{\text{REPORT}}$ pin. For input undervoltage fault, the SS pin is also pulled low.

When multiple LT8228s are in parallel, tie all the DRXN pins together to operate all LT8228s in the same regulation mode. In the parallel configuration, the common DRXN node must be pulled up to an external voltage source through a pull-up resistor. If an external voltage source is not available, each LT8228 needs its own pull-up resistor in series with a diode whose anode is connected to its own $INTV_{CC}$ pin. This diode prevents unintentional boost mode selection when one or more channels are disabled. Refer to the Paralleling Multiple LT8228s in Applications Information section for more information.

ENABLE AND SOFT-START (ENABLE AND SS)

The LT8228 enters shutdown through the ENABLE pin. Pulling this pin below 1.2V typically disables the controller and most of the internal circuitry. Pulling the ENABLE pin below 0.5V transitions the LT8228 into complete shutdown where the controller only consumes 2µA of

OPERATION

shutdown current from the BIAS pin and 10µA from the V1 and V2 pins to ground typically. The ENABLE pin can be directly driven by logic or it can be connected to BIAS for an always-on operation. In normal operation when the controller is not switching, the controller consumes 4mA of quiescent current from the BIAS pin, 200µA from the V1 pin and 10µA from the V2 pin to ground typically.

In buck mode, the LT8228 limits the V_1 input and the V_2 output current by regulating the ISET1P and ISET2P pin voltages respectively to the lower of the SS pin voltage and the internal reference voltage of 1.21V typically. The SS pin programs a current limit soft-start when connecting an external capacitor, C_{SS}, from the SS pin to ground, limiting inrush current during start-up. When the LT8228 is enabled, after the DRV_{CC} and $INTV_{CC}$ voltages exceed their undervoltage thresholds, and after the internal diagnostics are successfully completed, DG1 pin is charged with a 10µA pull-up current. If dual MOSFET configuration is used at the V_1 terminal, inrush current is controlled through C_{DG1} and V1D is charged to V_1 as DG1 voltage exceeds it undervoltage threshold. If single MOSFET configuration is used, V1D is a forward diode drop away from V_1 at start-up and charged to V_1 as DG1 rises. Next, DG2 starts charging and after DG2 voltage exceeds its threshold voltage, an internal 10µA pull-up current charges the C_{SS} capacitor and creates a voltage ramp on the SS pin. As the SS voltage rises linearly from 0V to the internal reference voltage, the LT8228 starts switching and the input and output current limits are increased to the values set by the R_{SET1P} and R_{SET2P} resistors respectively.

In boost mode, the LT8228 limits the V_2 input and the V_1 output current by regulating the ISET2N and ISET1N pin voltages respectively to the lower of the SS pin voltage and the internal reference voltage of 1.21V typically. Similar to the buck mode, the SS pin programs a soft-start when connecting an external capacitor, C_{SS}, from the SS pin to ground. When the LT8228 is enabled, after the DRV_{CC} and $INTV_{CC}$ voltages exceed their undervoltage thresholds, after the internal diagnostics are successfully completed, DG2 pin is charged with a 10µA pull-up current. If dual MOSFET configuration is used at the V_2 terminal, inrush current is controlled through C_{DG2} and V_{2D} is charged to V_2 as DG2 voltage exceeds it undervoltage threshold. If single MOSFET configuration is used, V_{2D} is a forward diode drop away from V_2 at start-up and charged to V_2 as DG2 rises. Charging V_{2D} also charges V1D through the body diode of TG MOSFET M3 and inductor. As the DG2 charging continues past its undervoltage threshold, V1D is higher than V_2 due to the residual current of inductor and reverse current prevention by the body diode of the TG MOSFET M3. Next DG1 starts charging and the output current is limited through DG1 by regulating the ISET1N pin voltage to 1.4V. In addition, the LT8228 includes an adjustable fault timer to protect the V_1 protection MOSFETs from excessive power dissipation damage. Refer to the V1 Protection MOSFET Controller Operation section for more details. After DG1 voltage exceeds its threshold voltage, an internal 10µA pull-up current charges the C_{SS} capacitor and creates a voltage ramp on the SS pin. As the SS voltage rises linearly from 0V to the internal reference voltage, the LT8228 starts switching and the input and output current limits are increased to the values set by the R_{SET2N} and R_{SET1N} resistors respectively.

When the LT8228 is disabled, or a fault is detected (refer to the Fault Conditions in Applications Information section for all the fault conditions), the LT8228 stops switching and the SS pin is actively pulled low by an internal MOSFET to reset the soft-start.

PARALLELING MULTIPLE CONTROLLERS (ISHARE AND IGND)

The LT8228 provides masterless fault tolerant output current sharing among multiple LT8228s in parallel, enabling higher load current, better heat management and redundancy. Each LT8228 regulates to the average output current eliminating the need for a master controller. When an individual LT8228 is disabled or in a fault condition, it stops contributing to the average bus, making the current sharing scheme fault tolerant. When multiple LT8228s are in parallel, all the DRXN pins are tied together to operate all LT8228s in the same regulation mode.

In buck mode when DRXN is high, the ISHARE pin outputs a current equal to the current out of the ISET2P pin which represents V_2 output current. In boost mode when

OPERATION

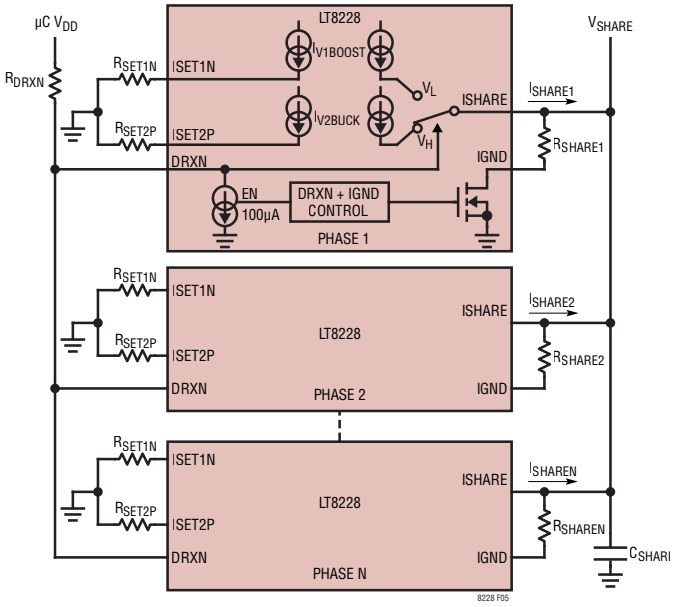


Figure 5. ISHARE and IGND Connection

DRXN is low, the ISHARE pin outputs a current equal to the current out of the ISET1N pin which represents V_1 output current. Each LT8228 contributes this current into the common ISHARE node. When paralleling, the ISHARE pins of all the LT8228s are tied together as shown in Figure 5. For each LT8228, a local resistor R_{SHARE} is connected from the ISHARE pin to its own IGND pin. Connect a filtering capacitor between the ISHARE pin and ground for average current regulation. The voltage at the common ISHARE node V_{SHARE} is found according to Equation 14.

$$V_{SHARE} = \frac{\sum_{n=1}^{N} I_{SHAREn}}{\sum_{n=1}^{N} \frac{1}{R_{SHAREn}}} \quad (14)$$

When all the R_{SHARE} resistors are equal, VS_{HARE} represents the average output current I_{OUTAVG} as shown in Equation 15.

$$I_{OUTAVG} = \frac{1}{N} \sum_{n=1}^{N} I_{SHAREn}$$
$$I_{SHARE} = \frac{R_{SHARE}}{N} \sum_{n=1}^{N} I_{SHAREn} = I_{OUTAVG} \bullet R_{SHARE} \quad (15)$$

In buck mode, ISET2P pin voltage regulates to the ISHARE pin voltage. To regulate each LT8228's V_2 output current to the average output current, make R_{SET2P} and R_{SHARE} equal. In boost mode, ISET1N pin voltage regulates to the ISHARE pin voltage. To regulate each LT8228's V_1 output current to the average output current, make R_{SET1N} and R_{SHARE} values equal. If R_{SET2P} and R_{SET1N} are set at different values, change the value of R_{SHARE} based on the mode of operation defined by the DRXN pin.

When the LT8228 is enabled and the internal diagnostic routine is passed, the IGND pin connects R_{SHARE} to ground through a typically 120Ω switch. During shutdown or a faulted condition, ISHARE stops generating current and the switch at the IGND pin is opened so that no current flows through the current sharing resistor. This disconnects the R_{SHARE} resistor from the V_{ISHARE} node so that V_{ISHARE} continues to represent the average output current of the remaining active LT8228's in parallel. With this scheme, any paralleled LT8228 can be added or subtracted without affecting current sharing accuracy. The IGND pin along with the ISHARE pin provides current sharing that is masterless as well as fault tolerant. Refer to the Paralleling Multiple LT8228s in Applications Information section for more information.

BIAS SUPPLY AND V_{CC} REGULATORS

Power for the top and bottom N-channel MOSFET drivers comes from the DRV_{CC} pin. An internal LDO (low-dropout linear regulator) supplies 10V to DRV_{CC} from the BIAS pin. Another internal LDO generates 4V at the $INTV_{CC}$ pin from DRV_{CC}. The $INTV_{CC}$ LDO supplies the internal low-voltage start-up and regulation circuitry. To enable the LT8228, a minimal 8V BIAS supply is needed. If no external voltage source is available, BIAS can be connected to either V_1 or V_2 or both diode-ORed for redundancy. If the BIAS supply experiences negative voltage, place a diode in series. Attention should be made to the power dissipation inside the controller by supplying BIAS with a lower voltage supply if available.

OPERATION

STRONG GATE DRIVERS

The LT8228 contains very low impedance drivers capable of supplying amperes of current to slew large N-channel MOSFET gates quickly. These strong drivers minimize transition losses and allow paralleling MOSFETs for higher current applications. A 100V capable floating high side gate driver controls the top MOSFET M2 and a low side gate driver drives the bottom MOSFET M3. The DRV_{CC} LDO directly supplies the bottom side gate drive circuitry. The top gate drivers are biased from the floating bootstrap capacitor, C_{BST}, which is recharged during each bottom gate off cycle through an external diode from DRV_{CC}. In low dropout conditions where it is possible that the bottom MOSFET will be off for an extended period, an internal timeout guarantees that the bottom MOSFET is turned on at least once every 50µs to refresh C_{BST} typically.

FREQUENCY SELECTION, SPREAD SPECTRUM AND PHASE-LOCKED LOOP (RT AND SYNC)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing N-channel MOSFET switching losses but requires larger inductance and/or capacitance to maintain low output ripple voltage. The switching frequency of the LT8228 gate drive controllers is selected using the RT pin. If the SYNC pin is not being driven by an external clock source, the RT pin can be used to program the controller's operating frequency from 80kHz to 600kHz. A single resistor from the RT pin to ground determines the switching frequency. The controller regulates the RT pin voltage to 800mV. The regulated current through the RT resistor commands a specific frequency. See the Applications Information section for the method of selecting RT for a fixed frequency.

An integrated phase-locked loop (PLL) and filter network synchronizes the internal oscillator to an external clock source driving the SYNC pin. The PLL locks to any frequency in the range of 80kHz to 600kHz. The frequency setting resistor R_{RT} must always be present to (1) set the controller's initial switching frequency before locking to the external clock and (2) provide a default switching frequency if the external clock source is no longer present.

Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. To improve the EMI performance, the LT8228 includes the ability to spread out the frequency spectrum of the external N-channel MOSFETs. This spreading feature is only available when the frequency of the controller is set by the RT pin. Setting the SYNC pin to logic high typically above 1V will activate the spread spectrum capability. If enabled, the spread spectrum feature modulates the internal clock frequency ±30% of the full-scale value programmed by the RT pin resistor. To disable the spread spectrum feature, connect SYNC to ground.

$\overline{\text{FAULT}}$ MONITORING AND $\overline{\text{REPORT}}$ FEATURE

The LT8228 provides internal and external fault monitoring and reporting. The part checks and reports the functionality of the error amplifiers, current sense amplifiers and the oscillator at start-up while the internal reference, temperature, internal regulators and DG pin voltages are checked and reported continuously. See the FAULT Conditions and $\overline{\text{REPORT}}$ Feature in the Applications Information section for full list of all the external faults. If the controller detects any fault, switching stops, $\overline{\text{FAULT}}$ pin is pulled and low and the failure is reported at the $\overline{\text{REPORT}}$ pin. The $\overline{\text{REPORT}}$ pin uses the SYNC pin as its data clock. Therefore, the report functionality is only available when the LT8228 is syncing to an external clock. The continuous monitoring and the reporting function allow the controller to improve the safety rating of the system it is used in. Refer to the Applications Information section for more details.

APPLICATIONS INFORMATION

INTRODUCTION

The Applications Information section serves as a guideline for selecting external component based on the details of the application. For this section, refer to the typical application circuit in the front page and the Block Diagram section. Component selection typically follows the approach described below.

1. Switching frequency (f_{SW}) and Inductor value (L) are chosen to optimize efficiency, physical size and cost.
2. The inductor current sense resistor R_{SNS2} along with its input gain resistors R_{IN2} are selected for peak inductor current limit, efficiency and current sense accuracy.
3. The buck output current limit, boost input current limit, and V_2 current monitor are set by the R_{SET2P}, R_{SET2N} and R_{MON2} resistors respectively. The V_1 current sense resistor R_{SNS1} along with its input gain resistors R_{IN1} is selected to optimize efficiency and current sense accuracy. Then the boost output current limit, buck input current limit, and V_1 current monitor are set by the R_{SET1N}, R_{SET1P} and R_{MON1} resistors respectively. Capacitors parallel to the R_{SET} resistors are selected to set the current limits to the average current of the current sense resistors.
4. The regulation voltages and overvoltage thresholds of V1D and V_{2D} are set by selecting the resistive dividers to the FB1 and FB2 pins. The undervoltage threshold of V_1 and V_2 are set by selecting the resistive dividers to the UV1 and UV2 pins.
5. MOSFETs (M1, M2, M3 and M4) are selected based on efficiency and breakdown voltage considerations. Schottky diodes (D2 and D3) (optional) are selected based on efficiency consideration. Top MOSFET driver supply (C_{BST}, D_{BST}) are selected to store adequate charge to drive the top MOSFET.
6. The capacitor C_{DM2} is chosen to optimize the buck input and boost output ripple voltage and thermal requirements. Likewise, the capacitor C_{DM4} is chosen to optimize the boost input and buck output ripple voltage and thermal requirements. The capacitor C_{DM1} at V1D pin is used to bypass noise. The dampening capacitor C_{V1} and C_{V2} are selected with their ESR to reduce the resonance due to series wire inductance connected to V_1 and V_2 respectively.
7. The compensations for the buck and boost regulation loops are chosen to optimize bandwidth and stability.
8. Inrush current control limits are set by choosing C_{DG1} and C_{DG2}. R_{DG1} is set to compensate boost mode output current limit loop when V1D is higher than V_1.
9. C_{SS} is selected to set soft-start behavior.

The examples and equations in this section assume continuous conduction mode unless otherwise noted. All electric characteristics referred to in this section represent typical values unless otherwise specified.

PROGRAMMING THE SWITCHING FREQUENCY

The RT frequency adjust pin allows the user to program the switching frequency from 80kHz to 600kHz to optimize efficiency/performance and external component size. Higher frequency operation yields smaller component size but increases switching losses and gate driving current and may not allow sufficiently high or low duty cycle operation. Lower frequency operation gives better performance at the cost of larger external component size. For an appropriate R_T resistor value see Table 1. An external resistor from the RT pin to ground is required. Do not leave this pin open. Refer to the RT Pin Resistance vs Switching Frequency curve in the Typical Performance Characteristics section.

Table 1. RT Pin Resistance vs Switching Frequency

R_{RT} (k)	f_{PROG} (kHz)	R_{RT} (k)	f_{PROG} (kHz)	R_{RT} (k)	f_{PROG} (kHz)
124	81	61.9	158	30.9	303
110	91	57.6	169	28.7	325
100	100	53.6	181	26.7	347
97.6	102	51.1	190	24.3	378
82.5	120	48.7	199	22.6	403
78.7	126	43.2	222	20.0	450
75.0	132	40.2	238	17.8	499
69.8	141	38.3	249	15.8	552
64.9	151	34.0	278	14.0	604

APPLICATIONS INFORMATION

FREQUENCY SYNCHRONIZATION AND SPREAD SPECTRUM

The LT8228 switching frequency can be synchronized to an external clock using the SYNC pin. The rising edge of the external clock signal is synced with the turn-on of the top MOSFET in forward buck mode or bottom MOSFET in reverse boost mode. Driving SYNC with a 50% duty cycle waveform is strongly recommended, otherwise maintain the duty cycle between 5% and 95%. When there is no clock signal at the SYNC pin, it is used as the enable pin for spread spectrum. If there is a logic high DC signal at the SYNC pin, spread spectrum is enabled. The threshold for logic high is 1V. The spread spectrum feature modulates the internal clock frequency between ±30% of the base frequency set by the RT pin resistor. At logic low signal at the SYNC pin, the controller operates with the frequency set by RT pin without any spread spectrum. The threshold for logic low signal is 0.5V.

INDUCTOR SELECTION

The selection of the LT8228's inductor value is driven by a trade-off between component size, efficiency and operating frequency of the system. The inductor value has a direct effect on its ripple current. Lower ripple current reduces core losses in the inductor, ESR losses in the capacitors and output ripple voltage. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor.

A reasonable starting point is to choose a peak-to-peak ripple current that is 20% to 40% of the maximum average current of the inductor. Due to the bidirectional capability of the LT8228, the same inductor is used for both buck and boost regulation. In buck mode, the inductor current is the V_2 output current and in boost mode, the inductor current is the V_2 input current. For a given inductor ripple current, the minimum inductor value in buck and boost mode for their respective maximum average current is given by Equation 16.

$$L_{BUCK} > \frac{V_2 \bullet (V_{1(MAX)} - V_2)}{f \bullet \Delta I_L \bullet V_{1(MAX)}}$$
$$L_{BOOST} > \frac{V_2 \bullet (V_1 - V_2)}{f \bullet \Delta I_L \bullet V_1} \quad (16)$$

where f is switching frequency and Δ_{IL} is the inductor ripple current. For buck mode operation, the maximum ripple current occurs when the input voltage V_1 is highest. For boost mode operation, the maximum ripple occurs when the input voltage V_2 is half of the output voltage V_1. For bidirectional operation, the chosen inductor value should satisfy both minimum conditions set by the buck and boost modes.

In addition to ripple requirements, the inductance should be large enough to prevent subharmonic oscillations. In a current mode regulator, the current sense loop creates a double pole at half the switching frequency which can degrade system stability when its quality factor (QCS) is much greater than 1.0. The current sense loop damping is a function of the slopes of the inductor current and the internal slope compensating ramp. Lowering the inductance increases QCS, and a sufficiently undersized inductor will result in subharmonic oscillation for duty cycles above 50% The minimum inductance for subharmonic stability is given by Equation 17.

$$L_{SUBHARMONIC,MIN} > 2 \bullet 10^5 \bullet \frac{R_{SNS2}}{R_{IN2}} \bullet \frac{1}{f_{SW}} \quad (17)$$

The LT8228 slope compensation scheme is designed to provide single-cycle settling of the current sense loop (QCS = 0.637) when the inductor value is twice the minimum for subharmonic stability. This simplifies loop compensation as the current sense loop damping becomes independent of duty cycle and switching region. Selecting $L_{OPTIMAL}$ also optimizes line regulation and line step response performance (see Equation 18).

$$L_{OPTIMAL} > 4 \bullet 10^5 \bullet \frac{R_{SNS2}}{R_{IN2}} \bullet \frac{1}{f_{SW}} \quad (18)$$

If V_2 is higher than 50V in buck mode or the difference between V1D and V_2 is higher than 50V in boost mode, the optimal inductor value is higher than the value stated in the equation. Increase the inductor value by the same percentage increase in V_2 in buck mode or in the difference between V1D and V_2 after 50V to get the optimal value.

APPLICATIONS INFORMATION

For high efficiency, choose an inductor with low core loss. Also, the inductor should have low DC resistance to reduce the I^2R losses and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a shielded inductor.

R_{SNS2} AND R_{IN2} SELECTION FOR PEAK INDUCTOR CURRENT

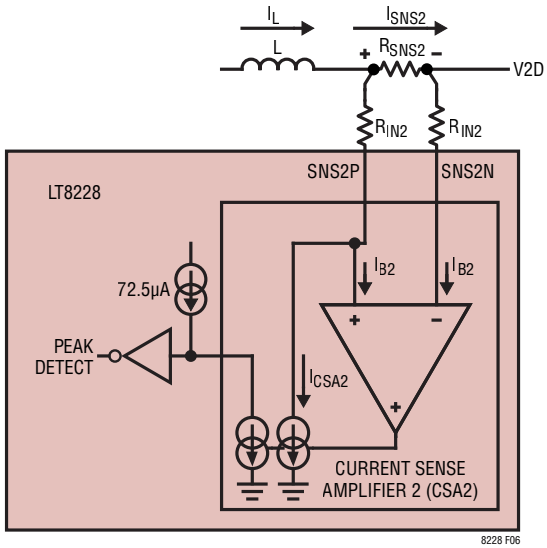
The LT8228 sets the peak inductor current by selecting the current sense resistor R_{SNS2} and the input gain resistors R_{IN2}. To select a peak inductor current, start with finding the maximum current in the inductor. The LT8228 uses the same inductor for both the buck and boost mode operation. In buck mode, inductor current is the V_2 output current and in boost mode, the inductor current is the V_2 input current. For maximum inductor current in each mode, add the maximum average current and half the maximum peak-to-peak ripple current as shown in Equation 19.

$$I_{LMAXBUCK} = I_{V2P(LIM)} + \frac{1}{2}\frac{V_2 \bullet (V_{1(MAX)} - V_2)}{f \bullet L \bullet V_{1(MAX)}}$$

$$I_{LMAXBOOST} = I_{V2N(LIM)} + \frac{1}{2}\frac{V_2 \bullet (V_1 - V_2)}{f \bullet L \bullet V_1} \quad (19)$$

where f is the switching frequency, L is the selected inductor value, $I_{V2P(LIM)}$ is the buck mode V_2 output current limit and $I_{V2N(LIM)}$ is the boost mode V_2 input current limit. ADI recommends setting the peak inductor current at least 20% to 30% above the higher maximum inductor current of the buck and boost modes. This ensures the maximum average current regulation is not affected by the peak inductor current limit in either mode of operation.

The inductor current is sensed using R_{SNS2} which is placed in series with the inductor. Current sense polarity is positive when current flows from the inductor to V_{2D}. Input gain resistors R_{IN2} are placed between R_{SNS2} and the positive and negative sense pins, SNS2P and SNS2N of the V_2 bidirectional current sense amplifier CSA2 as shown in Figure 6. The figure shows the circuit operation



$$I_{SNS2} = I_L - (I_{B2} + I_{CSA2})$$

$$I_{B2} = \begin{cases} 90\mu A \text{ FOR } V_{SNS2P} > 2.5V \\ -50\mu A \text{ FOR } V_{SNS2P} = 0V \end{cases}$$

$$I_{CSA2} = \frac{I_{SNS2} \bullet R_{SNS2}}{R_{IN2}}$$

$$I_{L(PEAK)} = \frac{R_{IN2} \bullet 72.5\mu A}{R_{SNS2}} \text{ FOR } I_L >> I_{B2} = I_{CSA2}$$

Figure 6. V_2 Current Sense Amplifier Operation for Positive Inductor Current

of CSA2 for positive inductor current. When there is no inductor current, both sense pins draw equal bias currents I_{B2} through R_{IN2}. As inductor current flows through R_{SNS2}, CSA2 draws feedback current I_{CSA2} to servo the SNS2P pin to the SNS2N pin voltage. The current through R_{SNS2} is equal to the inductor current for inductor currents much larger than CSA2's bias and feedback currents. The peak inductor current $I_{L(PEAK)}$ is detected when I_{CSA2} reaches 72.5µA typically. When the current through the sense resistor reverses direction, the current sense amplifier is reconfigured to draw feedback current to servo the SNS2N pin to the SNS2P pin voltage. As a result, the peak inductor current is same in both buck and boost mode of operation.

High R_{SNS2} values improve current sense accuracy while low R_{SNS2} values improve efficiency. Input referred offset voltage of CSA2 is guaranteed across temperature to ±0.5mV at 50µA feedback current. Maximum power loss occurs at the peak inductor current. Select the value of R_{SNS2} so that the input referred offset voltage does not

APPLICATIONS INFORMATION

affect current sense accuracy while minimizing power loss. ADI recommends a R_{SNS2} value that sets the voltage across R_{SNS2} at the peak inductor current between 50mV to 200mV. The power dissipation at the current sense amplifier should not exceed its power rating for all operating conditions.

Next, select R_{IN2} to set the peak inductor current limit according to Equation 20.

$$R_{IN2} = \frac{I_{L(PEAK)} \bullet R_{SNS2}}{72.5\mu A} \quad (20)$$

The typical bias current into the SNS2P and SNS2N pins is 90µA. For input common mode voltage lower than 2.5V, the bias currents decrease and reverse polarity. When the input common mode voltage reaches 0V, the typical bias current is –50µA. Refer to the Input Bias Current curve in the Typical Performance Characteristics section for more information.

The current sense resistor R_{SNS2} and input gain resistors R_{IN2} are also used to sense the V_2 output current in buck mode and V_2 input current in boost mode. In buck mode, the sensed V_2 output current is generated out of the ISET2P and IMON2 pins for output current regulation and monitoring. In boost mode, the sensed V_2 input current is generated out of the ISET2N, ISHARE and IMON2 pins for output current regulation, sharing and monitoring. Refer to the ISET2P, ISET2N, ISHARE and IMON2 gain error curves in the Typical Performance Characteristics section for more information.

Additionally, the current sense resistor R_{SNS2} and input gain resistors R_{IN2} are used to sense BG or TG MOSFET short fault. During such short faults, the current through R_{SNS2} is higher than peak current. A short fault current is detected when I_{CSA2} reaches 105µA typically. Anytime such a fault is detected through R_{SNS2} , the LT8228 shuts down all four external N-channel MOSFETs, pulls the SS pin low, asserts the $\overline{FAULT}$ pin, IGND goes high impedance and reports the status at the $\overline{REPORT}$ pin. The part restarts after waiting 1024 switching clock cycles.

The CSA2 is internally compensated. Any capacitive load at the SNS2P and SNS2N affects the feedback compensation of the amplifier and makes it unstable.

R_{SET2P} SELECTION FOR V_2 OUTPUT CURRENT LIMIT (BUCK MODE)

In buck mode, V_2 output current limit is programmed by connecting a resistor R_{SET2P} from ISET2P to ground. The V_2 current sense amplifier CSA2 outputs current at the ISET2P pin that is proportional to the current ISNS2 flowing through the sense resistor R_{SNS2} as shown in Figure 7. The current through the sense resistor is equal to the V_2 output current for V_2 output currents much higher than CSA2's input bias current as stated in the R_{SNS2} and R_{IN2} Selection for Peak Inductor Current section.

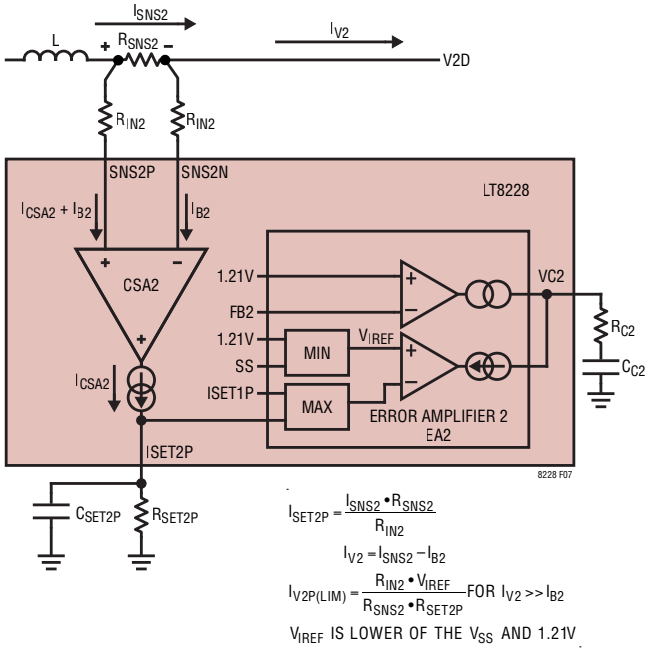


Figure 7. V_2 Input Current Limit Programming at ISET2P

During current limit, the LT8228 regulates the voltage at the ISET2P pin to the typical internal reference voltage of 1.21V. For V_2 output current limit $I_{V2P(LIM)}$, calculate R_{SET2P} according to Equation 21.

$$R_{SET2P} = \frac{R_{IN2} \bullet 1.21V}{R_{SNS2} \bullet I_{V2P(LIM)}} \quad (21)$$

For example, if the values of R_{SNS2} and R_{IN2} set to 2mΩ and 1.5k respectively, setting R_{SET2P} to 22.6k programs the V_2 output current limit to 40.1A. During current limit, current out of the ISET2P pin is 53.5µA.

APPLICATIONS INFORMATION

The current at the ISET2P pin represents the inductor current. To ensure the current limit is set to the desired average current, a parallel capacitor C_{SET2P} to R_{SET2P} is required. The parallel capacitor C_{SET2P} reduces the ripple voltage at the ISET2P pin and duty cycle jitter due to noise. The capacitor C_{SET2P} should not be arbitrarily large as it will affect the stability of the current regulation loop. Stability of the current regulation loop is discussed in detail in the Regulation Loop and Stability section.

For applications such as battery charging and discharging, the V_2 output current limit is set according to the charge current requirement. If V_2 is connected to a current or resistive load, set the V_2 output current limit 10% to 20% above the maximum load current to allow for large transient events and $I_{V2P(LIM)}$ threshold variations. Dynamic current control can also be achieved through modulating the ISET2P pin resistance. Some dynamic methods include digital potentiometers or modulating the ground node of the ISET2P resistor using a DAC or injecting and subtracting current from the ISET2P node.

R_{SET2N} SELECTION FOR V_2 INPUT CURRENT LIMIT (BOOST MODE)

In boost mode, V_2 input current limit is programmed by connecting a resistor R_{SET2N} from ISET2N to ground. The V_2 current sense amplifier CSA2 outputs current at the ISET2N pin that is proportional to the current ISNS2 flowing through the sense resistor R_{SNS2} as shown in Figure 8. The current through the sense resistor is equal to the V_2 input current for V_2 input currents much higher than CSA2's input bias and feedback currents as stated in the Peak Inductor Current section.

During current limit, the LT8228 regulates the voltage at the ISET2N pin to the typical internal reference voltage of 1.21V. For V_2 input current limit $I_{V2N(LIM)}$, calculate R_{SET2N} according to Equation 22.

$$R_{SET2N} = \frac{R_{IN2} \bullet 1.21V}{R_{SNS2} \bullet I_{V2N(LIM)}} \quad (22)$$

For example, if the values of R_{SNS2} and R_{IN2} set to 2mΩ and 1.5k respectively, setting R_{SET2N} to 22.6k programs the V_2 input current limit to 40A. During current limit, current out of the ISET2N pin is 53.5µA.

The current at the ISET2N pin represents the inductor current. To ensure the current limit is set to the desired average current, a parallel capacitor C_{SET2N} to R_{SET2N} is required. The parallel capacitor C_{SET2N} reduces the ripple voltage at the ISET2N pin and duty cycle jitter due to noise. The capacitor C_{SET2N} should not be arbitrarily large as it will affect the stability of the current regulation loop. Stability of the current regulation loop is discussed in detail in the Regulation Loop and Stability section.

For applications such as battery charging and discharging, the V_2 input current limit is set according to the discharge current requirement. If V_1 is connected to a current or resistive load, set the V_2 input current limit 10% to 20% above the maximum input current required to provide the maximum load current at V_1 to allow for large transient events and $I_{V2N(LIM)}$ threshold variations. Dynamic current control can also be achieved through modulating the ISET2N pin resistance. Some dynamic methods include digital potentiometers or modulating the ground node of the ISET2N resistor using a DAC or injecting and subtracting current from the ISET2N node.

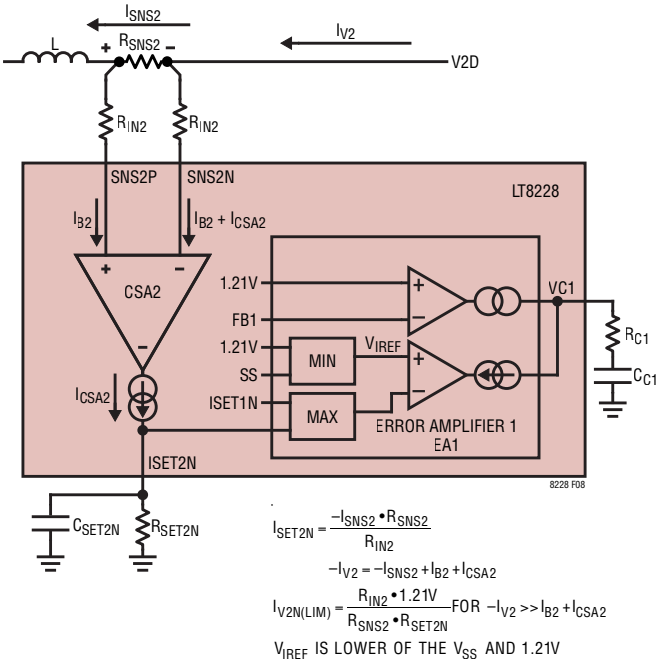


Figure 8. V2 Input Current Limit Programming at ISET2N

APPLICATIONS INFORMATION

R_{MON2} SELECTION FOR V_2 CURRENT MONITORING

The current out of IMON2 pin is equal to the absolute voltage across the current sense resistor R_{SNS2} divided by the value of the input sense resistor R_{IN2} as shown in Figure 9. This current represents V_2 output current in buck mode and V_2 input current in boost mode. Connecting a resistor R_{MON2}, from IMON2 to ground generates a voltage V_{MON2} for monitoring by an ADC. The maximum output voltage $V_{MON2MAX}$ is typically set to be between 80% to 90% of the ADC input dynamic range. Limit $V_{MON2MAX}$ to less than 2.5V. Calculate the value of R_{MON2} with Equation 23.

$$R_{MON2} = \frac{R_{IN2}}{I_{SNS2MAX} \bullet R_{SNS2}} V_{MON2MAX} \quad (23)$$

where $I_{SNS2MAX}$ is the greater of the programmed V_2 output current limit $I_{V2P(LIM)}$ in buck mode and the programmed V_2 input current limit $I_{V2N(LIM)}$ in boost mode. A filtering capacitor C_{MON2} can be added to reduce ripple voltage at the IMON2 pin.

For positive current through R_{SNS2} , V_2 output current is less by CSA2's bias current. For negative current through R_{SNS2}, V_2 input current is greater by CSA2's bias and feedback currents. As a result, for low V_2 currents, CSA2's bias and feedback currents introduce error to the current monitor output IMON2.

R_{SNS1} AND R_{IN1} SELECTION

The V_1 current sense resistor R_{SNS1} and input gain resistor RIN1 are used to sense the V_1 input current in buck mode and V_2 output current in boost mode. R_{SNS1} is placed between V1D and the drain of the top MOSFET. The V_1 current sense amplifier CSA1 operates similarly as the V_2 current sense amplifier as shown in Figure 10. For positive current through R_{SNS1}, CSA1 draws feedback current I_{CSA1} to servo the SNS1P pin to the SNS1N pin voltage. For negative current, CSA1 draws feedback current to servo the SNS1N pin to the SNS1P pin voltage. The current through R_{SNS1} is equal to V_1 current for V_1 currents much larger than CSA1's bias and feedback currents.

The typical bias current into the SNS1P and SNS1N pins is 90µA. For input common mode voltage lower than 2.5V, the bias currents decrease and reverse polarity. When the input common mode voltage reaches 0V, the typical bias current is –50µA. Refer to the Input Bias Current curve in the Typical Performance Characteristics section for more information.

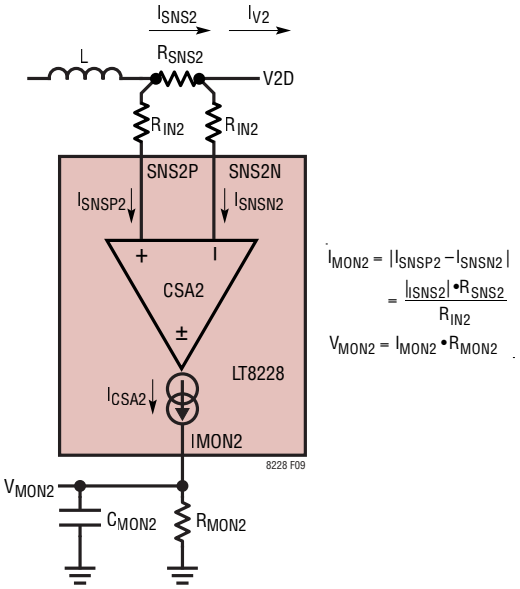


Figure 9. V_1 V_2 Current Monitoring at IMON2

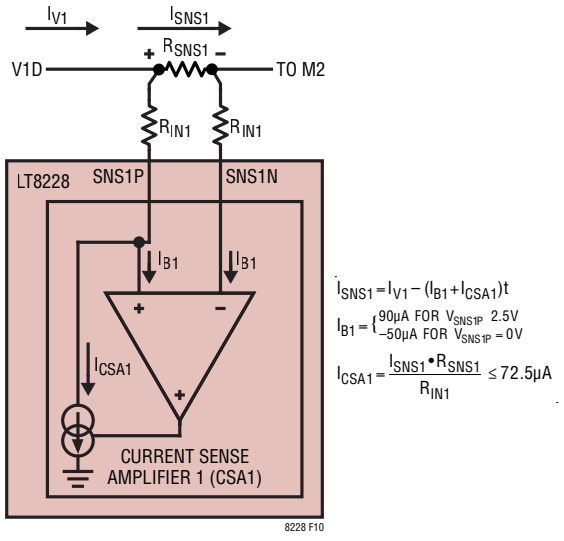


Figure 10. V_1 Current Sense Amplifier Operation for Positive Current

APPLICATIONS INFORMATION

In buck mode, CSA1's feedback current is generated out of the ISET1P and IMON1 pins for input current regulation and monitoring. In boost mode, CSA1's feedback current is generated out of the ISET1N, ISHARE and IMON1 pins for output current regulation, sharing and monitoring. Refer to the ISET1P, ISET1N, ISHARE and IMON1 gain error curves in the Typical Performance Characteristics section for more information.

High R_{SNS1} values improve current sense accuracy while low R_{SNS1} values improve efficiency. Input referred offset voltage of CSA1 is guaranteed across temperature to ±0.5mV at 50µA feedback current. Select the value of R_{SNS1} so that the input referred offset voltage does not affect current sense accuracy while minimizing power loss. The current through R_{SNS1} is discontinuous in both buck and boost mode. the voltage across R_{SNS1} is highest at the peak inductor current. However, power loss at the sense resistor depends on the peak inductor current, power stage duty ratio, and the capacitors at the R_{SNS1} terminals. ADI recommends a R_{SNS1} value that sets the maximum voltage across R_{SNS1} to a value between 50mV to 200mV. The power dissipation at the current sense amplifier should not exceed its power rating for all operating conditions.

Next, select R_{IN1} to set the gain of the V_1 current sense amplifier to maintain the following condition for current sense accuracy (see Equation 24).

$$R_{IN1} > \frac{I_{SNS1(MAX)} \bullet R_{SNS1}}{72.5\mu A} \quad (24)$$

Additionally, the current sense resistor R_{SNS1} and input gain resistors R_{IN1} are used to sense BG or TG MOSFET short fault. A short fault current is detected when I_{CSA1} reaches 120µA typically. Anytime such a fault is detected through R_{SNS1}, the LT8228 shuts down all four external N-channel MOSFETs, pulls the SS pin low, asserts the $\overline{FAULT}$ pin, IGND goes high impedance and reports the status at the $\overline{REPORT}$ pin. The part restarts after waiting 1024 switching clock cycles. The CSA1 is internally compensated. Any capacitive load at the SNS1P and SNS1N affects the feedback compensation of the amplifier and makes it unstable.

R_{SET1P} SELECTION FOR V_1 INPUT CURRENT LIMIT (BUCK MODE)

In buck mode, V_1 input current limit is programmed by connecting a resistor R_{SET1P} from ISET1P to ground. The V_1 current sense amplifier CSA1 outputs current at the ISET1P pin that is proportional to the current ISNS1 flowing through the sense resistor R_{SNS1} as shown in Figure 11. The current through the sense resistor is equal to the V_1 input current for V_1 input currents much higher than CSA1's input bias and feedback currents as stated in the R_{SNS1} and R_{IN1} Selection section.

During current limit, the LT8228 regulates the voltage at the ISET1P pin to the typical internal reference voltage of 1.21tV. For V_1 output current limit $I_{V1P(LIM)}$, calculate R_{SET1P} according to Equation 25.

$$R_{SET1P} = \frac{R_{IN1} \bullet 1.21V}{R_{SNS1} \bullet I_{V1P(LIM)}} \quad (25)$$

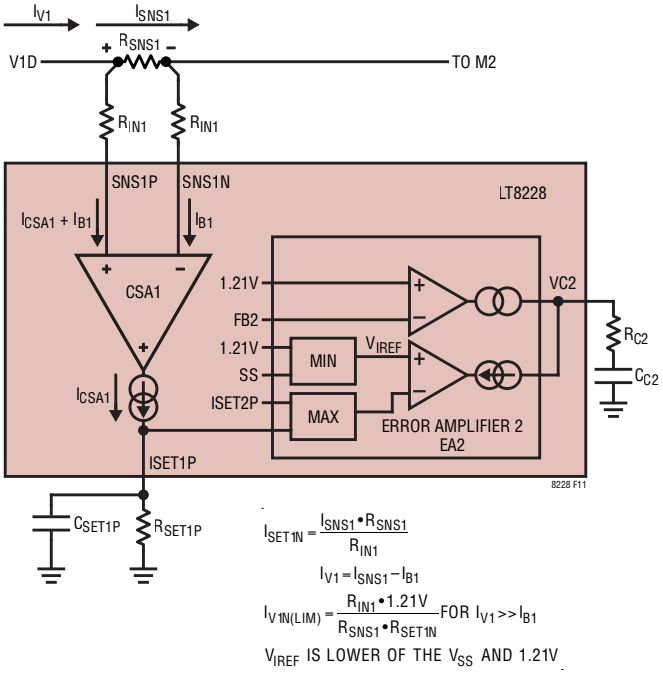


Figure 11. V_1 Output Current Limit Programming at ISET1P

APPLICATIONS INFORMATION

For example, if the values of R_{SNS1} and R_{IN1} set to 2mΩ and 1.5k respectively, setting R_{SET1P} to 37.4k programs the V_1 input current limit to 24.3A. During current limit, current out of the ISET1P pin is 32.4µA.

The current at the ISET1P pin represents the inductor when the top MOSFET is on during switching. The current is discontinuous with high slew rate. To ensure the current limit is set to the desired average current, a parallel capacitor C_{SET1P} to R_{SET1P} is required. The parallel capacitor C_{SET1P} reduces the ripple voltage at the ISET1P pin and duty cycle jitter due to noise. The capacitor C_{SET1P} should not be arbitrarily large as it will affect the stability of the current regulation loop. Stability of the current regulation loop is discussed in detail in the Regulation Loop and Stability section.

For applications such as battery charging and discharging, the V_1 input current limit is set according to the discharge current requirement. If V_2 is connected to a current or resistive load, set the V_1 input current limit 10% to 20% above the maximum input current required to provide the maximum load current at V_2 to allow for large transient events and $I_{V1P(LIM)}$ threshold variations. Dynamic current control can also be achieved through modulating the ISET1P pin resistance. Some dynamic methods include digital potentiometers or modulating the ground node of the ISET1P resistor using a DAC or injecting and subtracting current from the ISET1P node.

R_{SET1N} SELECTION FOR V_1 OUTPUT CURRENT LIMIT (BOOST MODE)

In buck mode, V_1 output current limit is programmed by connecting a resistor R_{SET1N} from ISET1N to ground. The V_1 current sense amplifier CSA1 outputs current at the ISET1N pin that is proportional to the current ISNS1 flowing through the sense resistor R_{SNS1} as shown in Figure 12. The current through the sense resistor is equal to the V_1 output current for V_1 output currents much higher than CSA1's input bias current as stated in the R_{SNS1} and R_{IN1} Selection section.

During current limit, the LT8228 regulates the voltage at the ISET1N pin to the typical internal reference voltage of 1.21V. For V_1 input current limit $I_{V1N(LIM)}$, calculate R_{SET1N} according to Equation 26.

$$R_{SET1N} = \frac{R_{IN1} \bullet 1.21V}{R_{SNS1} \bullet I_{V1N(LIM)}} \quad (26)$$

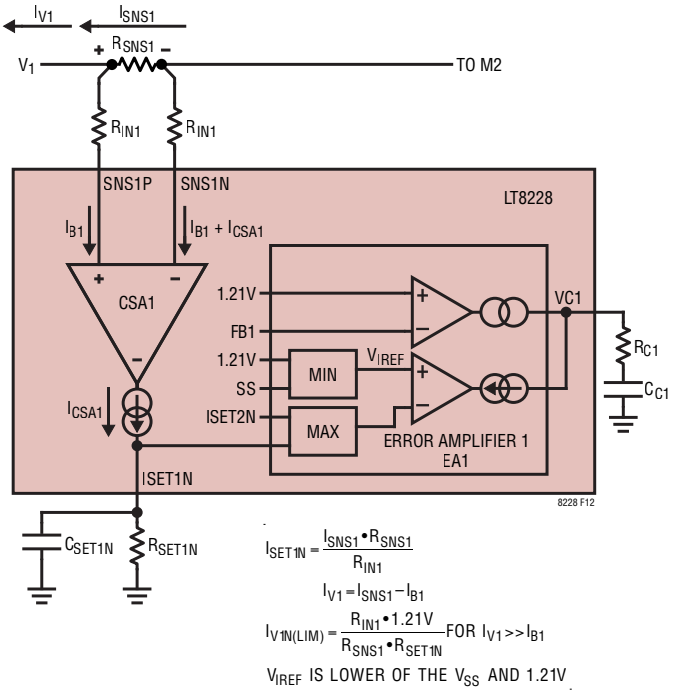


Figure 12. V_1 Output Current Limit Programming at ISET1N

For example, if the values of R_{SNS1} and R_{IN1} set to 2mΩ and 1.5k respectively, setting R_{SET1N} to 88.7k programs the V_1 output current limit to 10.2A. During current limit, current out of the ISET1N pin is 13.6µA.

The current at the ISET1N pin represents the inductor when the top MOSFET is on during switching. The current is discontinuous with high slew rate. To ensure the current limit is set to the desired average current, a parallel capacitor C_{SET1N} to R_{SET1N} is required. The parallel capacitor C_{SET1N} reduces the ripple voltage at the ISET1N pin and duty cycle jitter due to noise. The capacitor C_{SET1N} should not be arbitrarily large as it will affect the stability of the current regulation loop. Stability of the current regulation loop is discussed in detail in the Regulation Loop and Stability section.

APPLICATIONS INFORMATION

For applications such as battery charging and discharging, the V_1 output current limit is set according to the charge current requirement. If V_1 is connected to a current or resistive load, set the V_1 output current limit 10% to 20% above the maximum load current to allow for large transient events and $I_{V1P(LIM)}$ threshold variations. Dynamic current control can also be achieved through modulating the ISET1N pin resistance. Some dynamic methods include digital potentiometers or modulating the ground node of the ISET1N resistor using a DAC or injecting and subtracting current from the ISET1N node.

R_{MON1} SELECTION FOR V_1 CURRENT MONITORING

The current out of IMON1 pin is equal to the absolute voltage across the current sense resistor R_{SNS1} divided by the value of the input sense resistor R_{IN1} as shown in Figure 13. This current represents V_1 input current in buck mode and V_1 output current in boost mode. Connecting a resistor R_{MON1}, from IMON1 to ground generates a voltage V_{MON1} for monitoring by an ADC. The maximum output voltage $V_{MON1MAX}$ is typically set to be between 80% to 90% of the ADC input dynamic range. Limit $V_{MON1MAX}$ to less than 2.5V. Calculate the value of R_{MON1} with Equation 27.

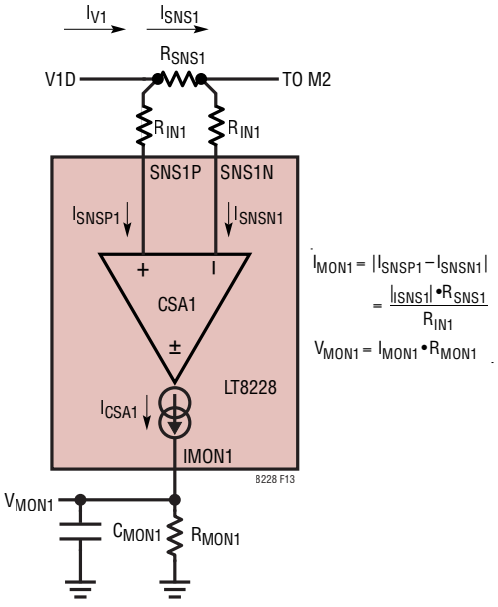


Figure 13. V_1 Current Monitoring at IMON1

$$R_{MON1} = \frac{R_{IN1}}{I_{SNS1MAX} \bullet R_{SNS1}} V_{MON1MAX} \quad (27)$$

where $I_{SNS1MAX}$ is the greater of the programmed V_1 input current limit I_{V1PLIM} in buck mode and the programmed V_1 output current limit I_{V1NLIM} in boost mode. A filtering capacitor C_{MON1} can be added to reduce ripple voltage at the IMON1 pin.

For positive current through R_{SNS1}, V_1 input current is less by CSA1's bias and feedback currents. For negative current through R_{SNS1}, V_1 output current is greater by CSA1's bias current. As a result, for low V_1 currents, CSA1's bias and feedback currents introduce error to the current monitor output IMON1.

OUTPUT VOLTAGE, INPUT UNDERVOLTAGE AND OUTPUT OVERVOLTAGE PROGRAMMING

In buck mode, the LT8228 has a regulated V_{2D} output voltage range of 1.21V to 100V. The output voltage is set by the ratio of two external resistors, R_{FB2A} and R_{FB2B}, at the FB2 pin as shown in Figure 14. The LT8228 servos the output to maintain the FB2 pin voltage at 1.21V referenced to ground. Calculate the output voltage using the formula in Figure 14. In boost mode, the LT8228 has a regulated V1D output voltage range of 1.21V to 100V. The output voltage is set by the ratio of two external resistors, R_{FB1A} and R_{FB1B}, at the FB1 pin. Calculate the V1D output voltage similarly to V_{2D}.

In boost mode, the LT8228 has V_2 input undervoltage detection at the UV2 pin. The falling undervoltage threshold V_{2UVTH} is set by the ratio of two external resistors, R_{UV2A} and R_{UV2B}, as shown in Figure 14. No DC current flows into the UV2 pin. Calculate the undervoltage threshold using the formula in Figure 14. In buck mode, the LT8228 has V_1 input undervoltage detection at the UV1 pin. The falling undervoltage threshold V_{1UVTH} is set by the ratio of two external resistors, R_{UV1A} and R_{UV1B}. Calculate the undervoltage threshold similarly to V_{2UVTH}. After the undervoltage thresholds have triggered, the rising thresholds increase by 100mV typically. If application does not require reverse voltage protection, the diode in series with the external resistors is not needed.

APPLICATIONS INFORMATION

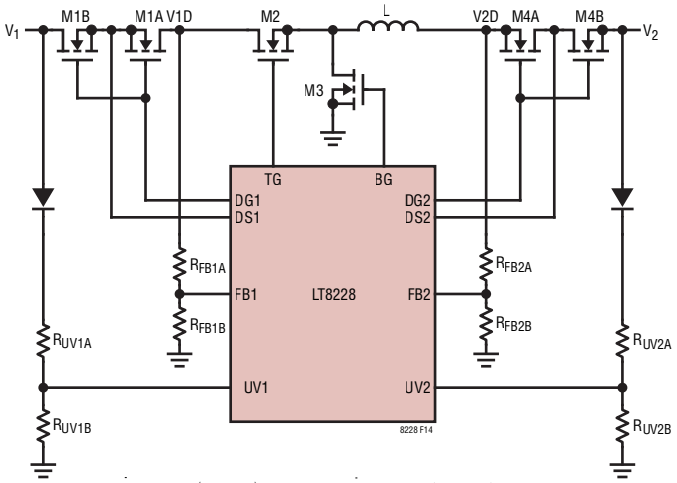


Figure 14. V_{2D} and V_{1D} Output Voltage, Input Undervoltage and Output Overvoltage Programming

The output overvoltage threshold is set about 10% higher than the output regulation voltage. In buck mode, the LT8228 has V_{2D} output overvoltage detection at the FB2 pin. The rising overvoltage threshold V_{2DOVTH} is set by the same ratio of the two external resistors, R_{FB2A} and R_{FB2B}, as shown in Figure 14. In boost mode, the LT8228 has V1D output overvoltage detection at the FB1 pin. The rising overvoltage threshold $V1_{DOVTH}$ is set by the same ratio of the two external resistors, R_{FB1A} and R_{FB1B}, as shown in Figure 14. After the overvoltage thresholds have triggered, the falling thresholds decrease by 100mV typically.

POWER MOSFET SELECTION AND EFFICIENCY CONSIDERATIONS

The LT8228 requires six external N-channel MOSFETs as shown in Figure 15: (1) the V_1 protection MOFSETs M1A and M1B, (2) the V_2 protection MOSFETs M4A and M4B, (3) the switching top MOSFET M2 and (4) the switching bottom MOSFET M3. M1B and M4B are optional if no inrush current control or protection against M3 short fault is not required. Important parameters for selecting the MOSFETs are the breakdown voltage BV_{DSS}, threshold voltage $V_{GS(TH)}$, on-resistance $R_{DS(ON)}$, maximum power dissipation $P_{D(MAX)}$ and safe operating area (SOA). For the switching MOSFETs M2 and M3, the miller capacitance C_{MILLER} is another important parameter. Since the selection criteria for choosing the protection MOSFETs and the switching MOSFETs are different, they are discussed in separate sections.

Protection MOSFETs (M1 and M4) Selection

The drain-to-source breakdown voltage BV_{DSS} of the protection MOSFETs M1 and M4 must be higher than the maximum drain-to-source voltage that might apply.

For the protection MOSFET M1A, the drain is connected to V1D. For the protection MOSFET M1B, the drain is connected to the V_1 Terminal. The sources of both M1A and M1B are connected to DS1. If V_1 is shorted to ground or connected to a reverse supply, M1A will be stressed by the V1D voltage. In buck start-up when V1D voltage is 0V, M1B will be stressed by the full supply voltage at V_1. A single MOSFET configuration at the V_1 terminal will have the same maximum stress voltage as M1A.

For the protection MOSFET M4A, the drain is connected to V_{2D}. For the protection MOSFET M4B, the drain is connected to the V_2 Terminal. The sources of both M4A and M4B are connected to DS2. If V_2 is shorted to ground or connected to a reverse supply, M4A will be stressed by the V_{2D} voltage. In boost start-up when V_{2D} voltage is 0V, M4B will be stressed by the full supply voltage at V_2. A single MOSFET configuration at the V_2 terminal will have the same maximum stress voltage as M4A.

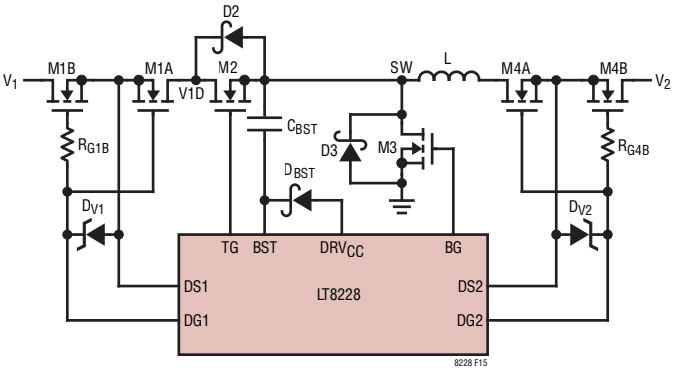


Figure 15. Power MOSFETs and Components Selection

APPLICATIONS INFORMATION

The LT8228 drives the gates of the protection MOSFETs M1 and M4 to a typical value of 10V above their sources. Internal clamps limit the gate drives to 12V maximum across temperature. For applications with V_1 or V_2 voltages higher than 24V, an external Zener clamp must be added between the gate and source of M1 and M4 in order to not exceed the MOSFETs' $V_{GS(MAX)}$ during extreme transients. This external Zener clamp can also be used to lower the gate drive voltage for use with logic-level MOSFETs. The DG1 and DG2 undervoltage thresholds are set at 5V typically. The gate drive should not be lower than 5.5V. Also, gate resistors R_{G1B} and R_{G4B} are necessary to prevent MOSFET parasitic oscillations and must be placed close to M1B and M4B respectively.

The MOSFETs' on-resistance, $R_{DS(ON)}$, directly affects the forward voltage drop and power dissipation. ADI recommends a forward voltage drop V_{FWD} of 100mV or less for reduced power dissipation. Ensure that the $R_{DS(ON)}$ of the MOSFETs meet the Equation 28 condition.

$$R_{DS(ON)} < \frac{V_{FWD}}{I_{M1,4(MAX)}} \quad (28)$$

where $I_{M1,4(MAX)}$ is the maximum current through M1 or M4. The higher of the V_1 input and output current limit is the maximum current through M1. The higher of the V_2 input and output current limit is the maximum current through M4.

Next, calculate the maximum power dissipation of the protection MOSFETs according to Equation 29.

$$P_{DM1,4(MAX)} = I^2M1,4(MAX) \bullet R_{DS(ON)} \quad (29)$$

The maximum power dissipation of M1 and M4 should be lower than the power dissipation parameter given in the MOSFET's data sheet. Give careful consideration to the temperature effect of the MOSFET's $R_{DS(ON)}$ and $P_{D(MAX)}$ parameter given in the Typical Characteristics curves in the MOSFET's data sheet to ensure the operation of the MOSFETs in their safe operating area. Multiple MOSFETs can be used in parallel to lower $R_{DS(ON)}$ and meet power and thermal requirements.

In buck start-up, when DG1 is turned on, inrush current flows from V_1 to charge C_{DM1} and C_{DM2}. During the inrush current, M1B is stressed by the full supply voltage. Control the inrush current to maintain M1B is its safe operating area. In boost start-up, when DG2 is turned on, inrush current flows from V_2 to charge C_{DM4} and CDM2. During the inrush current, M4B is stressed by the full supply voltage. Control the inrush current to maintain M4B is its safe operating area. In addition, when DG1 is turned on in boost mode, inrush current flows from V1D to V_1 terminal to charge the output load till V_1 and V1D voltages are equal. During this in-rush period, M1A is stressed by the voltage at V1D. M1A is again stressed in boost mode if V_1 is shorted to ground. The LT8228 employs an adjustable timer feature to maintain M1A in its safe operating area. Refer to the Inrush Current Control section for more information.

Switching MOSFETs (M2 and M3) Selection

The most important parameter for the switching MOSFETs M2 and M3 in high voltage applications is the breakdown voltage BV_{DSS}. Both the top gate and bottom MOSFETs will see maximum input voltage plus any additional ringing on the switch node across their drain-to-source during their off-time. Therefore, the MOSFETs must be chosen with the appropriate breakdown specification.

Since most MOSFETs in the 60V to 100V range have higher thresholds (typically $V_{GS(TH)} \geq 4V$), the LT8228 is designed with a 10V gate drive supply at the DRV_{CC} pin. The M2 and M3 must satisfy the 10V maximum VGS requirement.

It is also important to consider power dissipation when selecting power MOSFETs. Power dissipation must be limited to improve the system efficiency and avoid overheating that might damage the MOSFETs. The parameters that determine the power dissipation includes on-resistance $R_{DS(ON)}$, input voltage, output voltage, maximum output current, and Miller capacitance C_{MILLER}.

In buck mode, V1D is the input voltage and V_{2D} is the output voltage. M2 is the main switch and M3 is the synchronous switch. In boost mode, V_{2D} is the input voltage and V1D is the output voltage. M3 is the main switch and M2 is the synchronous switch.

APPLICATIONS INFORMATION

Miller capacitance C_{MILLER} is the most important selection criteria for determining the transition loss in the main switch MOSFET but is not directly specified on MOSFET manufacturer's data sheets. However, it can be approximated from the gate charge curve usually provided on the MOSFET data sheet. The curve is generated by forcing a constant input current into the gate of a common source, current source loaded stage and then plotting the gate voltage versus time as shown in Figure 16. The initial slope is the effect of the gate-to-source and the gate-to-drain capacitance. The flat portion of the curve is the result of the Miller multiplication effect of the drain-to-gate capacitance as the drain drops the voltage across the current source load. The upper sloping line is due to the drain-to-gate accumulation capacitance and the gate-to-source capacitance. The Miller charge (the increase in coulombs on the horizontal axis from a to b, while the curve is flat) is specified for a given V_{DS} drain voltage, but can be adjusted for different V_{DS} voltages by multiplying by the ratio of the application V_{DS} to the curve specified VD_S values. A way to estimate the C_{MILLER} term is to take the change in gate charge from points a to b on a manufacturers data sheet and divide by the stated V_{DS} voltage specified.

In buck and boost modes, the power dissipation equation for M2 and M3 are different as they swap roles between the main switch and the synchronous switch of the power stage. The MOSFET power dissipations in buck mode at maximum output current are given by Equation 30.

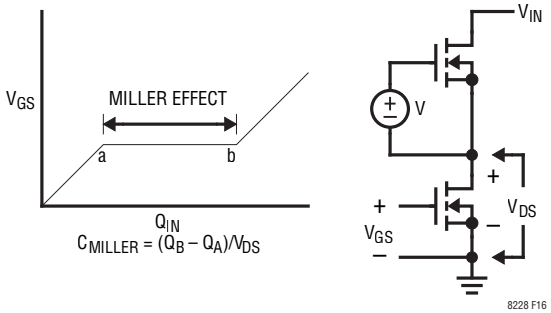


Figure 16. Gate Charge Characteristics and Miller Capacitance Calculation

$$P_{M2(BUCK)} = \frac{V_{2D}}{V_{1D}} \bullet (I_{V2,MAX})^2 \bullet (1+\delta)R_{DS(ON)} + V_{1D}{}^2 \bullet \frac{I_{V2,MAX}}{2} \bullet R_{DR} \bullet C_{MILLER} \bullet \left[\frac{1}{V_{DRVCC} - V_{TH(IL)}} + \frac{1}{V_{TH(IL)}}\right] f \quad (30)$$

$$P_{M3(BUCK)} = \frac{V_{1D} - V_{2D}}{V_{1D}} \bullet (I_{V2,MAX})^2 \bullet (1+\delta)R_{DS(ON)}$$

In boost mode, the power dissipation at maximum current is given by Equation 31.

$$P_{M2(BOOST)} = \frac{V_{2D}}{V_{1D}} \bullet (I_{V1,MAX})^2 \bullet (1+\delta)R_{DS(ON)}$$

$$P_{M3(BOOST)} = \frac{(V_{1D} - V_{2D}) \bullet V_{ID}}{V_{2D}{}^2} \bullet (I_{V1,MAX})^2 \bullet (1+\delta)R_{DS(ON)} + k \bullet I_{V1,MAX} \bullet \frac{V_{2D}{}^3}{V_{1D}} \bullet C_{MILLER} \bullet f \quad (31)$$

Here δ is the temperature coefficient of $R_{DS(ON)}$, and R_{DR} is the effective top driver resistance approximately 1.5Ω at $V_{GS} = V_{MILLER}$. The term $(1 + \delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve but δ equal to 0.6%/°C multiplied by the temperature difference can be used as an approximation for high voltage MOSFETs. $V_{TH(IL)}$ is the typical gate threshold voltage specified in the power MOSFET data sheet. The constant k, which accounts for the loss caused by reverse recovery current, is proportional to the gate drive current and has an empirical value of 1.7. C_{MILLER} is the calculated capacitance using the gate charge curve from the MOSFET data sheet and the technique described above.

APPLICATIONS INFORMATION

In buck mode, both MOSFETs have I^2R losses while the main switch MOSFET M2 has an additional term for transition loss that increases as V_{1D} voltage increases. For low V_{1D} voltages, larger MOSFETs (lower R_{DSON}) generally improve efficiency at high currents. For high V_{1D} voltages, a smaller MOSFET (higher R_{DSON}, lower C_{MILLER}) for the main switch may provide higher efficiency due to the transition loss dominating the I^2R loss. The synchronous switch MOSFET M3 losses are greater at higher V_{1D} voltages when the top MOSFET duty cycle factor is lower or during a short-circuit when the synchronous switch is on close to 100% of the switching period.

In boost mode, both MOSFETs have I^2R losses while the main switch bottom MOSFET M3 has an additional term for transition loss that increases as V_{2D} voltage decreases. For high V_{2D} voltages, larger MOSFETs (lower R_{DSON}) generally improve efficiency at high currents. For low V_{2D} voltages, a smaller MOSFET (higher R_{DSON}, lower C_{MILLER}) for the main switch may provide higher efficiency due to the transition loss dominating the I^2R loss. The synchronous switch MOSFET M2 losses are greater at higher V_{2D} voltages when the top MOSFET duty cycle factor is lower or during overvoltage when the synchronous switch is on close to 100% of the switching period.

In typical LT8228 applications, V_{1D} is higher than V_{2D} as V_{1D} is the buck input and boost output while V_{2D} is the buck output and boost input respectively. As a result, buck mode demands a smaller M2 (higher R_{DSON} but lower C_{MILLER}) while boost mode demands a larger M2 (lower R_{DSON}). Similarly, buck mode demands a larger M3 (lower R_{DSON}) while boost mode demands a smaller M3 (higher R_{DSON} but lower C_{MILLER}). Select top MOSFET M2 and bottom MOSFET M3 to optimize efficiency in both buck and boost modes.

Multiple MOSFETs can be used in parallel to lower $R_{DS(ON)}$ to meet the current and thermal requirements of the application. The LT8228 contains large low impedance drivers capable of driving large gate capacitances without significantly slowing transition times. When driving MOSFETs with very low gate charge, it is sometimes helpful to slow down the drivers by adding small gate resistors (2Ω or less) to reduce switch node ringing and EMI caused by fast switch node transitions.

OPTIONAL SCHOTTKY DIODE (D2 AND D3) SELECTION

In buck mode, the body diode of the bottom MOSFET M3 conducts during the transition time when the main switch MOSFET M2 turns off and the synchronous switch MOSFET M3 turns on. As the M3 body diode conducts during this dead time, it stores charge. A Schottky diode D3 is placed in parallel to bottom MOSFET M3 as shown in the Block Diagram section to significantly reduce reverse recovery current due to the body diode conduction which improves the system efficiency and lowers power dissipation at M3. Similar to the buck mode, the body diode of the top MOSFET M2 conducts during the transition time in boost mode when the main switch bottom MOSFET M3 is turning off and the synchronous switch top MOSFET M2 is turning on. A Schottky diode D2 is placed in parallel to top MOSFET M2 as shown in the Block Diagram section to reduce the reverse recovery current, improve system efficiency and lowers power dissipation at M2.

In order for the diode to be effective, the inductance between it and the switch must be as small as possible, mandating that these components be placed adjacently. For applications with V_{1D} voltages typically greater than 40V, avoid Schottky diodes with excessive reverse leakage currents particularly at high temperatures. Some ultralow V_F diodes will trade off increased high temperature leakage current for reduced forward voltage. The combination of high reverse voltage and current can lead to self-heating of the diode. Besides reducing efficiency, this can increase leakage current which increases temperatures even further. Choose packages with lower thermal resistance to minimize self-heating of the diodes.

APPLICATIONS INFORMATION

TOP MOSFET DRIVER SUPPLY (C_{BST}, D_{BST})

An external bootstrap capacitor, CB_{ST}, connected from the SW to the BST pins, supplies the gate drive voltage for the top MOSFET M2. When the switch node is low, DRV_{CC} charges this capacitor through an external diode D_{BST}. When M2 turns on, the switch node rises to V_1 and the BST pin rises to approximately $V_1 + DRV_{CC}$. The boost capacitor needs to store about 100 times the gate charge required by the top MOSFET. In most applications a 0.1µF to 0.47µF X5R or X7R dielectric capacitor is adequate.

The reverse breakdown of the external diode, D_{BST}, must be greater than $V_{1(MAX)}$. Another important consideration for the external diode is its reverse recovery and reverse leakage, either of which may cause excessive reverse current flow at full reverse voltage. If the reverse current times the reverse voltage exceeds the maximum allowable power dissipation, the diode may get damaged. For best results, use a diode that has very fast recovery and low leakage.

POWER PATH CAPACITOR SELECTION

Capacitor Selection at V_1 (C_{V1}, C_{DM1} and C_{DM2})

In applications where the V_1 terminal is connected to a voltage source or load through long conducting wires, parasitic wire inductance and C_{DM1} form a high-Q LC resonant tank circuit. During a large V_1 transient such as a short, the resonant frequency creates large voltage oscillations at V_1. In this case, V_1 goes negative which turns off the V_1 protection MOSFET M1. To prevent the drain-to-source voltage breakdown of M1, add a bypass capacitor, C_{V1}, with series resistance at V_1 which dampens the resonant circuit. Since high ESR capacitors such as aluminum electrolytic cannot tolerate negative voltages, use low ESR ceramic capacitors with additional resistors in series.

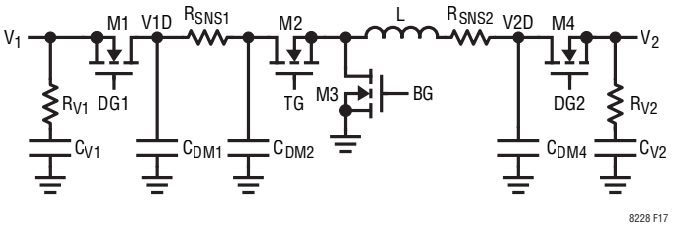


Figure 17. Power Path Capacitor Selection at V_1 and V_2

The drain of the top MOSFET M2 is the input of the buck power stage and output of the boost power stage. The capacitor at this node, C_{DM2}, and at V_{1D}, C_{DM1} serve as input bypass capacitors in buck mode and output filtering capacitors in boost mode. R_{SNS1} connected between the drain of M2 and V_{1D} is used to monitor and regulate in the V_1 input and output current. RS_{NS1} is also used to sense the instantaneous current through M2 for MOSFET short detection. Due to their relative placement in the board, R_{SNS1} does not sense the M2 instantaneous current coming out of C_{DM2}. Thus, any capacitance at C_{DM2} hinders LT8228's MOSFET short detection capability. On the other hand, capacitance of C_{DM2} is needed to reduce the EMI and AC energy in the hot loop. The capacitance distribution between C_{DM1} and C_{DM2} needs to ensure effective MOSFET short detection as well as low EMI and AC energy dissipation.

The current through the top MOSFET M2 is discontinuous in both buck and boost modes. In buck continuous mode operation, the drain current of the top MOSFET is approximately a square wave of duty cycle V_{2D}/V_{1D} which is instantaneously supplied by $C_{DM1\ and}$ C_{DM2}. To prevent large input voltage transients in buck mode, use a low ESR capacitor sized for the maximum RMS current through the top MOSFET M2, I_{RMS}, given by Equation 32.

$$I_{RMS} = I_{V2(MAX)} \bullet \frac{V_{2D}}{V_{1D}} \sqrt{\frac{V_{1D}}{V_{2D}} - 1} \quad (32)$$

where $I_{V2(MAX)}$ is the maximum output current in buck mode. This formula has a maximum when the V_{1D} voltage is twice the regulated V_{2D} voltage, where I_{RMS} is half of $I_{V2(MAX)}$. This simple worst-case condition is commonly used for design. Note that the ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required.

APPLICATIONS INFORMATION

C_{DM1} and C_{DM2} also serves as the output filtering capacitors in boost mode to reduce the ripple voltage caused by the discontinuous current through the top MOSFET M2. For boost mode, the effects of ESR and the bulk capacitance must be considered when choosing the capacitor for a given output ripple voltage. The maximum steady-state ripple voltage due to charging and discharging the bulk capacitance is given by Equation 33.

$$\Delta V_{BULK} = \frac{I_{V1(MAX)} \bullet (V_{1D} - V_{2D(MIN)})}{C_{DM2} \bullet V_{1D} \bullet f} \quad (33)$$

where $I_{V1(MAX)}$ is the maximum output current in boost mode and f is the switching frequency. The steady-state ripple due to the voltage drop across the ESR is given by Equation 33.

$$\Delta V_{ESR} = I_{L(MAX)} \bullet ESR \quad (34)$$

where $I_{L(MAX)}$ is the maximum inductor current in boost mode. The voltage ripple at the drain of the top MOSFET M2 is the total ripple caused by the buck capacitance and ESR. Low ESR tantalum and OS-CON capacitors are typically not available in voltages above 35V. Therefore, ceramics or aluminum electrolytics must be used for high V_1 and V_2 voltages.

Give extra consideration to the use of ceramic capacitors. Manufacturers make ceramic capacitors with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics provide high C-V products in a small package at low cost, but exhibit strong voltage and temperature coefficients. The X5R and X7R dielectrics yield much more stable characteristics and are more suitable for use as the C_{DM2} capacitor.

The X7R type works over a wider temperature range and has better temperature stability, while the X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors; the X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance changes due to DC bias are less with X5R and X7R capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases, but expected capacitance at operating voltage should be verified.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress is induced by vibrations in the system or thermal transients. The resulting voltages produced can cause appreciable amounts of noise.

A combination of aluminum electrolytic capacitors and ceramic capacitors are typically needed to meet the size or height requirements in a design. When used together, the percentage of RMS current that will flow through the aluminum electrolytic capacitor is given by Equation 35.

$$\%I_{RMS,ALUM} \approx \frac{100\%}{\sqrt{1+\left(8 \bullet f \bullet C_{CER} \bullet \left(R_{ESR(ALUM)}\right)\right)^2}} \quad (35)$$

where $R_{ESR(ALUM)}$ is the ESR of the aluminum electrolytic capacitor and C_{CER} is the overall capacitance of the ceramic capacitors. This reduces the RMS current at C_{DM2} allowing smaller capacitance. The ESR of the aluminum electrolytic capacitors helps to dampen the high Q of the ceramic, minimizing ringing. Additionally, it provides the bulk capacitance for supplies with high source impedance such as batteries.

Ensure the capacitor selection of C_{DM1} and C_{DM2} satisfies both the buck and boost requirements for RMS current and output ripple voltage respectively.

Capacitor Selection at V_2 (C_{DM4} and C_{V2})

The drain of the V_2 protection MOSFET M4 is the input of the boost power stage and the output of the buck power stage. The capacitor C_{DM4} serves as an output filtering capacitor in buck mode and as an input bypass capacitor in boost mode. The current through the V_2 protection MOSFET M4 is continuous in both buck and boost modes.

APPLICATIONS INFORMATION

In buck mode, the selection of C_{DM4} is primarily determined by the ESR required to minimize output ripple voltage followed by filtering and RMS current rating requirements. The output ripple voltage (ΔV_{2D}) is approximately equal to Equation 36.

$$\Delta V_{2D} = \Delta I_L \bullet \left(ESR + \frac{1}{8 \bullet f \bullet C_{DM4}} \right) \quad (36)$$

Since Δ_{IL} increases with input voltage, the output ripple is highest at maximum input voltage. ESR also has a significant effect on the load transient response. Fast load transitions at the output will appear as voltage across the ESR of C_{DM4} until the feedback loop in the LT8228 can change the inductor current to match the new load current value. Typically, once the output ripple voltage requirement is satisfied, the capacitance is adequate for filtering and has the required RMS current rating.

In boost mode, the minimum required value of C_{DM4} is a function of the source impedance at V_2, and typically the higher the source impedance, the higher the required capacitance. The required amount of boost input capacitance is also greatly affected by the duty cycle. High output current applications that also experience high duty cycles can place great demands on the input supply, both in terms of DC current and ripple current.

As with C_{DM2}, C_{DM4} needs to satisfy both the buck and boost requirements for output ripple voltage and source impedance, respectively. A combination of aluminum electrolytic capacitors and ceramic capacitors are typically needed to meet the size or height requirements in a design.

In applications where the V_2 terminal is connected to a voltage source or load through long conducting wires, parasitic wire inductance and C_{DM4} form a high-Q LC resonant tank circuit. During a large V_2 transient such as a short, the resonant frequency creates large voltage oscillations at V_2. In this case, V_2 goes negative which turns off the V_2 protection MOSFET M4. To prevent the drain-to-source voltage breakdown of M4, add a bypass capacitor, C_{V2}, at V_2 with series resistance R_{V2} which dampens the resonant circuit. Since high ESR capacitors such as aluminum electrolytic cannot tolerate negative voltages, use low ESR ceramic capacitors with additional resistors in series.

LOOP COMPENSATION

There are three feedback loops to consider in both buck and boost modes when setting up the compensation for the LT8228. The loops are (1) the output voltage loop, (2) the output current limit loop and (3) the input current limit loop. In buck mode, the LT8228 uses an internal transconductance error amplifier EA2 to regulate V_{2D} output voltage, V_2 output current limit and V_1 input current limit. The error amplifier output V_{C2} compensates the buck mode voltage and current limit loops. In boost mode, the LT8228 uses a separate transconductance error amplifier EA1 to regulate V_{1D} output voltage, V_1 output current limit and V_2 input current limit. The error amplifier output V_{C1} compensates the boost mode voltage and current loops. Separate compensation pins allow individual optimization of both buck and boost modes. The voltage loop stability is determined by the inductor value, the current sense resistor and its input gain resistors, the output capacitance, the load current and the V_C compensation resistor and capacitor. The current loop stability is determined by the inductor value, the I_{SET} resistor and its capacitor, and the V_C compensation resistor and capacitor. The inductor, current sense resistor, input gain resistors, output capacitor and I_{SET} resistors have been chosen based on performance, size and cost as discussed in the previous sections. The V_C compensation resistor and capacitor and the I_{SET} capacitor are set to optimize the voltage and current loop response and stability.

Buck mode compensation consists of a resistor R_{C2} and a capacitor C_{C2} connected in series between the VC2 pin and ground. An optional parallel capacitor can also be connected between the VC2 pin and ground to filter high frequency noise. Set R_{C2} and C_{C2} based on the V_{2D} voltage loop stability. For typical buck mode applications, a 10nF compensation capacitor C_{C2} is adequate. Lowering the compensation capacitance increases the bandwidth of the loop. However, higher bandwidth may make the loop unstable due to the LC output filer pole. Higher CC_2 value might be needed for stability if the output capacitance at V_{2D} is reduced. The series resistor R_{C2} is used to increase

APPLICATIONS INFORMATION

the slew rate of the VC2 pin to maintain tighter regulation of the output current during a load or input transient. If the resistance is too high, the loop gets unstable whereas if it is too low, the transient response is too slow. For typical buck mode applications, setting R_{C2} to 2kΩ is a good starting point. Initially use an "R/C box" to quickly iterate towards the final compensation value where the bandwidth is highest with sufficient phase margin. Check the loop stability at no load, maximum load, and all points in between over the entire input voltage range with 20% variation on the compensation values.

Once the R_{C2} and C_{C2} are set, select the I_{SET} capacitors next. Since the output capacitance is not part of the current loops; the typical output impedance of 1Meg at the VC2 pin with C_{C2} is the dominant pole in the loop. Set the ISET1P and ISET2P capacitors so that the pole formed by the ISET pin resistor and capacitor does not make the loop unstable.

Similarly, boost mode compensation consists of a resistor R_{C1} and a capacitor C_{C1} connected in series between the VC1 pin and ground. An optional parallel capacitor can also be connected between the VC1 pin and ground to filter high frequency noise. Set R_{C1} and C_{C1} based on the V_{1D} voltage loop stability. For typical boost mode applications, a 4nF compensation capacitor C_{C1} is adequate. Lowering the compensation capacitance increases the bandwidth of the loop. However, higher bandwidth may make the loop unstable due to the LC output filer pole. Higher C_{C1} value might be needed for stability if the output capacitance at V_{1D} is reduced. The series resistor R_{C1} is used to increase the slew rate of the VC1 pin to maintain tighter regulation of the output current during a load or input transient. If the resistance is too high, the loop gets unstable whereas if it is too low, the transient response is too slow. For typical boost mode applications, setting R_{C1} to 8k is a good starting point. Initially use an "R/C box" to quickly iterate towards the final compensation value where the bandwidth is highest with sufficient phase margin. Check the loop stability at no load, maximum load, and all points in between over the entire input voltage range with 20% variation on the compensation values.

Once the R_{C1} and C_{C1} are set, select the I_{SET} capacitors next. Since the output capacitance is not part of the current loops; the typical output impedance of 1Meg at the VC1 pin with C_{C1} is the dominant pole in the loop. Set the ISET1N and ISET2N capacitors so that the pole formed by the ISET pin resistor and capacitor does not make the loop unstable.

INRUSH CURRENT CONTROL

In buck start-up, when DG1 is turned on, inrush current flows from V_1 to charge C_{DM1} and C_{DM2}. During the inrush current, M1B is stressed by the full supply voltage at V_1. Unless the inrush current is controlled, M1B

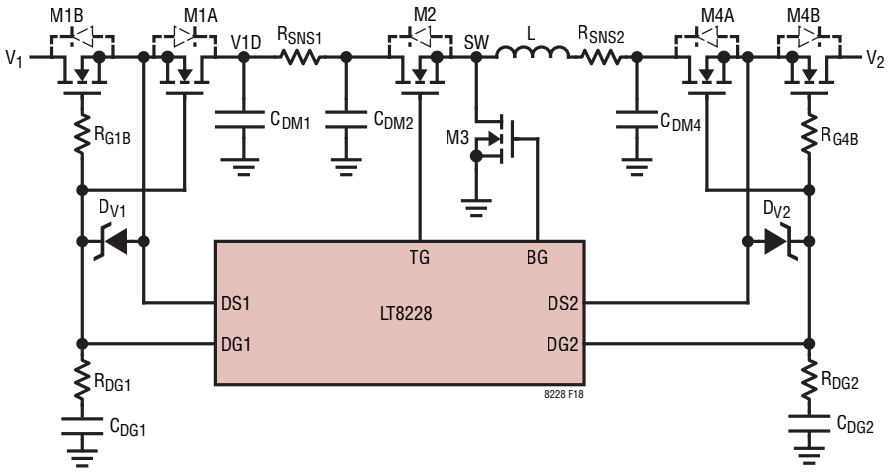


Figure 18. Input Inrush Current Control

APPLICATIONS INFORMATION

operates outside its SOA and gets damaged. The LT8228 limits the inrush current by controlling the DG1 pin voltage slew rate. As shown in Figure 18, the compensation resistor R_{DG1} and capacitor C_{DG1} are used for this purpose. At start-up, a 10µA pull-up current charges DG1, pulling up both M1A and M1B gates. M1B operates as a source follower and Equation 37.

$$I_{INRUSH,BUCK} = \frac{10\mu A \bullet (C_{DM1} + C_{DM2})}{C_{DG1}} \quad (37)$$

In typical applications, a C_{DG1} of 6.8nF and R_{DG1} of 10kΩ is recommended. Carefully consider the SOA of M1B to ensure it can withstand the maximum stress applied by maximum voltage at V_1 and inrush current $I_{INRUSH,BUCK}$.

In boost start-up, when DG2 is turned on, inrush current flows from V_2 to charge C_{DM4}, C_{DM2} and C_{DM1}. During the inrush current, M4B is stressed by the full supply voltage at V_2. Unless the inrush current is controlled, M4B operates outside its SOA and gets damaged. The LT8228 limits the inrush current by controlling the DG2 pin voltage slew rate. As shown in Figure 18, the resistor R_{DG2} and capacitor C_{DG2} are used for this purpose. At start-up, a 10µA pull-up current charges DG2, pulling up both M4A and M4B gates. M4B operates as a source follower and Equation 38.

$$I_{INRUSH,BOOST} = \frac{10\mu A \bullet (C_{DM1} + C_{DM2} + C_{DM4})}{C_{DG2}} \quad (38)$$

In typical applications, a C_{DG2} of 3.3nF and R_{DG1} of 10k is recommended. Carefully consider the SOA of M4B to ensure it can withstand the maximum stress applied by maximum voltage at V_2 and inrush current $I_{INRUSH,BOOST}$.

In boost mode, DG2 is charged first which charged V_{2D} to V_2 and V_{1D} higher than V_{2D}. When DG2 voltage exceeds it undervoltage threshold, DG1 starts charging. Inrush current flow from V_{1D} to charge the load at V_1. Similar to buck mode, the boost output inrush current is limited by capacitor C_{DG1}. M1A operates as a source follower and Equation 39.

$$I_{INRUSH,BOOST,OUTPUT} = \frac{10\mu A \bullet (C_{V1})}{C_{DG1}} \quad (39)$$

In buck mode, there is no output inrush current as V_{2D} is 0V as DG2 starts charging. However, if the V_2 is pre-biased at start-up, output inrush current flows from V_2 to V_{2D} which is similar to input inrush current in boost mode.

BOOST OUTPUT SHORT PROTECTION AND TIMER

Boost Output V_1 Short Current Control

In boost mode when V_1 drops below V_2 due to excessive load or V_1 is shorted to ground, the output current cannot be regulated through the switching MOSFET due to the body diode of the TG MOSFET M2. Unlike other boost controllers that cannot limit current under such conditions, the LT8228 limits the output short current using the V_1 protection MOSFET M1 (M1A is dual MOSFET configuration). As shown in Figure 19, the LT8228 senses the output current across the resistor R_{SNS1} and outputs a proportional current at the ISET1N pin. M1 limits the output current so that the ISET1N pin voltage is 1.4V by controlling DG1. The output short current $I_{V1,SHORT}$ is set according to Equation 40.

$$I_{V1,SHORT} = \frac{R_{IN1}}{R_{SNS1} \bullet R_{SET1N}} \bullet 1.4V \quad (40)$$

The current limit can be lowered by injecting additional current into the ISET1N pin or by dynamically increasing the I_{SET1N} resistor. As the ISET1N pin voltage is regulated above the typical switching current limit reference during V_1 short current control, the boost V_1 output current limit loop stops the LT8228's switching. This also ensures that V_1 output short current control has no interference during V_1 output current limit in boost mode. If dual back-to-back MOSFET configuration is used, external compensation resistor R_{DG1} and capacitor C_{DG1} are used to stabilize the V_1 output short current control loop. R_{DG1} and capacitor C_{DG1} are connected in series from DG1 to ground in dual back-to-back MOSFET configuration. In single MOSFET configuration, they are placed across the DG1 and DS1 pins (the gate and source of the V_1 protection MOSFET M1). C_{DG1} is already set to limit the inrush current. Set R_{DG1} to cancel the pole created by R_{SET1N} and C_{SET1N}.

APPLICATIONS INFORMATION

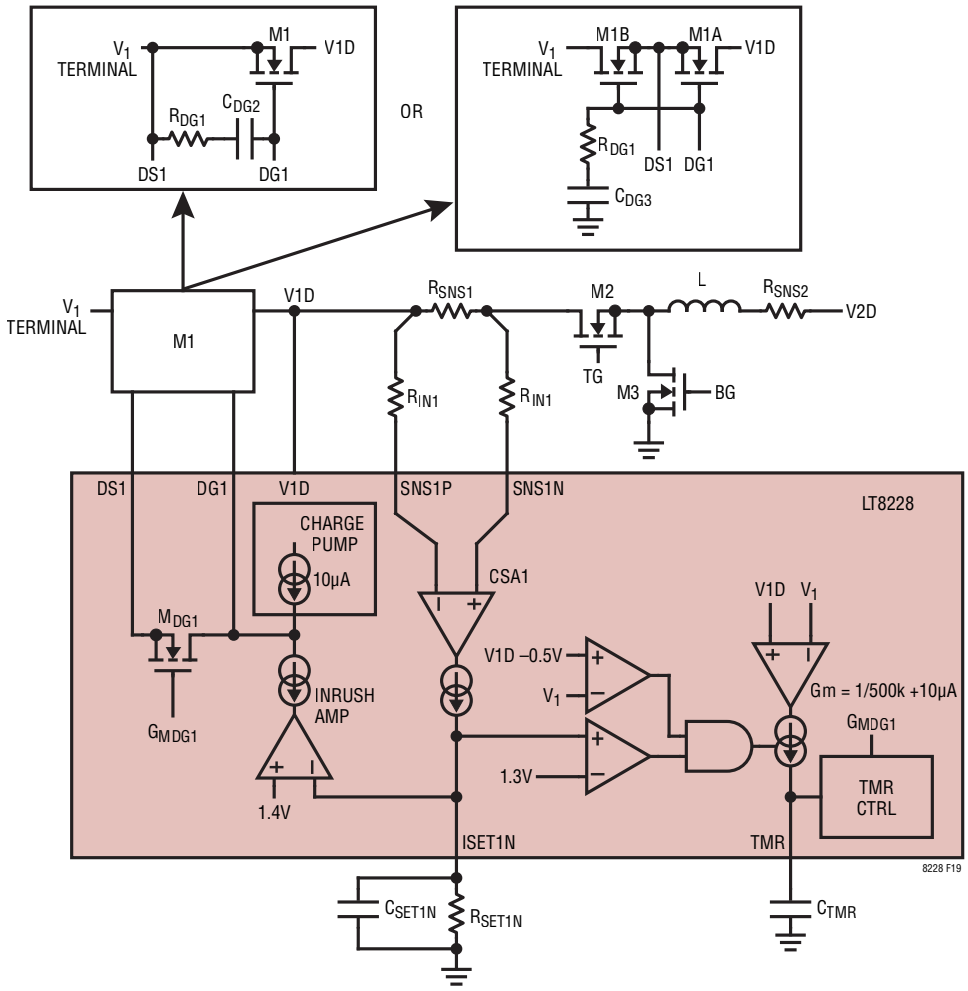


Figure 19. M1 Protection During Output Short in Boost Mode

Overcurrent Fault and Fault Timer

During the V_1 output short current control period, M1 or M1A is stressed by the V_{1D} voltage which can be as high as V_2 supply. Coupled with the current set by ISET1N, the energy dissipation at M1 might take it out of its safe operating area (SOA). To keep M1 operating in its SOA, the LT8228 includes an overcurrent fault detection and an adjustable fault timer. An overcurrent fault occurs when the current limit circuitry at ISET1N has been engaged for longer than the timeout delay set by the timer capacitor at the TMR pin and V_{1D} is higher than V_1 (sensed using DS1) by 500mV. The DG1 pin is then immediately pulled low by 80mA to the DS1 pin, turning off the M1. After the fault condition has disappeared and a cool down period has transpired, the DG1 pin is allowed to pull back up and turn on the protection MOSFET M1.

Connecting a capacitor from the TMR pin to ground sets the delay period before the MOSFET M1 is turned off during an overcurrent fault condition. The same capacitor also sets the cool down period before M1 is allowed to turn back on after the fault condition has disappeared. The current limit circuitry at ISET1N engages when the ISET1N voltage is higher than 1.3V (Refer to the ISET1N inrush current limit threshold curve in the Typical Performance Characteristics section). Once the current limit circuitry at ISET1N has engaged, a current source charges up the TMR pin. The current level varies depending on the voltage drop across the V1D pin and the DS1

APPLICATIONS INFORMATION

pin, corresponding to the MOSFET M1's or M1A's VDS. The on time is inversely proportional to the voltage drop across the MOSFET. This scheme therefore takes better advantage of the available safe operating area (SOA) of the MOSFET than would a fixed timer current.

During an overcurrent fault, the timer current starts at 10µA with 0.5V of $V_{1D} – V_1$ and increases to 210µA with 100V of $V_{1D} – V_2$ (see Figure 20 and Equation 41).

$$I_{TMR(UP)OC} = 10\mu A + 2[\mu A / V] \bullet (V_{1D} – V_1 – 0.5V) \quad (41)$$

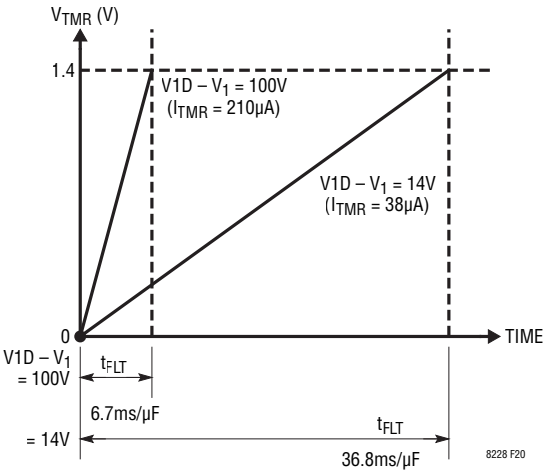


Figure 20. Fault Timer Current of the LT8228

This arrangement allows the pass device to turn off faster during an overcurrent event with high V_{DS} voltage at M1, since more power is dissipated. Refer to the Typical Performance Characteristics section for the timer current at different $V_{1D} – V_1$ in overcurrent events.

When the voltage at the TMR pin crosses the 1.4V threshold, the pass device M1 turns off immediately. Assuming $V_{1D} – V_1$ remains constant, the on-time of DG1 during an overcurrent fault is shown in Equation 41.

$$T_{OC} = \frac{C_{TMR} \bullet 1.4V}{I_{TMR(UP)OC}} \quad (42)$$

As soon as TMR reaches 1.4V and DG1 pulls low in a fault condition, the TMR pin starts discharging with a 2µA current. When the TMR pin voltage drops to 0.4V, TMR charges with 2µA. When TMR reaches 1.4V, it starts discharging again with 2µA. This pattern repeats 32 times to form a long cool down timer period before retrying. At the end of the cool down period (when the TMR pin voltage drops to 0.4V the 32nd time), the LT8228 retries, pulling the DG1 pin up and turning on the pass device M1. The total cool down timer period is given by Equation 43.

$$T_{COOL} = \frac{63 \bullet C_{TMR} \bullet 1V}{2\mu A} \quad (43)$$

Refer to the Typical Performance Characteristics section for the V_1 protection MOSFET M1's duty cycle under an overcurrent fault.

$\overline{\text{FAULT}}$ CONDITIONS

The $\overline{\text{FAULT}}$ pin is an open-drain logic output which flags internal and external faults. Pull up the pin with a series resistor to a microcontroller supply or the $INTV_{CC}$ pin. An LED can be added in series with the pull-up resistor for visual status indication. The LT8228 pulls down on the $\overline{\text{FAULT}}$ pin under the following conditions.

1. **Temperature Fault:** The junction temperature exceeds 165°C typically.
2. **V_{CC} Fault:** DRV_{CC} or $INTV_{CC}$ falls below their undervoltage threshold. The threshold is set at 6.5V for DRV_{CC} and 3.4V for $INTV_{CC}$ typically.
3. **Input Undervoltage Fault:** In buck mode, UV1 falls below its undervoltage threshold of 1.2V typically. In boost mode, UV2 falls below its undervoltage threshold of 1.2V typically.
4. **Output Overvoltage Fault:** In buck mode, FB2 rises above its overvoltage threshold of 1.3V typically. In boost mode, FB1 rises above its overvoltage threshold of 1.3V typically.
5. **DG Fault:** The DG1 or the DG2 falls below their undervoltage threshold of 4.5V typically.
6. **TG MOSFET M2 or BG MOSFET M3 Short Fault**: The LT8228 detects the M2 or the M3 short damage using the R_{SNS1} and R_{SNS2} resistors.
7. **Reference Fault:** The two internal references are more that 10% away from each other.

APPLICATIONS INFORMATION

8. **Internal Diagnostic Fault:** The LT8228 checks the functionality of the error amplifiers EA1 and EA2 and the current sense amplifiers CSA1 and CSA2 and the oscillator at start-up. Failure to pass the functionality test results in internal diagnostic fault.

When the $\overline{FAULT}$ pin asserts, the LT8228 stops switching and pulls the SS pin low except for the output overvoltage fault. For a sink current of 2mA, the maximum voltage over temperature at the $\overline{FAULT}$ pin is 0.5V.

SOFT-START

The LT8228 limits the input and the output currents by limiting the corresponding ISET pin voltages to a current limit reference voltage V_{IREF} which is the lower of the SS pin voltage and the internal reference voltage of 1.21V typically as shown in Figure 21. Connecting an external capacitor, C_{SS}, from the SS pin to ground programs a current limit soft-start during start-up. When the LT8228 is enabled, an internal 10µA pull-up current is activated while the SS pin voltage remains low due to an active pull down by an internal MOSFET. The pull-down is maintained under the following fault conditions.

1. **Temperature Fault:** The junction temperature exceeds 165°C typically.
2. **VCC Fault:** DRV_{CC} or $INTV_{CC}$ falls below their undervoltage threshold. The threshold is set at 6.5V for DRV_{CC} and 3.4V for $INTV_{CC}$ typically.
3. **Input Undervoltage Fault:** In buck mode, UV1 falls below its undervoltage threshold of 1.2V typically. In boost mode, UV2 falls below its undervoltage threshold of 1.2V typically.

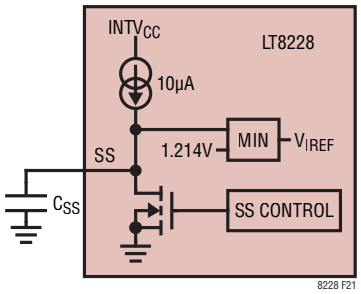


Figure 21. Soft-Start Pin Control

4. **DG Fault:** The DG1 or the DG2 falls below their undervoltage threshold of 4.5V typically.
5. **TG MOSFET M2 or BG MOSFET M3 Short Fault:** The LT8228 detects the M2 or the M3 short damage using the R_{SNS1} and R_{SNS2} resistors.
6. **Internal Diagnostic Fault:** The LT8228 checks the functionality of the references and the error amplifiers EA1 and EA2 and the current sense amplifiers C_{SA1} and C_{SA2} and the oscillator at start-up. Failure to pass the functionality test results in internal diagnostic fault.

If none of the fault conditions exist, SS pull-down is disabled allowing the SS pin voltage to rise linearly. Once the SS pin voltage reaches the internal reference voltage, the input and output current limits are set to their maximum value. The total soft-start time t_{SS} is given by Equation 44.

$$T_{SS} = C_{SS} \bullet \frac{1.21V}{10\mu A} \quad (44)$$

$\overline{REPORT}$ FEATURE

The LT8228 checks internal circuit blocks, fault conditions, and external MOSFETs for errors and reports the result at the $\overline{REPORT}$ pin. The pin is an active low open-drain output. Pull up the $\overline{REPORT}$ pin to a microcontroller supply through a series resistor. Set the resistance of the pull-up resistor to meet the logic level needs of the application. For a sink current of 2mA, the maximum voltage over temperature at the $\overline{REPORT}$ pin is 0.5V. The pin is functional as long as the part is enabled and the $INTV_{CC}$ pin voltage is higher than 2.8V typically. The $\overline{FAULT}$ pin can be used as an interrupt for the microcontroller since it is pulled "low" during an error. The microcontroller can always read the $\overline{REPORT}$ pin data or only when interrupted by the $\overline{FAULT}$ pin. At start-up, while $INTV_{CC}$ is rising from 0V to 4V with 20mA charging current, the $\overline{FAULT}$ pin pull-down activates at 1.2V typically. However, the $\overline{REPORT}$ is not active until 2.8V typically. If microcontroller is reading the $\overline{REPORT}$ pin data when interrupted by the $\overline{FAULT}$ pin, allow enough time for the $INTV_{CC}$ capacitor to get charged to 2.8V at start-up. Refresh the enable pin to reset all the error latches.

APPLICATIONS INFORMATION

The LT8228 continuously reports a 32-bit word at the active low $\overline{\text{REPORT}}$ pin using the SYNC pin as the data clock. If the SYNC pin is unused, the $\overline{\text{REPORT}}$ pin remains high impedance. The 32-bit word starts with a header which consists of a sequence of 8 logic high (V_H) synchronization bits. During the 8 "V_H" synchronization bits, the LT8228 checks the $\overline{\text{REPORT}}$ pin voltage at every clock cycle to ensure external pull-up. The threshold voltage for external pull-up detection is 1V typically. If the voltage drops below the threshold voltage during the 8 "V_H" synchronization bits, the part restarts the header. This mechanism allows implementation of the "Chip Select" feature where a multiplexer can be used to read multiple LT8228 $\overline{\text{REPORT}}$ pins by a single microcontroller input.

Once the LT8228 completes the header bits without external pull-up error, it finishes reporting the rest of the 24 bits starting with a logic low (V_L) bit, followed by 6 status bits, a parity bit, a "V_L" bit, followed by another 6 status bits, a parity bit, a "V_L" bit, followed by another 4 status bits, 2 counter bits and a parity bit as shown in Figure 22. The corresponding error of each status bit is listed in Table 2. A status bit of "V_L" indicates an error. The parity bits ensure an even number of V_H's in the preceding 7 bits. The count bits are the output of 2-bit counter which counts the number of times the 32-bit word is repeated. The counter restarts after every 4 counts. Once a fault is detected, it is reported for a minimum of 3 counts. If a fault condition lasts longer than 3 counts, the part reports the fault till the condition no longer exists.

Table 2. Report Address Allocation and Check Time

BIT	DIAGNOSTIC	CHECK TIME
01010(S0)	Overtemperature	Always
01011(S1)	DRV_{CC} Under/Overvoltage	Always
01100(S2)	$INTV_{CC}$ Under/Overvoltage	Always
01101(S3)	Input Undervoltage	Always
01110(S4)	Output Overvoltage	Always
01111(S5)	Reverse Current	Buck Only
10010(S6)	DG1 Undervoltage	Always
10011(S7)	DG2 Undervoltage	Always
10100(S8)	BG MOSFET M3 Short	Always
10101(S9)	TG MOSFET M2 Short	Always
10110(S10)	Reference	Always
10111(S11)	EA1	At Start-Up
11010(S12)	EA2	At Start-Up
11011(S13)	CSA1	At Start-Up
11100(S14)	CSA2	At Start-Up
11101(S15)	Oscillator	At Start-Up

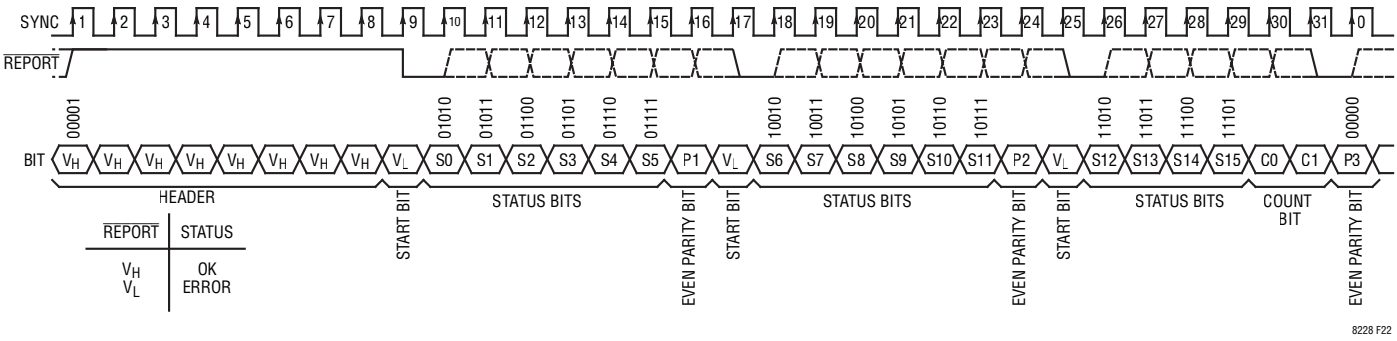


Figure 22. The Address Sequence at the $\overline{\text{REPORT}}$ Pin

APPLICATIONS INFORMATION

Over Temperature (01010)

If the die junction temperature reaches 165°C typically, the LT8228 shuts down all four external N-channel MOSFETs, pulls the SS pin low, asserts the $\overline{FAULT}$ pin, IGND goes high impedance and reports the status as a logic low.

DRV_{CC} (01001): If the DRV_{CC} pin voltage falls below its undervoltage threshold of 6.5V typically, or rises above its overvoltage threshold of 15.2V typically, the LT8228 shuts down all four external N-channel MOSFETs, pulls the SS pin low, IGND goes high impedance and the status is reported as a logic low. This error stops switching, asserts the $\overline{FAULT}$ pin, pulls the SS pin low, and IGND goes high impedance.

$INTV_{CC}$ (01100): If the $INTV_{CC}$ pin voltage falls below its undervoltage threshold of 3.6V typically, or rises above its overvoltage threshold of 4.7V typically, the LT8228 shuts down all four external N-channel MOSFETs, pulls the SS pin low, IGND goes high impedance and the status is reported as a logic low. This error stops switching, asserts the $\overline{FAULT}$ pin, pulls the SS pin low, and IGND goes high impedance.

Input Undervoltage (01101): Input undervoltage is detected by the LT8228 by the UV1 and UV2 pins. In buck mode, if the UV1 voltage falls below the undervoltage threshold, the status is reported as a logic low. In boost mode, if the UV2 voltage falls below the undervoltage threshold, the status is reported as a logic low. This error stops switching, asserts the $\overline{FAULT}$ pin, pulls the SS pin low, and IGND goes high impedance.

Output Overvoltage (01110): Output overvoltage is detected by the LT8228 by the FB1 and FB2 pins. In buck mode, if the FB2 voltage rises above the overvoltage threshold of 1.3V typically, the status is reported as a logic low. In boost mode, if the FB1 voltage rises above the overvoltage threshold of 1.3V typically, the status is reported as a logic low. This error stops switching and asserts the $\overline{FAULT}$ pin.

Reverse Current (01111): In buck mode, if the V_1 voltage drops close to V_2 voltage by 500mV or lower and the current through R_{SNS1} is higher than the reverse current threshold, the status is reported as a logic low. The LT8228 shorts the DG1 pin to V1 pin, turning off the protection MOSFET M1. As a result, the status of DG1 Undervoltage fault is also reported as a logic low. This error stops switching, asserts the $\overline{FAULT}$ pin, pulls the SS pin low, and IGND goes high impedance.

DG1 Undervoltage (0101): The LT8228 continuously monitors the gate-to-source voltage of the V_1 protection MOSFET M1 (DG1 – V_1). If the voltage drops below 4.5V typically, the status is reported as a logic low. In buck mode, this error stops switching, asserts the $\overline{FAULT}$ pin, pulls the SS pin low, and IGND goes high impedance. In boost mode, this error stops switching.

DG2 Undervoltage (0111): The LT8228 continuously monitors the gate-to-source voltage of the V_2 protection MOSFET M4 (DG2 – V_2). If the voltage drops below 4.5V typically, the status is reported as a logic low. This error stops switching, asserts the $\overline{FAULT}$ pin, pulls the SS pin low, and IGND goes high impedance.

BG MOSFET M3 Short (10100): The LT8228 checks for an BG MOSFET M3 short by looking at the overcurrent conditions at R_{SNS1} or R_{SNS2} . If the LT8228 detect BG MOSFET M3 short error, it shuts down all four external N-channel MOSFETs, pulls the SS pin low, asserts the $\overline{FAULT}$ pin, IGND goes high impedance and reports the status as a logic low.

TG MOSFET M2 Short (10101): The LT8228 checks for an TG MOSFET M3 short by looking at the overcurrent conditions at R_{SNS1} or R_{SNS2} . If the LT8228 detect TG MOSFET M2 short error, it shuts down all four external N-channel MOSFETs, pulls the SS pin low, asserts the $\overline{FAULT}$ pin, IGND goes high impedance and reports the status as a logic low.

Reference (10110): The LT8228 has two independent references. If one of the reference fall below or rises above the other reference by 10%, the LT8228 asserts the $\overline{FAULT}$ pin and reports the status as a logic low. When the controller is enabled or when any of the DRV_{CC} or $INTV_{CC}$ pin voltages are recovering from an undervoltage condition, and the LT8228 detects reference error, the part does not start-up.

EA1 (10111): The V_1 error amplifier regulates the FB1, ISET1N and ISET2N voltages for boost mode V_{1D} output voltage, V_1 output current and V_2 input current regulation respectively. When the controller is enabled or when any

APPLICATIONS INFORMATION

of the DRV_{CC} or $INTV_{CC}$ pin voltages are recovering from an undervoltage condition, the LT8228 checks the amplifier to validate its functionality. If EA1 fails this functionality check, the LT8228 does not start-up and the status is reported as a logic low.

EA2 (11010): The V_2 error amplifier regulates the FB2, ISET1P and ISET2P voltages for buck mode V_{2D} output voltage, V_1 input current and V_2 output current regulation respectively. When the controller is enabled, or when any of the DRV_{CC} or $INTV_{CC}$ pin voltages are recovering from an undervoltage condition, the LT8228 checks the amplifier to validate its functionality. If EA2 fails this functionality check, the LT8228 does not start-up and the status is reported as a logic low.

CSA1 (11011): The V_1 current sense amplifier senses V_1 current for current limiting and monitoring. When the controller is enabled or when any of the DRV_{CC} or $INTV_{CC}$ pin voltages are recovering from an undervoltage condition, the LT8228 checks the amplifier to validate its functionality. If CSA1 fails this functionality check, the LT8228 does not start-up and the status is reported as a logic low.

CSA2 (11100): The V_2 current sense amplifier senses V_2 current for current limiting and monitoring and inductor current sensing for current mode control. When the controller is enabled or when any of the DRV_{CC} or $INTV_{CC}$ pin voltages are recovering from an undervoltage condition, the LT8228 checks the amplifier to validate its functionality. If CSA2 fails this functionality check, the LT8228 does not start-up and the status is reported as a logic low.

Oscillator (11101): The oscillator is used to generate the LT8228's switching frequency and to synchronize with an external clock on the SYNC pin. When the controller is enabled, or when any of the DRV_{CC} or $INTV_{CC}$ pin voltages are recovering from an undervoltage condition, the LT8228 checks to see if the oscillator is functional. If it fails to oscillate, the LT8228 does not start-up and the status is reported as a logic low.

PARALLELING MULTIPLE LT8228s

The LT8228 provides masterless fault tolerant output current sharing among multiple LT8228s in parallel, enabling higher load current, better heat management and redundancy by using the ISHARE and IGND pins. The principle of the operation has been described in Paralleling Multiple Controllers in the Operation section.

In buck mode when the DRXN pin voltage is high, the ISHARE pin outputs a current equal to the ISET2P pin output current which represents V_2 output current. In boost mode when the DRXN pin voltage is low, the ISHARE pin outputs a current equal to the ISET1N pin output current which represents V_1 output current. Each LT8228 contributes their ISHARE pin current into a common node. When paralleling, tie the ISHARE pins of all the LT8228s together. For each LT8228, a local resistor R_{SHARE} is connected from the ISHARE pin to its own IGND pin. In buck mode, the ISET2P pin voltage regulates to the common ISHARE node voltage by modulating the internal reference voltage. To regulate each LT8228's V_2 output current to the average output current of all the LT8228s, make R_{SET2P} and R_{SHARE} equal. In boost mode, ISET1N pin voltage regulates to the ISHARE node voltage by modulating the internal reference voltage. To regulate each LT8228's V_1 output current to the average output current, make R_{SET1N} and R_{SHARE} values equal.

The maximum modulation of the internal reference voltage is ±5%. Refer to the Internal Reference vs ISHARE curve in the Typical Performance Characteristics section. The capacitor C_{SHARE} at the common ISHARE node is used for average current sharing. Select the ISET pin and ISHARE pin capacitors C_{SET2P}, C_{SET1N} and C_{SHARE} respectively such that the voltage ripple at these pins do not cause significant duty cycle jitter. Minimum capacitance of C_{SHARE} is equal or higher than the capacitance of C_{SET2P} or C_{SET1N}. The ground noise between the parallel stages can be coupled to the V_{C1}/V_{C2} nodes through ISHARE. This noise translates to SW node jitter. Decrease the compensation resistors R_{C1}/R_{C2} if such jitter problem arises.

APPLICATIONS INFORMATION

R_{SET2P} and R_{SET1N} can be set at different values as long as the ISHARE resistance is changed based on the mode of operation defined by the DRXN pin. An implementation is shown in Figure 23 where the ISHARE resistance is decreased when the DRXN pin voltage is high. This implementation is useful for applications where the buck output current is higher than the boost output current.

When multiple LT8228s are in parallel, they need to be in the same mode of operation to prevent cross-conduction between the phases. To keep the LT8228s in the same mode of operation, the DRXN pins of all the phases are connected together. Figure 24 shows two methods of configuring the DRXN pin for automatic mode selection. In the first method, the DRXN pins are tied together and pulled-up with a single resistor to an independent supply voltage. Only one phase is required to make the decision to enter boost mode while all phases are required to make the decision to enter buck mode. The pull-up resistor at the common DRXN node should be 50k or higher to ensure proper automatic mode selection.

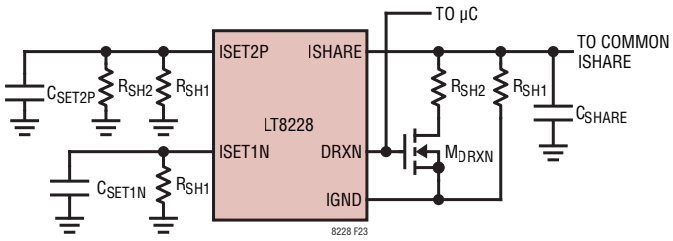


Figure 23. ISHARE Resistance Change Based on DRXN

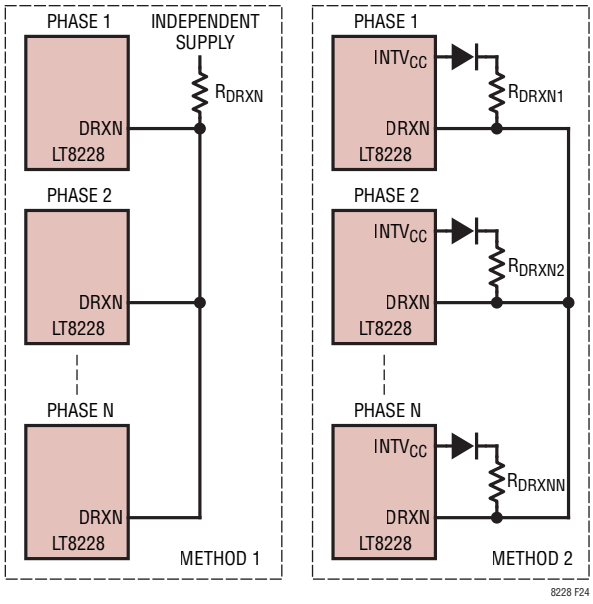


Figure 24. DRXN Pin Connection for Parallel LT8228s

In the second method, each LT8228's DRXN pin is pulled-up with its own pull-up resistor through a series diode to its own $INTV_{CC}$ pin and tied to a common DRXN node. The diode prevents any back conduction when an LT8228 is disabled or in a fault condition where $INTV_{CC}$ pin voltage is out of regulation. The resistance of the parallel connection of all the pull-up resistors should be 50k or higher to ensure proper automatic mode selection.

LT8228s are typically paralleled in high current applications. Since the ISHARE node is shared between the LT8228s but the grounds are not, differences in ground potential will impact the accuracy of current sharing. The differences between the ground potential of all the phases should be minimized. When possible, kelvin all grounds to a common ground.

BIAS, DRV_{CC}, $INTV_{CC}$ AND POWER DISSIPATION

An internal P-channel low dropout regulator produces 10V at the DRV_{CC} pin from the BIAS supply pin. Another P-channel low dropout regulator produces 4V at the $INTV_{CC}$ pin from the DRV_{CC} pin. DRV_{CC} powers the gate drivers and is the supply for the $INTV_{CC}$ regulator. $INTV_{CC}$ powers the internal circuitry.

The DRV_{CC} pin regulator supplies a peak current of 160mA and must be bypassed to ground with a minimum of 2.2µF ceramic capacitor. An additional 0.1µF ceramic capacitor placed directly adjacent to the DRV_{CC} pin and ground is highly recommended. Good bypassing is necessary to supply the high transient current required by MOSFET gate drivers.

Applications where the BIAS pin is supplied with high voltage or where large MOSFETs are being driven at high frequencies may cause the LT8228 to exceed its maximum junction temperature of 125°C (LT8228E, LT8228I) or 150°C (LT8228H). The LT8228 incorporates current

APPLICATIONS INFORMATION

limit, power fold back and thermal overload protection for the DRV_{CC} regulator. The current limit at DRV_{CC} should be carefully considered when selecting the switching frequency and the switching MOSFETs. For maximum current capability, externally supply BIAS with voltage 20V or less. Refer to the DRV_{CC} Current Limit Fold back curve in the Typical Performance Characteristics section.

The DRV_{CC} current is typically dominated by the top and bottom MOSFET gate charge current. The gate charge current can be estimated by multiplying the total gate charge Qg of the MOSFET and the switching frequency f of the LT8228. The total power dissipation PD inside the LT8228 in normal operation is approximated by Equation 45.

$$P_D = \left(V_{BIAS} - V_{DRVCC}\right) \bullet \left(\left(Q_{g(TOP)} + Q_{g(BOTTOM)}\right) \bullet f + I_{QBIAS}\right) \quad (45)$$

where I_{QBIAS} is the BIAS quiescent current when the LT8228 is enabled. Once the power dissipation is known, the junction temperature can be estimated by Equation 46.

$$T_J = T_A + \left(P_D \bullet \theta_{JA}\right) \quad (46)$$

where θ_{JA} (in °C/W) is the package thermal resistance from junction to ambient. For example, a typical application operating in continuous current operation where the Infineon BSC035N10NS5 with Q_g of 70nC is used for top and bottom MOSFET and the BIAS pin voltage is 48V while the LT8228 is operating at 150kHz switching frequency, the junction temperature is calculated by Equation 47.

$$T_J = 70°C + (48V - 10V) \bullet \left((70nC + 70nC) \bullet 150kHz + 3mA\right) \bullet 25°C/W = 92.8°C \quad (47)$$

The BIAS pin supplies the gate driver and the internal circuitry of the LT8228. This pin requires a minimum voltage of 8V. Since the BIAS pin is supplying the DRV_{CC} and $INTV_{CC}$ regulators, it should have the same level of capacitance or higher as the DRV_{CC} pin. Three possible options for the BIAS pin connection are shown in Figure 25.

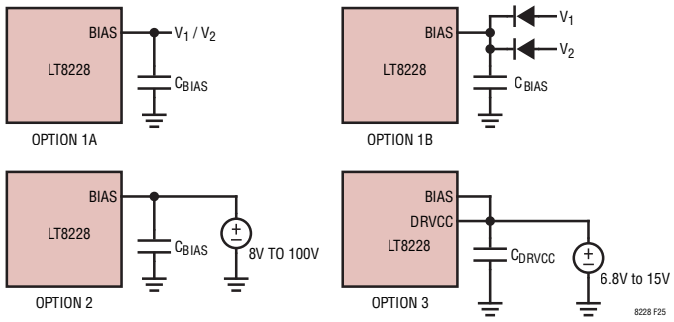


Figure 25. Possible Connections of BIAS Pin

1. Connect BIAS to either V_1 or V_2. The BIAS pin does not have negative voltage protection. Connect BIAS to the OR node of V_1 and V_2 using diodes if the terminal voltages may go negative. A minimum 8V is required at the BIAS pin for the LT8228 start-up and operation.
2. Connect BIAS to an independent supply. Minimize the voltage at the BIAS pin to lower power dissipation. Lowering the BIAS pin as low as 8V forces the DRV_{CC} LDO into dropout mode. Low BIAS pin voltage reduces the maximum DRV_{CC} current to 100mA. Refer to the DRV_{CC} Current Limit Fold back curve in the Typical Performance Characteristics section.
3. Connect BIAS to an independent supply and tie the BIAS and DRV_{CC} pins together. This ensures zero power dissipation in the DRV_{CC} regulator. Limit the supply voltage to 15V.

THERMAL SHUTDOWN

If the die junction temperature reaches approximately 165°C, the controller goes into thermal shutdown. All four external N-channel MOSFETs M1, M2, M3 and M4 are turned off, the $\overline{FAULT}$ and SS pins are pulled low and an over temperature error is reported at the $\overline{REPORT}$ pin. The controller will be re-enabled when the die temperature has dropped by 10°C typically. After re-enabling, the controller will turn on the V_1 and V_2 protection MOSFETs, perform a soft-start and then enter normal operation.

APPLICATIONS INFORMATION

PIN CLEARANCE/CREEPAGE CONSIDERATION

The LT8228 is available in FE38 Package. FE38 package has 0.5mm pitch between adjacent pins. ADI recommends conformal coating for FE38 packages in applications above 50V. For more information, refer to the printed circuit board design standards described in IPC-2221 (www.ipc.org).

EFFICIENCY CONSIDERATIONS

The efficiency of a switching regulator is equal to the output power divided by the input power times 100. It is often useful to analyze individual losses to determine what is limiting the efficiency and which changes would produce the most improvements. Although all dissipative elements in the circuit produce losses, four main sources account for most of the losses in LT8228 circuits:

1. DC I^2R Losses. These arise from the resistances of the MOSFETs, current sensing resistors, inductor and PC board traces which cause the efficiency to drop at high output currents.
2. Switching Losses. These losses arise from the brief amount of time top MOSFET M2 or bottom MOSFET M3 spends in the saturated region during switch node transitions. Power loss depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors. See the Power MOSFET Selection and Efficiency Considerations section for more details.
3. DRV_{CC} Current. This is the sum of the MOSFET driver current and internal $INTV_{CC}$ pin current. The difference between the BIAS input voltage and DRV_{CC} regulator's output voltage times the DRV_{CC} current represents lost power. This loss can be reduced by supplying BIAS with a voltage close to 10V plus the dropout voltage of the DRV_{CC} regulator from a high efficiency source. Refer to the DRV_{CC} Dropout Voltage curve in the Typical Performance Characteristics section. Lower capacitance MOSFETs can also reduce DRV_{CC} current and power loss.
4. C_{DM2} Loss. The capacitor at the drain of top MOSFET M2 filters the large input RMS current in buck mode and the large output RMS current in boost mode. C_{DM2} is required to have low ESR to minimize the AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.
5. Other Losses. Schottky diodes D2 and D3 are responsible for conduction losses during dead time and light load conduction periods. Inductor core loss occurs predominantly at light loads.

When adjusting to improve efficiency, the input current is the best indicator of changes in efficiency. If one change is made and the input current decreases, then the efficiency has increased. If there is no change in input current, then there is no change in efficiency.

PC BOARD LAYOUT CHECKLIST

The basic PC board layout requires a dedicated ground plane layer. For high current, a multilayer board provides heat sinking for power components.

- The ground plane layer should not have any traces and it should be as close as possible to the layer with the power MOSFETs.
- Place C_{DM2}, top MOSFET M2, bottom MOSFET M3 and D3 in one compact area.
- Use immediate vias to connect the components to the ground plane if the components are not in the same layer as the ground plane. Use several large vias for each power component.
- Use planes for V_1 and V_2 to maintain good voltage filtering and to keep power losses low.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to ground nets.
- Separate the signal and power grounds. All small-signal components should return to the exposed pad ground pin at one point.

APPLICATIONS INFORMATION

- Place bottom MOSFET M3 as close to the controller as possible, keeping the GND, BG and SW traces short.
- Keep the high dV/dT SW, BST, and TG nodes away from sensitive small-signal nodes.
- The C_{DM4} (–) terminal should be connected as close as possible to the (–) terminal of the C_{DM2} capacitor.
- Connect the top driver bootstrap capacitor, C_{BST}, closely to the BST and SW pins.
- Route the current sense leads, SNS1N with SNS1P and SNS2N with SNS2P, together with minimum PC trace spacing. Avoid sense lines passing through noisy areas, such as switch nodes. Ensure accurate current sensing with kelvin connections at the current sense resistors.
- Connect both VC pin compensation networks close to the IC, between the VC pins and the exposed pad ground pin.
- Connect the DRV_{CC} bypass capacitor, C_{DRVCC}, close to the IC, between the DRV_{CC} and exposed pad ground pin. This capacitor carries the MOSFET drivers' current peaks. An additional 0.1µF ceramic capacitor placed immediately next to the DRV_{CC} and exposed pad ground pin can help improve noise performance substantially.
- Connect the $INTV_{CC}$ bypass capacitor, C_{INTVCC}, close to the IC, between the $INTV_{CC}$ and the exposed pad ground pin.

DESIGN EXAMPLE

Requirements

Buck Mode:

Input Voltage, V_1 = 24V to 54V

Output Voltage, V_2 = 14V

Output Voltage Ripple, ΔV_2 = 100mV

V_2 Output Current Limit, $IV_{2P(LIM)}$ = 40A

V1 Input Current Limit, $I_{V1P(LIM)}$ = 24A

Boost Mode:

Input Voltage, V2 = 8V to 18V

Output Voltage, V_1 = 48V

Output Voltage Ripple, ΔV_1 = 300mV

V_2 Input Current Limit, $I_{V2N(LIM)}$ = 40A

V_1 Output Current Limit, $I_{V1N(LIM)}$ = 10A

Switching Frequency, f = 125kHz

Maximum Ambient Temperature, $T_{A(MAX)}$ = 70°C

Reverse voltage protection needed at both the V_1 and the V_2 terminal.

R_T Selection: From Table 1, the R_T resistance for 125kHz switching frequency is 78.7kΩ.

Inductor Selection: In buck mode, the maximum inductor ripple current occurs at highest input voltage. For 40% maximum inductor peak-to-peak ripple current, the minimum inductance requirement for buck mode is given by Equation 48.

$$L_{BUCK} > \frac{14V(54V-14V)}{125kHz \bullet 16A \bullet 54V} = 5.2\mu H \quad (48)$$

In boost mode, the maximum inductor ripple current occurs when the V_2 voltage is half of the V_1 voltage. Since the maximum V_2 voltage is not as high as half of the V_1 voltage in this application, the maximum inductor ripple current happens when the V_2 voltage is highest. For 40% maximum inductor peak-to-peak ripple current, the minimum inductance requirement for boost mode is given by Equation 49.

$$L_{BOOST} > \frac{18V(48V-18V)}{125kHz \bullet 16A \bullet 48V} = 5.6\mu H \quad (49)$$

A 10µH inductor is selected due to availability which produces 20.7% ripple current in buck mode and 22.5% ripple current in boost mode.

R_{SNS2}, and R_{IN2} Selection: The maximum current in the inductor in buck and boost modes are given by Equation 50

$$L_{LMAXBUCK} = 40A + \frac{1}{2}\frac{14V(54V-14V)}{125kHz \bullet 10\mu H \bullet 54V} = 44.1A$$
$$L_{LMAXBOOST} = 40A + \frac{1}{2}\frac{18V(48V-18V)}{125kHz \bullet 10\mu H \bullet 48V} = 44.5A \quad (50)$$

APPLICATIONS INFORMATION

The maximum inductor current in boost mode is higher than the buck mode. The peak inductor current $I_{L(PEAK)}$ is selected to be 54A which is 21% higher than the maximum inductor current in buck mode. The voltage drop across R_{SNS2} current sense resistor is selected to be 80mV for 40A V_2 output current limit. R_{SNS2} value is calculated according to Equation 51.

$$R_{SNS2} = \frac{80mV}{40A} = 2m\Omega \quad (51)$$

R_{IN2} value is calculated according to Equation 52.

$$R_{IN2} = \frac{54A \bullet 2m\Omega}{72.5\mu A} = 1.5k\Omega \quad (52)$$

R_{SNS2} and R_{IN2} resistance values are selected to be 2mΩ and 1.5kΩ respectively based on availability. The power dissipation at the current sense resistor R_{SNS2} at V_2 output current limit is given by Equation 53.

$$P_{RSNS2} = 80mV \bullet 40A = 3.2W \quad (53)$$

The selected R_{SNS2} has a power rating of 5W to ensure performance. This combination of R_{SNS2}, R_{IN2}, and switching frequency and Inductor also satisfies the condition for $L_{OPTIMAL}$ given in the inductor selection section.

R_{SET2P} and R_{SET2N} Selection: The resistance values of R_{SET2P} and R_{SET2N} are calculated using Equation 54 based on the given specification for V_2 output current limit $I_{V2P(LIM)}$ in buck mode and V_2 input current limit $I_{V2N(LIM)}$ in boost mode.

$$R_{SET2P} = \frac{1.5k\Omega}{2m\Omega \bullet 40A} \bullet 1.21V = 22.7k\Omega$$
$$R_{SET2N} = \frac{1.5k\Omega}{2m\Omega \bullet 40A} \bullet 1.21V = 22.7k\Omega \quad (54)$$

R_{SET2P} and R_{SET2N} resistance values are selected to be 22.6kΩ based on availability.

R_{MON2} Selection: $V_{MON2MAX}$ is selected to be 2V based on the ADC input specification. The resistance of R_{MON2} is calculated using Equation 55.

$$R_{MON2} = \frac{1.5k\Omega}{40A \bullet 2m\Omega} \bullet 2V = 37.5k\Omega \quad (55)$$

R_{MON2} resistance value is selected to be 37.4kΩ based on availability.

R_{SNS1} and R_{IN1} Selection: For accuracy consideration, the maximum voltage drop across R_{SNS1} is selected to be 100mV. Maximum current through R_{SNS1} is 54A peak inductor current. The R_{SNS1} resistance is calculated using Equation 56 based on the buck mode specification.

$$R_{SNS1} = \frac{100mV}{54A} = 1.9m\Omega \quad (56)$$

R_{SNS1} is selected to be 2mΩ due to availability. R_{IN1} is chosen so that the maximum feedback current in CSA1 is less than 72.5µA (Equation 57).

$$R_{IN1} = \frac{54A \bullet 2m\Omega}{72.5\mu A} = 1.5k\Omega \quad (57)$$

R_{SNS1} and R_{IN1} resistance values are selected to be 2mΩ and 1.5kΩ respectively. The power dissipation at the current sense resistor R_{SNS1} at V_1 input current limit is given byEquation 58.

$$P_{RSNS1} = (24A)^2 \bullet 2m\Omega = 1.2W \quad (58)$$

The selected R_{SNS1} has a power rating of 3W to ensure performance.

R_{SET1P} and R_{SET1N} Selection: The resistance values of R_{SET1P} and R_{SET1N} are calculated using Equation 59 based on the given specification for V_1 input current limit $I_{V1P(LIM)}$ in buck mode and V_1 output current limit $I_{V1N(LIM)}$ in boost mode.

$$R_{SET1P} = \frac{1.5k\Omega}{2m\Omega \bullet 24A} \bullet 1.21V = 37.8k\Omega$$
$$R_{SET1N} = \frac{1.5k\Omega}{2m\Omega \bullet 10A} \bullet 1.21V = 90.8k\Omega \quad (59)$$

R_{SET1P} and R_{SET1N} resistance values are selected to be 37.4kΩ and 88.7kΩ respectively based on availability.

R_{MON1} Selection: $V_{MON1MAX}$ is selected to be 2V based on the ADC input specification. The resistance of R_{MON1} is calculated using Equation 60.

$$R_{MON1} = \frac{1.5k\Omega}{24A \bullet 2m\Omega} \bullet 2V = 62.5k\Omega \quad (60)$$

APPLICATIONS INFORMATION

R_{MON1} resistance value is selected to be 61.9kΩ based on availability.

R_{FB2B}, R_{FB2A}, R_{FB1B} and R_{FB2B} Selection: The bottom resistors R_{FB2B} and R_{FB1B} are selected to be 1.21kΩ for 1mA bias current in the resistor dividers. The resistance R_{FB2A} and R_{FB1A} are calculated based on Equation 61.

$$R_{FB2A} = \left(\frac{14V}{1.21V} - 1\right) \bullet 1.21k\Omega = 12.8k\Omega$$
$$R_{FB1A} = \left(\frac{48V}{1.21V} - 1\right) \bullet 1.21k\Omega = 46.8k\Omega \quad (61)$$

R_{FB2B} and R_{FB1B} resistance values are selected to be 13kΩ and 47.5kΩ respectively based on availability.

R_{UV2B}, R_{UV2A}, R_{UV1B} and R_{UV2B} Selection: The bottom resistors R_{UV2B} and R_{UV1B} are selected to be 12.1kΩ for 100µA bias current in the resistor dividers. The resistance R_{UV2A} and R_{UV1A} are calculated by Equation 62.

$$R_{FB2A} = \left(\frac{14V}{1.21V} - 1\right) \bullet 1.21k\Omega = 12.8k\Omega$$
$$R_{FB1A} = \left(\frac{48V}{1.21V} - 1\right) \bullet 1.21k\Omega = 46.8k\Omega \quad (62)$$

R_{UV2A} and RU_{V1A} resistance values are selected to be 69.8kΩ and 232kΩ respectively based on availability.

M1, M2, M3 and M4 Selection: In case of V_1 protection MOSFETs, the maximum voltage requirement is 54V. V_2 protection MOSFETs need to protect against reverse voltage. Therefore, the maximum voltage requirement is 28V. The Infineon IPT007N06N has:

BVD_{SS} = 60V

$R_{DS(ON)}$ = 0.75mΩ (max)

$V_{TH(IL)}$ = 2.8V

The power dissipations of the MOSFETs are checked in their worst-case condition. For V_1 protection MOSFET M1, the worst case is when the V_1 input current is maximum in buck mode (Equation 63).

$$P_{d(M1)} = 24^2 \bullet 0.75m\Omega = 0.43W \quad (63)$$

For V_2 protection MOSFET M4, the worst case is when V_2 output current is maximum in buck mode (Equation 64).

$$P_{d(M4)} = 40^2 \bullet 0.75m\Omega = 1.2W \quad (64)$$

The maximum voltage requirement for the switching MOSFETs M2 and M3 are 54V plus some ringing. The Infineon IAUC70N08S5N074 has:

BVD_{SS} = 80V

$R_{DS(ON)}$ = 7.4mΩ (Max)

C_{MILLER} = 130pF

$V_{TH(IL)}$ = 3.0V

J_A = 42K/W

To reduce the temperature rise to meet ambient temperature specification, 4 MOSFETs are used in parallel for both the TG MOSFET M2 and BG MOSFET M3. In buck mode, power dissipation in the top MOSFET M2 and the bottom MOSFET M3 are given by Equation 65.

$$P_{M2(BUCK)} = \frac{14V}{48V} \bullet \left(\frac{40}{4}\right)^2 \bullet 7.4m\Omega + 48V^2 \bullet \frac{40A}{2} \bullet 2\Omega \bullet 130pF \bullet \left[\frac{1}{10V - 3V} + \frac{1}{3V}\right] \bullet 125kHz = 0.86W + 0.96W = 1.83W$$
$$P_{M3(BUCK)} = \frac{48V - 14V}{48V} \bullet \left(\frac{40}{4}\right)^2 \bullet 7.4m\Omega = 2.10W \quad (65)$$

In Boost mode, power dissipation in the top MOSFET M2 and the bottom MOSFET M3 are given by Equation 66.

$$P_{M2(BOOST)} = \frac{14V}{48V} \bullet \left(\frac{40}{4}\right)^2 \bullet 7.4m\Omega = 0.86W$$
$$P_{M3(BOOST)} = \frac{48V = 14V \bullet 48V}{14V^2} \bullet \left(\frac{10}{4}\right)^2 \bullet 7.4m\Omega + \frac{48V^3}{14V} \bullet \frac{10}{4}\frac{1}{2} \bullet 2\Omega \bullet 130pF \bullet \left[\frac{1}{10V - 3V} + \frac{1}{3V}\right] \bullet 125kHz = 1.54W + 0.02W = 1.56W \quad (66)$$

APPLICATIONS INFORMATION

The worst-case power dissipation is 1.83W in M2 and 2.10W in M3.

C_{DM2} and C_{DM1} Selection: C_{DM1} and C_{DM2} are selected to meet the RMS current requirement in buck mode. For $I_{LMAXBUCK}$ of 40A, the maximum RMS current is 20A. Ten TDKCKG57NX72A capacitors are tied in parallel for C_{DM1} where each capacitor has 2A of RMS current. Each capacitor is 22µF with 10mΩ of ESR. One aluminum electrolytic capacitor with high bulk capacitance of 68µF and high ESR of 320mΩ is selected for C_{DM1} to reduce the source impedance. Six TDKCKG32KX7RA capacitors are tied in parallel for C_{DM1} where each capacitor has 2A of RMS current. Each capacitor is 1µF with 10mΩ of ESR.

The ESR dominates the boost mode ripple voltage which is given by Equation 67.

$$\Delta V_{ESR(CDM2)} = 44.5A \bullet \frac{10m\Omega}{16} = 278mV \quad (67)$$

Therefore, the selected capacitors for C_{DM2} meet the given voltage ripple specification for boost output.

C_{DM4} Selection: C_{DM4} is selected to meet the ripple voltage requirement at V_{2D} in buck mode. Eight TDKCGA8P1X7R capacitors are tied in parallel at the V_{2D} node. The ripple voltage is given by Equation 68.

$$\Delta V2D = 44.5A \bullet \frac{10m\Omega}{16} = 278mV \quad (68)$$

Therefore, the selected capacitors for C_{DM4} meet the given voltage ripple specification for buck output. One aluminum electrolytic capacitor with high bulk capacitance of 100µF and high ESR of 30mΩ are also added to reduce the source impedance.

CV1 and CV2 Selection: A 10µF ceramic capacitor with 100mΩ series resistance is used at each V_1 and V_2 node for input bypass and resonance reduction.

C_{DG1}, CDG2, R_{DG1}, and R_{DG2} Selection: For 500mA of buck inrush current (Equation 69).

$$C_{DG1} = \frac{10\mu A \bullet (68\mu F + 10 \bullet 22\mu F)}{500mA} = 5.76nF \quad (69)$$

C_{DG1} is selected to be 6.8nF based on availability. R_{DG1} is selected to be 20kΩ to stabilize boost V_1 short current regulation loop.

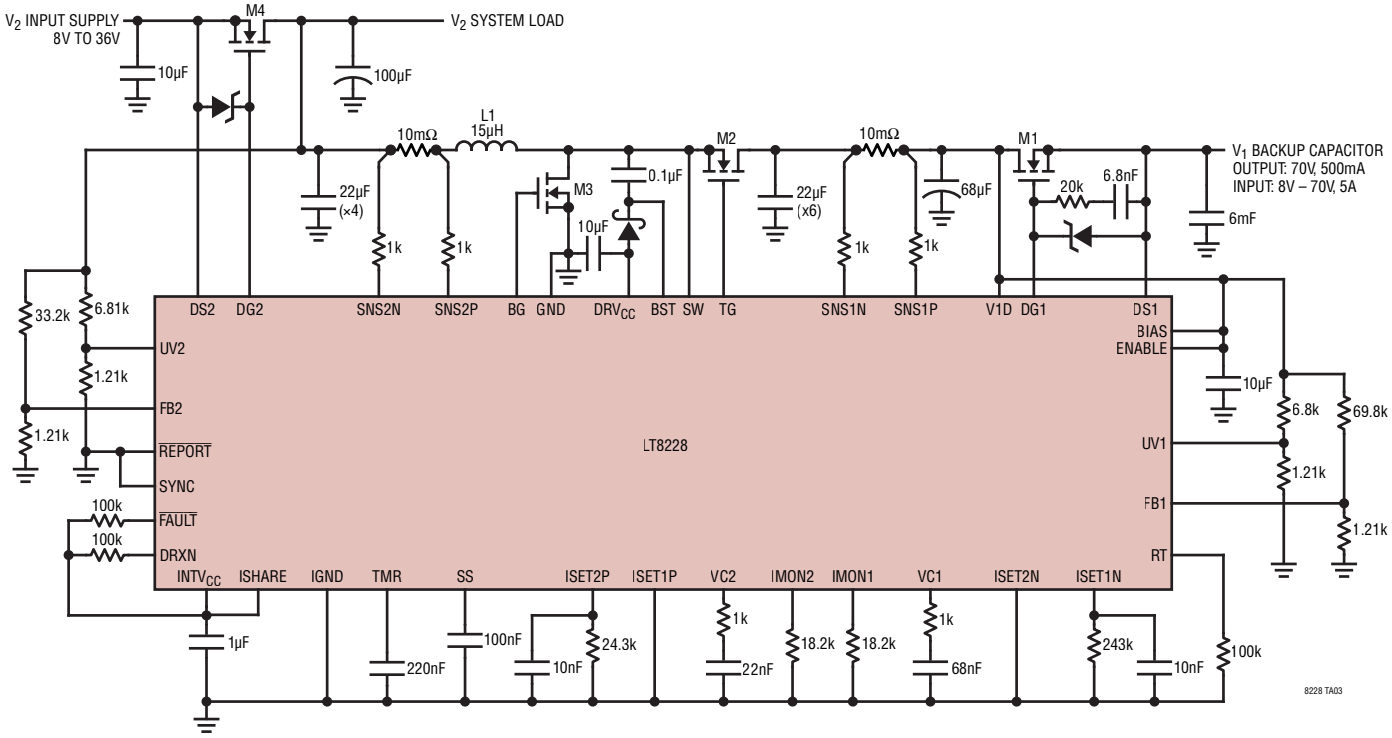
For 1A of boost inrush current (Equation 70).

$$C_{DG2} = \frac{10\mu A \bullet (100\mu F + 8 \bullet 22\mu F)}{1A} = 2.76nF \quad (70)$$

C_{DG2} is selected to be 3.3nF based on availability. R_{DG2} is selected to be 10kΩ to prevent slowdown of DG2 turn-off speed.

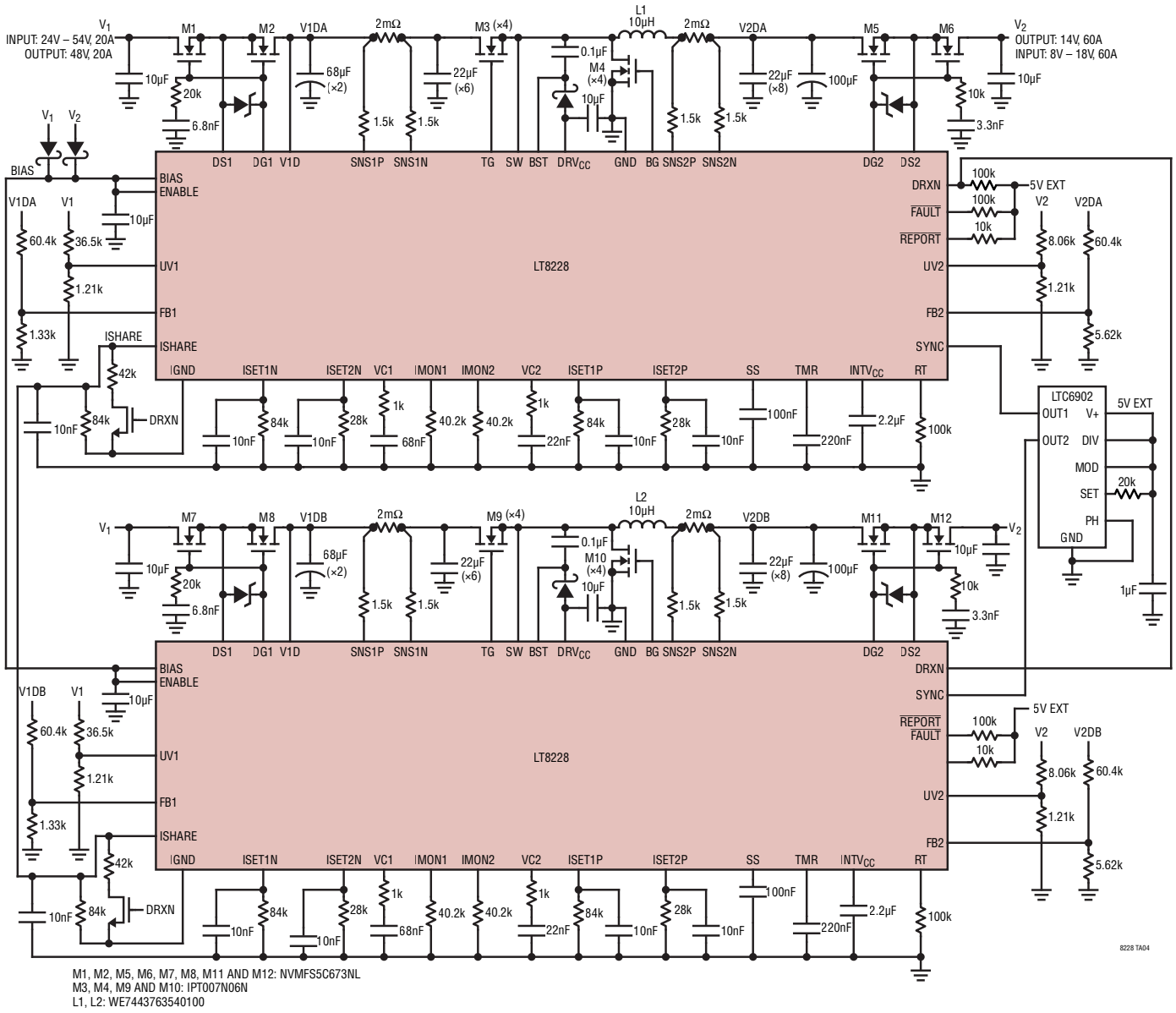
TYPICAL APPLICATIONS

2.5J Power Interrupt Protection



TYPICAL APPLICATIONS

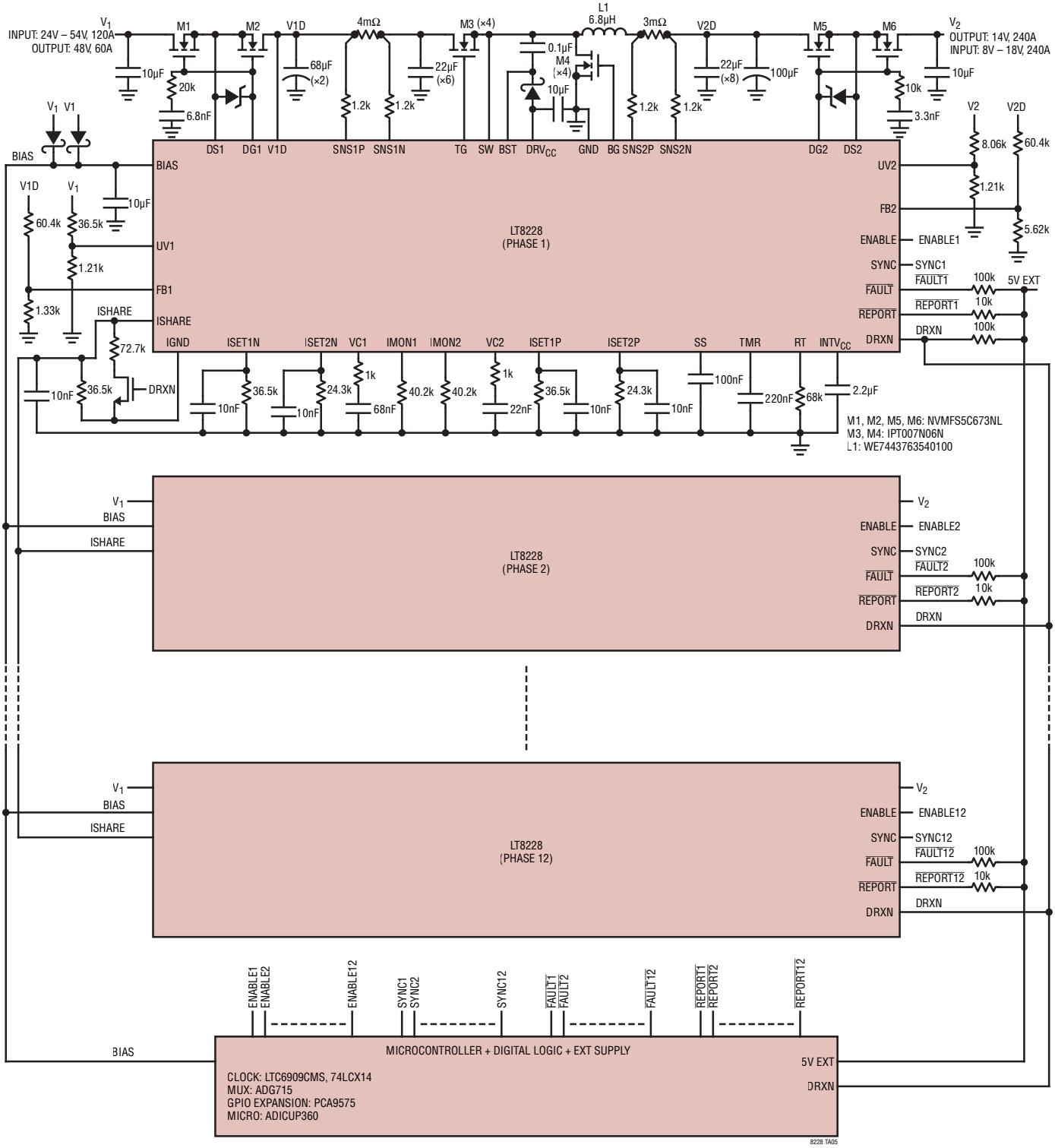
Buck 840W (14V 60A) and Boost 960W (48V 20A) Parallel Regulators



M1, M2, M5, M6, M7, M8, M11 AND M12: NVMFS5C673NL
M3, M4, M9 AND M10: IPT007N06N
L1, L2: WE7443763540100

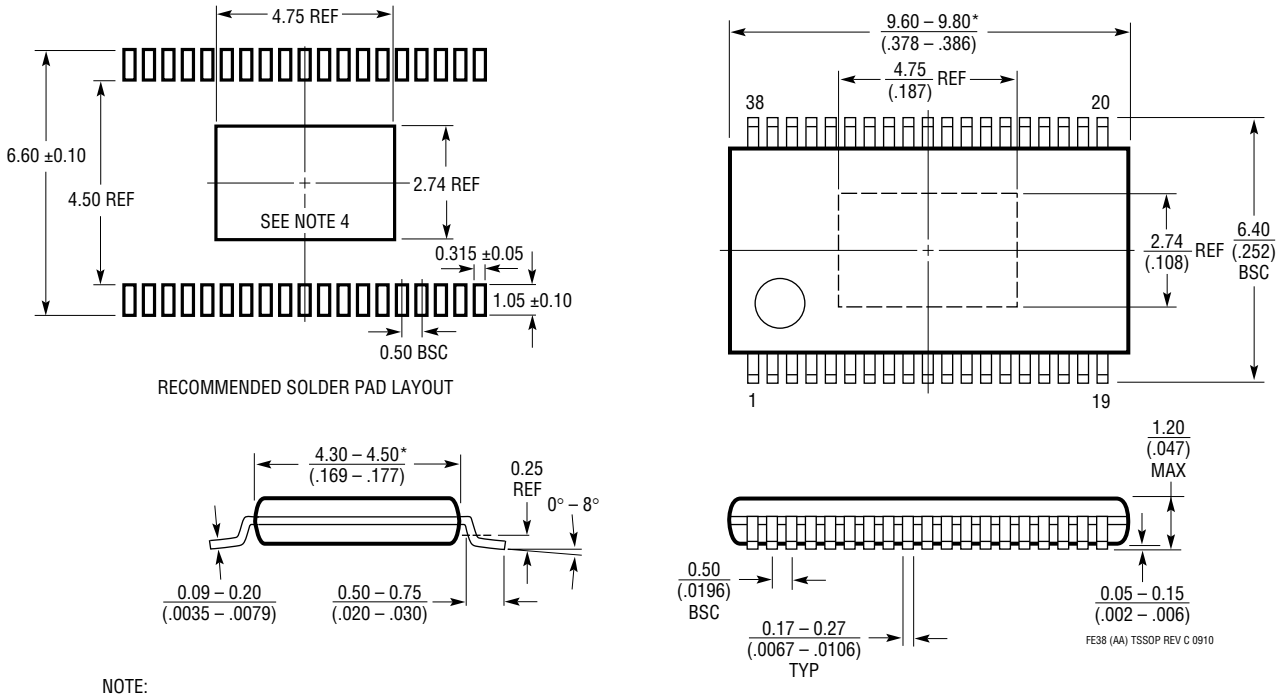
TYPICAL APPLICATIONS

3kW (14V 240A) and Boost 3kW (48V 60A) 12-Phase Parallel Regulators



PACKAGE DESCRIPTION

FE Package
38-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1772 Rev C)
Exposed Pad Variation AA

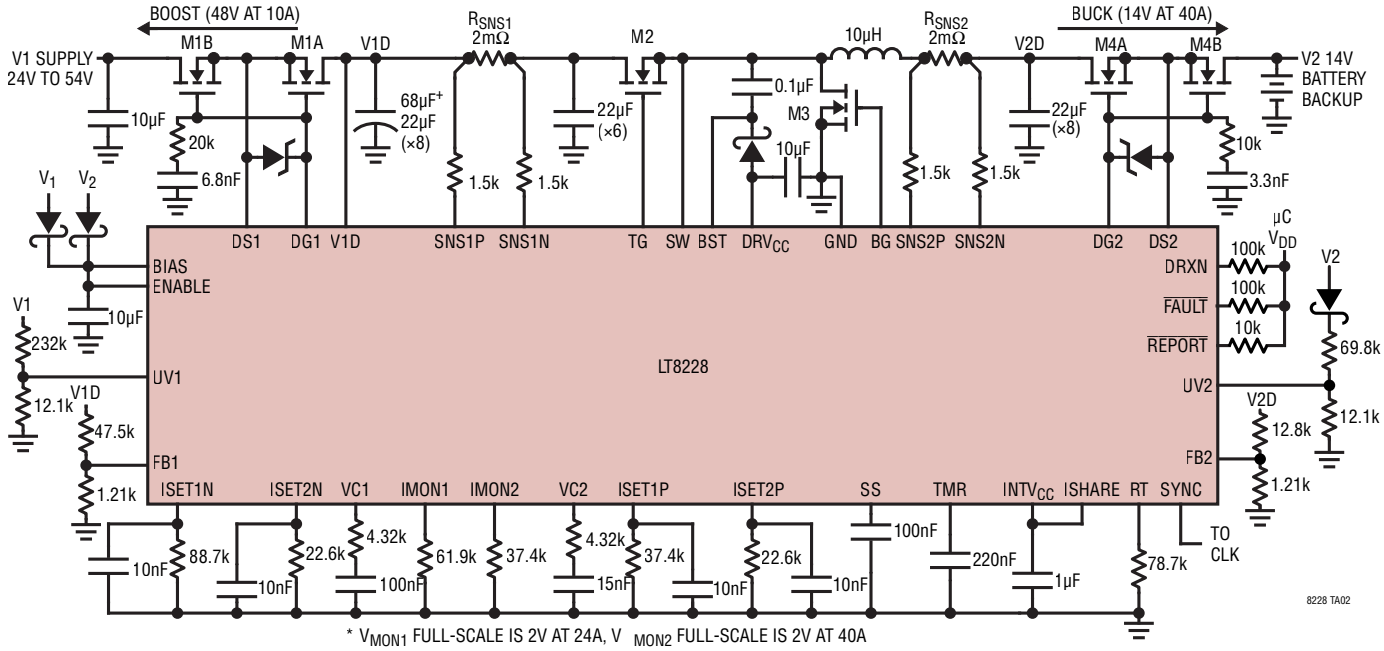


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

TYPICAL APPLICATION

Buck 560W (14V 40A) and Boost 480W (48V 10A) Parallel Regulators



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8708	80V Bidirectional Synchronous 4-Switch Buck-Boost DC/DC Controller	2.8V (Need $EXTV_{CC}$ > 6.4V) ≤ V_{IN} ≤ 80V, 1.3V ≤ V_{OUT} ≤ 80V, 5mm × 8mm QFN-40. Ideal for Automotive Same Battery Voltage
LTC®3871	Bidirectional Multiphase DC/DC Synchronous Buck or Boost On-Demand Controller	V_{IN} Up to 100V, V_{OUT} Up to 30V, Ideal for High Power 48V/12V Automotive Battery Applications
LT8705A	80V V_{IN} and V_{OUT} Synchronous 4-Switch Buck-Boost DC/DC Controller	2.8V ≤ V_{IN} ≤ 80V, Input and Output Current Monitor, 5mm × 7mm QFN-38 and TSSOP-38
LTC3779	150V V_{IN} and V_{OUT} Synchronous 4-Switch Buck-Boost Controller	4.5V ≤ V_{IN} ≤ 150V, 1.2V ≤ V_{OUT} ≤ 150V, Up to 99% Efficiency Drives Logic-Level or STD Threshold MOSFETs, TSSOP-38
LTC7813	60V Low I_Q Synchronous Boost + Buck Controller Low EMI and Low Input/Output Ripple	4.5V (Down to 2.2V After Start-up) ≤ V_{IN} ≤ 60V, Boost V_{OUT} Up to 60V, 0.8V ≤ Buck V_{OUT} ≤ 60V, I_Q = 29µA, 5mm × 5mm QFN-32
LTC3899	60V, Triple Output, Buck/Buck/Boost Synchronous Controller with 29µA Burst Mode Operation I_Q	4.5V (Down to 2.2V After Start-Up) ≤ V_{IN} ≤ 60V, V_{OUT} Up to 60V, Buck V_{OUT} Range: 0.8V to 60V, Boost V_{OUT} Up to 60V
LTC3769	60V Low I_Q Synchronous Boost Controller	4.5V (Down to 2.5V After Start-Up) ≤ V_{IN} ≤ 60V, V_{OUT} Up to 60V, I_Q = 28µA PLL Fixed Frequency 50kHz to 900kHz.
LTM®8056	58V Buck-Boost µModule Regulator, Adjustable Input and Output Current Limiting	5V≤ V_{IN} ≤ 58V, 1.2V ≤ V_{OUT} ≤ 48V, 15mm × 15mm × 4.92mm BGA Package
LTC3895/ LTC7801	150V Low I_Q, Synchronous Step-Down DC/DC Controller with 100% Duty Cycle	4V ≤ V_{IN} ≤ 140V, 150V ABS Max, PLL Fixed-Frequency 50kHz to 900kHz, 0.8V ≤ V_{OUT} ≤ 60V, Adjustable 5V to 10V Gate Drive, I_Q = 40µA, 4mm × 5mm QFN-24, TSSOP-24, TSSOP-38(31)
LTC7103	105V, 2.3A Low EMI Synchronous Step-Down Regulator	4.4V ≤ V_{IN} ≤ 105V, 1V ≤ V_{OUT} ≤ V_{IN}, I_Q = 2µA, Fixed-Frequency 200kHz to 2MHz, 5mm × 6mm QFN

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Switching Controllers ***category:***

Click to view products by Analog Devices ***manufacturer:***

Other Similar products are found below :

AZ7500EP-E1 NCP1218AD65R2G NCP1234AD100R2G NCP1244BD065R2G NCP1336ADR2G NCP6153MNTWG NCP81101BMNTXG NCP81205MNTXG SJE6600 SMBV1061LT1G SG3845DM NCP4204MNTXG NCP6132AMNR2G NCP81102MNTXG NCP81203MNTXG NCP81206MNTXG NX2155HCUPTR UBA2051C MAX8778ETJ+ NTBV30N20T4G NCP1015ST65T3G NCP1240AD065R2G NCP1240FD065R2G NCP1361BABAYSNT1G NTC6600NF NCP1230P100G NCP1612BDR2G NX2124CSTR SG2845M NCP81101MNTXG TEA19362T/1J IFX81481ELV NCP81174NMNTXG NCP4308DMTTWG NCP4308DMNTWG NCP4308AMTTWG NCP1251FSN65T1G NCP1246BLD065R2G NTE7154 NTE7242 LTC7852IUFD-1#PBF LTC7852EUFD-1#PBF MB39A136PFT-G-BND-ERE1 NCP1256BSN100T1G LV5768V-A-TLM-E NCP1365BABCYDR2G NCP1365AABCYDR2G MCP1633T-E/MG MCP1633-E/MG NCV1397ADR2G