60V 2MHz Low-I_Q Boost, SEPIC and Flyback Controller

FEATURES

- **Wide Input Voltage Range: 3V to 60V**
- **Low I_Q Burst Mode® Operation: 8µA**
- **Up to 95% Efficiency at 2MHz**
- **±1.5% Internal 1V Voltage Reference**
- 5V Split Gate Drive for Efficiency and EMI Optimization
- 100kHz to 2MHz Fixed Switching Frequency with External Clock Synchronization
- Spread Spectrum Frequency Modulation for Low EMI
- Accurate Enable Threshold with Hysteresis
- Programmable Output Soft-Start and Tracking
- Thermally-Enhanced 12-Lead MSOP Package

APPLICATIONS

- Automotive and Industrial Systems
- Battery-Powered Systems
- Portable Electronic Equipment

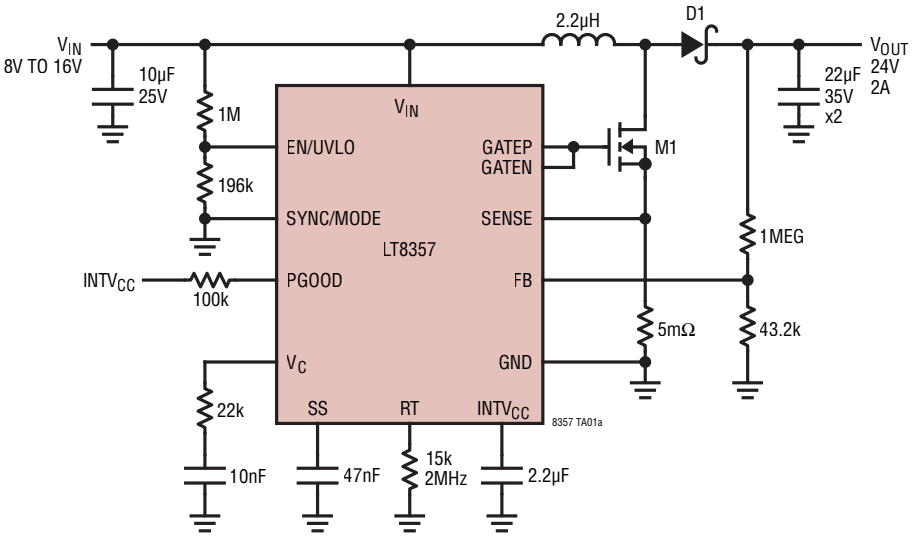
DESCRIPTION

The LT®8357 is a wide input range, current mode, DC/DC controller which can be configured as a boost, SEPIC or flyback converter. The LT8357 drives a low side N-channel power MOSFET with 5V split gate drive. The current mode architecture allows adjustable and synchronizable 100kHz to 2MHz fixed frequency operation, or internal 19% triangle spread spectrum operation for low EMI. At light load, either pulse-skipping mode or low-ripple Burst Mode operation can be selected. Additional features include output power good and output short circuit protection in SEPIC and flyback configurations.

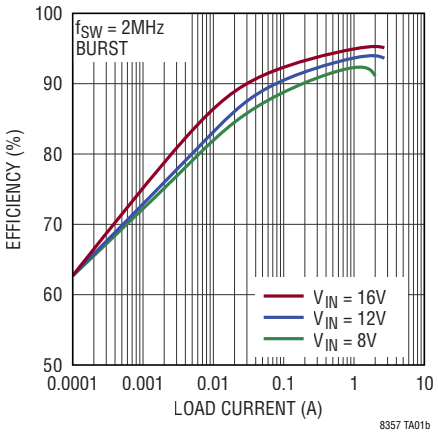
With a wide 3V to 60V input voltage range and 8µA low quiescent current, the LT8357 provides a simple, compact and efficient solution for automotive, industrial, and battery-powered systems.

TYPICAL APPLICATION

2MHz, 8V to 16V Input, 24V/2A Output Boost Converter



Efficiency vs Load Current

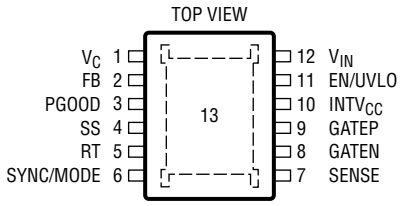


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, EN/UVLO ..... –0.3V to 60V
SENSE ..... –0.3V to 0.3V
$INTV_{CC}$ ..... –0.3V to 6V
SYNC/MODE, RT, SS, PGOOD, FB, V_C ..... –0.3V to 6V
GATEP, GATEN ..... (Note 2)
Operating Junction Temperature Range (Notes 3, 4)
LT8357E ..... –40°C to 125°C
LT8357J ..... –40°C to 150°C
LT8357H ..... –40°C to 150°C
Storage Temperature Range
MSOP ..... –65°C to 150°C

PIN CONFIGURATION



MSE PACKAGE
12-LEAD PLASTIC MSOP

θ_{JA} = 40°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8357EMSE#PBF	LT8357EMSE#TRPBF	8357	12-Lead Plastic MSOP	–40°C to 125°C
LT8357JMSE#PBF	LT8357JMSE#TRPBF	8357	12-Lead Plastic MSOP	–40°C to 150°C
LT8357HMSE#PBF	LT8357HMSE#TRPBF	8357	12-Lead Plastic MSOP	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 3). V_{IN} = 12V, EN/UVLO = 1.5V, C_{INTVCC} = 2.2µF to GND, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply						
V_{IN} Operating Voltage Range		●	3		60	V
V_{IN} Quiescent Current						
In Shutdown	$V_{EN/UVLO}$ = 0.3V			1.7	3	µA
In Sleep Mode (Not Switching)	V_{FB} = 1.05V, $V_{SYNC/MODE}$ = 0V			8	20	µA
In Active Mode (Not Switching)	V_{FB} = 1.05V, $V_{SYNC/MODE}$ = Float			830	1200	µA
Logic Input						
EN/UVLO Shutdown Threshold		●	0.3	0.6	0.9	V
EN/UVLO Enable Threshold	Rising	●	1.183	1.220	1.257	V
EN/UVLO Enable Hysteresis				42		mV
EN/UVLO Input Bias Current	$V_{EN/UVLO}$ = 60V		-50		50	nA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 3). V_{IN} = 12V, EN/UVLO = 1.5V, C_{INTVCC} = 2.2µF to GND, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Linear Regulator						
$INTV_{CC}$ Regulation Voltage	I_{INTVCC} = 20mA		4.70	4.95	5.20	V
$INTV_{CC}$ Current Limit	V_{INTVCC} = 4.5V		40	60	80	mA
$INTV_{CC}$ Undervoltage Lockout Threshold	Falling		2.4	2.5	2.6	V
$INTV_{CC}$ Undervoltage Lockout Hysteresis				100		mV
Error Amplifier						
FB Regulation Voltage		●	0.985	1.000	1.015	V
FB Line Regulation	3V < V_{IN} < 60V			0.1	0.4	%
FB Input Bias Current	V_{FB} = 1V		–20		20	nA
FB Error Amplifier Transconductance g_m				200		µS
V_C Output Impedance				2		MΩ
Current Comparator						
SENSE Maximum Current Threshold	V_{FB} = 0.85V, $V_{SYNC/MODE}$ = 0V	●	45	60	75	mV
SENSE Burst Current Threshold	V_{FB} = 1.05V, $V_{SYNC/MODE}$ = 0V			10		mV
SENSE Over Current Threshold				105		mV
SENSE Pin Bias Current	V_{FB} = 1.05V, V_{SENSE} = 0V, Out of Pin			27		µA
Fault						
PGOOD Upper Threshold Offset from V_{FB}	Rising	●	6	8	10	%
PGOOD Lower Threshold Offset from V_{FB}	Falling	●	–10	–8	–6	%
PGOOD Pull-Down Resistance				110		Ω
SS Strong Pull-Down Resistance				55		Ω
SS Pull-Up Current	V_{SS} = 0V			15		µA
SS Pull-Down Current	V_{SS} = 2V			1.5		µA
Oscillator						
Switching Frequency	R_T = 95.3kΩ R_T = 15.0kΩ	 ●	315 1900	350 2000	385 2100	kHz kHz
SYNC Frequency	$f_{SYNC/MODE}$ = f_{RT}		100		2000	kHz
SYNC Threshold Voltage			0.4		2.5	V
Highest Spread Spectrum Above Oscillator Frequency	$V_{SYNC/MODE}$ = 5V, R_T = 95.3kΩ $V_{SYNC/MODE}$ = 5V, R_T = 15.0kΩ			19 19		% %
Gate Driver						
GATE Pull-Up Resistance				2.2		Ω
GATE Pull-Down Resistance				0.9		Ω
GATE Minimum Duty Cycle	R_T = 95.3kΩ R_T = 15.0kΩ		2 8	3.5 11	5 14	% %
GATE Maximum Duty Cycle	R_T = 95.3kΩ R_T = 15.0kΩ		92.5 87	95 90	97.5 93	% %

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 3). V_{IN} = 12V, EN/UVLO = 1.5V, C_{INTVCC} = 2.2µF to GND, unless otherwise noted.

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

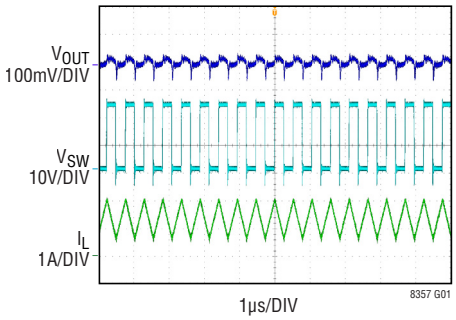
Note 2: Do not apply a positive or negative voltage source to these pins, otherwise permanent damage may occur.

Note 3: The LT8357E is guaranteed to meet performance specifications from 0°C to 125°C operating junction temperature. Specifications over the -40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8357J and LT8357H are guaranteed over the –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 4: The LT8357 includes over temperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability.

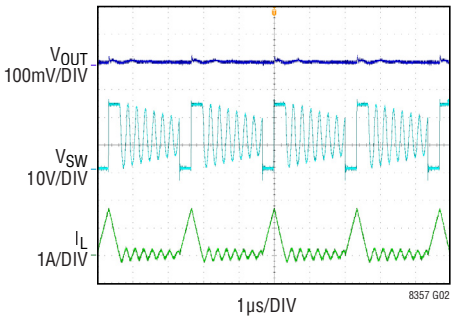
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Switching Waveforms (in CCM)



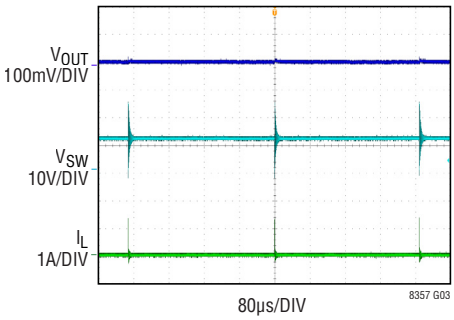
FRONT PAGE APPLICATION
V_{IN} = 12V, V_{OUT} = 24V, I_{OUT} = 600mA

Switching Waveforms (in DCM/ Light Burst Mode)



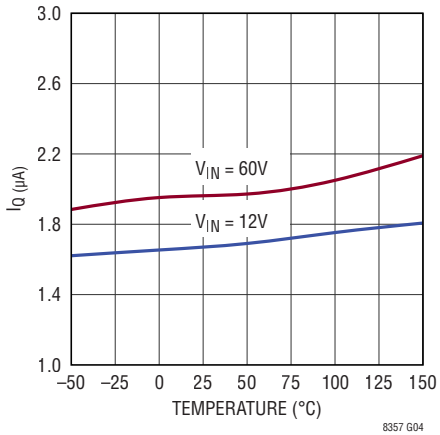
FRONT PAGE APPLICATION
V_{IN} = 12V, V_{OUT} = 24V, I_{OUT} = 100mA

Switching Waveforms (in Deep Burst Mode)

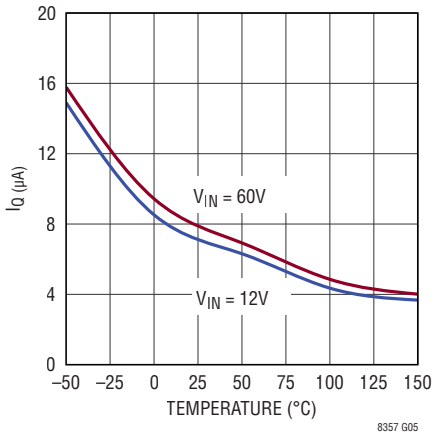


FRONT PAGE APPLICATION
V_{IN} = 12V, V_{OUT} = 24V, I_{OUT} = 0mA

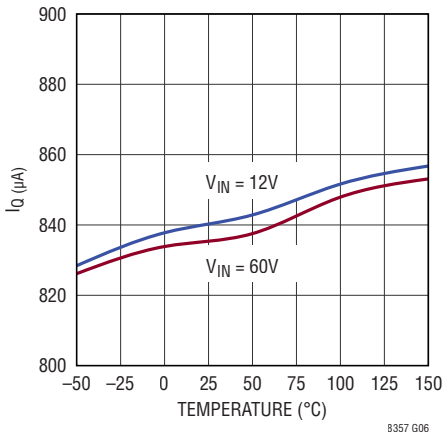
V_{IN} Quiescent Current (Shutdown) vs Temperature



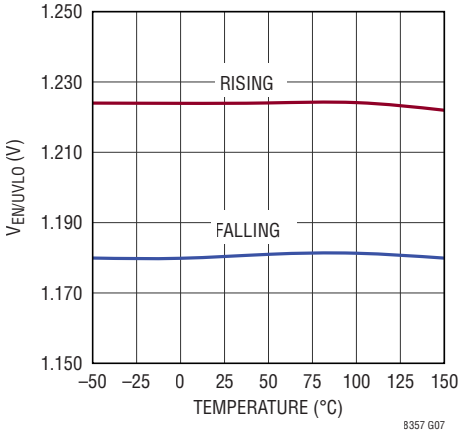
V_{IN} Quiescent Current (Sleep Mode) vs Temperature



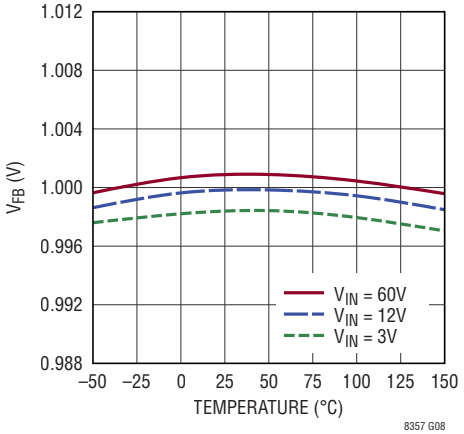
V_{IN} Quiescent Current (Active Mode) vs Temperature



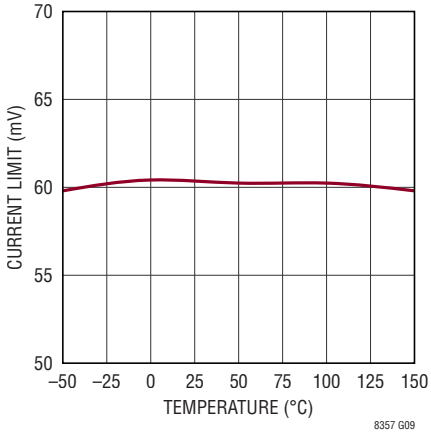
EN/UVLO Enable Threshold vs Temperature



FB Regulation Voltage vs Temperature

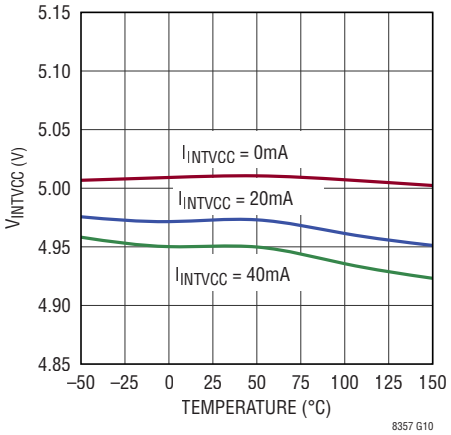


Maximum Current Sense Threshold vs Temperature

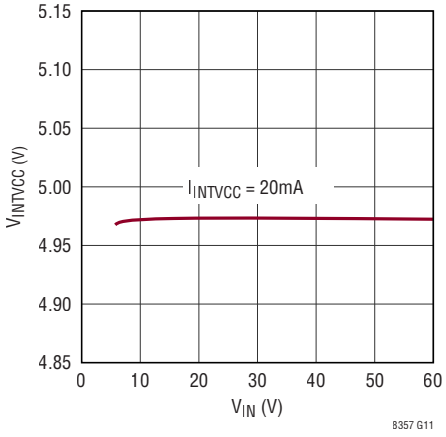


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

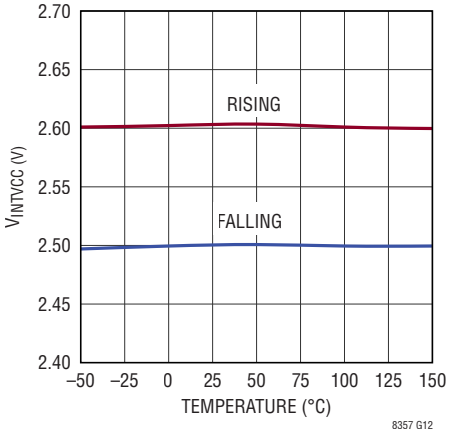
$INTV_{CC}$ Voltage vs Temperature



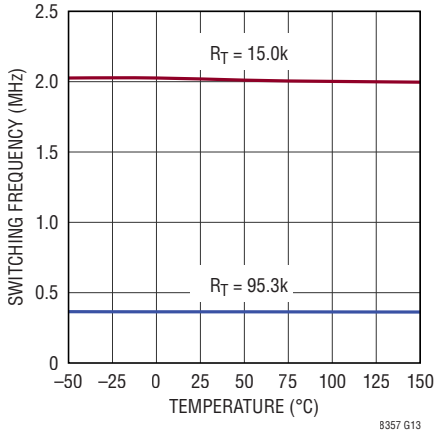
$INTV_{CC}$ Voltage vs V_{IN}



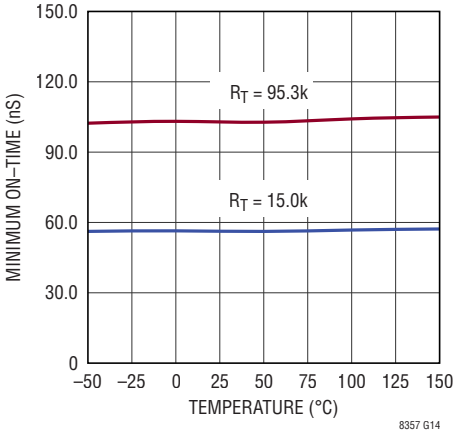
$INTV_{CC}$ UVLO Threshold vs Temperature



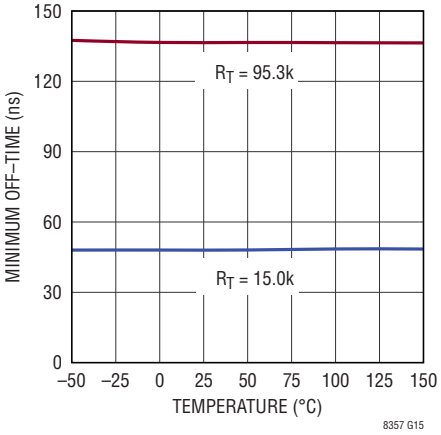
Oscillator Frequency vs Temperature



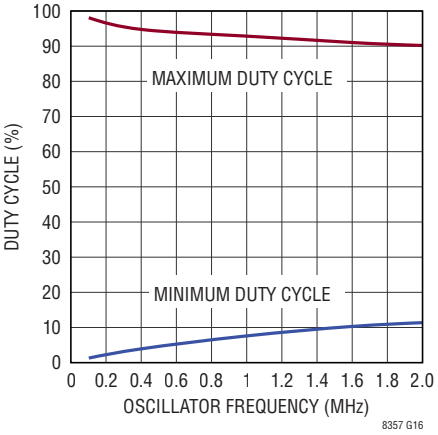
Minimum On-Time vs Temperature



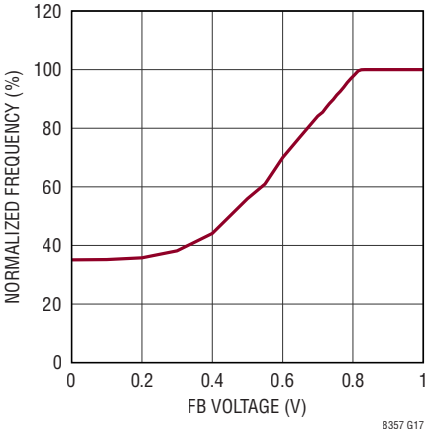
Minimum Off-Time vs Temperature



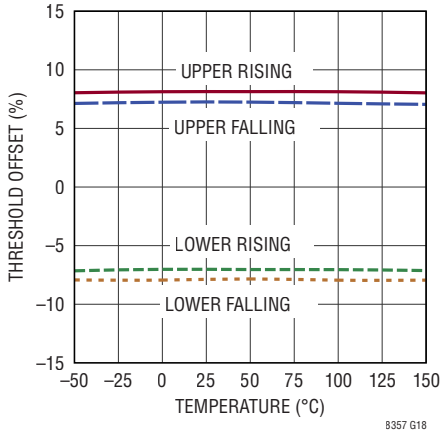
Minimum/Maximum Duty Cycle vs Oscillator Frequency



Normalized Oscillator Frequency vs FB Voltage



PGOOD Threshold vs Temperature



PIN FUNCTIONS

V_C: Error Amplifier Compensation. Place an external RC network to compensate the control loop.

FB: Output Voltage Feedback Input. Tie this pin to a resistor divider from the output to ground to set the output regulation voltage. The FB pin is regulated to 1V during normal operation.

PGOOD: Power Good Open Drain Output. The PGOOD pin is pulled low when the FB pin is beyond ±8% of the final regulation voltage. To function, the pin requires an external pull-up resistor.

SS: Soft-Start Timer Setting. Connect a capacitor between this pin and ground to set the output soft-start time. An internal 15µA pull-up current charging the SS capacitor gradually ramps up FB regulation voltage. UVLO or thermal shutdown immediately pulls SS pin to ground and stops switching.

RT: Switching Frequency Setting. Connect a resistor from this pin to ground to set the internal oscillator frequency from 100kHz to 2MHz.

SYNC/MODE: External Frequency Synchronization and Operation Mode Selection. This pin allows five selectable modes for optimization of performance:

1. External clock: For external frequency synchronization and pulse-skipping mode at light load.
2. $INTV_{CC}$: For spread spectrum frequency modulation and pulse-skipping mode at light load.
3. Float: For internal oscillator frequency and pulse-skipping mode at light load.
4. 100kΩ resistor to GND: For spread spectrum frequency modulation and low-ripple Burst Mode at light load.
5. GND: For internal oscillator frequency and low-ripple Burst Mode at light load.

SENSE: Current Sense Comparator Input. Kelvin connect this pin to the positive terminal of the current sense resistor in the source of the bottom MOSFET. The negative terminal of the current sense resistor should be connected to ground plane close to the chip.

GATEP: MOSFET Gate Pull-Up Drive. Drives the gate of N-Channel MOSFET with a voltage swing from ground to $INTV_{CC}$.

GATEN: MOSFET Gate Pull-Down Drive. Drives the gate of N-Channel MOSFET with a voltage swing from ground to $INTV_{CC}$.

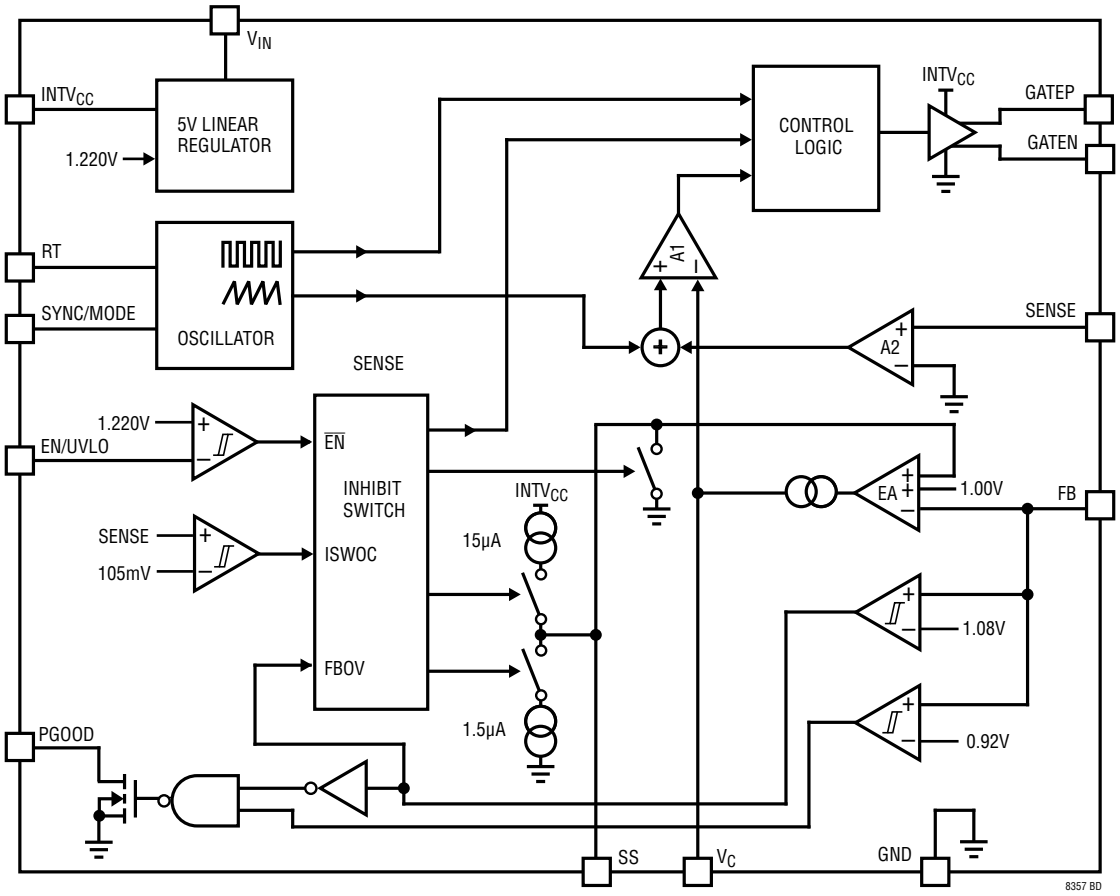
$INTV_{CC}$: Internal 5V Linear Regulator Output. Supplied from V_{IN} pin, the $INTV_{CC}$ linear regulator powers internal control circuitry and gate driver. Do not load the $INTV_{CC}$ pin with external circuitry. Locally bypass this pin to ground with a minimum 2.2µF ceramic capacitor.

EN/UVLO: Enable and Undervoltage Lockout. Force the pin below 0.3V to shut down the part and reduce V_{IN} quiescent current below 3µA. Force the pin above its accurate enable threshold to enable the part. The accurate enable threshold can be used to program an undervoltage lockout (UVLO) threshold with a resistor divider from V_{IN} to ground. If neither function is used, tie this pin to V_{IN}.

V_{IN}: Input Supply. The V_{IN} pin is normally tied to the power input supply or the boost converter output, and supplies $INTV_{CC}$ linear regulator. Locally bypass this pin to ground with a 0.1µF ceramic capacitor.

GND (Exposed Pad): Ground. Solder the exposed pad directly to the ground plane.

BLOCK DIAGRAM



OPERATION

Main Control Loop

The LT8357 uses a fixed frequency, current mode control scheme to provide excellent line and load regulation. Operation can be best understood by referring to the Block Diagram. The inductor current is sensed through the current sense resistor from the SENSE pin to ground. The current sense voltage is gained up by amplifier A2 and added to a slope compensation ramp signal from the internal oscillator. The summing signal is then fed into the positive terminal of the current comparator A1. The negative terminal of A1 is controlled by the voltage on the V_C pin, which is the output of the error amplifier EA. The EA amplifies the difference between the feedback voltage on the FB pin and the 1V reference voltage, and adjusts the V_C voltage accordingly to set the correct peak switch current level to keep the output voltage in regulation.

Light Load Current Operation

At light load, the user can program the SYNC/MODE pin to allow the LT8357 running either in the pulse-skipping mode or low ripple Burst Mode operation. When operating in the pulse-skipping mode, the power switches are held off for multiple clock cycles (i.e., skipping pulses) to maintain the regulation and improve the efficiency. To further enhance the efficiency while minimizing the input quiescent current and output voltage ripple, the LT8357 can also operate in the low ripple Burst Mode. When in the Burst Mode operation, the LT8357 delivers a single small pulse of current to the output capacitor every switching cycle, followed by a long sleep period where the output power is supplied by the output capacitor. During the sleep period, the LT8357 shuts down most of the circuits and thus consumes very low (8µA typical) input quiescent current.

As the output load decreases, the frequency of the single current pulse decreases (see Figure 1) and the percentage of sleep period increases, resulting in much higher light load efficiency than typical converters. To optimize the quiescent current performance at light load, the current in the feedback resistor divider must be minimized as it appears to the output as load current. In addition, all possible leakage currents from the output should also be minimized as they all add to the equivalent output load. The largest contributor to leakage current can be due to the reverse biased leakage of the output diode (see the Output Diode Selection in the Applications Information section).

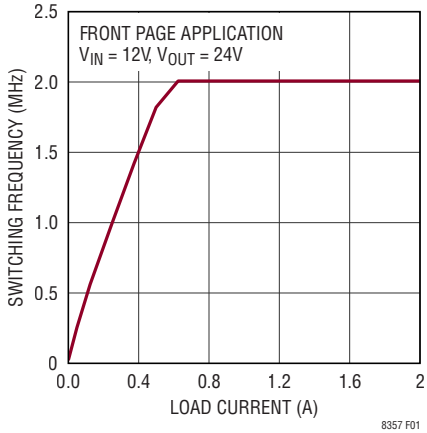


Figure 1. Burst Frequency vs Load Current

When in Burst Mode operation, the switch current limit is approximately 10mV (typical) on the SENSE pin, resulting in low output voltage ripple. Increasing the output capacitance will decrease the output ripple proportionally. As the output load ramps upward from zero, the switching frequency will increase but only up to the fixed oscillator frequency set by the resistor on the RT pin, as shown in Figure 1. The output load at which the LT8357 reaches the fixed frequency varies based on input voltage, output voltage and inductor choice.

OPERATION

Shutdown and Power-On-Reset

The LT8357 enters shutdown mode and drains less than 3µA quiescent current when the EN/UVLO pin is below its shutdown threshold (0.3V minimum). Once the EN/UVLO pin is above its shutdown threshold (0.9V maximum), the LT8357 wakes up the startup circuitry, generates the bandgap reference, and powers up the internal $INTV_{CC}$ LDO. The $INTV_{CC}$ LDO supplies the internal control circuitry and gate driver. The LT8357 then enters undervoltage lockout (UVLO) mode. When in UVLO mode, the part is in a power-on-reset (POR) state, waking up the entire internal control circuitry and settling to the right initial conditions. When the $INTV_{CC}$ pin is charged above its rising UVLO threshold (2.60V typical), the EN/UVLO pin passes its rising enable threshold (1.220V typical), and the junction temperature is less than the thermal shutdown limit (165°C typical), the LT8357 enters enable mode, and the part is ready and waiting for the control signals to start switching.

The LT8357 has an accurate enable threshold (typically 1.220V rising and 1.178V falling) on the EN/UVLO pin to enable the part. The accurate enable threshold allows the user to program an undervoltage lockout (UVLO) threshold with a resistor divider from the input supply V_{IN} to ground. When operating in Burst Mode, the current flowing through the resistor divider can easily exceed the quiescent current consumed by the part. Therefore, the resistor divider values should be large enough to minimize its effect on the efficiency at light load conditions.

Start-Up and Fault Protection

When the LT8357 is in the initial POR state, the SS pin is hard pulled down to ground with a 55Ω internal resistor. Once the part enters enable mode, the POR signal is reset, but the SS pin is still hard pulled down to ground and the part waits for 10µs so that all the internal circuits and logic can settle to the correct states before initiating the start-up sequence. After the 10µs, the SS pin is then charged up by a 15µA pull-up current while the switching is disabled. When the SS pin is charged above 0.25V, switching of the power switches is enabled and the start-up of the output voltage V_{OUT} is controlled by the voltage on the SS pin. When the SS pin voltage is less than 1V, the LT8357 regulates the FB pin voltage to the SS pin voltage instead of the 1V reference. This allows the SS pin to be used to program soft-start by connecting an external capacitor from the SS pin to ground. The internal 15µA pull-up current charges up the capacitor, creating a voltage ramp on the SS pin. As the SS pin voltage rises linearly from 0.25V to 1V (and beyond), the output voltage V_{OUT} rises smoothly to its final regulation voltage. After passing 1V, the SS pin continues to be charged up until exceeding 1.55V, then the start-up period is finished. Before the SS pin rising above 1.55V, the control logic forbids synchronizing from external clock and disables the Burst Mode operation and spread spectrum frequency modulation. After the SS pin rising above 1.55V, both external frequency synchronization and operation mode selection is controlled by the SYNC/MODE pin setting.

Once the switch over current fault is detected on the SENSE pin, the LT8357 disables the switching immediately with the over current fault flag being latched, and the SS pin is discharged by a 1.5µA pull-down current. During the period when the over current fault is detected and being latched, the part forbids the Burst Mode operation. Once the SS pin is discharged below 0.2V, the over current fault flag is reset and the SS pin is charged up by the 15µA pull-up current again. Once the SS pin rises above 0.25V, switching is enabled and the soft start-up is re-initiated again.

Once the FB pin voltage exceeds 8% (typical) above its 1V regulation voltage, the output overvoltage fault will be triggered, which disables the switching immediately. After the FB pin voltage drops below the overvoltage threshold, the switching will be enabled again. No soft start-up will be re-initiated in this fault case.

OPERATION

When V_{OUT} is very low during start-up or a short-circuit fault on the output, the switching regulator must operate at low duty cycle to maintain the power switch current within the current limit range, since the inductor current decay rate is very low during switch off time. The minimum on-time limitation may prevent the switcher from attaining a sufficiently low duty cycle at the programmed switching frequency. Therefore, the switch current will keep increasing through each switch cycle, exceeding the programmed current limit. To prevent the peak switch current from exceeding the programmed limit, the LT8357 implements a frequency foldback function, which starts to fold back the switching frequency as the FB voltage drops below 75% of its regulation voltage (see the Normalized Oscillator Frequency vs FB Voltage in the Typical Performance Characteristics section). The frequency foldback function prevents the inductor current from exceeding the programmed limit because of the minimum on-time. Once the frequency is folded back, external clock synchronization, Burst Mode operation and spread spectrum frequency modulation are all disabled to prevent interference to the frequency foldback operation.

APPLICATIONS INFORMATION

The front page shows a typical LT8357 application circuit. This Applications Information section serves as a guideline for selecting external components for typical applications. The examples and equations in this section assume continuous conduction mode unless otherwise specified.

Switching Frequency Selection

The LT8357 uses a constant frequency control scheme between 100kHz and 2MHz. Selection of the switching frequency is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses, but requires larger inductor and capacitor values. For high power applications, consider operating at lower frequencies to minimize MOSFET heating from switching losses. For low power applications, consider operating at higher frequencies to minimize the total solution size.

In addition, the specific application also plays an important role in switching frequency selection. In a noise-sensitive system, the switching frequency is usually selected to keep the switching noise out of a sensitive frequency band.

Switching Frequency Setting

The switching frequency of the LT8357 is set by the internal oscillator. With frequency synchronization disabled, the switching frequency can be set by placing a resistor from the RT pin to ground. Table 1 shows R_T resistor values for common switching frequencies.

Table 1. Switching Frequency vs R_T Value (1% Resistor)

f_{OSC} (kHz)	R_T (kΩ)
100	357
200	174
350	95.3
400	82.5
600	53.6
800	40.2
1000	31.6
1200	26.1
1400	22.1
1600	19.1
1800	16.9
2000	15.0

Spread Spectrum Frequency Modulation

Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. To improve EMI performance, the LT8357 implements a triangle spread spectrum frequency modulation scheme. When the SYNC/MODE pin is tied to $INTV_{CC}$ or a 100kΩ resistor is placed from the SYNC/MODE pin to ground, the LT8357 spreads its switching frequency 19% above the internal oscillator frequency. Figure 2 and Figure 3 show the noise spectrum of the front page application with spread spectrum frequency modulation enabled and disabled.

Split Gate Drive

It is critical to optimize gate drive for EMI performance in switching regulators by adding an external gate resistor, but there is a trade-off between power efficiency and EMI. Slow gate drive with pull-up gate resistor improves EMI but at the cost of reduced efficiency. Strong pull-down gate drive is always required because the fast slew rate of SW node may pull up the gate of the power MOSFET and falsely turn it on. A single gate drive can only have a single gate resistor that cannot optimize both efficiency and EMI at the same time. In the LT8357, a split gate drive is implemented, which allows using a large pull-up resistor and low pull-down resistor to achieve an optimized efficiency and EMI performance.

APPLICATIONS INFORMATION

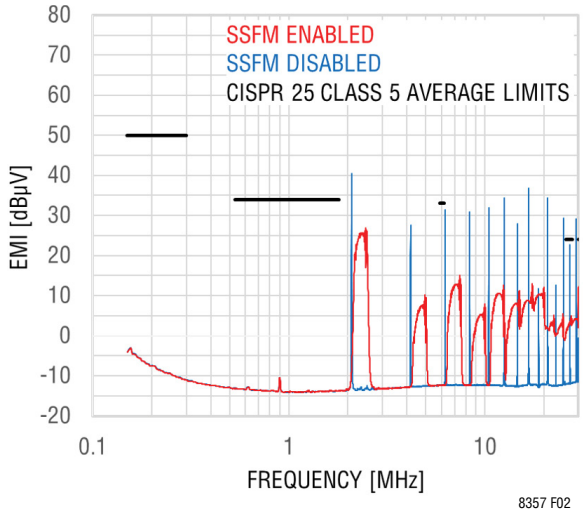


Figure 2. Average Conducted EMI

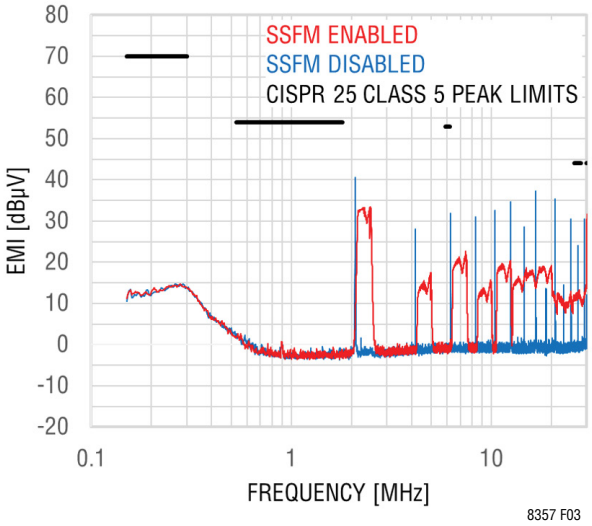


Figure 3. Peak Conducted EMI

Frequency Synchronization and Mode Selection

The switching frequency of the LT8357 can also be synchronized to an external clock using the SYNC/MODE pin. Driving the SYNC/MODE pin with a 50% duty cycle waveform is always a good choice, otherwise maintain the duty cycle between 10% and 90%. The high level of the external clock must be higher than 2.5V, and the low level must be lower than 0.4V. The frequency range must be between 100kHz and 2MHz. The R_T resistor is still required in this case, and the resistance should correspond to the frequency of the external clock. If the external clock ever stops, the LT8357 will rely on the R_T resistor to set the frequency. When synchronizing to an external clock, the LT8357 will forbid entering Burst Mode operation at light load conditions, but instead operate in the pulse-skipping mode to maintain regulation.

In addition to the frequency synchronization, the LT8357 also provides four operation mode options with the switching frequency set by the internal oscillator, which can be selected by programming the SYNC/MODE pin. At light load conditions, the user can choose either pulse-skipping mode or Burst Mode operation. The spread spectrum frequency modulation can also be enabled or disabled depending on the EMI performance requirement of the applications. Please refer to the Pin Functions section for more details on mode selection.

Programming V_{IN} UVLO

A resistor divider from V_{IN} to the EN/UVLO pin implements V_{IN} undervoltage lockout (UVLO). The EN/UVLO enable rising threshold is set at 1.220V (typical) and falling threshold is set at 1.178V (typical) with 42mV hysteresis. The programmable UVLO thresholds are:

$$V_{IN(UVLO+)} = 1.220V \bullet \frac{R1+R2}{R2}$$

$$V_{IN(UVLO-)} = 1.178V \bullet \frac{R1+R2}{R2}$$

Figure 4 shows the implementation of external shut-down control while still using the UVLO function. The NMOS grounds the EN/UVLO pin when turned on, and puts the LT8357 in shutdown with quiescent current less than 3µA.

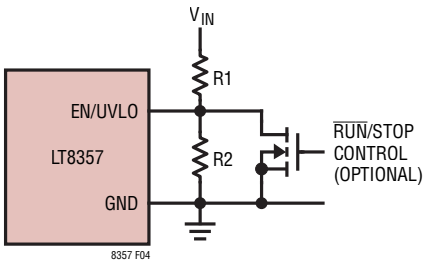


Figure 4. V_{IN} Undervoltage Lockout (UVLO)

APPLICATIONS INFORMATION

$INTV_{CC}$ Regulator

An internal P-channel low dropout regulator produces 5V at the $INTV_{CC}$ pin from the V_{IN} supply pin. The $INTV_{CC}$ powers the internal circuitry and MOSFET gate driver in the LT8357. The $INTV_{CC}$ regulator can supply a peak current of 60mA (typical) and must be bypassed to ground with a minimum of 2.2µF ceramic capacitor. Good local bypass is necessary to supply the high transient current required by the MOSFET gate driver.

Higher input voltage applications with large power MOSFET being driven at higher switching frequencies may cause the maximum junction temperature rating for the LT8357 to be exceeded. The system supply current is normally dominated by the gate charge current. Additional external loading of the $INTV_{CC}$ also needs to be taken into account for the power dissipation calculation. The total LT8357 power dissipation in this case is $V_{IN} \bullet I_{INTVCC}$, and overall efficiency is lowered. The junction temperature can be estimated by using the equation:

$$T_J = T_A + P_D \bullet \theta_{JA}$$

where θ_{JA} (in °C/W) is the package thermal resistance.

To prevent maximum junction temperature from being exceeded, the input supply current must be checked when operating in continuous mode at maximum V_{IN}.

Duty Cycle Consideration

Switching duty cycle is a key variable defining converter operation. As such, its limits must be considered. The minimum on-time is the smallest time duration that the LT8357 is capable of turning on the power MOSFET. In each switching cycle, the LT8357 also keeps the power MOSFET off for a minimum amount of time duration, which is the minimum off-time. Both minimum on-time and minimum off-time will increase as the switching frequency decreases (see the Minimum/Maximum Duty Cycle vs Oscillator Frequency in the Typical Performance Characteristics section).

The minimum on-time $T_{MIN\_ON\_TIME}$ and minimum off-time $T_{MIN\_OFF\_TIME}$ and the switching frequency f define the minimum and maximum switching duty cycles that the converter is able to operate at:

$$\text{Minimum Allowable Duty Cycle} = T_{MIN\_ON\_TIME(MAX)} \bullet f_{(MAX)}$$

$$\text{Maximum Allowable Duty Cycle} = 1 - T_{MIN\_OFF\_TIME(MAX)} \bullet f_{(MAX)}$$

Programming the Output Voltage and Thresholds

The LT8357 has a voltage feedback pin FB that can be used to program its output regulation voltage. The output voltage can be set by selecting the values of R3 and R4 (Figure 5) according to the following equation:

$$V_{OUT} = 1V \bullet \frac{R3+R4}{R4}$$

In addition, the FB pin voltage also determines output overvoltage threshold and output power good thresholds. For an application with small output capacitors, the output voltage may excessively overshoot during load transient event. Once the FB pin hits its overvoltage threshold 1.08V (typical), the LT8357 stops switching immediately by turning off the power MOSFET. The output overvoltage threshold is set with the equation:

$$V_{OUT(OVP)} = 1.08V \bullet \frac{R3+R4}{R4}$$

When the LT8357 is operating in Burst Mode, the current flowing through the feedback resistor divider can easily exceed the input quiescent current consumed by the part. Therefore, high resistor values are preferred for R3 and R4 to achieve high light-load efficiency.

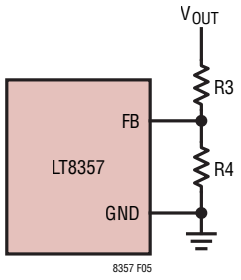


Figure 5. Feedback Resistor Connection

APPLICATIONS INFORMATION

Power GOOD (PGOOD) Pin

The LT8357 provides an open-drain status pin, PGOOD, which is pulled high when the FB pin voltage is within ±8% (typical) of the 1V regulation voltage. The PGOOD pin is pulled up by an external resistor to $INTV_{CC}$ or an external voltage source up to 6V.

Programming the SENSE Pin

For control and protection, the LT8357 measures the power MOSFET current by using a sense resistor (R_{SENSE}) from the MOSFET source to GND. Figure 6 shows a typical waveform of the sense voltage (V_{SENSE}) across the sense resistor. It is important to use Kelvin traces between the SENSE pin and R_{SENSE}, and place the IC GND as close as possible to the GND terminal of R_{SENSE} for proper operation.

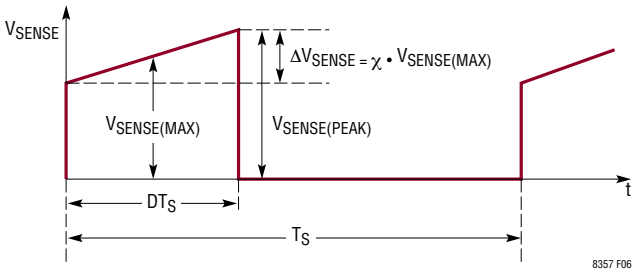


Figure 6. The Sense Voltage Waveform

Due to the current limit function of the SENSE pin, R_{SENSE} should be selected to guarantee that the peak switch current sense voltage $V_{SENSE(PEAK)}$ in the steady state of normal operation does not exceed the SENSE maximum current threshold (60mV typical). Then, the maximum switch current ripple percentage can be calculated using the following equation:

$$\chi = \frac{\Delta V_{SENSE}}{60mV - 0.5 \bullet \Delta V_{SENSE}}$$

χ will be used in the subsequent design examples to calculate inductor value. ΔV_{SENSE} is the ripple voltage across R_{SENSE}. The final R_{SENSE} value should be lower than the calculated R_{SENSE}. A 20% to 30% margin is usually recommended. Always choose a low ESL current sense resistor.

The LT8357 uses a time interval close to the minimum on-time to blank the ringing on the switch current sense signal immediately after the power MOSFET is turned on. This ringing is caused by the parasitic inductance and capacitance of the PCB trace, the sense resistor, the diode, and the MOSFET. The blanking time interval increases along with the minimum on-time as the switching frequency decreases. In applications that have very large and long ringing on the current sense signal, a small RC filter can be added to filter out the excess ringing.

Soft-Start

As explained in the Operation section, the SS pin can be used to program the output voltage soft-start by connecting an external capacitor from the SS pin to GND. The internal 15µA (typical) pull-up current charges up the capacitor, creating a voltage ramp on the SS pin. As the SS pin voltage rises linearly from 0.25V to 1V (and beyond), the output voltage rises smoothly into its final voltage regulation. The soft-start time can be calculated as:

$$T_{SS} = 1V \bullet \frac{C_{SS}}{15\mu A}$$

Make sure the C_{SS} is at least five to ten times larger than the compensation capacitor on the V_C pin for a well-controlled output voltage soft-start. A 22nF ceramic capacitor is a good starting point.

The SS pin is also used as a fault timer. Once a switch over current fault is detected, the LT8357 enters a low duty cycle auto-retry hiccup mode. In this scenario, the switching is disabled immediately and a 1.5µA (typical) pull-down current is activated to discharge C_{SS}. Once the SS pin voltage is discharged below 0.2V, the 15µA pull-up current charges up the SS pin again. If the switch over current fault condition has not been removed, then a new hiccup cycle will be initiated. This will continue until the fault is removed. Once the switch over current condition is removed, the output will have a smooth recovery due to soft-start.

APPLICATIONS INFORMATION

Loop Compensation

The LT8357 uses an internal transconductance error amplifier, the output of which, V_C, compensates the control loop. The external inductor, output capacitor, and the compensation resistor and capacitor determine the loop stability.

The inductor and output capacitor are chosen based on performance, size and cost. The compensation resistor and capacitor on the V_C pin are set to optimize control loop response and stability. For a typical application, a 2.2nF compensation capacitor on the V_C pin is adequate, and a series resistor should always be used to increase the slew rate on the V_C pin to maintain tight output voltage regulation during fast transients.

APPLICATION CIRCUITS

The LT8357 can be configured in different topologies. The first topology to be analyzed will be the boost converter, followed by the flyback and SEPIC converters.

Boost Converter: Switch Duty Cycle and Frequency

The LT8357 can be configured as a boost converter for applications where the converter output voltage is higher than the input voltage. Remember that boost converters are not short-circuit protected. Under a shorted output condition, the inductor current is limited only by the input supply capability. For applications requiring a step-up converter that is short-circuit protected, please refer to the Applications Information section covering SEPIC converters.

The conversion ratio as a function of duty cycle is

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D}$$

in continuous conduction mode (CCM).

For a boost converter operating in CCM, the duty cycle of the main switch can be calculated based on the output voltage (V_{OUT}) and the input voltage (V_{IN}). The maximum duty cycle (D_{MAX}) occurs when the converter has the minimum input voltage:

$$D_{MAX} = \frac{V_{OUT} - V_{IN(MIN)}}{V_{OUT}}$$

Discontinuous conduction mode (DCM) provides higher conversion ratios at a given frequency but at the cost of reduced efficiencies and higher switching currents.

Boost Converter: Inductor and Sense Resistor Selection

For the boost topology, the maximum average inductor current is:

$$I_{L(MAX)} = I_{O(MAX)} \bullet \frac{1}{1-D_{MAX}}$$

Then, the ripple current can be calculated by:

$$\Delta I_L = \chi \bullet I_{L(MAX)} = \chi \bullet I_{O(MAX)} \bullet \frac{1}{1-D_{MAX}}$$

The constant χ in the preceding equation represents the percentage peak-to-peak ripple current in the inductor, relative to $I_{L(MAX)}$.

The inductor ripple current has a direct effect on the choice of the inductor value. Choosing smaller values of ΔI_L requires large inductances and reduces the current loop gain (the converter will approach voltage mode). Accepting larger values of ΔI_L provides fast transient response and allows the use of low inductances, but results in higher input current ripple and greater core losses. It is recommended that χ fall within the range of 0.2 to 0.6.

Given an operating input voltage range, and having chosen the operating frequency and ripple current in the inductor, the inductor value of the boost converter can be determined using the following equation:

$$L = \frac{V_{IN(MIN)}}{\Delta I_L \bullet f} \bullet D_{MAX}$$

APPLICATIONS INFORMATION

The peak and RMS inductor current are:

$$I_{L(PEAK)} = I_{L(MAX)} \bullet (1 + \frac{\chi}{2})$$

$$I_{L(RMS)} = I_{L(MAX)} \bullet \sqrt{1 + \frac{\chi^2}{12}}$$

Based on these equations, the user should choose the inductors having sufficient saturation and RMS current ratings.

Set the sense voltage across the sense resistor R_{SENSE} at $I_{L(PEAK)}$ to be less than the maximum SENSE current limit threshold of 60mV (typical). The sense resistor value can then be calculated as:

$$R_{SENSE} = \frac{60mV}{I_{L(PEAK)}}$$

The final R_{SENSE} value should be lower than the calculated R_{SENSE}. A 20% to 30% margin is usually recommended. Always choose a low ESL current sense resistor.

Boost Converter: Power MOSFET Selection

Important parameters for the power MOSFET include the drain-source voltage rating (V_{DS}), the threshold voltage ($V_{GS(TH)}$), the on-resistance ($R_{DS(ON)}$), the gate to source and gate to drain charges (Q_{GS} and Q_{GD}), the maximum drain current ($I_{D(MAX)}$) and the MOSFET's thermal resistances ($R_{\theta JC}$ and $R_{\theta JA}$).

The power MOSFET will see full output voltage, plus a diode forward voltage, and any additional ringing across its drain-to-source during its off-time. It is recommended to choose a MOSFET whose breakdown voltage BV_{DSS} is higher than V_{OUT} by a safety margin (a 10V safety margin is usually sufficient).

The power dissipated by the MOSFET in a boost converter is:

$$P_{FET} = I^2_{L(MAX)} \bullet R_{DS(ON)} \bullet D_{MAX} + 2 \bullet V^2_{OUT} \bullet I_{L(MAX)} \bullet C_{RSS} \bullet f / 1A$$

The first term in this equation represents the conduction losses in the device, and the second term represents the switching loss. C_{RSS} is the reverse transfer capacitance of the MOSFET. f is the switching frequency. For maximum efficiency, $R_{DS(ON)}$ and C_{RSS} should be minimized.

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following equation:

$$T_J = T_A + P_{FET} \bullet \theta_{JA} = T_A + P_{FET} \bullet (\theta_{JC} + \theta_{CA})$$

T_J must not exceed the MOSFET maximum junction temperature rating. It is recommended to measure the MOSFET temperature in steady state to ensure that absolute maximum ratings are not exceeded.

To achieve 2MHz operation, Q_G and $R_{DS(ON)}$ of the power MOSFET must be carefully selected. High performance power MOSFETs with low Q_G and low $R_{DS(ON)}$ must be used. Since the gate drive voltage is set by the 5V $INTV_{CC}$ supply, logic-level threshold MOSFETs must be used in LT8357 applications. When switching at high frequency like 2MHz, the substantial gate charge current from $INTV_{CC}$ can be estimated as:

$$I_{INTVCC} = f \bullet Q_G$$

Make sure the total required $INTV_{CC}$ current not exceeding the $INTV_{CC}$ current limit in the data sheet. Typically, MOSFETs with less than 10nC Q_G are recommended.

Boost Converter: Output Diode Selection

To maximize efficiency, a fast switching diode with low forward voltage drop and low reverse leakage is desirable. The peak reverse voltage that the diode must withstand is equal to the regulator output voltage plus any additional ringing across its anode-to-cathode during the on-time. The average forward current in normal operation is equal to the output current, and the peak current is equal to:

$$I_{D(PEAK)} = I_{L(PEAK)} = I_{L(MAX)} \bullet (1 + \frac{\chi}{2})$$

It is recommended that the peak repetitive reverse voltage rating V_{RRM} is higher than V_{OUT} by a safety margin (a 10V safety margin is usually sufficient).

APPLICATIONS INFORMATION

The power dissipated by the diode is:

$$P_D = I_{O(MAX)} \bullet V_D$$

and the diode junction temperature is:

$$T_J = T_A + P_D \bullet R_{\theta JA}$$

The $R_{\theta JA}$ to be used in this equation normally includes the $R_{\theta JC}$ for the device plus the thermal resistance from the board to the ambient temperature in the enclosure. T_J must not exceed the diode maximum junction temperature rating.

Boost Converter: Output Capacitor Selection

Contributions of ESR (equivalent series resistance), ESL (equivalent series inductance) and the bulk capacitance must be considered when choosing the correct output capacitors for a given output ripple voltage. The effect of these three parameters (ESR, ESL and bulk C) on the output voltage ripple waveform for a typical boost converter is illustrated in Figure 7.

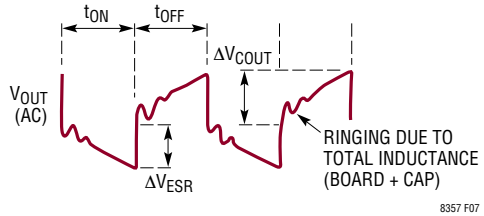


Figure 7. The Output Voltage Ripple Waveform of a Boost Converter

The choice of components begins with the maximum acceptable ripple voltage (expressed as a percentage of the output voltage), and how this ripple should be divided between the ESR step ΔV_{ESR} and the charging/discharging ΔV_{COUT}. For the purpose of simplicity, we will choose 2% for the maximum output ripple, to be divided equally between ΔV_{ESR} and ΔV_{COUT}. This percentage ripple will change, depending on the requirements of the application, and the following equations can easily be modified. For a 1% contribution to the total ripple voltage, the ESR of the output capacitor can be determined using the following equation:

$$ESR_{COUT} \le \frac{0.01 \bullet V_{OUT}}{I_{D(PEAK)}}$$

For the bulk C component, which also contributes 1% to the total ripple:

$$C_{OUT} \ge \frac{I_{O(MAX)}}{0.01 \bullet V_{OUT} \bullet f}$$

The output capacitor in a boost regulator experiences high RMS ripple currents, as shown in Figure 7. The RMS ripple current rating of the output capacitor can be determined using the following equation:

$$I_{RMS(COUT)} \ge I_{O(MAX)} \bullet \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$

Multiple capacitors are often paralleled to meet ESR requirements. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the required RMS current rating. Additional ceramic capacitors in parallel are commonly used to reduce the effect of parasitic inductance in the output capacitor. Ceramic capacitors should be placed from V_{OUT} to GND as close to the LT8357 pins as possible to suppress high frequency switching noise on the converter output. X5R or X7R dielectrics are preferred, as these materials retain their capacitance over wide voltage and temperature ranges. Many ceramic capacitors, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired operating voltage.

Boost Converter: Input Capacitor Selection

The input capacitor of a boost converter is less critical than the output capacitor, due to the fact that the inductor is in series with the input, and the input current waveform is continuous. The input voltage source impedance determines the size of the input capacitor, which is typically in the range of 10µF to 100µF. A low ESR ceramic capacitor is also recommended, although it is not as critical as for the output capacitor. Place the ceramic capacitors from V_{IN} to GND as close to the LT8357 pins as possible to reduce input ripple voltage. Similar to the output capacitors, X5R or X7R dielectrics and 0805 or 0603 case sizes are also preferred for the input capacitor selection.

APPLICATIONS INFORMATION

The RMS input capacitor ripple current for a boost converter is:

$$I_{RMS(CIN)} = 0.3 \bullet \Delta I_L$$

FLYBACK CONVERTER APPLICATIONS

The LT8357 can be configured as a flyback converter for the applications where the converters have multiple outputs, high output voltages or isolated outputs. Figure 8 shows a simplified flyback converter using LT8357.

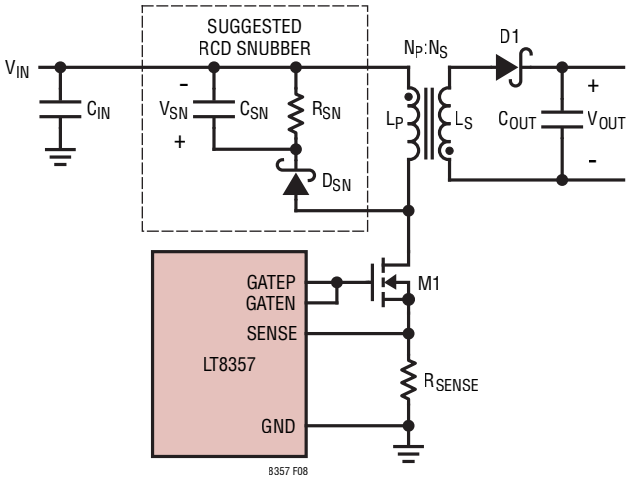


Figure 8. A Simplified Flyback Converter

The flyback converter has a very low part count for multiple outputs, and with prudent selection of turns ratio, can have high output/input voltage conversion ratios with a desirable duty cycle. However, it has low efficiency due to the high peak currents, high peak voltages and consequent power loss. The flyback converter is commonly used for an output power of less than 50W.

The flyback converter can be designed to operate either in continuous or discontinuous mode. Compared to continuous mode, discontinuous mode has the advantage of smaller transformer inductance and easier loop compensation, and the disadvantage of higher peak-to-average current and lower efficiency. In the high output voltage applications, the flyback converters can be designed to operate in discontinuous mode to avoid using large transformers.

Flyback Converter: Switch Duty Cycle and Turns Ratio

The flyback converter conversion ratio in the continuous mode operation is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{N_S}{N_P} \bullet \frac{D}{1-D}$$

where N_S/N_P is the second to primary turns ratio.

Figure 9 shows the waveforms of the flyback converter in discontinuous mode operation, where V_{SW}, I_{SW} and I_D represent primary switch node voltage, power MOSFET current and output diode current, respectively. During each switching period T_S, three subintervals occur: DT_S, $D2T_S$, $D3T_S$. During DT_S, power MOSFET M1 is on, and output diode D1 is reverse-biased. During $D2T_S$, M1 is off, and L_S is conducting current. Both L_P and L_S currents are zero during $D3T_S$.

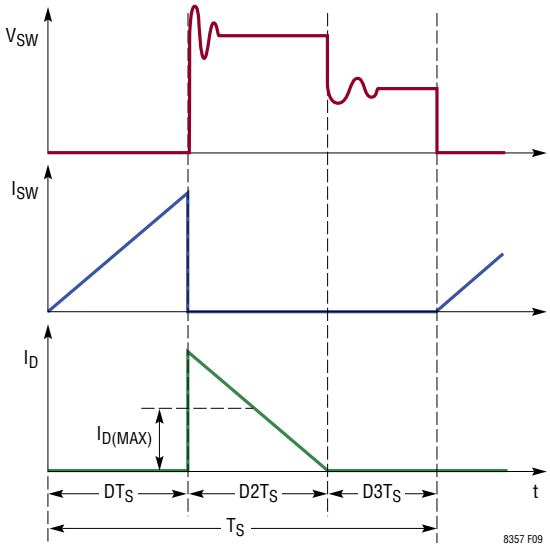


Figure 9. Waveforms of the Flyback Converter in Discontinuous Mode Operation

APPLICATIONS INFORMATION

The flyback converter conversion ratio in the discontinuous mode operation is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{N_S}{N_P} \bullet \frac{D}{D2}$$

According to the preceding equations, the user has relative freedom in selecting the switch duty cycle or turns ratio to suit a given application. The selections of the duty cycle and the turns ratio are somewhat iterative processes, due to the number of variables involved. The user can choose either a duty cycle or a turns ratio as the start point. The following trade-offs should be considered when selecting the switch duty cycle or turns ratio, to optimize the converter performance. A higher duty cycle affects the flyback converter in the following aspects:

- Lower MOSFET RMS current $I_{SW(RMS)}$, but higher MOSFET V_{DS} peak voltage
- Lower diode peak reverse voltage, but higher diode RMS current $I_{D(RMS)}$
- Higher transformer turns ratio (N_P/N_S)

The choice,

$$\frac{D}{D+D2} = \frac{1}{3}$$

(for discontinuous mode operation with a given D3) gives the power MOSFET the lowest power stress (the product of RMS current and peak voltage). However, in the high output voltage applications, a higher duty cycle may be adopted to limit the large peak reverse voltage of the diode. The choice,

$$\frac{D}{D+D2} = \frac{2}{3}$$

(for discontinuous mode operation with a given D3) gives the diode the lowest power stress (the product of RMS current and peak voltage). An extreme high or low duty cycle results in high power stress on the MOSFET or diode, and reduces efficiency. It is recommended to choose a duty cycle, D, between 20% and 80%.

Flyback Converter: Transformer Design for Discontinuous Mode Operation

The transformer design for discontinuous mode of operation is chosen as presented here. According to Figure 9, the minimum D3 ($D3_{MIN}$) occurs when the converter has the minimum V_{IN} and the maximum output power (P_{OUT}). Choose $D3_{MIN}$ to be equal to or higher than 10% to guarantee the converter is always in discontinuous mode operation (choosing higher D3 allows the use of lower inductance, but results in a higher switch peak current).

The user can choose a D_{MAX} as the start point. Then, the maximum average primary currents can be calculated by the following equation:

$$I_{LP(MAX)} = I_{SW(MAX)} = \frac{P_{OUT(MAX)}}{D_{MAX} \bullet V_{IN(MIN)} \bullet \eta}$$

where η is the converter efficiency. If the flyback converter has multiple outputs, $P_{OUT(MAX)}$ is the sum of all the output power.

The maximum average secondary current is:

$$I_{LS(MAX)} = I_{D(MAX)} = \frac{I_{OUT(MAX)}}{D2}$$

where:

$D2 = 1 - D_{MAX} - D3$

The primary and secondary RMS currents are:

$$I_{LP(RMS)} = 2 \bullet I_{LP(MAX)} \bullet \sqrt{\frac{D_{MAX}}{3}}$$

$$I_{LS(RMS)} = 2 \bullet I_{LS(MAX)} \bullet \sqrt{\frac{D2}{3}}$$

According to Figure 9, the primary and secondary peak currents are:

$I_{LP(PEAK)} = I_{SW(PEAK)} = 2 \bullet I_{LP(MAX)}$

$I_{LS(PEAK)} = I_{D(PEAK)} = 2 \bullet I_{LS(MAX)}$

APPLICATIONS INFORMATION

The primary and second inductor values of the flyback converter transformer can be determined using the following equations:

$$L_P = \frac{D^2_{MAX} \bullet V^2_{IN(MIN)} \bullet \eta}{2 \bullet P_{OUT(MAX)} \bullet f}$$

$$L_S = \frac{D2^2 \bullet (V_{OUT} + V_D)}{2 \bullet I_{OUT(MAX)} \bullet f}$$

The primary to second turns ratio is:

$$\frac{N_P}{N_S} = \sqrt{\frac{L_P}{L_S}}$$

Flyback Converter: Snubber Design

Transformer leakage inductance (on either the primary or secondary) causes a voltage spike to occur after the MOSFET turn-off. This is increasingly prominent at higher load currents, where more stored energy must be dissipated. In some cases, a snubber circuit will be required to avoid overvoltage breakdown at the MOSFET's drain node. There are different snubber circuits (such as RC snubber, RCD snubber, etc.), and Application Note 19 is a good reference on snubber design. An RCD snubber is shown in Figure 8.

The snubber resistor value (R_{SN}) can be calculated by the following equation:

$$R_{SN} = 2 \bullet \frac{V^2_{SN} - V_{SN} \bullet V_{OUT} \bullet \frac{N_P}{N_S}}{I^2_{SW(PEAK)} \bullet L_{LK} \bullet f}$$

where V_{SN} is the snubber capacitor voltage. A smaller V_{SN} results in a larger snubber loss. A reasonable V_{SN} is 2 to 2.5 times of:

$$\frac{V_{OUT} \bullet N_P}{N_S}$$

L_{LK} is the leakage inductance of the primary winding, which is usually specified in the transformer characteristics. L_{LK} can be obtained by measuring the primary inductance with the secondary windings shorted. The snubber capacitor value (C_{SN}) can be determined using the following equation:

$$C_{SN} = \frac{V_{SN}}{\Delta V_{SN} \bullet R_{SN} \bullet f}$$

where ΔV_{SN} is the voltage ripple across C_{SN}. A reasonable ΔV_{SN} is 5% to 10% of V_{SN}. The reverse voltage rating of D_{SN} should be higher than the sum of V_{SN} and $V_{IN(MAX)}$.

Flyback Converter: Sense Resistor Selection

In a flyback converter, when the power MOSFET is turned on, the current flowing through the sense resistor (I_{SENSE}) is:

$$I_{SENSE} = I_{LP}$$

Set the sense voltage at $I_{LP(PEAK)}$ to be less than the maximum SENSE current limit threshold of 60mV (typical). The sense resistor value can then be calculated as:

$$R_{SENSE} = \frac{60mV}{I_{LP(PEAK)}}$$

The final R_{SENSE} value should be lower than the calculated R_{SENSE}. A 20% to 30% margin is usually recommended. Always choose a low ESL current sense resistor.

Flyback Converter: Power MOSFET Selection

For the flyback configuration, the MOSFET is selected with a V_{DC} rating high enough to handle the maximum V_{IN}, the reflected secondary voltage and the voltage spike due to the leakage inductance. Approximate the required MOSFET V_{DC} rating using:

$$BV_{DSS} > V_{DS(PEAK)}$$

where

$$V_{DS(PEAK)} = V_{IN(MAX)} + V_{SN}$$

The power dissipated by the MOSFET in a flyback converter is:

$$P_{FET} = I^2_{M(RMS)} \bullet R_{DS(ON)} + 2 \bullet V^2_{DS(PEAK)} \bullet I_{L(MAX)} \bullet C_{RSS} \bullet f / 1A$$

APPLICATIONS INFORMATION

The first term in this equation represents the conduction losses in the device, and the second term represents the switching loss. C_{RSS} is the reverse transfer capacitance of the MOSFET. f is the switching frequency. For maximum efficiency, $R_{DS(ON)}$ and C_{RSS} should be minimized.

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following equation:

$$T_J = T_A + P_{FET} \bullet \theta_{JA} = T_A + P_{FET} \bullet (\theta_{JC} + \theta_{CA})$$

T_J must not exceed the MOSFET maximum junction temperature rating. It is recommended to measure the MOSFET temperature in steady state to ensure that absolute maximum ratings are not exceeded.

To achieve high switching frequency (such as 2MHz) operation, Q_G and $R_{DS(ON)}$ of the power MOSFET must be carefully selected. High performance power MOSFETs with low Q_G and low $R_{DS(ON)}$ must be used. Since the gate drive voltage is set by the 5V $INTV_{CC}$ supply, logic-level threshold MOSFETs must be used in LT8357 applications. When switching at high frequency like 2MHz, the substantial gate charge current from $INTV_{CC}$ can be estimated as:

$$I_{INTVCC} = f \bullet Q_G$$

Make sure the total required $INTV_{CC}$ current not exceeding the $INTV_{CC}$ current limit in the data sheet. Typically, MOSFETs with less than 10nC Q_G are recommended.

Flyback Converter: Output Diode Selection

The output diode in a flyback converter is subject to large RMS current and peak reverse voltage stresses. A fast switching diode with a low forward drop and a low reverse leakage is desired. Schottky diodes are recommended if the output voltage is below 100V.

Approximate the required peak repetitive reverse voltage rating V_{RRM} using:

$$V_{RRM} > \frac{N_S}{N_P} \bullet V_{IN(MAX)} + V_{OUT}$$

The power dissipated by the diode is:

$$P_D = I_{O(MAX)} \bullet V_D$$

and the diode junction temperature is:

$$T_J = T_A + P_D \bullet R_{\theta JA}$$

The $R_{\theta JA}$ to be used in this equation normally includes the $R_{\theta JC}$ for the device plus the thermal resistance from the board to the ambient temperature in the enclosure. T_J must not exceed the diode maximum junction temperature rating.

Flyback Converter: Output Capacitor Selection

The output capacitor of the flyback converter has a similar operation condition as that of the boost converter. Refer to the Boost Converter: Output Capacitor Selection section for the calculation of C_{OUT} and ESR_{COUT}.

The RMS ripple current rating of the output capacitors in discontinuous operation can be determined using the following equation:

$$I_{RMS(COUT),DISCONTINOUS} \geq I_{O(MAX)} \bullet \sqrt{\frac{4-(3\bullet D2)}{3\bullet D2}}$$

Flyback Converter: Input Capacitor Selection

The input capacitor in a flyback converter is subject to a large RMS current due to the discontinuous primary current. To prevent large voltage transients, use a low ESR input capacitor sized for the maximum RMS current. The RMS ripple current rating of the input capacitors in discontinuous operation can be determined using the following equation:

$$I_{RMS(CIN),DISCONTINUOUS} \geq \frac{P_{OUT(MAX)}}{V_{IN(MIN)} \bullet \eta} \bullet \sqrt{\frac{4-(3\bullet D_{MAX})}{3\bullet D_{MAX}}}$$

SEPIC CONVERTER APPLICATIONS

The LT8357 can be configured as a SEPIC (single-ended primary inductance converter), as shown in Figure 10. This topology allows for the input to be higher, equal, or lower than the desired output voltage. The conversion ratio as a function of duty cycle is:

$$\frac{V_{OUT} + V_D}{V_{IN}} = \frac{D}{1-D}$$

in continuous conduction mode (CCM).

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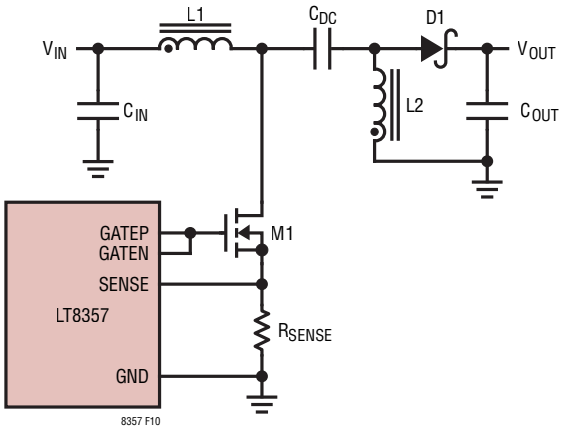


Figure 10. A Simplified SEPIC Converter

In a SEPIC converter, no DC path exists between the input and output. This is an advantage over the boost converter for applications requiring the output to be disconnected from the input source when the circuit is in shutdown.

Compared to the flyback converter, the SEPIC converter has the advantage that both the power MOSFET and the output diode voltages are clamped by the capacitors (C_{IN}, C_{DC} and C_{OUT}). Therefore, there is less voltage ringing across the power MOSFET and the output diode. The SEPIC converter requires much smaller input capacitors than those of the flyback converter. This is due to the fact that, in the SEPIC converter, the inductor L1 is in series with the input, and the ripple current flowing through the input capacitor is continuous.

SEPIC Converter: Switch Duty Cycle and Frequency

For a SEPIC converter operating in CCM, the duty cycle of the main switch can be calculated based on the output voltage (V_{OUT}), the input voltage (V_{IN}) and the diode forward voltage (V_D).

The maximum duty cycle (D_{MAX}) occurs when the converter operates at the minimum input voltage:

$$D_{MAX} = \frac{V_{OUT} + V_D}{V_{IN(MIN)} + V_{OUT} + V_D}$$

Conversely, the minimum duty cycle (D_{MIN}) occurs when the converter operates at the maximum input voltage:

$$D_{MIN} = \frac{V_{OUT} + V_D}{V_{IN(MAX)} + V_{OUT} + V_D}$$

Be sure to check that D_{MAX} and D_{MIN} obey:

$$D_{MAX} < 1 - T_{MIN\_OFF\_TIME(MAX)} \bullet f_{(MAX)}$$

and

$$D_{MIN} > T_{MIN\_ON\_TIME(MAX)} \bullet f_{(MAX)}$$

where Minimum Off-Time $T_{MIN\_OFF\_TIME}$, Minimum On-Time $T_{MIN\_ON\_TIME}$ and Switching Frequency f are specified in the Electrical Characteristics table.

SEPIC Converter: Inductor and Sense Resistor Selection

As shown in Figure 10, the SEPIC converter contains two inductors: L1 and L2. L1 and L2 can be independent, but can also be wound on the same core, since identical voltages are applied to L1 and L2 throughout the switching cycle.

For the SEPIC topology, the current through L1 is the converter input current. Based on the fact that, ideally, the output power is equal to the input power, the maximum average inductor currents of L1 and L2 are:

$$I_{L1(MAX)} = I_{IN(MAX)} = I_{O(MAX)} \bullet \frac{D_{MAX}}{1 - D_{MAX}}$$

$$I_{L2(MAX)} = I_{O(MAX)}$$

In a SEPIC converter, the switch current is equal to I_{L1} + I_{L2} when the power switch is on, therefore, the maximum average switch current is defined as:

$$I_{SW(MAX)} = I_{L1(MAX)} + I_{L2(MAX)} = I_{O(MAX)} \bullet \frac{1}{1 - D_{MAX}}$$

and the peak switch current is:

$$I_{SW(PEAK)} = \left(1 + \frac{\chi}{2}\right) \bullet I_{O(MAX)} \bullet \frac{1}{1 - D_{MAX}}$$

The constant χ in the preceding equations represents the percentage peak-to-peak ripple current in the switch,

APPLICATIONS INFORMATION

relative to $I_{SW(MAX)}$, as shown in Figure 11. Then, the switch ripple current ΔI_{SW} can be calculated by:

$$\Delta I_{SW} = \chi \bullet I_{SW(MAX)}$$

The inductor ripple currents ΔI_{L1} and ΔI_{L2} are identical:

$$\Delta I_{L1} = \Delta I_{L2} = 0.5 \bullet \Delta I_{SW}$$

The inductor ripple current has a direct effect on the choice of the inductor value. Choosing smaller values of ΔI_L requires large inductances and reduces the current loop gain (the converter will approach voltage mode). Accepting larger values of ΔI_L allows the use of low inductances, but results in higher input current ripple and greater core losses. It is recommended that χ falls in the range of 0.2 to 0.4.

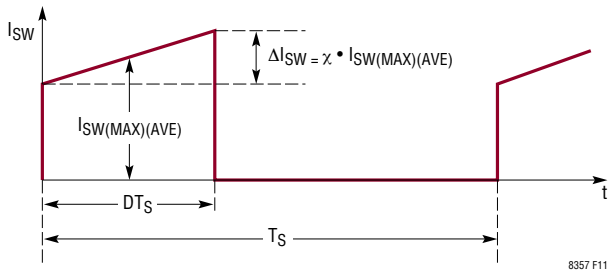


Figure 11. The Switch Current Waveform of the SEPIC Converter

Given an operating input voltage range and having chosen the operating frequency and ripple current in the inductor, the inductor value (L1 and L2 are independent) of the SEPIC converter can be determined using the following equation:

$$L1 = L2 = \frac{V_{IN(MIN)}}{0.5 \bullet \Delta I_{SW} \bullet f} \bullet D_{MAX}$$

For most SEPIC applications, the equal inductor values will fall in the range of 1µH to 100µH. By making L1 = L2, and winding them on the same core, the value of inductance in the preceding equation is replaced by 2L, due to mutual inductance:

$$L = \frac{V_{IN(MIN)}}{\Delta I_{SW} \bullet f} \bullet D_{MAX}$$

This maintains the same ripple current and energy storage in the inductors. The peak inductor currents are:

$$I_{L1(PEAK)} = I_{L1(MAX)} + 0.5 \bullet \Delta I_{L1}$$

$$I_{L2(PEAK)} = I_{L2(MAX)} + 0.5 \bullet \Delta I_{L2}$$

The RMS inductor currents are:

$$I_{L1(RMS)} = I_{L1(MAX)} \bullet \sqrt{1 + \frac{\chi_{L1}^2}{12}}$$

where:

$$\chi_{L1} = \frac{\Delta I_{L1}}{I_{L1(MAX)}}$$

$$I_{L2(RMS)} = I_{L2(MAX)} \bullet \sqrt{1 + \frac{\chi_{L2}^2}{12}}$$

where:

$$\chi_{L2} = \frac{\Delta I_{L2}}{I_{L2(MAX)}}$$

Based on the preceding equations, the user should choose the inductors having sufficient saturation and RMS current ratings.

In a SEPIC converter, when the power switch is turned on, the current flowing through the sense resistor (I_{SENSE}) is the switch current I_{SW}. Set the sense voltage at $I_{SW(PEAK)}$ to be less than the maximum SENSE current limit threshold of 60mV (typical). The sense resistor value can then be calculated as:

$$R_{SENSE} = \frac{60mV}{I_{SW(PEAK)}}$$

APPLICATIONS INFORMATION

The final R_{SENSE} value should be lower than the calculated R_{SENSE}. A 20% to 30% margin is usually recommended. Always choose a low ESL current sense resistor.

SEPIC Converter: Power MOSFET Selection

For the SEPIC configuration, choose a MOSFET with a V_{DC} rating higher than the sum of the output voltage and input voltage by a safety margin (a 10V safety margin is usually sufficient).

The power dissipated by the MOSFET in a SEPIC converter is:

$$P_{FET} = I^2_{SW(MAX)} \bullet R_{DS(ON)} \bullet D_{MAX} + 2 \bullet (V_{IN(MIN)} + V_{OUT})^2 \bullet I_{L(MAX)} \bullet C_{RSS} \bullet f / 1A$$

The first term in this equation represents the conduction losses in the device, and the second term represents the switching loss. C_{RSS} is the reverse transfer capacitance of the MOSFET. f is the switching frequency. For maximum efficiency, $R_{DS(ON)}$ and C_{RSS} should be minimized.

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following equation:

$$T_J = T_A + P_{FET} \bullet \theta_{JA} = T_A + P_{FET} \bullet (\theta_{JC} + \theta_{CA})$$

T_J must not exceed the MOSFET maximum junction temperature rating. It is recommended to measure the MOSFET temperature in steady state to ensure that absolute maximum ratings are not exceeded.

To achieve high switching frequency (such as 2MHz) operation, Q_G and $R_{DS(ON)}$ of the power MOSFET must be carefully selected. High performance power MOSFETs with low Q_G and low $R_{DS(ON)}$ must be used. Since the gate drive voltage is set by the 5V $INTV_{CC}$ supply, logic-level threshold MOSFETs must be used in LT8357 applications. When switching at high frequency like 2MHz, the substantial gate charge current from $INTV_{CC}$ can be estimated as:

$$I_{INTVCC} = f \bullet Q_G$$

Make sure the total required $INTV_{CC}$ current not exceeding the $INTV_{CC}$ current limit in the data sheet. Typically, MOSFETs with less than 10nC Q_G are recommended.

SEPIC Converter: Output Diode Selection

To maximize efficiency, a fast switching diode with a low forward drop and low reverse leakage is desirable. The average forward current in normal operation is equal to the output current, and the peak current is equal to:

$$I_{D(PEAK)} = (1 + \frac{\chi}{2}) \bullet I_{O(MAX)} \bullet \frac{1}{1 - D_{MAX}}$$

It is recommended that the peak repetitive reverse voltage rating V_{RRM} is higher than V_{OUT} + $V_{IN(MAX)}$ by a safety margin (a 10V safety margin is usually sufficient).

The power dissipated by the diode is:

$$P_D = I_{O(MAX)} \bullet V_D$$

and the diode junction temperature is:

$$T_J = T_A + P_D \bullet R_{\theta JA}$$

The $R_{\theta JA}$ to be used in this equation normally includes the $R_{\theta JC}$ for the device plus the thermal resistance from the board to the ambient temperature in the enclosure. T_J must not exceed the diode maximum junction temperature rating.

SEPIC Converter: Output and Input Capacitor Selection

The selections of the output and input capacitors of the SEPIC converter are similar to those of the boost converter. Please refer to the Boost Converter, Output Capacitor Selection and Boost Converter, Input Capacitor Selection sections.

SEPIC Converter: Selecting the DC Coupling Capacitor

The DC voltage rating of the DC coupling capacitor (C_{DC}, as shown in Figure 10) should be larger than the maximum input voltage:

$$V_{CDC} > V_{IN(MAX)}$$

APPLICATIONS INFORMATION

C_{DC} has nearly a rectangular current waveform. During the switch off-time, the current through C_{DC} is I_{IN}, while approximately $-I_O$ flows during the on-time. The RMS rating of the coupling capacitor is determined by the following equation:

$$I_{RMS(CDC)} > I_{O(MAX)} \bullet \sqrt{\frac{V_{OUT} + V_D}{V_{IN(MIN)}}}$$

A low ESR and ESL, X5R or X7R ceramic capacitor works well for C_{DC}.

Efficiency Considerations

The power efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in circuits produce losses, five main sources account for most of the losses in LT8357 circuits:

1. DC $I \bullet V_D$ loss. The largest power loss comes from the forward voltage drop of the output diode and it causes the efficiency drop at high output currents.
2. DC $I^2 \bullet R$ losses. These arise from the resistances of the power MOSFET, sense resistor, inductor and PC board traces and cause the efficiency to drop at high output currents.
3. Transition loss. This loss arises from the brief amount of time the power MOSFET spends in the saturated region during switch node transition. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors.
4. $INTV_{CC}$ current. This is the sum of the power MOSFET gate driver and control circuit currents.
5. C_{IN} and C_{OUT} loss. The input capacitor has the difficult job of filtering the large RMS input current in the flyback converter. The output capacitor has the difficult job of filtering the large RMS output current in the boost, flyback and SEPIC converters. Both C_{IN} and C_{OUT} are required to have low ESR to minimize the AC $I^2 \bullet R$ loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.

When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If you make a change and the input current decreases, then the efficiency has increased. If there is no change in the input current, then there is no change in efficiency.

PC Board Layout Checklist

The basic PC board layout requires a dedicated ground plane layer. Also, for high current, a multilayer board provides heat sinking for power components.

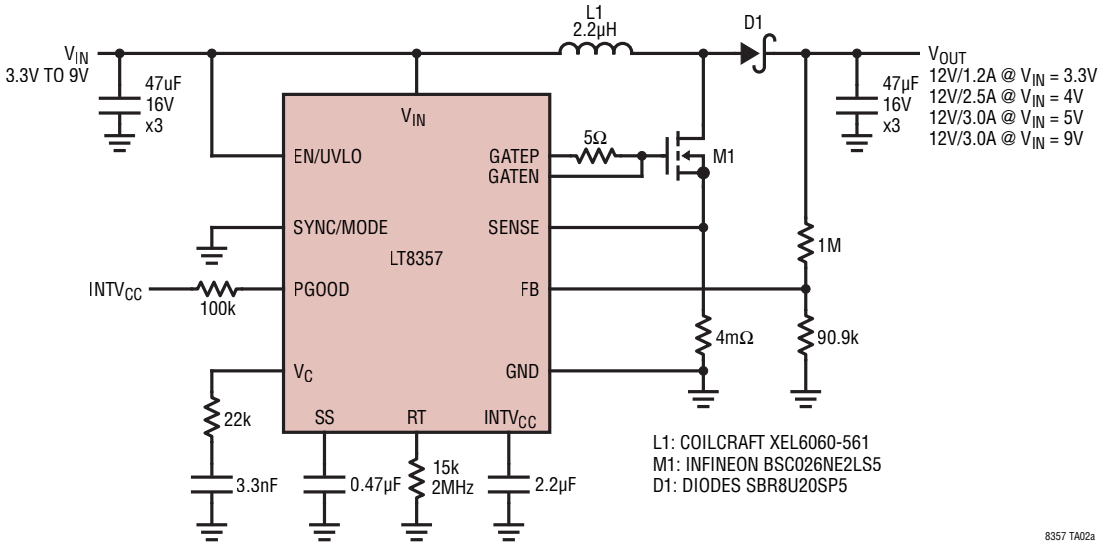
- The ground plane layer should not have any traces and it should be as close as possible to the layer with power MOSFET and output diode.
- Use immediate vias to connect the components to the ground plane. Use several large vias for each power component.
- Use planes for V_{IN} and V_{OUT} to maintain good voltage filtering and to keep power losses low.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to any DC net (V_{IN} or GND).
- Separate the signal and power grounds. All small-signal components should return to the exposed GND pad from the bottom, which is then tied to the power GND close to the power components.
- Place the power MOSFET and output diode as close to the controller as possible, keeping the power GND, power MOSFET gate drive signals and switch node traces short.
- Keep the high dV/dT switch nodes and power MOSFET gate drive signals away from sensitive small-signal nodes.
- Keep the following high dI/dT loops in different topologies as tight as possible with short leads and PCB trace lengths to reduce inductive ringing:

APPLICATIONS INFORMATION

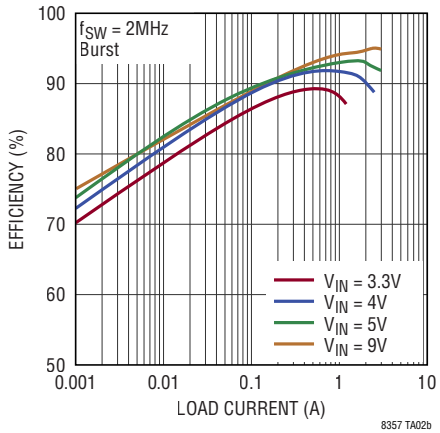
- In the boost configuration, the high dI/dT loop contains the output capacitor, sense resistor, power MOSFET and output diode.
- In the flyback configuration, the primary-side high dI/dT loop contains the input capacitor, primary winding, power MOSFET and sense resistor. The secondary-side high dI/dT loop contains the output capacitor, secondary winding and output diode.
- In the SEPIC configuration, the high dI/dT loop contains the power MOSFET, sense resistor, output capacitor, output diode and coupling capacitor.
- Place the sense resistor, R_{SENSE}, close to the SENSE pin of the IC, and route SENSE and power GND traces together. Avoid sense lines pass through noisy areas, such as switch nodes. If a filtering capacitor is used between SENSE and GND, place it as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the R_{SENSE} resistor. Low ESL sense resistor is recommended.
- Connect the V_C pin compensation network close to the IC, between V_C and the signal ground. The capacitor helps to filter the effects of PCB noise and output voltage ripple voltage from the compensation loop.
- Connect the $INTV_{CC}$ bypass capacitor, C_{INTVCC}, close to the IC, between the $INTV_{CC}$ and power GND. This capacitor carries the MOSFET gate driver's current peaks.

TYPICAL APPLICATIONS

2MHz, 3.3V to 9V Input, 12V Output Boost Converter

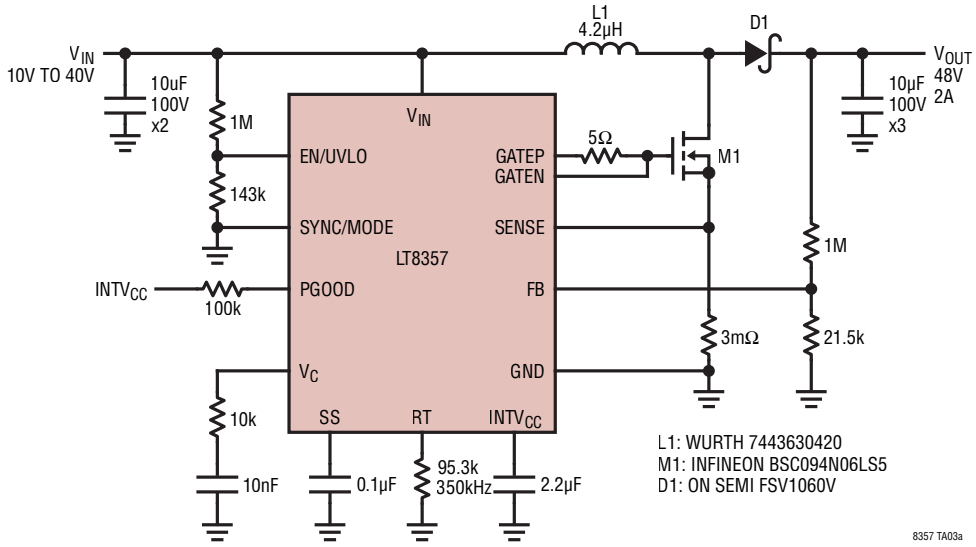


Efficiency vs Load Current

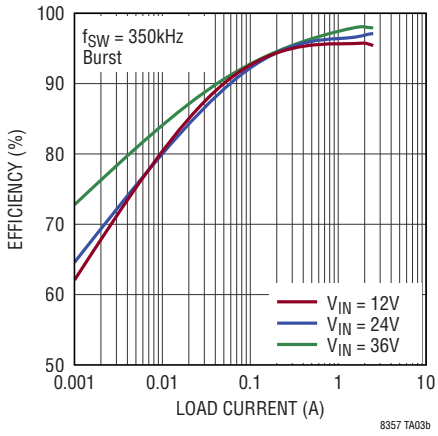


TYPICAL APPLICATIONS

10V to 40V Input, 48V/2A Output Boost Converter

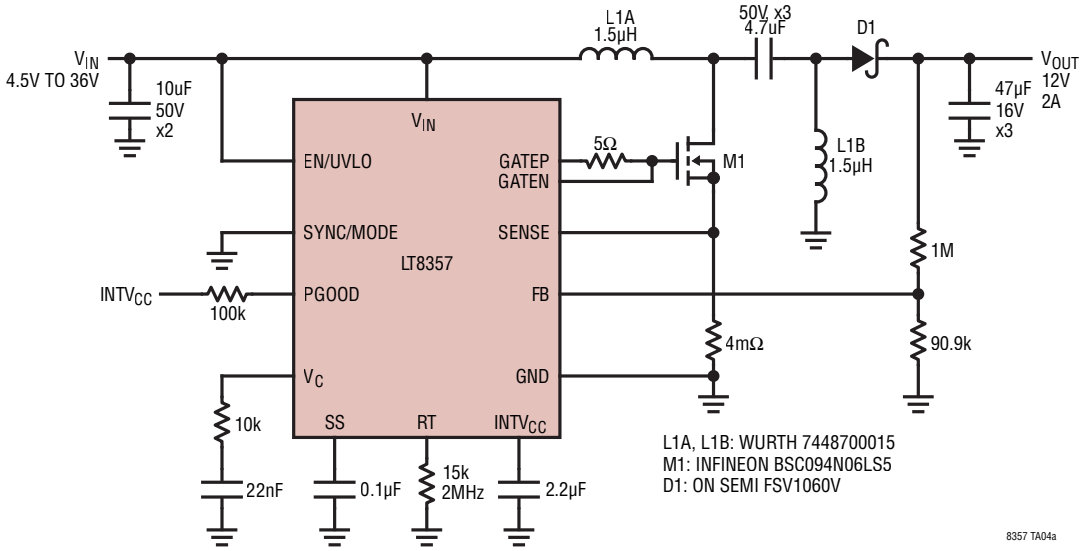


Efficiency vs Load Current

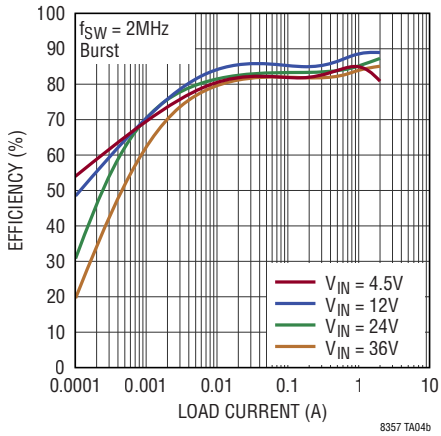


TYPICAL APPLICATIONS

2MHz, 4.5V to 36V Input, 12V/2A Output SEPIC Converter

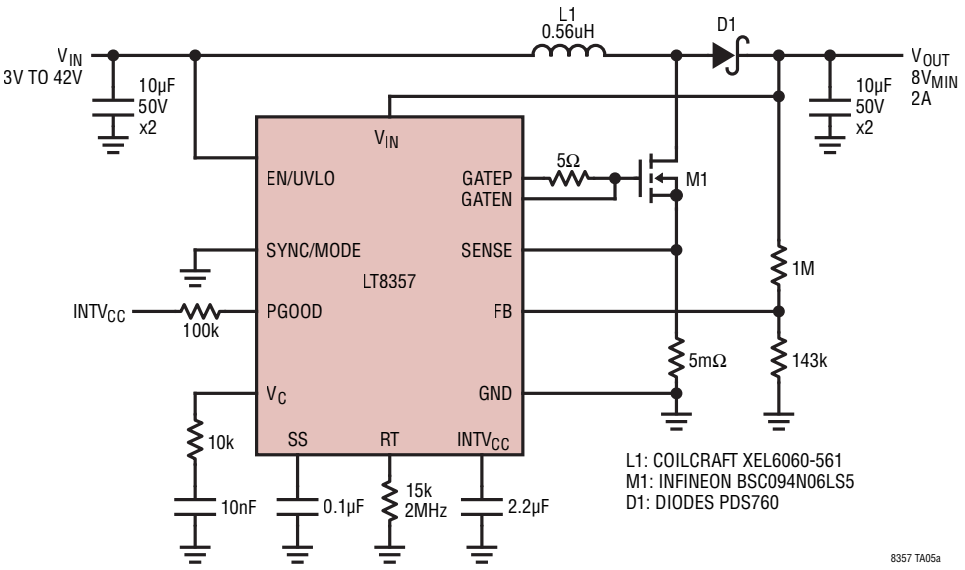


Efficiency vs Load Current

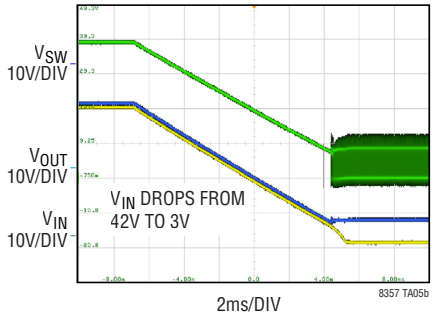


TYPICAL APPLICATIONS

2MHz, Low-I_Q Automotive Pre-Boost Application

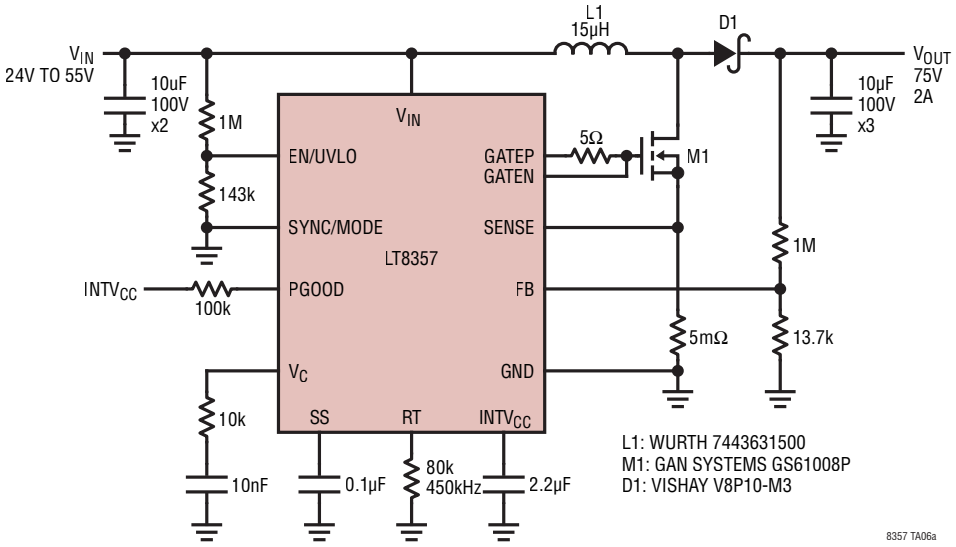


Line Transient Response
(Pass-Through to Boosting)

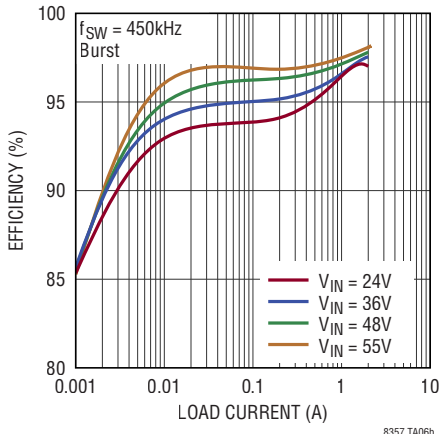


TYPICAL APPLICATIONS

24V to 55V Input, 75V/2A Output Boost Converter using GaN FET

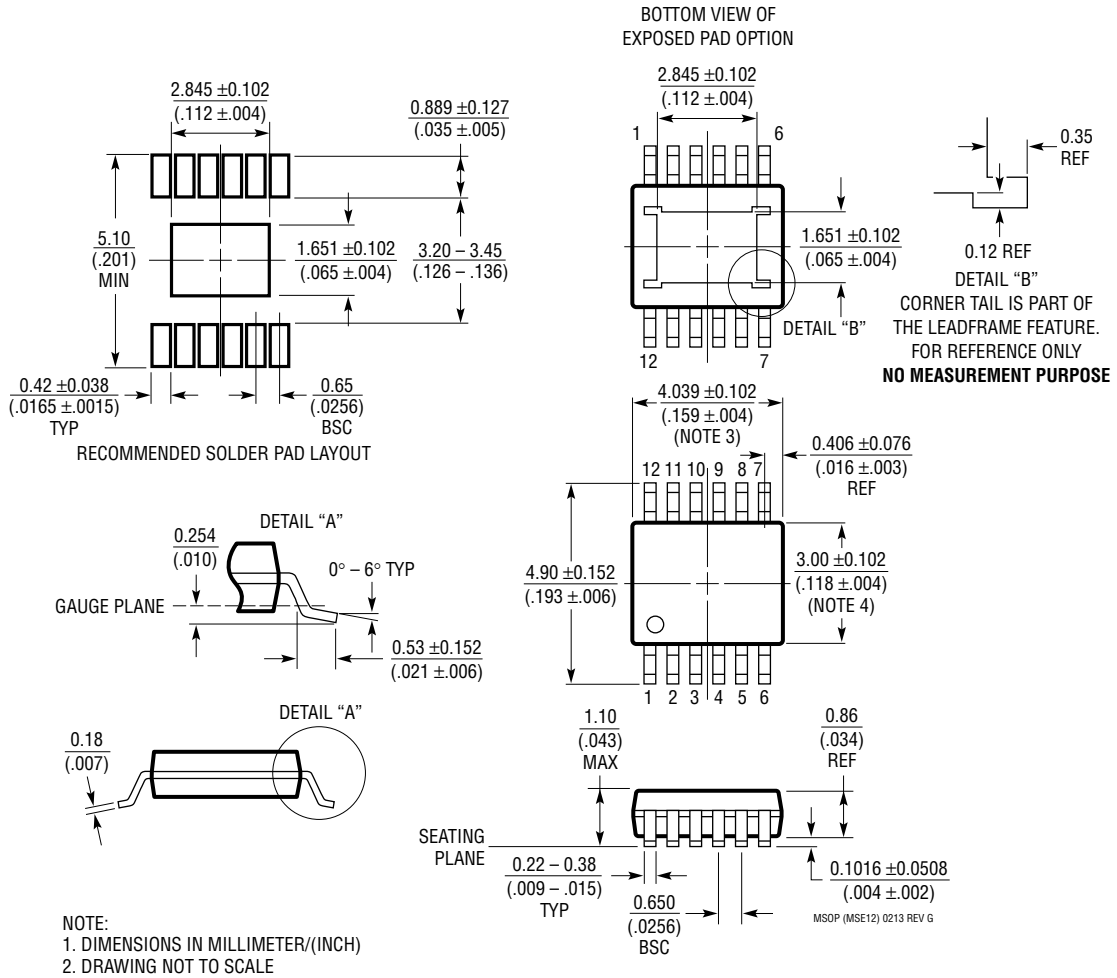


Efficiency vs Load Current



PACKAGE DESCRIPTION

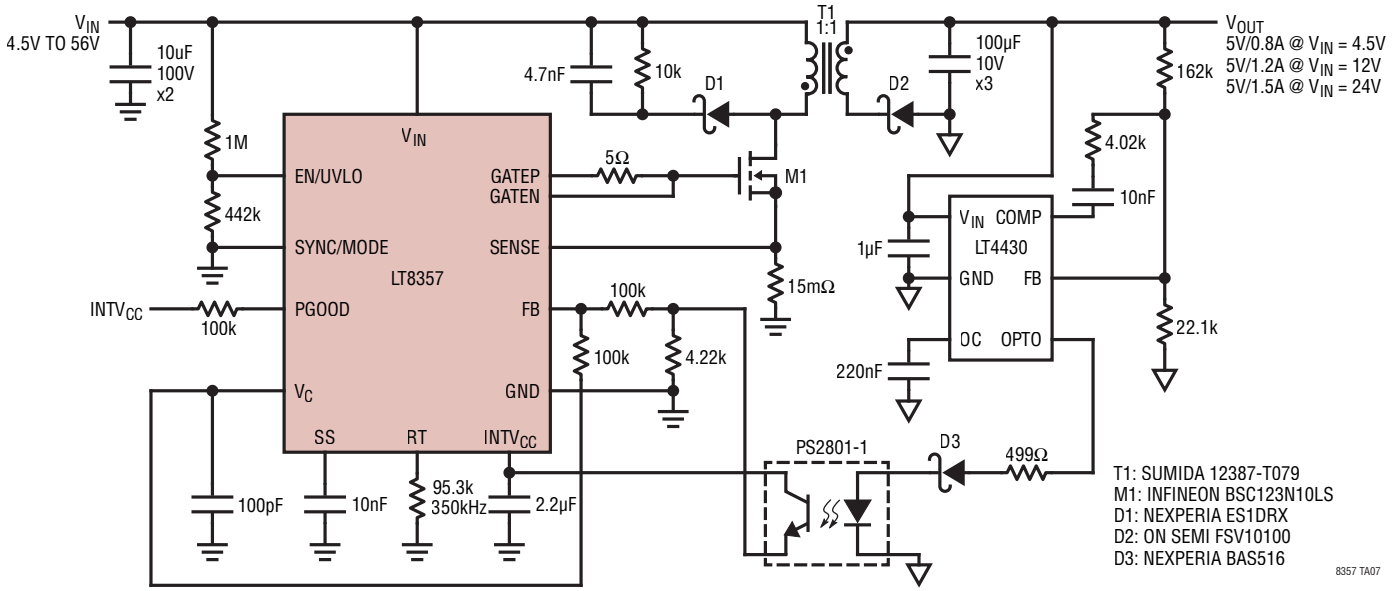
MSE Package
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev G)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

TYPICAL APPLICATION

4.5V to 56V Input, 5V Output Isolated Flyback Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3757/LT3757A	Boost, Flyback, SEPIC and Inverting Controllers	V_{IN}: 2.9V to 40V, Positive or Negative V_{OUT}, 3mm × 3mm DFN-10, MSOP-10E
LT3758/LT3758A	High Input Voltage, Boost, Flyback, SEPIC and Inverting Controllers	V_{IN}: 5.5V to 100V, Positive or Negative V_{OUT}, 3mm × 3mm DFN-10, MSOP-10E
LT3759	Boost, Flyback, SEPIC and Inverting Controller	V_{IN}: 1.6V to 42V, Positive or Negative V_{OUT}, MSOP-12E
LT8710	Synchronous SEPIC/Inverting/Boost Controller with Output Current Control	V_{IN}: 4.5V to 80V, Rail-to-Rail Output Current Monitor and Control, TSSOP-28
LT8330/LT8331/ LT8335	25V/60V/100V Low I_Q Boost/SEPIC/ Flyback/Inverting Converters	Low I_Q Monolithic with Integrated 28V/2A, 60V/1A and 140V/0.5A Switch, 3mm × 2mm DFN-8, MSOP-16(12)E
LT8362/LT8364	60V Low I_Q Boost/SEPIC/Inverting Converters	Low I_Q Monolithic with Integrated 60V/2A/4A Switch, 3mm × 3mm DFN-10, 4mm × 3mm DFN-12, MSOP-16(12)E

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