High Voltage, High Current Buck-Boost Battery Charge Controller with Maximum Power Point Tracking (MPPT)

FEATURES

- **V_{IN} Range: 6V to 80V**
- **V_{BAT} Range: 1.3V to 80V**
- **Single Inductor Allows V_{IN} Above, Below, or Equal to V_{BAT}**
- **Automatic MPPT for Solar Powered Charging**
- **Automatic Temperature Compensation**
- **No Software or Firmware Development Required**
- **Operation from Solar Panel or DC Supply**
- **Input and Output Current Monitor Pins**
- **Four Integrated Feedback Loops**
- Synchronizable Fixed Frequency: 100kHz to 400kHz
- 64-Lead (7mm × 11mm × 0.75mm) QFN Package

APPLICATIONS

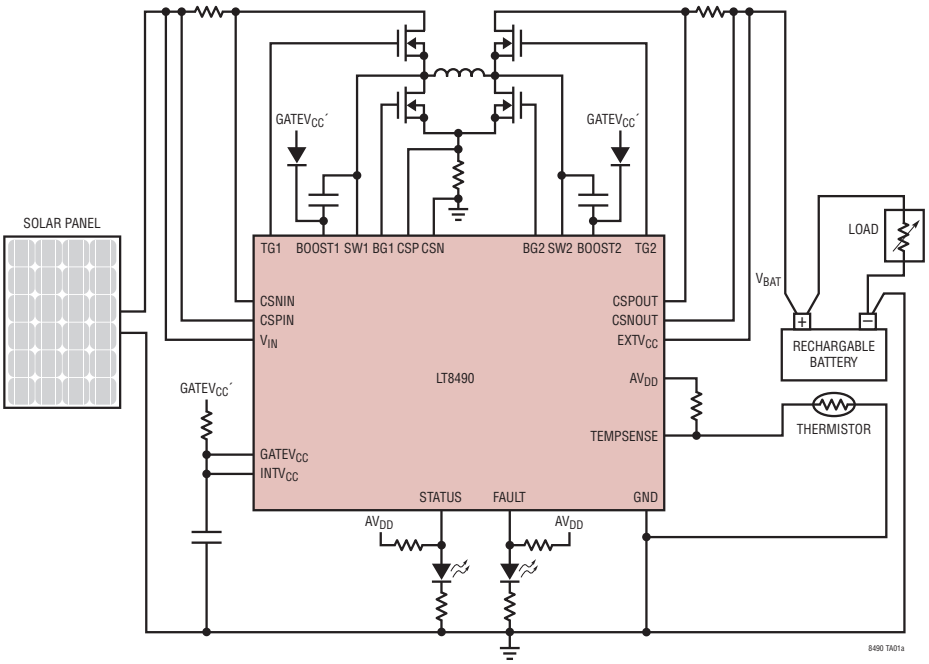
- Solar Powered Battery Chargers
- Multiple Types of Lead-Acid Battery Charging
- Li-Ion Battery Charger
- Battery Equipped Industrial or Portable Military Equipment

DESCRIPTION

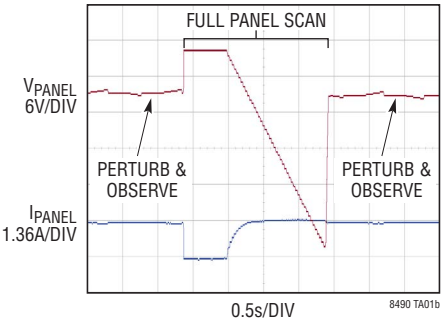
The LT®8490 is a buck-boost switching regulator battery charger that implements a constant-current constant-voltage (CCCV) charging profile used for most battery types, including sealed lead-acid (SLA), flooded, gel and lithium-ion. The device operates from input voltages above, below or equal to the output voltage and can be powered by a solar panel or a DC power supply. On-chip logic provides automatic maximum power point tracking (MPPT) for solar powered applications. The LT8490 can perform automatic temperature compensation by sensing an external thermistor thermally coupled to the battery. STATUS and FAULT pins containing charger information can be used to drive LED indicator lamps. The device is available in a low profile (0.75mm) 7mm × 11mm 64-lead QFN package.

TYPICAL APPLICATION

Simplified Solar Powered Battery Charger Schematic



Maximum Power Point Tracking



BACK PAGE APPLICATION

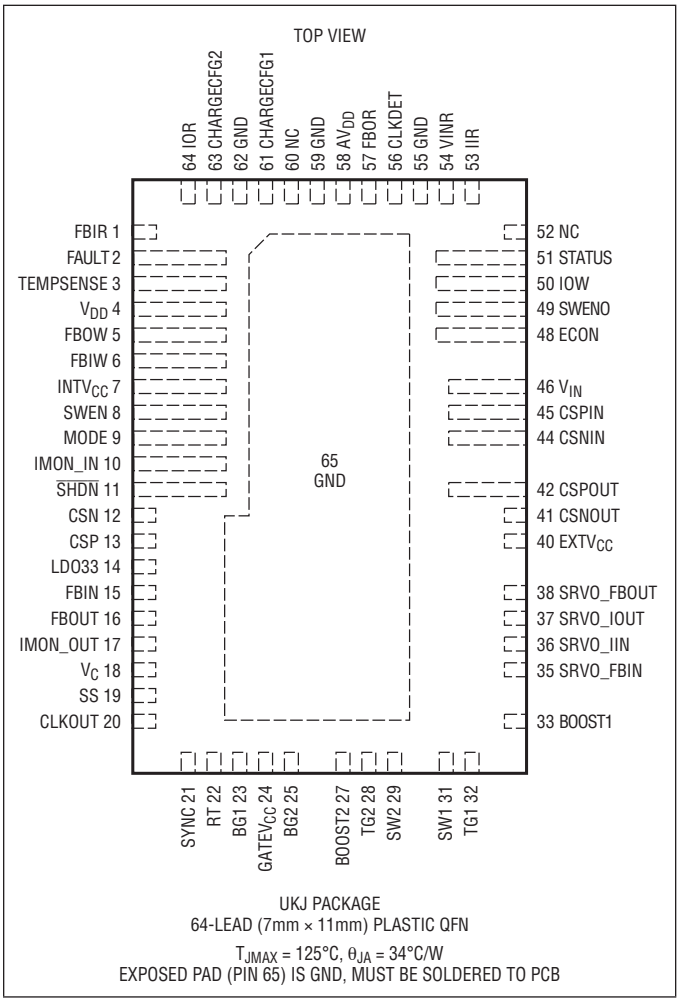
ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{CSP} – V_{CSN}$, $V_{CSPIN} – V_{CSNIN}$, $V_{CSPOUT} – V_{CSNOUT}$ ..... –0.3V to 0.3V
SS, CLKOUT, CSP, CSN Voltage ..... –0.3V to 3V
V_C Voltage (Note 2) ..... –0.3V to 2.2V
LDO33, V_{DD}, AV_{DD} Voltage ..... –0.3V to 5V
RT, FBOUT Voltage ..... –0.3V to 5V
IMON_IN, IMON_OUT Voltage ..... –0.3V to 5V
SYNC Voltage ..... –0.3V to 5.5V
$INTV_{CC}$, $GATEV_{CC}$ Voltage ..... –0.3V to 7V
$V_{BOOST1} – V_{SW1}$, $V_{BOOST2} – V_{SW2}$ ..... –0.3V to 7V
SWEN, MODE Voltage ..... –0.3V to 7V
SRVO_FBIN, SRVO_FBOUT Voltage ..... –0.3V to 30V
SRVO_IIN, SRVO_IOUT Voltage ..... –0.3V to 30V
FBIN, $\overline{SHDN}$ Voltage ..... –0.3V to 30V
CSNIN, CSPIN, CSPOUT, CSNOUT Voltage .. –0.3V to 80V
V_{IN}, $EXTV_{CC}$ Voltage ..... –0.3V to 80V
SW1, SW2 Voltage ..... 81V (Note 5)
BOOST1, BOOST2 Voltage ..... –0.3V to 87V
BG1, BG2, TG1, TG2 ..... (Note 4)
IOW, ECON, CLKDET Voltage ..... –0.3V to V_{DD} + 0.5V
SWENO, STATUS Voltage ..... –0.3V to V_{DD} + 0.5V
FBOW, FBIW, FAULT Voltage ..... –0.3V to V_{DD} + 0.5V
VINR, FBOR, IIR, IOR Voltage ..... –0.3V to V_{DD} + 0.5V
TEMPSENSE Voltage ..... –0.3V to V_{DD} + 0.5V
CHARGECFG2, CHARGECFG1 Voltage ..... –0.3V to V_{DD} + 0.5V

Operating Junction Temperature Range
  LT8490E (Notes 1, 3) ..... –40°C to 125°C
  LT8490I (Notes 1, 3) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UKJ PACKAGE
64-LEAD (7mm × 11mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 65) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8490EUKJ#PBF	LT8490EUKJ#TRPBF	LT8490UKJ	64-Lead (7mm × 11mm) Plastic QFN	–40°C to 125°C
LT8490IUKJ#PBF	LT8490IUKJ#TRPBF	LT8490UKJ	64-Lead (7mm × 11mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{DD} = AV_{DD} = 3.3V, $\overline{SHDN}$ = 3V unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Voltage Supply and Regulators						
V_{IN} Operating Voltage Range (Note 7)		●	6		80	V
V_{IN} Quiescent Current	Not Switching, V_{EXTVCC} = 0, V_{DD} = AV_{DD} = Float			2.65	4.2	mA
V_{IN} Quiescent Current in Shutdown	$V_{\overline{SHDN}}$ = 0V			0	1	µA
V_{DD} Quiescent Current	I_{AVDD} + I_{VDD}, V_{DD} = AV_{DD} = 3.3V	●	2.5	4	6.5	mA
$EXTV_{CC}$ Switchover Voltage	I_{INTVCC} = 20mA, V_{EXTVCC} Rising	●	6.15	6.4	6.6	V
$EXTV_{CC}$ Switchover Hysteresis				0.18		V
LDO33 Pin Voltage	5mA from LDO33 Pin	●	3.23	3.295	3.35	V
LDO33 Pin Load Regulation	I_{LDO33} = 0.1mA to 5mA			–0.25	–1	%
LDO33 Pin Current Limit		●	12	17.25	22	mA
LDO33 Pin Undervoltage Lockout	LDO33 Falling		2.96	3.04	3.12	V
LDO33 Pin Undervoltage Lockout Hysteresis				35		mV
Switching Regulator Control						
$\overline{SHDN}$ Input Voltage High	$\overline{SHDN}$ Rising to Enable the Device	●	1.184	1.234	1.284	V
$\overline{SHDN}$ Input Voltage High Hysteresis				50		mV
$\overline{SHDN}$ Input Voltage Low	Device Disabled, Low Quiescent Current	●			0.35	V
$\overline{SHDN}$ Pin Bias Current	$V_{\overline{SHDN}}$ = 3V $V_{\overline{SHDN}}$ = 12V			0 11	1 22	µA µA
SWEN Rising Threshold Voltage		●	1.156	1.206	1.256	V
SWEN Threshold Voltage Hysteresis				22		mV
MODE Pin Thresholds	Discontinuous Mode Forced Continuous Mode	● ●	 0.4		2.3	V V
IMON_OUT Rising threshold for CCM Operation	MODE = 0V	●	168	195	224	mV
IMON_OUT Falling threshold for DCM	MODE = 0V	●	95	122	150	mV
Voltage Regulation						
Regulation Voltage for FBOUT	V_C = 1.2V, $EXTV_{CC}$ = 0V	●	1.193	1.207	1.222	V
Regulation Voltage for FBIN	V_C = 1.2V, $EXTV_{CC}$ = 0V	●	1.184	1.205	1.226	V
FBOUT Pin Bias Current	Current Out of Pin			15		nA
FBIN Pin Bias Current	Current Out of Pin			10		nA
Current Regulation						
Regulation Voltage for IMON_IN and IMON_OUT	V_C = 1.2V, $EXTV_{CC}$ = 0V	●	1.187	1.208	1.229	V
IMON_IN Output Current	V_{CSPIN} – V_{CSNIN} = 50mV, V_{CSPIN} = 5.025V V_{CSPIN} – V_{CSNIN} = 50mV, V_{CSPIN} = 5.025V V_{CSPIN} – V_{CSNIN} = 0mV, V_{CSPIN} = 5V	 ● ●	54 53 2.5	57 57 7	60 61 11.5	µA µA µA
IMON_IN Overvoltage Threshold		●	1.55	1.61	1.67	V
IMON_OUT Output Current	V_{CSPOUT} – V_{CSNOUT} = 50mV, V_{CSPOUT} = 5.025V V_{CSPOUT} – V_{CSNOUT} = 50mV, V_{CSPOUT} = 5.025V V_{CSPOUT} – V_{CSNOUT} = 5mV, V_{CSPOUT} = 5.0025V V_{CSPOUT} – V_{CSNOUT} = 5mV, V_{CSPOUT} = 5.0025V	 ● ●	47.5 47 3.25 2.75	50 50 5 5	52.5 54.25 6.75 8	µA µA µA µA
IMON_OUT Overvoltage Threshold		●	1.55	1.61	1.67	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{DD} = AV_{DD} = 3.3V, $\overline{SHDN}$ = 3V unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Regulator Oscillator (OSC1)						
Switch Frequency Range	Syncing or Free Running		100		400	kHz
Switching Frequency, f_{OSC}	R_T = 365k R_T = 215k R_T = 124k	● ● ●	102 170 310	120 202 350	142 235 400	kHz kHz kHz
SYNC High Level for Synchronization		●	1.3			V
SYNC Low Level for Synchronization		●			0.5	V
SYNC Clock Pulse Duty Cycle	V_{SYNC} = 0V to 2V		20		80	%
Recommended Min SYNC Ratio, f_{SYNC}/f_{OSC}				3/4		
CLKOUT Output Voltage HIGH	1mA Out of CLKOUT Pin		2.3	2.45	2.55	V
CLKOUT Output Voltage LOW	1mA into CLKOUT Pin			25	100	mV
CLKOUT Duty Cycle	T_J = –40°C T_J = 25°C T_J = 125°C			22.7 44.1 77		% % %
Charging Control						
STATUS, FBOW, FBIW, SWENO, IOW, ECON Output Low Voltage	I_{OL} = 5mA	●		0.22	0.5	V
STATUS, FBOW, FBIW, SWENO, IOW, ECON Output High Voltage	I_{OH} = –5mA	●	2.7	3.0		V
FAULT Output Voltage Low	I_{OL} = 0.5mA	●		0.1	0.25	V
FAULT Output Voltage High	I_{OH} = –0.1mA	●	1.7	2.2		V
Power Supply Mode Detection Threshold (Note 6)	VINR Pin Falling	●	155	174		mV
Power Supply Mode Detection Threshold Hysteresis (Note 6)	VINR Pin			29		mV
Minimum VINR Voltage for Start-Up (Note 6)	Not in Power Supply Mode Low Power Mode Enabled Low Power Mode Disabled	 ● ●	 380 213	 395 225	 410 237	 mV mV
High Charging Current Threshold on IOR (Note 6)	IOR Rising → ECON Rising	●	168	195	224	mV
Low Charging Current Threshold on IOR (Note 6)	IOR Falling → ECON Falling	●	95	122	150	mV
Minimum CHARGECFG1 % of AV_{DD} to Disable Stage 3 (Note 6)	Temperature Compensation Enabled	●	94	95	96	%
Maximum CHARGECFG1 % of AV_{DD} to Disable Stage 3 (Note 6)	Temperature Compensation Disabled	●	4	5	6	%
Minimum CHARGECFG2 % of AV_{DD} to Disable Time Limits (Note 6)	Wide Valid Temperature Range	●	94	95	96	%
Maximum CHARGECFG2 % of AV_{DD} to Disable Time Limits (Note 6)	Narrow Valid Temperature Range	●	4	5	6	%
Minimum TEMPSENSE % of AV_{DD} to Detect Battery Disconnected (Note 6)		●	94.5	96	97.5	%
V_{CSPOUT} – V_{CSNOUT} Threshold for C/5 Detection (Note 6)	V_{CSxOUT} Common Mode = 5.0V, R_{TOTAL} from IMON_OUT to Ground = 24.3kΩ		9	10	11	mV
V_{CSPOUT} – V_{CSNOUT} Threshold for C/10 Detection (Note 6)	V_{CSxOUT} Common Mode = 5.0V, IOR Falling, R_{TOTAL} from IMON_OUT to Ground = 24.3kΩ		4.25	5	5.75	mV
FBIW, FBOW PWM Frequency (OSC2)				31.25		kHz
FBIW, FBOW PWM Resolution				8		Bits
STATUS UART Bit Rate		●	2160	2400	2640	Baud
Internal A/D Resolution				10		Bits

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Do not force voltage on the V_C pin.

Note 3: The LT8490E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8490I is guaranteed over the full –40°C to 125°C junction temperature range.

Note 4: Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only, otherwise permanent damage may occur.

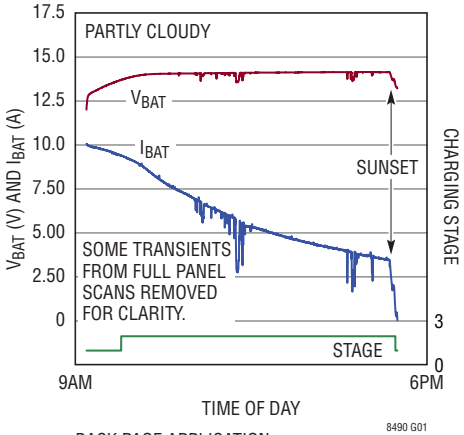
Note 5: Negative voltages on the SW1 and SW2 pins are limited in the applications by the body diodes of the external NMOS devices M2 and M3 or parallel Schottky diodes when present. The SW1 and SW2 pins are tolerant of these negative voltages in excess of one diode drop below ground, guaranteed by design.

Note 6: These thresholds are measured by the internal A-D converter. The A-D reference voltage is AV_{DD}. AV_{DD}, V_{DD} and an additional 2.8mA load are regulated by LDO33 to create the AV_{DD} reference for these measurements. The absolute threshold voltages will shift with corresponding changes in the AV_{DD} voltage.

Note 7: 10V minimum V_{IN} required for solar powered start-up if low power mode is enabled.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Solar Powered Charging Lead Acid Battery "A"



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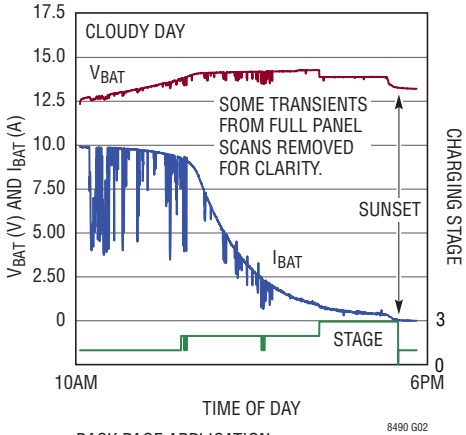
Solar Powered Charging Lead Acid Battery "B"



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Solar Powered Charging Lithium Ion Battery

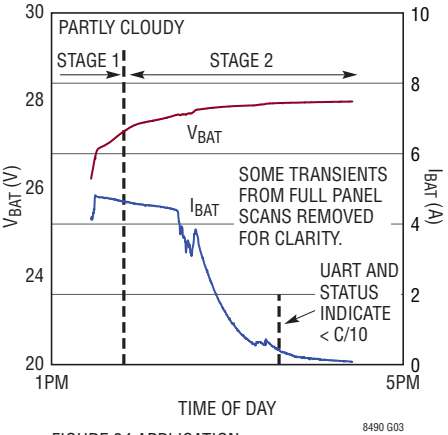
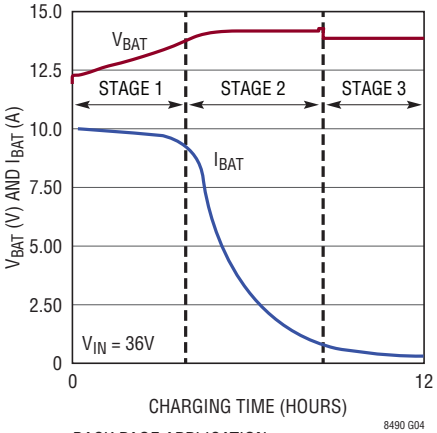


FIGURE 34 APPLICATION

Power Supply Mode Charging Lead Acid Battery "B"



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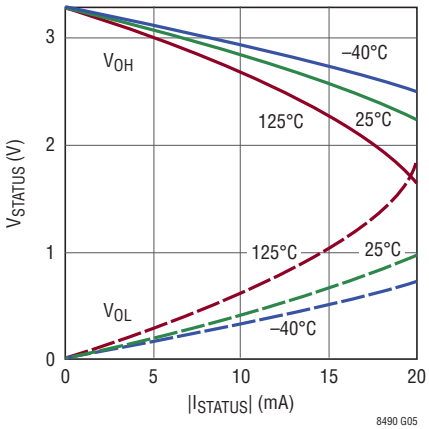
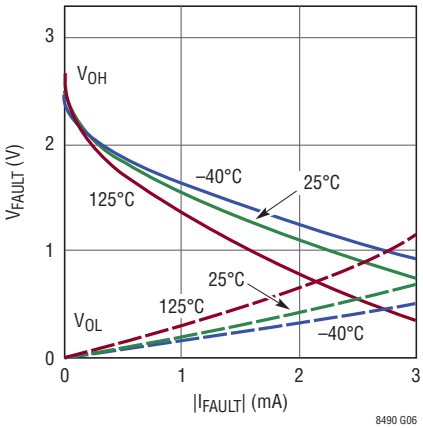
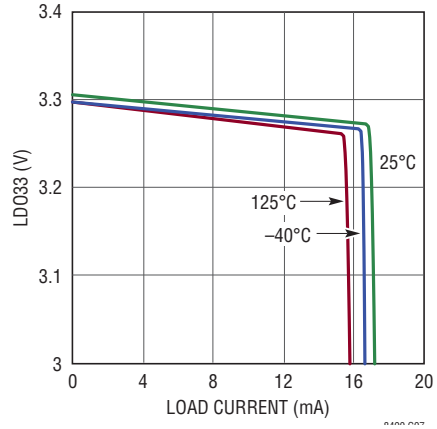
STATUS V_{OH} and V_{OL} (V_{DD} = AV_{DD} = 3.3V)



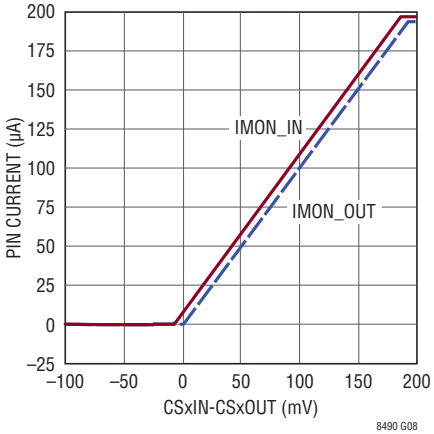
FAULT V_{OH} and V_{OL} (V_{DD} = AV_{DD} = 3.3V)



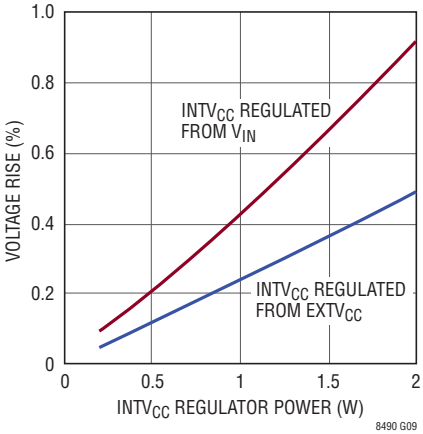
LDO33 Load Regulation (Not Connected to AV_{DD} and V_{DD})



IMON Output Currents



FBOUT, FBIN, IMONIN, IMONOUT Voltage Rise vs Power



TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Maximum Power Point Tracking

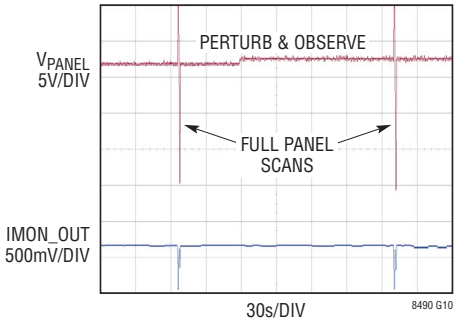


FIGURE 34 APPLICATION

Perturb and Observe

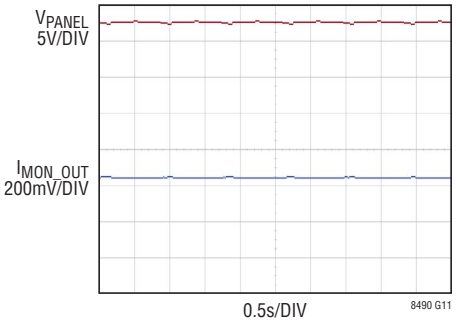


FIGURE 34 APPLICATION

Perturb and Observe

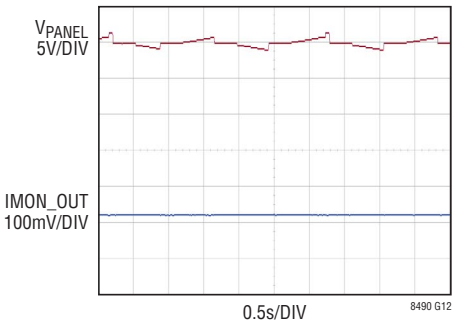


FIGURE 34 APPLICATION

Perturb and Observe Maximum Power Point Tracking

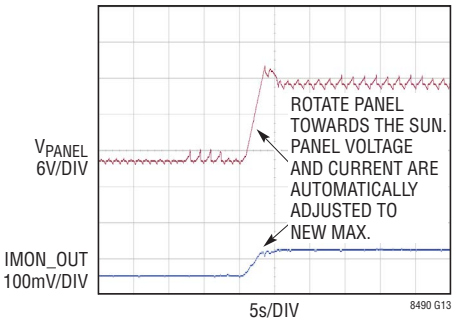


FIGURE 34 APPLICATION

Full Panel Scan Single Power Peak

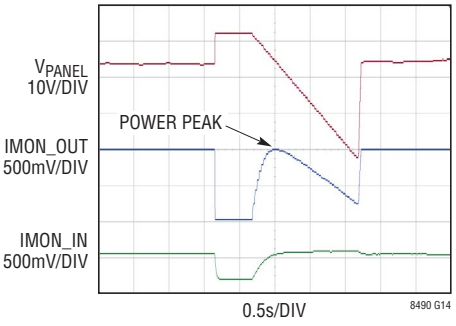


FIGURE 34 APPLICATION

Full Panel Scan—Partially Shaded with Dual Power Peaks

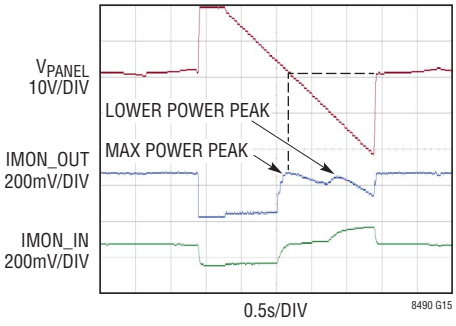


FIGURE 34 APPLICATION

Panel Voltage in Low Power Mode

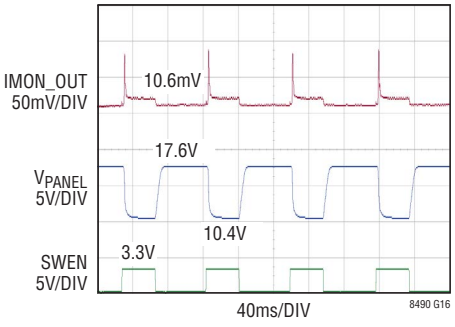


FIGURE 34 APPLICATION

Panel Voltage in Low Power Mode

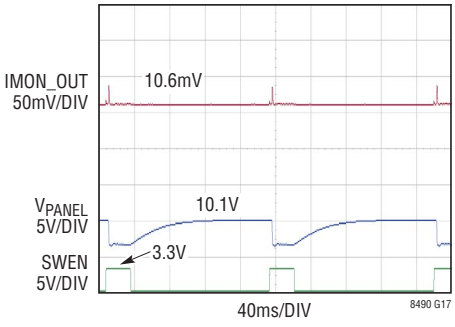


FIGURE 34 APPLICATION

PIN FUNCTIONS

FBIR (Pin 1): A/D Input Pin. Connects to FBIN pin to measure input feedback voltage.

FAULT (Pin 2): FAULT Pin. This pin generates an active high digital output that, when used with an LED, provides a visual indication of a fault event.

TEMPSENSE (Pin 3): A/D Input Pin. Connects to a thermistor divider network for sensing battery temperature or a resistor divider if unused. This pin is frequently monitored for temperature compensation and enforcing temperature limits.

V_{DD} (Pin 4): Control Logic Power Supply Pin. Connect this pin to LDO33 and AV_{DD}.

FBOW (Pin 5): PWM Digital Output Pin. Connects to FBOUT through an RCR network to temperature compensate the battery voltage.

FBIW (Pin 6): PWM Digital Output Pin. Connects to FBIN through an RCR network to adjust the solar panel voltage for MPPT.

$INTV_{CC}$ (Pin 7): Internal 6.35V Regulator Output Pin. Connects to the $GATEV_{CC}$ pin. $INTV_{CC}$ is powered from $EXTV_{CC}$ when the $EXTV_{CC}$ voltage is higher than 6.4V, otherwise $INTV_{CC}$ is powered from V_{IN}. Bypass this pin to ground with a minimum 4.7µF ceramic capacitor. See Switching Configuration - MODE Pin for additional details.

SWEN (Pin 8): Switch Enable Pin. Tie to the SWENO pin.

MODE (Pin 9): Mode Pin. The voltage applied to this pin sets the operating mode of the switching regulator. Tie this pin to $INTV_{CC}$ to make discontinuous current mode active. Tie this pin to ground to operate in discontinuous current mode for low battery charging currents and continuous current mode for high battery charging currents. Do not float this pin. See Switching Configuration - MODE Pin for additional details.

IMON_IN (Pin 10): Input Current Monitor Pin. The current out of this pin is proportional to the input current. See the Applications Information section for more information.

$\overline{SHDN}$ (Pin 11): Shutdown Pin. In conjunction with the UVLO (undervoltage lockout) circuit, this pin is used to enable/disable the chip. Do not float this pin.

CSN (Pin 12): The (–) Input to the Inductor Current Sense and Reverse Current Detect Amplifier.

CSP (Pin 13): The (+) Input to the Inductor Current Sense and Reverse Current Detect Amplifier. The V_C pin voltage and built-in offsets between the CSP and CSN pins set the current trip threshold.

LDO33 (Pin 14): 3.3V Regulator Output. This supply provides power to the V_{DD} and AV_{DD} pins. Bypass this pin to ground with a minimum 4.7µF ceramic capacitor.

FBIN (Pin 15): Input Feedback Pin. This pin is connected to the input error amplifier input.

FBOUT (Pin 16): Output Feedback Pin. This pin connects the error amplifier input to an external resistor divider from the output.

IMON_OUT (Pin 17): Output Current Monitor Pin. The current out of this pin is proportional to the average output current. See the Applications Information section for more information.

V_C (Pin 18): Error Amplifier Output Pin. Tie the external compensation network to this pin.

SS (Pin 19): Soft-Start Pin. Place 100nF of capacitance from this pin to ground. Upon start-up, this pin will be charged by an internal resistor to 2.5V.

CLKOUT (Pin 20): Switching Regulator Clock Output Pin. CLKOUT will toggle at the same frequency as the switching regulator oscillator (OSC1 on the Block Diagram) or as the SYNC pin, but is approximately 180° out-of-phase. CLKOUT can also be used as a temperature monitor of the switching regulator since the CLKOUT duty cycle varies linearly with the junction temperature of the switching regulator. It is connected to CLKDET through an RC filter. The CLKOUT pin can drive capacitive loads up to 200pF.

SYNC (Pin 21): To synchronize the switching frequency to an outside clock, simply drive this pin with a clock. The high voltage level of the clock needs to exceed 1.3V, and the low level should be less than 0.5V. Drive this pin to less than 0.5V to revert to the internal free-running clock (OSC1 in the Block Diagram).

PIN FUNCTIONS

RT (Pin 22): Timing Resistor Pin. Adjusts the switching regulator frequency (OSC1) when SYNC is not driven by a clock. Place a resistor from this pin to ground to set the free-running frequency of OSC1. Do not float this pin.

BG1, BG2 (Pin 23/Pin 25): Bottom Gate Drive. Drives the gates of the bottom N-channel MOSFETs between ground and $GATEV_{CC}$.

$GATEV_{CC}$ (Pin 24): Power Supply for Gate Drivers. Must be connected to the $INTV_{CC}$ pin. Do not power from any other supply. Locally bypass to ground.

BOOST1, BOOST2 (Pin 33/Pin 27): Boosted Floating Driver Supply. The (+) terminal of the bootstrap capacitor connects here. The BOOST1 pin swings from a diode voltage below GATEVcc up to V_{IN} + $GATEV_{CC}$. The BOOST2 pin swings from a diode voltage below $GATEV_{CC}$ up to V_{BAT} + $GATEV_{CC}$.

TG1, TG2 (Pin 32/Pin 28): Top Gate Drive. Drives the top N-channel MOSFETs with voltage swings equal to $GATEV_{CC}$ superimposed on the switch node voltages.

SW1, SW2 (Pin 31/Pin 29): Switch Nodes. The (–) terminal of the bootstrap capacitors connect here.

SRVO_FBIN (Pin 35): Open-Drain Logic Output. This pin is pulled to ground when the input voltage feedback loop is active. This pin is unused for most LT8490 applications and can be floated.

SRVO_IIN (Pin 36): Open-Drain Logic Output. This pin is pulled to ground when the input current feedback loop is active. This pin is unused for most LT8490 applications and can be floated.

SRVO_IOUT (Pin 37): Open-Drain Logic Output. This pin is pulled to ground when the output current feedback loop is active. This pin is unused for most LT8490 applications and can be floated.

SRVO_FBOUT (Pin 38): Open-Drain Logic Output. This pin is pulled to ground when the output voltage feedback loop is active. This pin is unused for most LT8490 applications and can be floated.

$EXTV_{CC}$ (Pin 40): External V_{CC} Input. When $EXTV_{CC}$ exceeds 6.4V (typical), $INTV_{CC}$ will be powered from this pin. When $EXTV_{CC}$ is lower than 6.22V (typical), $INTV_{CC}$ will be powered from V_{IN}. See Switching Configuration - MODE Pin for additional details.

CSNOUT (Pin 41): The (–) Input to the Output Current Sense Amplifier.

CSPOUT (Pin 42): The (+) Input to the Output Current Sense Amplifier. This pin and the CSNOUT pin measure the voltage across the sense resistor to provide the output current signals.

CSNIN (Pin 44): The (–) Input to the Input Current Sense Amplifier. This pin and the CSPIN pin measure the voltage across the sense resistor to provide the instantaneous input current signals.

CSPIN (Pin 45): The (+) Input to the Input Current Sense Amplifier.

V_{IN} (Pin 46): Main Input Supply Pin. Must be bypassed to local ground plane.

ECON (Pin 48): Digital Output Pin. Optional control output signal used to disconnect $EXTV_{CC}$ from the battery when the average charge current drops below a predetermined threshold.

SWENO (Pin 49): Digital Output Pin. Connect to SWEN. Enables the switching regulator. A 200kΩ pull-down resistor is required from this pin to ground.

IOW (Pin 50): Digital Output Pin. Connects to IMON_OUT through a resistor. By switching the pin between logic low and high impedance, the total R_{IMON_OUT} changes, which changes the output current limit.

STATUS (Pin 51): Digital Output Pin. When used with an LED, this signal provides a visual indication of the progress of the charging algorithm. In addition, STATUS transmits two UART bytes (8 bits, no parity, one stop bit, 2400 baud) every 3.5 seconds (typical), which indicates status and fault information.

IIR (Pin 53): A/D Input Pin. Connects to IMON_IN to read input current. Used to manage MPPT.

PIN FUNCTIONS

VINR (Pin 54): A/D Input Pin. Connects to resistive divider on VIN to measure input voltage. Used to manage MPPT and start-up.

CLKDET (Pin 56): A/D Input Pin. Connects to CLKOUT through an RC filter to detect the duty cycle of CLKOUT. Used to manage start-up.

FBOR (Pin 57): A/D Input Pin. Connects to FBOUT pin to read charger output voltage. Used to manage the charging algorithm.

AV_{DD} (Pin 58): A/D Positive Reference Pin. Tie this pin to V_{DD} and LDO33.

CHARGECFG1 (Pin 61): A/D Input Pin. Used to configure the float voltage, temperature compensation and enable stage 3 charging.

CHARGECFG2 (Pin 63): A/D Input Pin. Used to configure time limits and the valid battery temperature range.

IOR (Pin 64): A/D Input Pin. Connects to IMON_OUT pin to read the charger output current. Used to manage the charging algorithm.

GND (Exposed Pad 65 and Pins 55, 59, 62): Ground. Tie directly to local ground plane.

NC (Pins 52, 60): Not connected.

BLOCK DIAGRAM

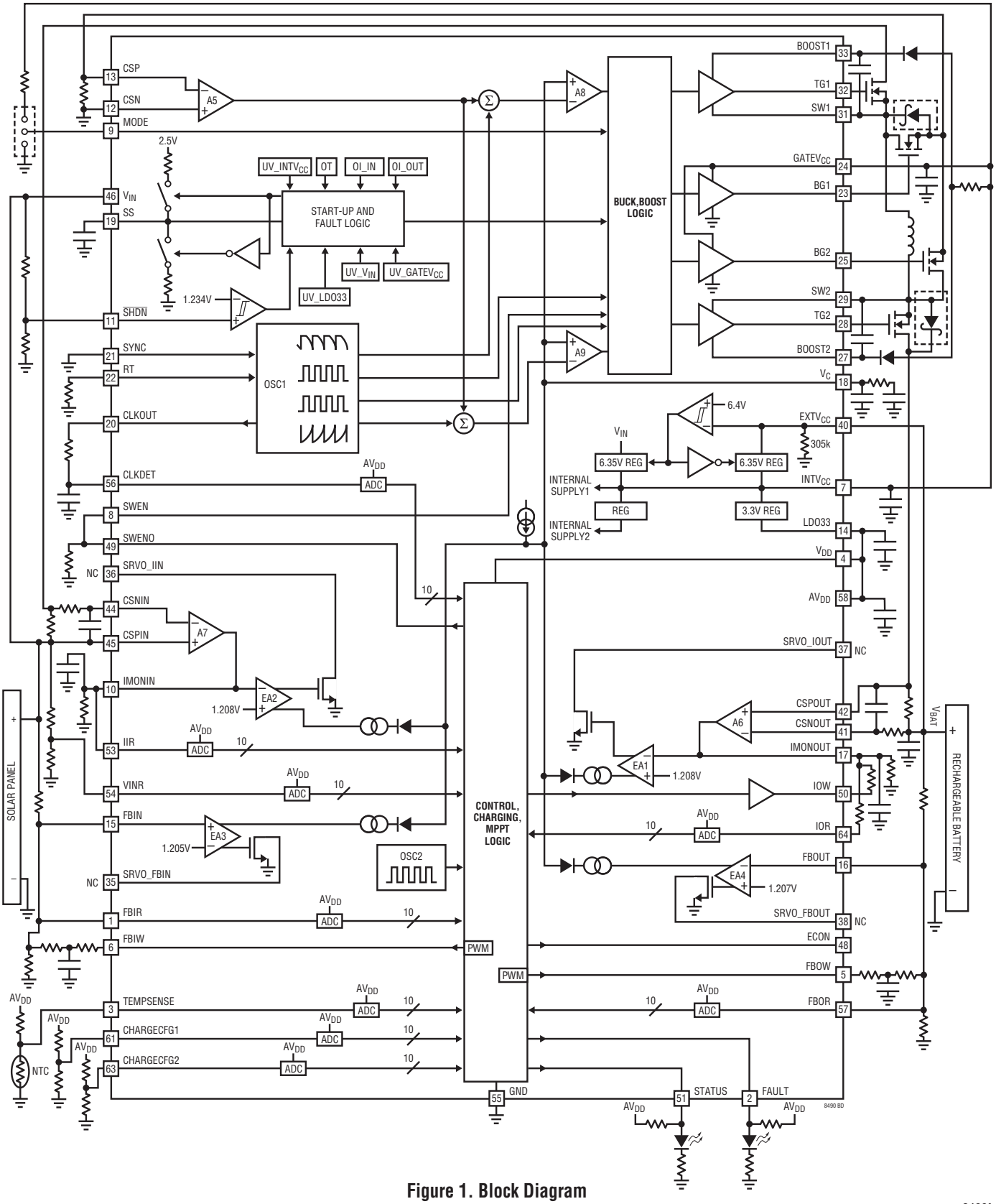


Figure 1. Block Diagram

OPERATION

Overview

The LT8490 is a powerful and easy to use battery charging controller with automatic maximum power point tracking (MPPT) and temperature compensation. The LT8490 is based on the LT8705 buck-boost controller with additional battery charging and MPPT control functions. Refer to the LT8705 data sheet for more detailed information about the switching regulator portions of the LT8490. Several reference applications are included in this data sheet to simplify system design. Many battery charging applications can be implemented using one of the reference applications with little or no modification required. Configuration for the various charging parameters is implemented in the hardware. No software or firmware development is required.

The LT8490 includes four different forms of regulation: output current, input current, input voltage and output voltage (EA1-EA4 respectively as shown in Figure 1). Whichever form of regulation requires the lowest voltage on the V_C pin limits the commanded inductor current. When powered by a solar panel, the MPPT function uses input voltage regulation to locate and track the maximum power point of the panel. Input current regulation is used to limit the maximum current drawn from the input supply. The output current regulation limits the battery charging current, and the output voltage regulation is used to set the maximum battery charging voltage.

The LT8490 offers user configurable timers that can be enabled with the appropriate resistor divider on the CHARGECFG2 pin. If a timer has been set and expires, the LT8490 will halt charging and communicate this through the STATUS and FAULT pins. Options for automatic restart of the charge cycle are discussed later in the Automatic Charger Restart and Fault Recovery section.

The LT8490 also includes a TEMPSENSE pin, which can be connected to an NTC resistor divider network thermally coupled to the battery pack. When connected, the TEMPSENSE pin can provide temperature compensated charging and/or can be used to disable charging when the battery is outside of safe temperature limits. The presence of the NTC resistor can also give an indication to the charger if the battery is connected or not.

The LT8490 also provides charging status and fault indicators through the STATUS and FAULT pins. The behavior of these pins is described in the STATUS and FAULT Indicators section.

Battery Charging Algorithm

The LT8490 implements a CCCV charging algorithm. The idealized charging profile is shown in Figure 2 and assumes constant temperature and adequate input power. As battery temperature and illumination conditions on the panel change, the actual current and voltage seen by the battery will vary accordingly.

After start-up, the LT8490 frequently measures the battery voltage and charging current to determine the proper charging stage.

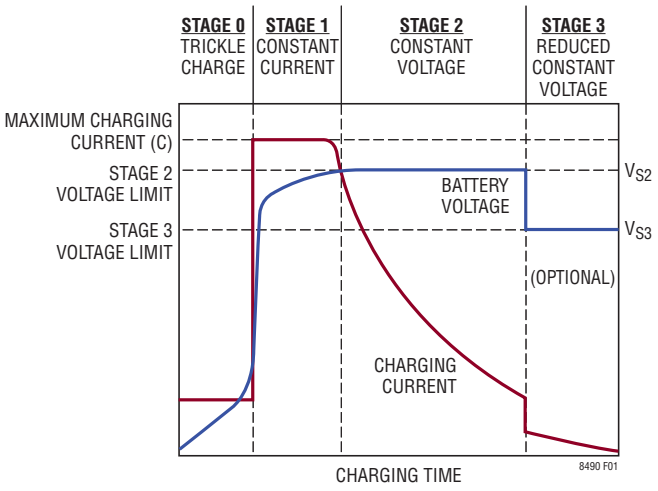


Figure 2. Typical Battery Charging Cycle

OPERATION

STAGE 0: In Stage 0 (reduced constant-current/trickle charge) the LT8490 charges the battery with a hardware configurable reduced constant current. This trickle charge stage occurs for battery voltages between 35% to 70% (typical) of the Stage 2 voltage limit (V_{S2}).

STAGE 1: In Stage 1 (full constant-current) the LT8490 charges the battery with a hardware configurable constant current equal to or higher than in Stage 0. This constant current stage occurs for battery voltages between 70% to 98% (typical) of the Stage 2 voltage limit. This charging stage is often referred to as bulk charging. This charging stage will be called Stage 1 for the remainder of this document.

STAGE 2: In Stage 2 (constant-voltage) the LT8490 charges the battery with a hardware configurable constant voltage. This constant voltage stage occurs for battery voltages above 98% (typical) of the Stage 2 voltage limit. This charging stage is often referred to as float charging for lithium-ion batteries and absorption charging for lead-acid batteries. To avoid confusion, this charging stage will be called Stage 2 for the remainder of this document.

If the optional Stage 3 is enabled, the LT8490 will proceed from Stage 2 to Stage 3 when the charging current drops below C/10. Other conditions for exiting Stage 2 depend on whether time limits are enabled for the charger. See the Charging Time Limits section for more details about Stage 2 termination.

STAGE 3 (OPTIONAL): Stage 3 is optional as configured with the CHARGECFG1 pin. In Stage 3 the LT8490 charges the battery with a hardware configurable reduced constant voltage. This charging stage is often referred to as float charging in lead-acid battery charging. This charging stage will be called Stage 3 for the remainder of this document.

Charging will automatically restart if, during Stage 3, the charging current exceeds C/5 or the battery voltage falls below 96% (typical) of the Stage 3 voltage limit (V_{S3}). In addition, an optional time limit can be enabled to terminate charging in Stage 3. See the Charging Time Limits section for more details about Stage 3 termination.

Table 1. Description of LT8490 Charging Stages

STAGE	NAME	METHOD	DURATION
0	Trickle Charge	Constant Current at a Configured Fraction of Full Charge Current	Until Battery Voltage Rises Above V_{S0} (70% of Stage 2 Voltage Limit)
			Optional Max Time Limit
1	Constant Current	Constant Full Charge Current	Until Battery Voltage Rises Above V_{S1} (98% of Stage 2 Voltage Limit)
			Optional Max Time Limit for Stage 1 + Stage 2
2	Constant Voltage	Constant Voltage	Until Charging Current Falls Below C/10 or Optional Indefinite Charging
			Optional Max Time Limit for Stage 1 + Stage 2
3 (Optional)	Reduced Constant Voltage	Constant Voltage at a Configured Fraction of Stage 2 Constant Voltage	Until Battery Voltage Falls below 96% of V_{S3} (Stage 3 Voltage Limit - Configurable) or Charging Current Rises Above C/5
			Optional Max Time Limit. The same duration as the Stage 1 + Stage 2 Time Limit.

Maximum Power Point Tracking

When powered by a solar panel, the LT8490 employs a proprietary Perturb and Observe algorithm for identifying the maximum power point. This algorithm provides accurate MPPT for slow to moderate changes in panel illumination. The panel is also scanned periodically to avoid settling on a false maximum power point for long periods of time, in the case of non-uniform panel illumination.

Fault Conditions

The LT8490 can indicate the presence of a fault condition through the STATUS and FAULT pins. These faults include: battery undervoltage, battery overtemperature, battery under temperature and timer expiration. Following a fault, the LT8490 will discontinue charging until the fault condition is removed, at which point it will continue or restart the charging cycle. See the Automatic Charger Restart and Fault Recovery section for more information.

APPLICATIONS INFORMATION

Input Voltage Sensing and Modulation Network

The passive component network shown in Figure 3 is required to properly measure and modulate the input supply voltage. This network is required whether the supply is a solar panel or a DC voltage source.

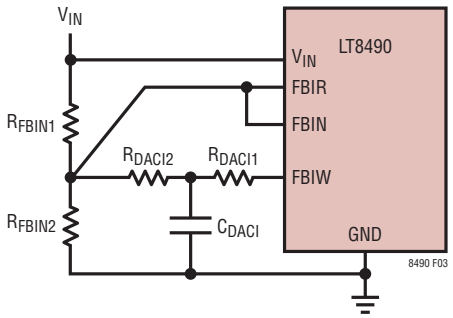


Figure 3. Input Feedback Resistor Network

Choosing the components requires knowing the maximum panel open-circuit voltage (V_{OCMAX}) as well as the maximum DC input supply voltage (V_{DCMAX}) desired (see the DC Supply Powered Charging section for more information). V_{OCMAX} typically occurs at cold temperatures and should be specified in the panel manufacturer's data sheet. Use the following equations to determine proper component values:

$$R_{FBIN1} = 100k \bullet \left[\frac{1+\left(\frac{4.470V}{V_{MAX}-6V}\right)}{1+\left(\frac{5.593}{V_{MAX}-6V}\right)} \right] \Omega$$

$$R_{DACI2} = 2.75 \bullet \left(\frac{R_{FBIN1}}{V_{MAX}-6V} \right) \Omega$$

$$R_{FBIN2} = \frac{1}{\left(\frac{1}{100k - R_{FBIN1}}\right) - \left(\frac{1}{R_{DACI2}}\right)} \Omega$$

$$R_{DACI1} = 0.2 \bullet R_{DACI2} \Omega$$

$$C_{DACI} = \frac{1}{1000 \bullet R_{DACI1}} F$$

where V_{MAX} is the greater of V_{OCMAX} and V_{DCMAX} with some additional margin. These resistors should have a 1% tolerance or better.

Due to the granularity of standard resistor values, simply rounding the calculated results to their nearest standard values may result in unwanted errors. Consider using multiple resistors in series to more closely match the calculated results. Otherwise, use standard resistor values and check the final results with the following equations:

$$V_{X2} = 1.205 \bullet \left[\frac{R_{FBIN1}}{R_{DACI1}+R_{DACI2}} + \left(\frac{R_{FBIN1}}{R_{FBIN2}} \right) + 1 \right]$$

V_{X2} indicates the actual V_{MAX} using the selected resistors. Make sure this result is greater than or equal to the desired V_{MAX} for the application.

$$V_{X1} = V_{X2} - 3.3 \bullet \left(\frac{R_{FBIN1}}{R_{DAC1}+R_{DAC2}} \right)$$

V_{X1} should be as close to 6V as possible. Iterations may be required to determine the best standard resistor values.

Table 2 shows good sets of standard value components for maximum input voltages of 20V, 40V, 60V and 80V. Iterative calculations were required to select these values that achieve the best overall results.

Table 2. Input Feedback Network vs Panel Voltage

V_{MAX} (V)	R_{FBIN1} (kΩ)	R_{FBIN2} (kΩ)	R_{DACI1} (kΩ)	R_{DACI2} (kΩ)	C_{DACI} (nF)
20	95.3	8.45	3.4	19.1	270
40	107	4.87	1.69	8.66	560
60	105	3.24	1.05	5.36	1000
80	133	3.09	1.05	4.87	1000

As discussed later in DC Supply Powered Charging, arbitrarily setting V_{MAX} to 80V may not result in the best operation of the LT8490 for all conditions, particularly at low input voltages. Be sure to give proper consideration to the required voltage range for each application.

Solar Powered Charging

VINR DIVIDER NETWORK: The LT8490 can be powered by a solar panel or a DC power supply. As discussed later in DC Supply Powered Charging, the VINR pin must be pulled low when being powered by a DC supply. Otherwise, VINR must be connected to the resistor divider network as shown in Figure 4.

APPLICATIONS INFORMATION

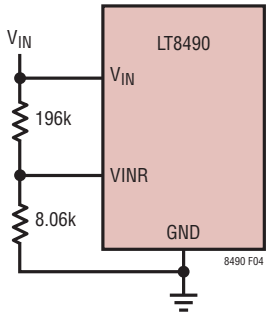


Figure 4. VINR Resistor Divider Circuit

The LT8490 uses this divider network to measure absolute panel voltage (as part of its maximum power point calculations) and to check for adequate input voltage to operate the charger. These resistors should have a 1% tolerance or better.

TIMER TERMINATION DISABLED: When powered by a solar panel, the timer termination option (see the Charging Time Limits section for more detail) is automatically disabled. This is due to the inability to guarantee full charging current during the entire charging cycle in cases where the panel illumination conditions change. In addition, the timers can reset if all power to the charger is lost due to insufficient lighting. This makes the use of timer termination potentially unreliable in solar powered applications.

C/10 DETECTION: When powered by a solar panel, charging current may drop below C/10 because the battery is approaching full charge, or because the solar panel has insufficient lighting. If sufficient panel power is available, the LT8490 can determine if the charging current has dropped below C/10 due to the battery approaching full charge. In this case, the charger will proceed from Stage 2 to the next appropriate stage. If the LT8490 is able to determine that the charging current has dropped below C/10 due to insufficient panel power, the charger will continue operating in Stage 2.

MINIMUM PANEL VOLTAGE REQUIREMENT: A minimum panel voltage of 6V is required to operate the charger. However, higher panel voltages are required in various other cases.

1. LOW POWER MODE ENABLED: Low power mode allows additional power to be recovered from the solar panel under very weak lighting conditions. When low power mode is enabled, the panel voltage must initially exceed 10V (typical – as measured through the VINR pin) before the charger will attempt to charge the battery. Read the Optional Low Power Mode section for more details.
2. LOW POWER MODE DISABLED: If low power mode is disabled the charger will attempt to charge the battery as long as the panel is above 6V. However, if sufficient panel current is not detected the LT8490 will temporarily stop charging. The charger will check for sufficient panel current at 30 second intervals (typical) or will check sooner if the LT8490 detects either a significant rise in panel voltage or a significant fall in battery voltage.
3. LOW INPUT VOLTAGE EFFECTS: Figure 5 shows the minimum input voltage, below which the maximum charging current can be reduced. This limit is a function of the input V_{MAX} as discussed previously in the Input Voltage and Modulation Network section. Maximum charging current can reduce as FBIN gets closer to its regulation voltage of 1.205V (typical). This is not normally a significant issue unless 1) the charger is powered by a low voltage DC power supply or 2) a low voltage panel is used with a charger that was configured for a much higher voltage panel. The farther that V_{IN} is below the Normal Configuration line in Figure 5 the more the current can reduce.

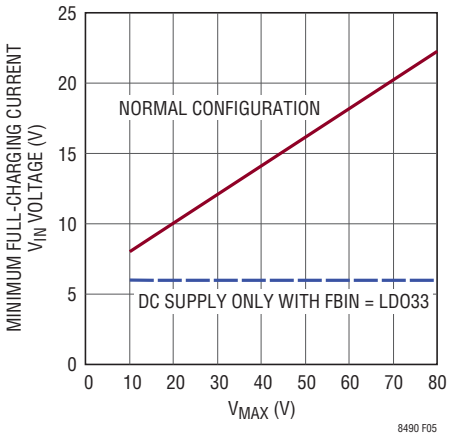


Figure 5. Minimum Full Charging Current V_{IN} Voltage

APPLICATIONS INFORMATION

When V_{IN} is powered by a DC voltage supply, maintain V_{IN} higher than the Normal Configuration line in Figure 5. Operating V_{IN} below this line can reduce the maximum charging current and the V_{S2} and V_{S3} charging voltages. If V_{IN} is never going to be supplied by a solar panel then FBIN can be disconnected from FBIR (see Figure 3) and reconnected to the LDO33 pin. This allows the charger to operate with V_{IN} as low as 6V with no charging current or voltage reduction.

When using a solar panel supply, choose a panel having a maximum open-circuit voltage (V_{OC}) close to V_{MAX} (discussed in the prior Input Voltage Sensing and Modulation Network section). The maximum power point voltage is typically well above the voltage limit in Figure 5 and current limiting is rarely an issue. Avoid using solar panels that operate dramatically below V_{MAX}, particularly if the maximum power point voltage is typically below the Normal Configuration line in Figure 5.

DC Supply Powered Charging

SELECTING POWER SUPPLY MODE: When powered by a DC voltage source, the VINR pin must be pulled below 174mV (typical) to activate power supply mode. This disables unnecessary solar panel functions and allows the LT8490 to operate properly from a DC voltage source. If the application is never powered by a solar panel, VINR can be grounded. If the application is only powered by a solar panel, then connect VINR as shown in Figure 4. Otherwise, see the Optional DC Supply Detection Circuit section for a method to pull down the VINR pin when a DC supply is detected.

MINIMUM INPUT VOLTAGE REQUIREMENT: When power supply mode is enabled, the LT8490 will operate from an input as low as 6V. However, charging current capability can become limited at low input voltages depending on the V_{MAX} voltage used to select the input voltage sensing network (see previous Input Voltage Sensing and Modulation Network section). Figure 5 shows the minimum input supply voltage required, below which charging current can become less than the maximum output current limit. If the LT8490 is powered by a DC supply only, the minimum input voltage shown in Figure 5 can be reduced to 6V by (1) disconnecting FBIN from FBIR and (2) connecting the FBIN pin directly to LDO33.

INPUT CURRENT LIMITING: Input current limiting should be considered when using DC power supplies. This is discussed later in the Input Current Limiting section.

In Situ Battery Charging

The LT8490 can be used to charge a battery while the battery is powering a load. The load should be directly connected to the battery terminals as shown in Figure 6. The variable nature of some loads can make charging times unpredictable. Due to this unpredictability it is recommended that charging time limits be disabled (see Charger Configuration – CHARGECFG2 Pin section for more information).

Because a load connected to the battery may draw more power than provided by the charger, the battery may discharge while the LT8490 is charging the battery. If this case occurs and the battery voltage falls below 31% (typical) of the Stage 2 voltage limit, the undervoltage fault will become active and the charger will halt until the battery voltage rises above 35% (typical) of the Stage 2 voltage limit. Consider automatically disabling the load if the battery depletes below an unacceptably low voltage.

The arrow in Figure 6 shows the proper disconnect point if removing the battery from the charger in an in situ battery charging application. This disconnect point is specified because the LT8490 is not designed to provide power directly to a load without the presence of a battery.

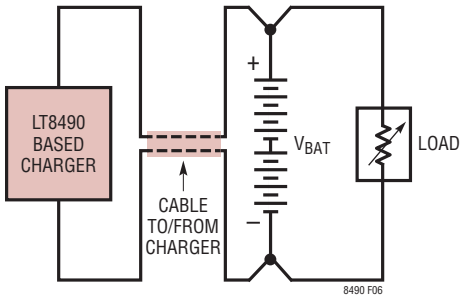


Figure 6. Load Connection to Battery in LT8490 Application

APPLICATIONS INFORMATION

Stage Voltage Limits

The Stage 2 voltage limit (V_{S2}) is the maximum battery charging voltage. The voltage limits for Stages 0, 1 and 3 are all related to the Stage 2 limit as shown in Table 3 and Figure 11. If temperature compensated charging is enabled, then V_{S2} will change with temperature as shown in Figure 13. As such, the limits for the other stages will also change with temperature since they are a constant proportion of V_{S2}.

Table 3. Typical Charging Stage Voltage Thresholds

STAGE TRANSITION	V_{BAT} RISING OR FALLING	TYPICAL V_{BAT}/V_{S2}	TYPICAL V_{BAT}/V_{S3}
V_{BAT} Undervoltage Fault → STAGE 0	Rising	35%	–
STAGE 0 → STAGE 1	Rising	70%	–
STAGE 1 → STAGE 2	Rising	98%	–
STAGE 3 → STAGE 0	Falling	–	96%
STAGE 2 → STAGE 1	Falling	95%	–
STAGE 1 → STAGE 0	Falling	66%	–
STAGE 0 → V_{BAT} Undervoltage Fault	Falling	31%	

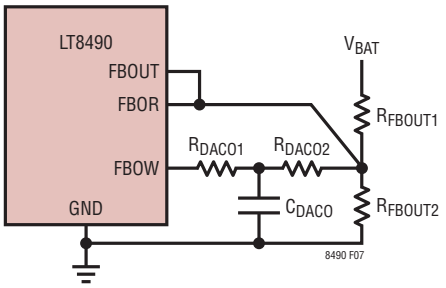


Figure 7. Output Feedback Resistor Network

SETTING THE STAGE 2 VOLTAGE LIMIT: The resistor network shown in Figure 7 is used to set the Stage 2 voltage limit. Battery manufacturers typically call for a higher Stage 2 voltage limit than the nominal battery voltage. For example, a 12V lead-acid battery used in automotive applications commonly has a Stage 2 charging voltage limit of 14.2V. If temperature compensated charging will be used (see Temperature Measurement, Compensation and Fault section) then use the 25°C value for V_{S2} in the equations below.

R_{FBOUT2} is often chosen between 4.99kΩ and 49.9kΩ. Choosing higher values for R_{FBOUT2} reduces the amount of current draw from the battery through the feedback network.

$$R_{FBOUT1} = R_{FBOUT2} \bullet \left[V_{S2} \bullet \left(\frac{1.241}{1.211} - 0.128 \right) - 1 \right] \Omega$$

$$R_{DACO2} = \frac{R_{FBOUT1} \bullet R_{FBOUT2} \bullet 0.833}{\left(R_{FBOUT2} \bullet V_{S2} \bullet \frac{1.241}{1.211} \right) - R_{FBOUT2} - R_{FBOUT1}} \Omega$$

$$R_{DACO1} = 0.2 \bullet R_{DACO2} \Omega$$

$$C_{DACO} = \frac{1}{500 \bullet R_{DACO1}} F$$

For greater charging voltage accuracy, it is recommended that 0.1% tolerance resistors be used for the output feedback resistor network.

Due to the granularity of standard resistor values, simply rounding the calculated results to their nearest standard values may result in unwanted errors. Consider using multiple resistors in series to match the calculated results. Otherwise, use standard resistor values and check the final results with the following equations.

$$V_{X3} = \left(\frac{R_{FBOUT1}}{R_{DACO1} + R_{DACO2}} \right) \bullet (X - 1.89)$$

where

$$X = 1.211 \bullet \left[1 + \left(\frac{R_{DACO1} + R_{DACO2}}{R_{FBOUT2}} \right) + \left(\frac{R_{DACO1} + R_{DACO2}}{R_{FBOUT1}} \right) \right]$$

V_{X3} indicates the actual 25°C V_{S2} voltage using the selected resistors.

$$N1 = \frac{X - 1.89}{X - 3.3}$$

N1 should be as close as possible to 1.22.

$$N2 = 1 - \frac{1.89}{X}$$

N2 should be as close as possible to 0.805. Iterations may be required to determine best standard resistor values.

APPLICATIONS INFORMATION

Table 4 shows good sets of standard value components for charging nominal battery voltages of 12V, 24V, 36V, 48V and 60V. Iterative calculations were required to select these values that achieve the best overall results.

Table 4. Standard Value Output Feedback Network vs Output Regulation Voltage

BATTERY VOLTAGE	TARGET V_{S2} (V)	R_{FBOUT1} (kΩ)	R_{FBOUT2} (kΩ)	R_{DACO1} (kΩ)	R_{DACO2} (kΩ)	C_{DACO} (nF)
12	14.2	274	23.2	26.1	124	82
24	28.4	487	20	28	107	68
36	42.6	787	21	22.6	121	100
48	56.8	1000	20	22.6	115	100
60	71.0	866	13.7	13.3	80.6	150

SETTING THE STAGE 3 VOLTAGE LIMIT: When enabled, Stage 3 charging maintains the battery voltage at 85% to 99% of V_{S2}. This proportion is adjustable and is discussed in the Charger Configuration – CHARGECFG1 Pin section.

BATTERY UNDERVOLTAGE LIMIT: Upon start-up, the LT8490 checks for battery voltage above 35% (typical) of the Stage 2 voltage limit. If the battery voltage is less than this, charging will not start and a battery undervoltage fault will be indicated on the FAULT pin. Charging will begin after the battery voltage rises above 35% (typical) of the Stage 2 voltage limit. If the battery voltage subsequently falls below 31% (typical), charging will again stop and the fault will be indicated on the FAULT and STATUS pins.

Charge Current Limiting

The maximum charging current is configured with the output current limiting circuit. The output current is sensed through R_{SENSE2} and converted to a proportional current flowing out of the IMON_OUT pin (see Figure 8).

IMON_OUT voltages above 1.208V (typical) cause V_C to reduce due to EA1, and thus limit the output current. IOW is either driven to ground or floated depending on charging conditions. This allows the current limit for Stage 0 ($I_{OUT(MAXS0)}$) to be set independently of the remaining Stages ($I_{OUT(MAX)}$) with proper selection of R_{IOW} and R_{IMON_OUT}. Use the following equations to configure the charging current limits:

$$R_{SENSE2} = \frac{0.0497}{I_{OUT(MAX)}}\Omega$$

$$R_{IMON\_OUT} = \frac{1208}{I_{OUT(MAXS0)} \bullet R_{SENSE2}}\Omega$$

$$R_{IOW} = \frac{24.3k \bullet R_{IMON\_OUT}}{R_{IMON\_OUT} - 24.3k}\Omega$$

$$R_{IOR} = 3.01k\Omega$$

$$C_{IMON\_OUT} = \text{read below}$$

where $I_{OUT(MAX)}$ is the maximum charging current in Amps, $I_{OUT(MAXS0)}$ is the maximum trickle charging current in Stage 0 and $I_{OUT(MAXS0)}$ is no greater than $I_{OUT(MAX)}$. For cases where $I_{OUT(MAX)} = I_{OUT(MAXS0)}$, it is OK to exclude R_{IOW} and float the I_{OW} pin. $I_{OUT(MAXS0)}$ must be at least 20% of $I_{OUT(MAX)}$.

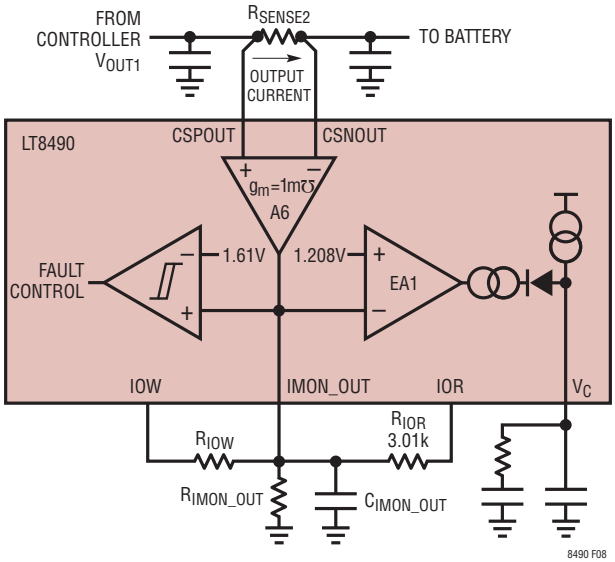


Figure 8. Output Current Regulation Loop

APPLICATIONS INFORMATION

C_{IMON_OUT} reduces IMON_OUT ripple and stabilizes the constant charging current control loop. Reducing C_{IMON_OUT} improves stability and minimizes inductor current overshoot that can occur if a discharged battery is quickly disconnected then reconnected to the charger. However, this is at the expense of increased IMON_OUT ripple that can introduce more noise into the ADC measurements. The higher frequency pole created at IMON_OUT must be adequately separated from the lower frequency pole at the V_C pin for proper stability. A C_{IMON_OUT} capacitor in the range of 4.7nF to 22nF is adequate for most applications.

Input Current Limiting

SOLAR PANEL SUPPLY: Solar panels are inherently current limited and may not be able to provide maximum charging power at the lowest input voltages. The LT8490 uses its MPPT algorithm to sweep the panel voltage as low as 6V to find the maximum power point. Make sure that the input current limit is set higher than the maximum panel current capability, plus at least 20% to 30% margin, in order to achieve the maximum charging capability of the system.

In addition, note that the LT8490 uses the same circuit (shown in Figure 9) to measure the input current as to limit it. The input current is measured by an A/D conversion of the IIR pin voltage which is connected to IMON_IN and is proportional to input current. The digitized input current is used to locate the maximum power point of the solar panel. Setting a higher input current limit reduces the resolution of the digitized reading of the input current. Avoid setting the input current limit dramatically higher than necessary, as this may affect the accuracy of the maximum power point calculations.

DC POWER SUPPLY: When charging a battery at maximum current, and thus power, a low voltage supply must provide more current than a high voltage supply. This can be seen by equating output power to input power, less some efficiency loss.

$$V_{IN} \bullet I_{IN} \bullet \eta = V_{BAT} \bullet I_{BAT}$$

or

$$I_{IN(MAX)} = \frac{V_{BAT} \bullet I_{BAT(MAX)}}{V_{IN(MIN)} \bullet \eta}$$

where the efficiency factor η is typically between 0.95 and 0.99.

When powered by a DC supply, appropriate input current limiting is recommended for supplies that might (1) become overloaded as the supply ramps up or down through 6V or (2) provide more input current than the charger components can tolerate.

SETTING THE INPUT CURRENT LIMIT: The input current is sensed through R_{SENSE1} as shown in Figure 9. The current through R_{SENSE1} is converted to a voltage on the IMON_IN pin according to the following equation:

$$V_{IMON\_IN} = \left[\left(\frac{I_{IN} \bullet R_{SENSE1}}{1000} + 7\mu A\right) \bullet R_{IMON\_IN}\right] V$$

IMON_IN voltages exceeding 1.208V (typical) cause the V_C voltage to reduce, thus limiting the input current. R_{IMON_IN} should be 21kΩ ± 1% or better. Using this information, the appropriate value for R_{SENSE1} can be calculated using the following equation:

$$R_{SENSE1} = \frac{1000 \bullet \left(\frac{1.208V}{21k\Omega} - 7\mu A\right)}{I_{IN(MAX)}} = \frac{0.0505}{I_{IN(MAX)}} \Omega$$

where $I_{IN(MAX)}$ is the maximum input current limit in Amps. R_{SENSE1} values greater than 25mΩ are not recommended.

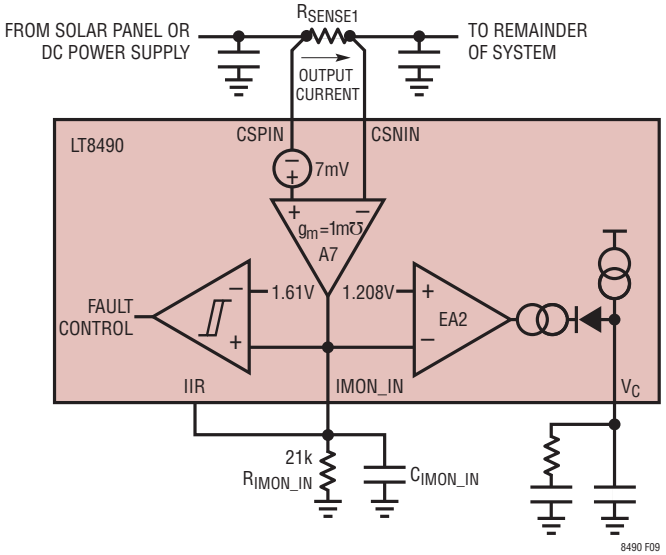


Figure 9. Input Current Regulation Loop

APPLICATIONS INFORMATION

C_{IMON_IN} reduces IMON_IN ripple and stabilizes the input current limit control loop. Reducing C_{IMON_IN} improves stability and minimizes possible inductor current overshoot. However, this is at the expense of increased IMON_IN ripple that can introduce more noise into the ADC measurements. The higher frequency pole created at IMON_IN must be adequately separated from the lower frequency pole at the V_C pin for proper stability. A C_{IMON_IN} capacitor of 4.7nF to 22nF is adequate for most applications.

Input and Output Current Sense Filtering

The C_{SX} and R_{SX} current sense filtering shown in Figure 10 can improve the accuracy of the input and output current measurements at low average current levels. Amplifiers A7 and A8 (Figures 8 and 9) can only amplify positive R_{SENSE} voltages. Although the average R_{SENSE} voltage is always positive, the voltage ripple at low average current levels may contain negative components that are averaged out by the filter. Recommended values for R_{S1}, R_{S2} and C_{S1}, C_{S2} are 10Ω and 470nF.

C_{C1} and C_{C2} may be required, depending on board layout, to reduce common mode noise that may reach the LT8490 pins. 100nF ceramic capacitors, with the appropriate voltage ratings, work well in most cases. Be sure to place all of the filter components (C_{SX}, R_{SX}, C_{CX}) close to the LT8490 for best performance.

Finally, note that a small voltage drop (typically ~0.25mV per 10Ω) will occur across R_{S1} and R_{S2} due to the input bias currents of CSNOUT and CSNIN. This represents a ~0.5% reduction in the maximum current limit which typically occurs with ~50mV across R_{SENSE}. The C/10 threshold (typically when 5mV is measured across CSPOUT and CSNOUT) will also reduce to C/10.5 due to the 0.25mV drop across R_{S2}.

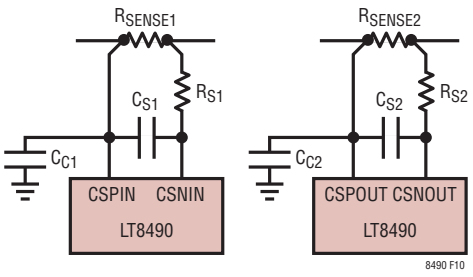


Figure 10. Recommended Current Sense Filter

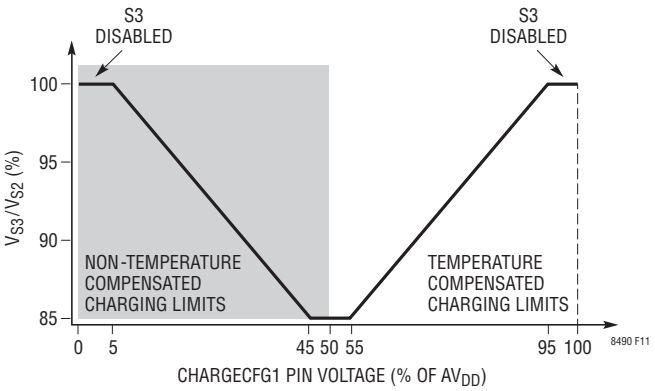


Figure 11. CHARGECFG1 Pin Configuration

Charger Configuration – CHARGECFG1 Pin

The CHARGECFG1 pin is a multifunctional pin as shown in Figure 11. Set this pin using a resistor divider totaling no less than 100kΩ to the AV_{DD} pin (see the Typical Applications section for examples). The voltage on CHARGECFG1, as a percentage of AV_{DD}, makes the selections discussed below. Avoid setting the divider ratio directly at any of the inflection points on Figure 11 (e.g. 5%, 45%, 50%, 55% or 95%)

ENABLE/DISABLE TEMPERATURE COMPENSATED VOLTAGE LIMITS: Setting the CHARGECFG1 pin in the upper half of the voltage range (> 50%) enables battery voltage temperature compensation, while using the bottom half (< 50%) disables the temperature compensation, even if a thermistor is coupled to the battery pack. The next section provides more detailed information.

DISABLE STAGE 3: Setting the CHARGECFG1 pin to AV_{DD} or 0V disables Stage 3. When the CHARGECFG1 pin is set in this manner, the charging algorithm will never proceed to Stage 3. Stage 3 is commonly used for lead-acid battery charging but is not typically used for lithium-ion battery charging.

ENABLE STAGE 3: Setting the CHARGECFG1 pin between 5% to 95% of AV_{DD} enables Stage 3 charging and sets the Stage 3 voltage limit (V_{S3}) as a percentage of the Stage 2 voltage limit (V_{S2}) according to the following formulas.

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When temperature compensated charging and Stage 3 are enabled, use:

$$CHARGECFG1\% = \left[\left(2.67 \bullet \left(\frac{V_{S3}}{V_{S2}} - 0.85\right)\right) + 0.55\right] \bullet 100\%$$

When temperature compensated charging is disabled and Stage 3 is enabled, use:

$$CHARGECFG1\% = \left[2.72 - \left(2.67 \bullet \left(\frac{V_{S3}}{V_{S2}}\right)\right)\right] \bullet 100\%$$

where V_{S3}/V_{S2} should be between 0.86 to 0.99.

For example, to enable temperature compensated charging with V_{S3} set to 93% of V_{S2}, choose a divider that puts CHARGECFG1 at 76% of AV_{DD}. For best accuracy use resistors that have a 1% tolerance or better.

Temperature Measurement, Compensation and Fault

The LT8490 can measure the battery temperature using an NTC (negative temperature coefficient) thermistor thermally coupled to the battery pack. The temperature monitoring function is enabled by connecting a 10kΩ, ß = 3380 NTC thermistor from the TEMPSENSE pin to ground and an 11.5kΩ (1% tolerance or better) resistor from AV_{DD} to TEMPSENSE (as shown in Figure 12). If battery temperature monitoring is not required, then use a 10kΩ resistor in place of the thermistor. This will indicate to the LT8490 that the battery is always at 25°C.

The LT8490 monitors the voltage on the TEMPSENSE pin to determine the battery temperature and also to detect if the thermistor is connected or not. A TEMPSENSE voltage greater than 96% of AV_{DD} (typical) indicates that the thermistor has been disconnected. Three charger functions rely on the TEMPSENSE information.

1. INVALID BATTERY TEMPERATURE FAULT: A temperature fault occurs when the battery temperature is outside of the valid range as configured on the CHARGECFG2 pin (–20°C to 50°C or 0°C to 50°C). The temperature fault condition remains until the temperature returns within –15°C to 45°C or 5°C to 45°C (5°C of hysteresis). During a temperature fault, charging is halted and the STATUS and FAULT pins follow the pattern described in Table 6. If timer termination is enabled with the CHARGECFG2 pin, the timer count is paused during the temperature fault and resumes when the fault state is exited.
2. BATTERY VOLTAGE TEMPERATURE COMPENSATION: Some battery chemistries charge best when the voltage limit is adjusted with battery temperature. Lead-acid batteries, in particular, experience a significant change in the ideal charging voltage as temperature changes. If enabled with the CHARGECFG1 pin, the battery charging voltage and all related voltage thresholds are automatically adjusted with battery temperature. As the voltage on the TEMPSENSE pin changes, the PWM duty cycle from the FBOW pin changes such that the voltage limits of the LT8490 follow the curve shown in Figure 13.

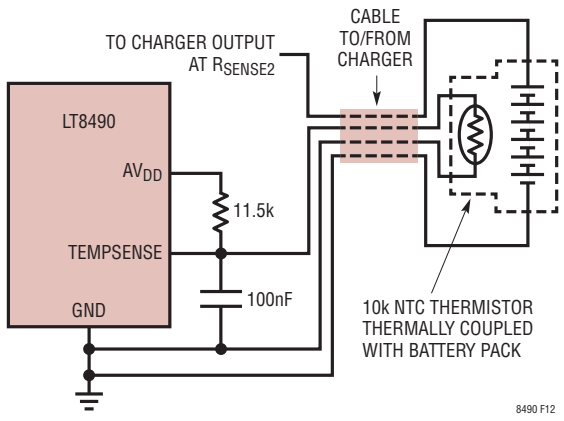

Figure 12. Battery Temperature Sensing Circuit

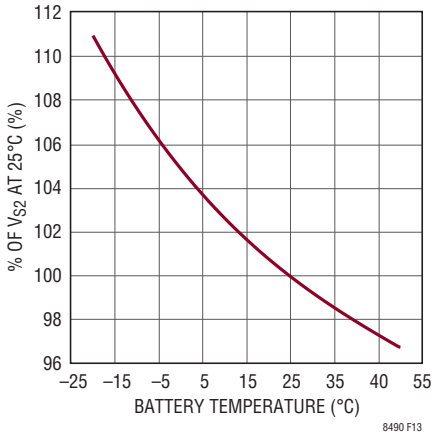

Figure 13. Stage 2 Voltage Limit vs Temperature When Temperature Compensation Is Enabled

APPLICATIONS INFORMATION

3. BATTERY DISCONNECT SENSING: The LT8490 detects if the battery and thermistor have been disconnected from the charger by monitoring the TEMPSENSE pin voltage. When the connection to the battery is severed, as shown by the arrow in Figure 12, the connection to the thermistor is also severed and the TEMPSENSE voltage rises up to AV_{DD} through the 11.5kΩ resistor. During the time when the battery is not present, the LT8490 halts charging. The charger automatically restarts the charging at Stage 0 when a battery (along with integrated thermistor or resistor) is sensed through the TEMPSENSE pin.

Charger Configuration – CHARGECFG2 Pin

The CHARGECFG2 pin is a multifunctional pin as shown in Figure 14. Set this pin using a resistor divider totaling no less than 100kΩ to the AV_{DD} pin (see the Typical Applications section for examples). The voltage on CHARGECFG2, as a percentage of AV_{DD}, makes the selections discussed below. Avoid setting the divider ratio directly at any of the inflection points on Figure 14 (e.g. 5%, 10%, 45%, 50%, 55%, 90% or 95%)

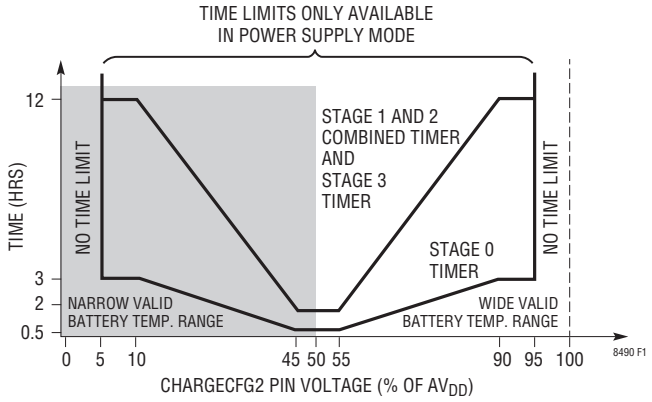

Figure 14. CHARGECFG2 Pin Voltage Settings

ENABLE/DISABLE CHARGING TIME LIMITS: The LT8490 supports charging time limits only when power supply mode is enabled (see the DC Supply Powered Charging section). When power supply mode is disabled, any finite time limit setting on CHARGECFG2 is interpreted as no time limit. This section discusses how to configure the time limits using the CHARGECFG2 pin. For more information about the operation of the time limits see the Charging Time Limits section.

Setting the CHARGECFG2 pin between 5% to 95% of AV_{DD} allows for time limit settings between 0.5 hours to 3 hours for Stage 0, 2 hours to 12 hours for Stage 1 and 2 combined and 2 hours to 12 hours for Stage 3. The Stage 0 time limit is always 1/4th of the Stage 1 + Stage 2 time limit and the Stage 3 time limit is always the same length as the Stage 1 + Stage 2 limit. When choosing a Stage 1 + Stage 2 time limit of 12 hours, choose a divider ratio very close to 7.5% or 92.5%. When choosing a Stage 1 + Stage 2 time limit of 2 hours, choose a divider ratio very close to 47.5% or 52.5%. For time limits in between, use one of the following formulas.

When the wide valid battery temperature range (–20°C to 50°C) is desired use:

$$CHARGECFG2\% = 3.5\% \bullet (T_{S1S2} - 2) + 55\%$$

where T_{S1S2} is the desired Stage 1 + Stage 2 time limit in hours between 2.1 and 11.9.

When the narrow valid battery temperature range (0°C to 50°C) is desired use:

$$CHARGECFG2\% = 45\% - 3.5\% \bullet (T_{S1S2} - 2)$$

where T_{S1S2} is the desired Stage 1 + Stage 2 time limit in hours between 2.1 and 11.9.

Setting CHARGECFG2 below 4% (i.e., ground) or above 96% of AV_{DD} (i.e., tie to AV_{DD}) disables the time limits, allowing the charging to run indefinitely in lieu of any fault conditions.

SELECT THE VALID BATTERY TEMPERATURE RANGE: Setting the CHARGECFG2 pin in the top half of the voltage range (> 50%) selects a wider valid battery temperature range (–20°C to 50°C), while using the bottom half of the voltage range (< 50%) selects a narrower valid battery temperature range (0°C to 50°C). Generally, lead-acid batteries would use the wide range, while lithium-ion batteries would use the narrow range. See the Temperature Measurement, Compensation and Fault section for more information about the invalid battery temperature fault.

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Charging Time Limits

Charging time limits can be enabled only in power supply mode by properly configuring the CHARGECFG2 pin (see the Charger Configuration – CHARGECFG2 Pin section). Charging time limits are not recommended for use when a load is present on the battery due to the unpredictable amount of time that may be required to achieve full charge.

When enabled, the appropriate timers start at the beginning of Stages 0, 1 and 3. If the timer expires while operating in its respective stage or the LT8490 returns to a charging stage after its respective timer has expired, charging stops immediately. As shown in Table 5, expiration of a timer is treated as either a fault or as done charging depending on the timer that expired and the configuration of the charger. In any case, when charging stops, the fault or done charging status is indicated on the STATUS and FAULT pins as described in the STATUS and FAULT Indicators section.

Table 5. Charger Conditions and Timer Expiration Results

CHARGING STAGE WHEN TIMER EXPIRES	STAGE 3 ENABLED?	TIMER USED	RESULT OF TIMER EXPIRATION
0	–	Stage 0	Fault
1	–	Stage 1 + Stage 2	Fault
2	–	Stage 1 + Stage 2	Fault
3	Yes	Stage 3	Done Charging

STAGE 2 TERMINATION (TIME LIMITS ENABLED): Timer expiration in Stage 2 causes a fault and charging stops immediately with a fault indication on the STATUS and FAULT pins. If the Stage 2 output current drops below C/10 before the timer expires and Stage 3 is disabled then charging stops and done charging is indicated on the STATUS pin.

STAGE 2 TERMINATION (TIME LIMITS DISABLED): If time limits are disabled, Stage 2 can only terminate if Stage 3 is also enabled. After charging current falls below C/10, charging will proceed to Stage 3. If Stage 3 is also disabled then the charger will operate in Stage 2 indefinitely unless the battery voltage falls enough for charging to revert back to Stage 1. During the indefinite Stage 2 charging, the STATUS pin will indicate if Stage 2 current is below C/10 or above C/5 (as shown in Tables 6 and 7).

STAGE 3 TERMINATION CONDITIONS: If Stage 3 is enabled and time limits are disabled, the LT8490 will remain in Stage 3 forcing reduced constant-voltage indefinitely unless the battery voltage falls below 96% of V_{S3} or charging current rises above C/5 causing the charger to revert back to Stage 0. If Stage 3 is enabled and time limits are enabled, timer expiration in Stage 3 will stop charging and communicate the done charging state through the STATUS pin (as shown in Tables 6 and 7).

Lithium-Ion Battery Charging

The LT8490 is well suited to charge lithium-ion batteries. Connecting the CHARGECFG1 and CHARGECFG2 pins to ground puts the LT8490 into a typical configuration for lithium-ion battery charging (0°C to 50°C valid battery temperature, Stage 3 disabled, no temperature compensation, no time limits). Figure 15 shows a typical lithium-ion charging cycle in this configuration.

If no timer termination has been selected, the LT8490 will charge the lithium-ion battery stack to the desired Stage 2 voltage limit, maintaining that limit indefinitely. When the charging current is < C/10, the STATUS pin will go high as described in Table 6.

NOTE: When solar charging a Li-Ion battery without time limits it is recommended that the Stage 2 voltage limit not exceed 95% of the lithium-ion maximum cell voltage. Since this configuration can charge indefinitely, following this guideline keeps the lifetime of the batteries from degrading quickly.

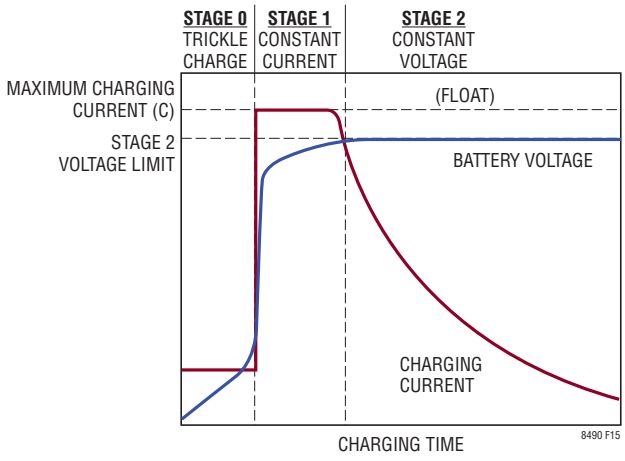

Figure 15. Lithium-Ion Battery Charging Cycle

APPLICATIONS INFORMATION

Lead-Acid Battery Charging

The LT8490 can be used to charge lead-acid batteries. Setting the CHARGECFG1 pin to 87.6% of AV_{DD} and CHARGECFG2 pin equal to AV_{DD} configures the LT8490 for typical lead-acid battery charging (–20°C to 50°C valid battery temperature, Stage 3 enabled with V_{S3}/V_{S2} = 97.2%, temperature compensated voltage limits, no time limits). Figure 16 shows a typical lead-acid charging cycle.

If time limits have been disabled, the LT8490 will charge the lead-acid battery stack to the desired Stage 3 voltage limit and restart the charging cycle if 1) the battery voltage falls below 96% of the Stage 3 voltage limit (V_{S3}) or 2) the charging current rises above C/5.

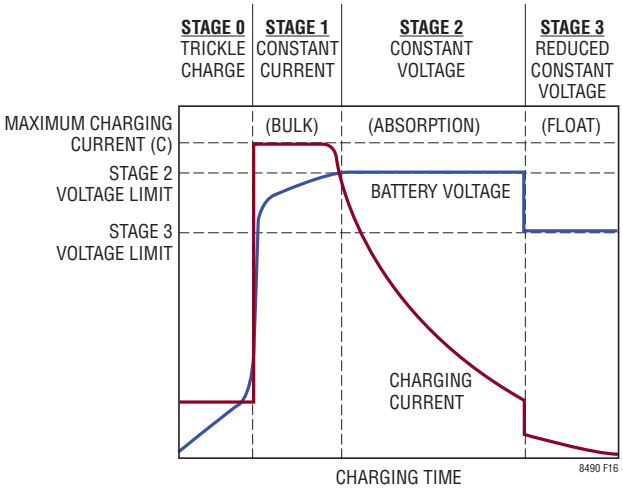

Figure 16. Lead-Acid Battery Charging Cycle

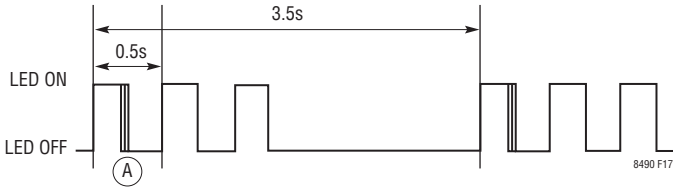

Figure 17. Example Waveform for STATUS Pin in STAGE 3

STATUS and FAULT Indicators

The LT8490 reports charger status through two outputs, the STATUS and FAULT pins. These pins can be used to drive LEDs for user feedback. In addition, the STATUS pin doubles as a UART output to send status information to a peripheral device. Table 6 describes the LED behavior of these pins in relationship to the charger status.

While the LT8490 is operating, the STATUS pin toggles on a 3.5 sec (typical) interval as shown in Figure 17. The three pulses shown in Figure 17 represent the charger operating in Stage 3. The STATUS and FAULT pins pull up to turn the LEDs on and drive to ground to turn the LEDs off.

Table 6. STATUS and FAULT LED INDICATORS

CHARGER STATUS	LED PULSES/3.5s, APPROXIMATE ON-TIME PER PULSE		FOR MORE INFORMATION SEE SECTION
	STATUS	FAULT	
Stage 0	1, 10ms	OFF	Battery Charging Algorithm
Stage 1	1, 250ms	OFF	Battery Charging Algorithm
Stage 2 and (Stage 3 Enabled or Time Limits Enabled or I_{OUT} Rising Above C/5)	2, 250ms	OFF	Battery Charging Algorithm and Charger Configuration Sections
Stage 2 and Stage 3 Disabled and Time Limits Disabled and I_{OUT} Falling Below C/10	ON	OFF	Battery Charging Algorithm and Charger Configuration Sections
Stage 3	3, 250ms	OFF	Battery Charging Algorithm
Done Charging	ON	OFF	Charging Time Limits
Battery Present Detection Fault	1, 10ms	1, 250ms	Temperature Measurement, Compensation and Fault
Invalid Battery Temperature Fault	1, 10ms	2, 250ms	Temperature Measurement, Compensation and Fault
Timer Expiration Fault	1, 10ms	3, 250ms	Charging Time Limits
Battery Undervoltage Fault	1, 10ms	4, 250ms	Stage Voltage Limits

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Driving LEDs with the STATUS and FAULT Pins

The STATUS and FAULT pins on the LT8490 can be used to drive LED indicators. Figure 18 shows the simplest configuration for driving LEDs from these two pins.

The STATUS pin can drive up to 2.5mA into an LED. Choose R_{DSA} to limit the LED current to 2.5mA or less when STATUS is driven close to 3.3V. Choose R_{DSB} to conduct a current equivalent to the LED current when STATUS is driven close to ground and R_{DSB} has ~3.3V across the terminals. D_S, in Figure 18, conducts ~2.5mA when STATUS is driven high. R_{DSB} conducts ~2.5mA when the STATUS is driven low.

The FAULT pin has a weak pull up in comparison to the STATUS pin (see the Typical Performance Characteristics section). The LED current is typically self-limited to less than 1mA by the FAULT pin driver. R_{DFB} in Figure 18 is typically 3.32kΩ and increases the FAULT LED current. When configured as shown in Figure 18, the D_F LED current should be limited to less than 1.5mA.

For driving higher current LEDs, the circuit in Figure 19 can be used. Note that the LED current for D_F is provided by the $INTV_{CC}$ regulator in this case. Excessive LED current can overload the $INTV_{CC}$ regulator and/or cause excessive heating in the LT8490. 7.5mA is a good starting point when using this circuit. Higher currents can be possible with careful board evaluation. Transistor Q2 must have a collector-emitter breakdown voltage greater than $INTV_{CC}$. The MMBT3646 has a breakdown voltage of 15V and is well suited for this application.

The LED current for D_S is provided by V_{IN} in this case. Do not draw current for D_S from $INTV_{CC}$ since this increases power dissipation in the LT8490. Transistor Q1 must have a collector-emitter breakdown greater than V_{IN}. The MMBT5550L has a breakdown voltage of 140V and is suitable for most applications.

To properly set the resistors shown in Figure 19, use the following equations:

$$R_{E1} \cong \frac{2.6}{I_D}\Omega$$

$$R_{C1} \cong \left(\frac{I_{NTVCC} - V_F}{I_D}\right)\Omega$$

$$R_{B1} = \frac{50}{I_D}\Omega$$

where $INTV_{CC}$ is typically 6.35V, V_F is the forward voltage of the LED (often about 1.7V) and I_D is the desired bias current through the LED.

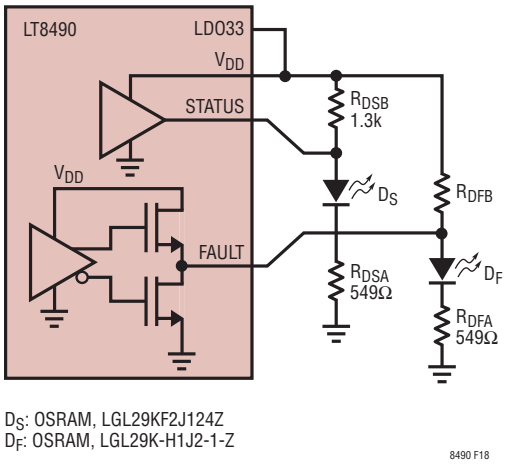

Figure 18. Default STATUS/FAULT LED Indicators

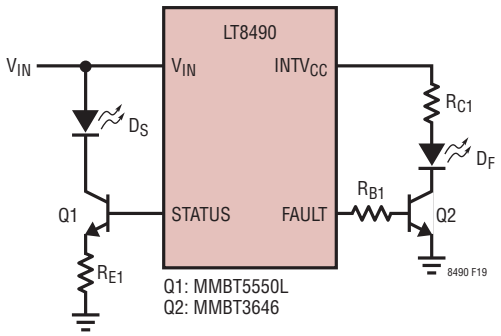

Figure 19. Higher Current Drive for STATUS/FAULT LEDs

APPLICATIONS INFORMATION

STATUS Pin UART

The STATUS pin also provides a UART (transmit only) communication function. This feature allows for remote monitoring of the LT8490. Immediately after each initial pulse described in Table 6 the STATUS pin sends out a synchronizing byte (0x55) followed by a status byte. UART data is transmitted with the LSB first. Figure 20 shows the zoomed in region labeled (A) from Figure 17.

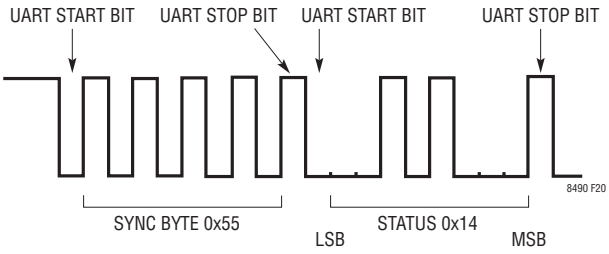

Figure 20. UART Transmission Waveform from Figure 17 Label (A)

The status byte shown in Figure 20 has information regarding the present charging stage as well as fault information. The data format for each UART byte is 8 data bits, no parity, with one stop bit. The baud rate is 2400 baud ±10% which may require auto baud rate detection, using the sync byte, for proper data reception. Figure 21 defines each bit present in the status byte. The status byte always contains an MSB of 0. Status bytes containing an MSB of 1 should be disregarded.

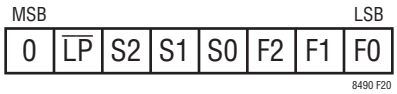

Figure 21. Status Byte Decode

$\overline{LP}$: "0" if in low power mode (see the Low Power Mode section)

S2/S1/S0: Stage description (see Table 7)

F2/F1/F0: Fault description (see Table 8)

Table 7. Stage Description

STAGE	CONDITIONS	S2	S1	S0
Stage 0	–	0	0	0
Stage 1	–	0	0	1
Stage 2	Stage 3 Enabled	0	1	0
	Timers and Stage 3 Disabled, Charging Current Has Risen Above C/5			
	Timers and Stage 3 Disabled, Charging Current Falls Below C/10	1	0	0
Stage 3	–	0	1	1
Done Charging	–	1	0	1

Table 8. Fault Description

FAULT INFORMATION	F2	F1	F0
No Faults Present	0	0	0
Battery Disconnected (Thermistor Disconnected)	0	0	1
Invalid Battery Temperature	0	1	0
Timer Fault	0	1	1
Battery Undervoltage	1	0	0

If multiple faults are present, the fault listed highest in Table 8 is reported through the STATUS and FAULT pins.

APPLICATIONS INFORMATION

Automatic Charger Restart and Fault Recovery

The LT8490 employs many features and checks that may cause the charger to stop until favorable operating conditions return. Table 9 summarizes the typical cause for the LT8490 to stop charging along with the conditions under which it will automatically restart charging. Upon automatic restart all timers are reset except when resuming from an invalid battery temperature fault.

Table 9. Automatic Restart Conditions

CAUSE FOR CHARGING TO STOP	REQUIREMENT FOR RESTART	RESTART OR RESUME CHARGING
Done Charging	Stage 3 disabled and V_{BAT} drops below 95% of V_{S2}	Restart
	Stage 3 enabled and V_{BAT} drops below 96% of V_{S3}	Restart
Battery Undervoltage Fault	V_{BAT} rises to 35% of V_{S2}	Restart
Stage 0 Timeout	V_{BAT} rises to 70% of V_{S2} or every hour after stopping (read below)	Restart
Stage 1 Timeout	V_{BAT} rises 5% or V_{BAT} rises to 98% of V_{S2} or every hour after stopping (read below)	Restart
Stage 2 Timeout	V_{BAT} falls below 66% of V_{S2} or every hour after stopping (read below)	Restart
Invalid Battery Temperature	Battery temperature returns within the valid temperature range with 5°C hysteresis	Resume
Battery Disconnected Fault	Re-Connect Thermistor	Restart

The charger will attempt to restart every hour (typically) after having stopped due to a timeout fault in Stage 0, Stage 1 or Stage 2. Configuring the charger in any of the following ways prevents the charger from automatically restarting every hour:

1. Stage 3 disabled and narrow battery temperature range selected and temperature compensated battery voltage not selected.
2. Not operating in power supply mode.
3. Timer limits disabled.

$\overline{SHDN}$ Pin Connection

The LT8490 requires 1.234V (typical) on the $\overline{SHDN}$ pin to start-up. A minimum of 5V on V_{IN} is also required for proper start-up operation; therefore, a resistor divider from V_{IN} to the $\overline{SHDN}$ pin is used to set this threshold. Connect the $\overline{SHDN}$ pin as shown in Figure 22 (1% resistor tolerance or better required).

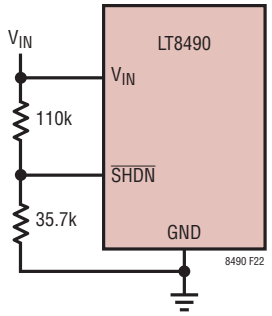

Figure 22. $\overline{SHDN}$ Pin Resistor Divider

APPLICATIONS INFORMATION

Switching Configuration – MODE Pin

The LT8490 has two modes of switching behavior controlled by the state of the MODE pin. Tying MODE to a voltage above 2.3V (i.e., V_{DD} or $INTV_{CC}$) configures the part for discontinuous conduction mode (DCM) which allows only positive current flow to the battery. More information about this mode of operation can be found in the LT8705 data sheet.

Tying the MODE pin below 0.4V (i.e. ground) changes the configuration as follows:

1. AUTOMATIC CCM/DCM MODE SWITCHING: Very large inductor current ripple can lead the LT8490 to operate at high currents while still in DCM. In this case, the M4 switch (highlighted in Figure 23) can become hot due to the battery charging current flowing through the body diode of this device.

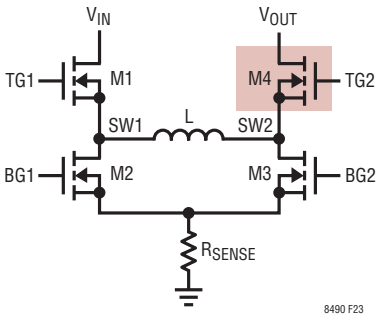

Figure 23. Simplified Diagram of Switches

Connecting the MODE pin low can reduce the M4 heating by activating the continuous conduction threshold mode (CCTM). In this mode the average charging current is monitored by the IMON_OUT pin. The LT8490 will operate in conventional DCM while the battery charging current, and thus IMON_OUT, is low (below 122mV typically). As the charging current increases, IMON_OUT will eventually rise above ~195mV signaling the LT8490 to enter CCM operation that will turn on M4 and reduce heating. While the average charging current will be positive, this mode does allow some negative current flow within each switching cycle. Use DCM operation if this behavior is not desired.

2. AUTOMATIC $EXTV_{CC}$ REGULATOR DISCONNECT: As discussed in more detail in the LT8705 data sheet, the $INTV_{CC}$ pin is regulated to 6.35V from one of two possible input pins, V_{IN} or $EXTV_{CC}$. The $EXTV_{CC}$ pin is often connected to the battery allowing $INTV_{CC}$ to be regulated from a low voltage supply which minimizes power loss and heating in the LT8490. However, $EXTV_{CC}$ should be disconnected from the battery when charging current is low to avoid discharging the battery.

   When MODE is low, the LT8490 automatically forces the $INTV_{CC}$ regulator to use V_{IN} instead of $EXTV_{CC}$ for the input supply when charging current becomes low. Charging current is monitored on the IMON_OUT pin. When IMON_OUT falls below 122mV (typical) the $INTV_{CC}$ regulator uses V_{IN} as the input supply. When IMON_OUT rises above ~195mV $INTV_{CC}$ will regulate from $EXTV_{CC}$ if $EXTV_{CC}$ is also above 6.4V (typical). This same functionality can be achieved when MODE is tied high by using the external circuit discussed in the Optional $EXTV_{CC}$ Disconnect section.

   Finally, a 305kΩ (typical) resistor is connected from $EXTV_{CC}$ to ground inside the LT8490. This resistor can draw current from the battery unless $EXTV_{CC}$ is disconnected. See the Optional $EXTV_{CC}$ Disconnect section for a way to automatically disconnect $EXTV_{CC}$ when charging current becomes low or charging stops.

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Optional Low Power Mode

When current from the solar panel is not high enough to reliably measure the maximum power point, the LT8490 may automatically begin operating in low power mode. Low power mode is automatically disabled when operating from a DC supply in power supply mode. Otherwise, the low power mode feature is enabled by default and allows the LT8490 to charge a battery under very low light conditions that would otherwise cause the LT8490 to stop charging. Low power mode can also be disabled with a method discussed later in this section.

In low power mode, the LT8490 momentarily stops charging, allowing the panel voltage to rise. When the panel has sufficiently charged the input capacitor, the LT8490 transfers energy from the input capacitor to the battery while drawing down the panel voltage. This behavior repeats rapidly, delivering charge to the battery as shown in the Panel Voltage in Low Power Mode plots in the Typical Performance Characteristics section.

MINIMUM INPUT CAPACITANCE FOR LOW POWER MODE: A minimum amount of energy must be transferred from the input capacitor to the battery during each charge transfer cycle. Otherwise the battery may be drained instead of being charged. Figure 24 shows the minimum input capacitance required when the charger is operating near the 10V minimum input voltage. As the panel voltage rises, due to increased illumination, more energy is stored in the input capacitor and a corresponding increase of energy is delivered to the battery. Carefully check the solar panel voltage for good stability and minimal ripple when operating with low input capacitance.

MINIMUM INPUT VOLTAGE: With low power mode enabled, the panel voltage must initially exceed 10V (typical – as measured through the VINR pin) before the charger will attempt to charge the battery. If adequate charge is not being delivered to the battery, the charger may temporarily wait for even more input voltage before transferring the input charge to the battery.

EXITING LOW POWER MODE: The charger will automatically exit low power mode and resume normal charging after adequate input current is detected. The charger typically requires the input current to exceed 2.5% to

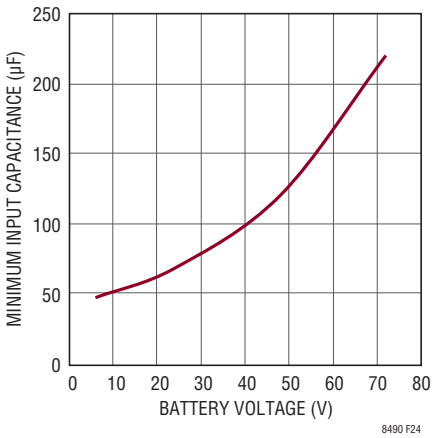

Figure 24. Minimum Input Capacitor Required for Low Power Mode

3% of the maximum input current limit to make a valid power point reading and exit low power mode. The panel voltage may be adjusted as low as 6V when searching for the maximum power point.

DISABLING LOW POWER MODE: If the minimum input capacitance, or 10V minimum start-up voltage are not suitable for the application, low power mode can be disabled by including the resistor R_{NLP} = 3.01kΩ as shown in Figure 25. When low power mode is disabled, the LT8490 will attempt to charge the battery after 6V or more is detected on the panel. If the input current is too low (typically less than 1.5% of the maximum input current limit) charging is temporarily halted. The LT8490 will attempt to charge the battery on 30 second intervals or when the LT8490 measures a significant rise in the panel voltage. When the LT8490 determines that there is sufficient panel current, normal charging operation will automatically resume.

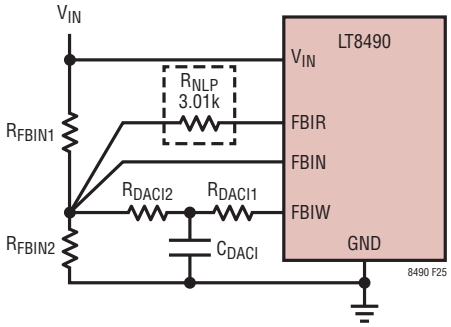

Figure 25. Disabling Low Power Mode with Resistor R_{NLP}

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Optional Output Feedback Resistor Disconnect

To measure and regulate the battery voltage, the LT8490 uses a resistor feedback network connected to the battery. Unless these resistors are disconnected from the battery, they will draw current from the battery even when it is not being charged as seen in Figure 26. This may be undesirable when using small capacity batteries.

If desired, the resistors can be automatically disconnected from the battery when charging stops by using the circuit shown in Figure 27. This circuit is controlled by the SWENO signal from the LT8490 and connects the resistor feedback network when charging is taking place. When charging stops, the network is disconnected and current draw from the battery becomes negligible.

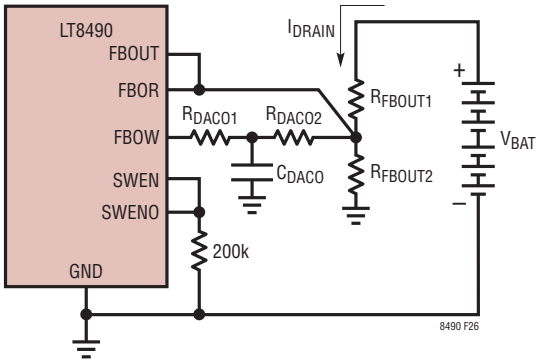

Figure 26. Battery Discharge When Not Charging

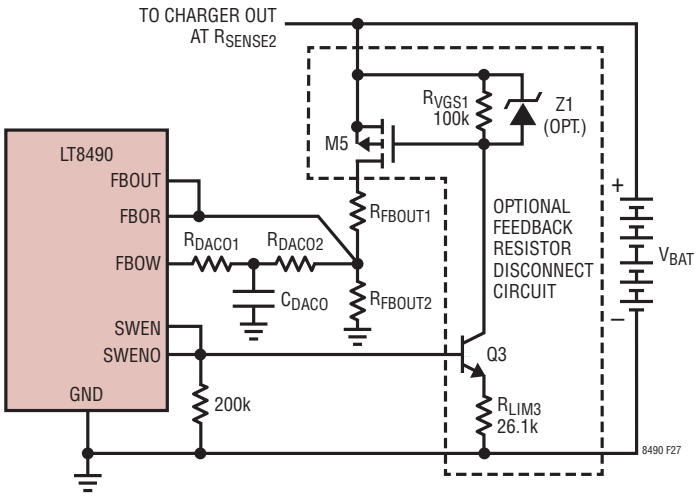

Figure 27. Optional Feedback Resistor Disconnect Circuit

SELECTING M5: This PMOS must have a drain to source breakdown voltage greater than the maximum V_{BAT}. The ZVP3310F is rated for 100V making it suitable for most applications.

SELECTING Q3: This NPN must have a collector to emitter breakdown voltage greater than the maximum V_{BAT}. The MMBT5550L is also suitable for most applications due to its 140V breakdown rating.

SELECTING R_{LIM3}: Using V_{GSon} and setting R_{VGS1} to 100kΩ

$$R_{LIM3} = \left[\left(\frac{R_{VGS1}}{V_{GSon}}\right) \bullet 2.6V\right]\Omega$$

where V_{GSon} is the desired gate to source voltage needed to turn on M5. If M5 is not properly selected, the on resistance may be large enough to cause a significant voltage drop across the drain-source terminal of this device. Check this voltage drop to determine if the application can tolerate this error.

SELECTING Z1: Due to the transients that may occur during hot-plugging of a battery, this Zener diode is recommended to protect device M5 from excessive gate to source voltage. If using device Z1, the reverse breakdown voltage should be selected such that $V_{GSon} < V_{Z1breakdown} < V_{GSMAX}$ where V_{GSMAX} is the maximum rated gate to source voltage specified by the device manufacturer. The BZT52C13 has a reverse breakdown voltage of 13V making it suitable for the R_{LIM3} value shown in Figure 27.

ALTERNATE CIRCUIT: For lower battery voltages (< 20V), Q3 in Figure 27 can saturate. To avoid this, consider connecting the emitter of Q3 directly to ground by removing R_{LIM3} and adding resistor R_{LIM4} to the base of Q3 as shown in Figure 28. Employing the optional feedback resistor disconnect at arbitrarily low battery voltages will be limited by the required gate to source voltage of M5.

Use the following equation to properly set R_{LIM4}:

$$R_{LIM4} = 91 \bullet \frac{R_{VGS1}}{V_{BAT}}$$

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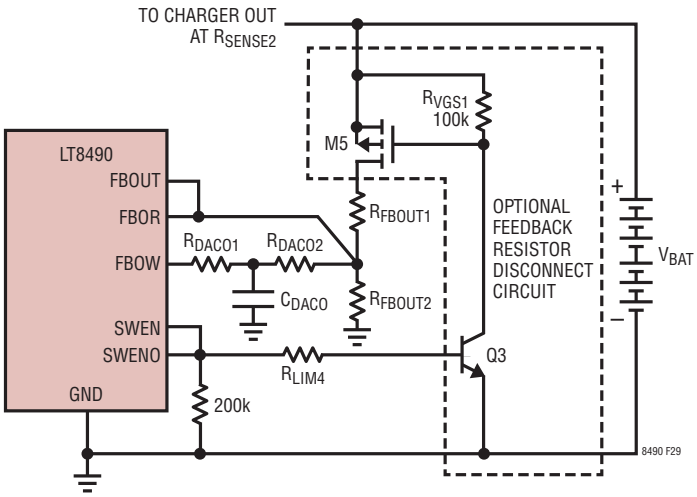

Figure 28. Optional Low Battery Voltage Feedback Resistor Disconnect Circuit

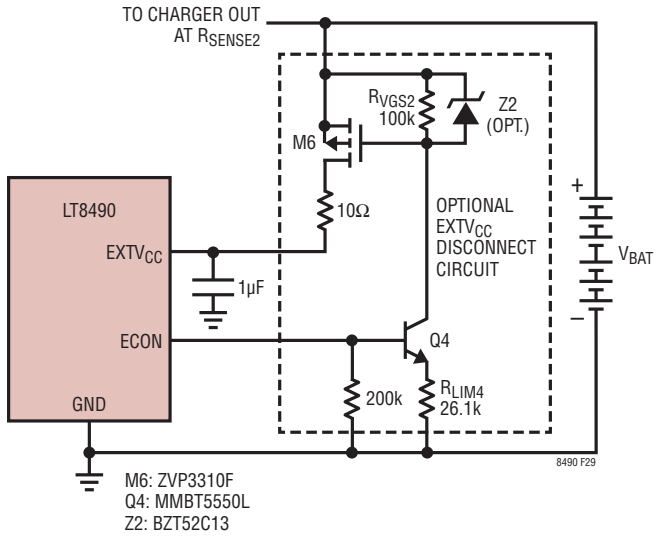

Figure 29. Optional $EXTV_{CC}$ Disconnect Circuit

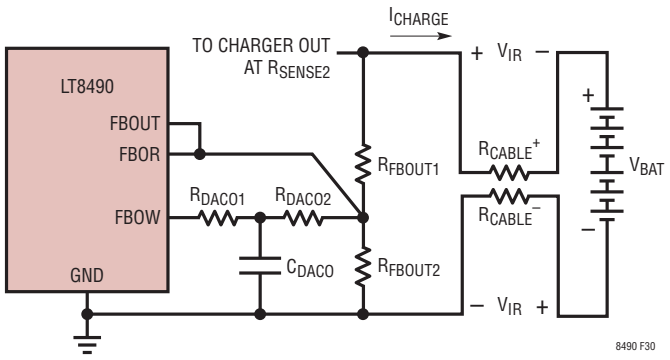

Figure 30. IR Drop Present in Battery Connection

Optional $EXTV_{CC}$ Disconnect

It is often desirable to connect $EXTV_{CC}$ to the battery to reduce power loss (increase efficiency) and heating in the LT8490. However, the LT8490 draws current into the EXT-V_{CC} pin that can drain the battery when charging currents are low or when charging stops. Tying the MODE pin low, as discussed in the Switching Configuration – MODE Pin section, eliminates most of the current draw from $EXTV_{CC}$ when the charging current becomes low. However, there is a 305kΩ (typical) path from $EXTV_{CC}$ to ground through the LT8490 at all times. If MODE is tied high or if the 305kΩ load is undesirable, $EXTV_{CC}$ can be disconnected with the optional circuit shown in Figure 29.

The LT8490, via the ECON signal, disconnects $EXTV_{CC}$ from the battery when charging current becomes low. Charging current is monitored by measuring the IMON_OUT pin voltage with the IOR pin's A/D input. When IMON_OUT falls below 122mV (typical) the ECON signal goes low and EXTVcc is disconnected from the battery. When IMON_OUT rises above 195mV (typical) the ECON signal goes high and $EXTV_{CC}$ is reconnected to the battery.

Follow the same recommendations and equations from the previous section for choosing components for the optional $EXTV_{CC}$ disconnect circuit.

Optional Remote Battery Voltage Sensing

The LT8490 measures the battery voltage continually during charging. The apparent battery voltage is sensed from ground of the LT8490 to the top of R_{FBOUT1}. During charging, resistance in the battery cables (R_{CABLE}^+/R_{CABLE}^- in Figure 30) causes the apparent voltage to be higher than the actual battery voltage by $2 \bullet V_{IR}$.

The effects of this cable drop are most significant when charging low voltage batteries at high currents. As an example, a 4 foot battery cable using 14 AWG wire can have a voltage drop exceeding 0.5V at 15A of current. Note however that the voltage drop, along with the charging current, reduces automatically as the battery approaches full charge.

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The most significant effects from the V_{IR} voltage drops are as follows:

1. When approaching full charge in Stage 2, the V_{IR} error causes the charger to reduce the charging current earlier than otherwise necessary. This increases the total charging time.
2. Terminating at C/10 in Stage 2 will occur at a reduced battery voltage equal to $C/10 \bullet (R_{CABLE}^{+} + R_{CABLE}^{-})$ which is 10% of the voltage drop at full charging current.
3. The STATUS pin will indicate a transition from Stage 1 to Stage 2 earlier than would otherwise occur without the cable drop.

Again, these effects become less significant at higher battery voltages because the charging current is typically lower and the cable drop becomes a smaller percentage of the total battery voltage. Using thicker and/or shorter battery cables is the simplest method for reducing these effects. Otherwise, the remote battery sensing circuit in Figure 31 can correct for these effects.

The R_{CABLE}^{+} measurement error is eliminated by including an additional (+) terminal sensing cable. The negative cable error is eliminated by subtracting the R_{CABLE}^{-} drop from the voltage measured at the positive battery terminal using a (–) terminal sensing cable, the LT1636, Q5 and R5. R'_{FBOUT}, R''_{FBOUT} and R5 are determined as follows:

$$R''_{FBOUT1} = \frac{0.5 \bullet R_{FBOUT1}}{V_{S2} - 1.211}\ \Omega$$

$$R'_{FBOUT1} = \left(R_{FBOUT1} - R''_{FBOUT1}\right)\Omega$$

$$R5 = R''_{FBOUT1}\ \Omega$$

where V_{S2} is the room temperature Stage 2 voltage limit and the solution for R_{FBOUT1} was discussed previously in the Stage Voltage Limits section. Solutions for determining R_{DACO1}, R_{DACO2}, R_{FBOUT2} and C_{DACO} are also discussed in the Stage Voltage Limits section.

Due to its low current draw (< 1mA) Q5 can be a small signal device with a collector-emitter breakdown voltage at least as high as the battery voltage. The MMBT3904 is a good BJT rated to 40V. Alternatively, the MMBT5550L is rated for 140V.

R3 is for safety in case the (+) battery sensing cable becomes disconnected. R3 prevents overcharging the battery in such an event by creating an alternate path to pull up the R''_{FBOUT1} battery voltage sensing resistor. The R3 resistance should be less than 1% of R_{FBOUT1}. Selecting R3 as a 100Ω resistor is often a good choice. During

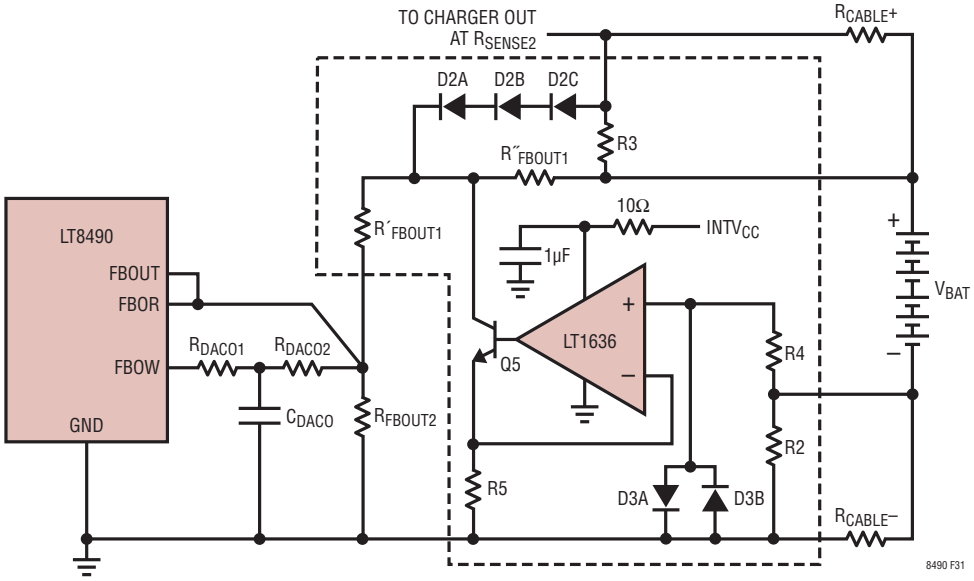

Figure 31. Remove (+) and (–) Cable V_{IR} Measurement Errors

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normal operation the voltage across R3 is about the same as across R_{CABLE}^+. However, R3 may experience voltage up to V_{S2}-V_{BAT} across its terminals if R_{CABLE}^+ becomes disconnected. R3 should be selected with an appropriate power rating, often at least 1W.

D2A-D2C protect the charger if the positive charging cable (R_{CABLE}^+) becomes disconnected while the others remain intact. Without the diodes, the output of the charger may overvoltage and become damaged. BAV99 diodes are a good choice and are available in a dual-diode package to minimize board space. Note that the diodes limit the maximum R_{CABLE}^+ error to 0.3V to 0.5V. If a greater voltage drop is typical in the positive cable then place more diodes in series. D2D protects the M5 device by limiting the gate to source voltage when making the remote sense connection.

D3A, D3B and R4 protect the input of the LT1636 from possible voltage extremes at the (–) battery terminal sensing connection. The dual-diode BAV99 is also suitable in this case. 4.99kΩ is a good value for R4.

R2 maintains a negative voltage reference in case R_{CABLE}^- becomes disconnected. Selecting R2 as a 100Ω resistor is often a good choice. During normal operation the voltage across R2 is about the same as across R_{CABLE}^-. However, R2 may experience voltage in excess of V_{S2}-V_{BAT} across its terminals if R_{CABLE}^- becomes disconnected. R2 should be selected with an appropriate power rating, often at least 1W due to the case where the (+) and (–) wires of the remote sense circuit are first connected to the battery to address hot plugging issues (see the Hot Plugging Considerations section for more detail).

Figure 32 shows how to combine the remote sensing circuit (Figure 31) and the feedback resistor disconnect (Figure 27) for applications that require the most accurate battery voltage sensing and negligible battery drain when charging completes. The R_{VGS1} resistor can no longer connect to the source of M5 (as in Figure 27) since the R_{VGS1} current would also flow through R''_{FBOUT1} causing an error in the measured battery voltage. Figure 31 shows that R_{VGS1} has been reconnected to the (+) battery sensing terminal.

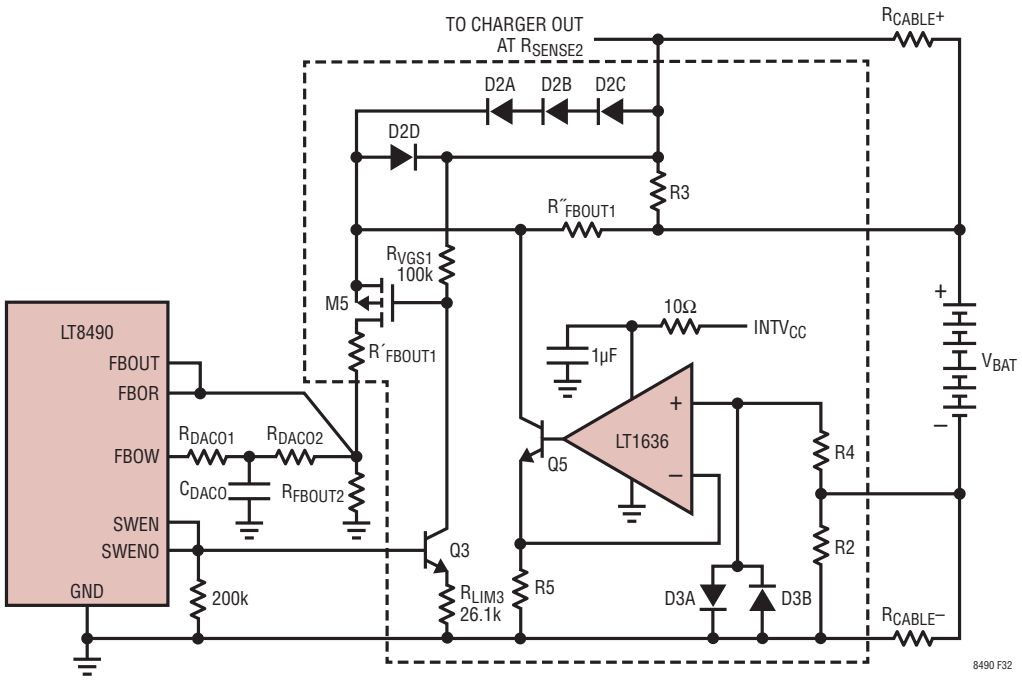

Figure 32. How to Combine Figure 27 and Figure 30

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Optional DC Supply Detection Circuit

A dual input application can be configured where the charger can be supplied by either a solar panel or a DC supply. When powered by a DC supply, the VINR pin must be pulled low to activate power supply mode. In addition, blocking diodes should be incorporated to prevent the supplies from back-feeding into each other. The circuit shown in Figure 33 shows a way to incorporate those features.

As shown in Figure 33, when the DC supply is connected the Q6 NPN pulls VINR below 174mV (typical) to activate the Power Supply Mode of the LT8490. Be sure to choose an NPN that can pull VINR below the power supply mode threshold before fully saturating. Alternatively, Q6 can be replaced with an NMOS device with proper care taken to avoid overvoltage of the NMOS gate.

Depending on the current limit settings, diodes D_{PANEL} and D_{VDC} can incur significant current and heat. Consider the use of Schottky diodes or an appropriate ideal diode such as the LTC4358, LTC4412, LTC4352, etc. to minimize heating.

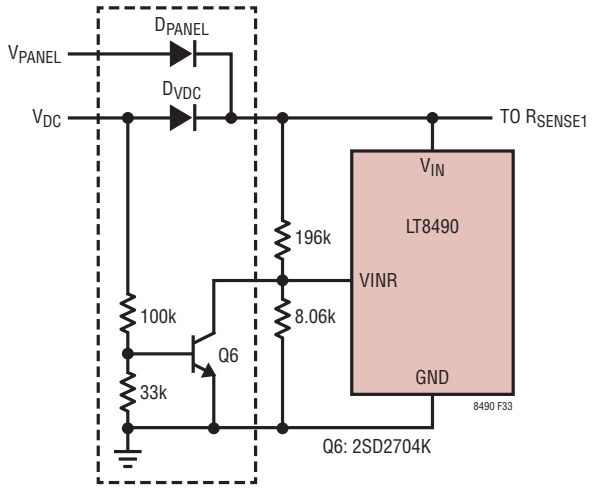

Figure 33. Optional DC Supply Detection Circuit

Board Layout Considerations

For all power components and board routing associated with the LT8705 portion of the LT8490, please refer to the LT8705 documentation for which a circuit board layout checklist and drawing is provided.

Hot Plugging Considerations

When connecting a battery to an LT8490 charger, there can be significant inrush current due to charge equalization between the partially charged battery stack and the charger output capacitors. To a lesser extent a similar effect can occur when connecting an illuminated panel or powered DC supply to the input. The magnitude of the inrush current depends on (1) the battery, panel or supply voltage, (2) ESR of the input or output capacitors, (3) initial voltage of the capacitors, and (4) cable impedance. Excessive inrush current can lead to sparking that can compromise connector integrity and/or voltage overshoot that can cause electrical overstress on LT8490 pins.

Excessive inrush current can be mitigated by first connecting the battery or supply to the charger through a resistive path, followed quickly by a short circuit. This can be accomplished using staggered length pins in a multi-pin connector. This can also be accomplished through the use of the optional circuit shown in Figure 31 by first connecting the (+) and (–) battery remote sense connections, which allow the charger output capacitors to charge through resistors R2 and R3. Alternatively, consider the use of a Hot Swap™ controller such as the LT1641, LT4256, etc. to make a current limited connection.

Design Example

In this design example, the LT8490 is paired with a 175W/5.4A panel (V_{MAX} < 53V) and a 12V flooded lead-acid battery. The desired maximum battery charging current (C) is 10A with a trickle charge current of 2.5A (C/4). Charger settings are as follows: –20°C to 50°C valid battery temperature range, temperature compensated charging limits, no time limits and Stage 3 is enabled with V_{S3}/V_{S2} = 97.2%. In this example resistors are rounded to the nearest standard value. If better accuracy is required then multiple resistors in series may be required.

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- With R_{FBOUT2} set at 20kΩ and a desired Stage 2 voltage limit of 14.2V, the top output feedback resistor, R_{FBOUT1}, is calculated according to the following equation:

$$R_{FBOUT1} = R_{FBOUT2} \bullet \left[V_{S2} \bullet \left(\frac{1.241}{1.211} - 0.128 \right) - 1 \right] \Omega$$

$$= 20k \bullet \left[14.2 \bullet \left(\frac{1.241}{1.211} - 0.128 \right) - 1 \right] \Omega$$

$$= 234,684\Omega$$

Choose R_{FBOUT1} = 237kΩ which is the closest standard value resistor.

- Following the calculation of R_{FBOUT1}, solve for R_{DACO1}, R_{DACO2} and C_{DACO} according to the following formulas:

$$R_{DACO2} = \frac{R_{FBOUT1} \bullet R_{FBOUT2} \bullet 0.833}{\left(R_{FBOUT2} \bullet V_{S2} \bullet \frac{1.241}{1.211} \right) - R_{FBOUT2} - R_{FBOUT1}} \Omega$$

$$= \frac{234,684 \bullet 20k \bullet 0.833}{\left(20k \bullet 14.2 \bullet \frac{1.241}{1.211} \right) - 20k - 234,684} \Omega$$

$$= 107,556\Omega$$

Choose R_{DACO2} = 107kΩ which is the closest standard value resistor.

$$R_{DACO1} = (0.2 \bullet R_{DACO2})\ \Omega$$

$$= 0.2 \bullet 107,556\Omega$$

$$= 21,511\Omega$$

Choose R_{DACO1} = 21.5kΩ which is the closest standard value resistor.

$$C_{DACO} = \frac{1}{500 \bullet R_{DACO1}} F$$

$$= \frac{1}{500 \bullet 21,511} F$$

$$= 93nF$$

- Using the standard value resistors calculated above, the V_{X3}, N_1 and N_2 checking equations yield the following:

V_{X3} = 14.31V

N_1 = 1.22

N_2 = 0.804

- In order to find a resistor combination that yields V_{X3} closer to the desired 14.2V, R_{FBOUT2} is increased to the next higher standard value and the above calculations are repeated.
- Iterations of the previous step are performed that include adjustments to R_{FBOUT1}, R_{DACO1} and R_{DACO2} until the following standard value feedback resistors were chosen:

R_{FBOUT1} = 274kΩ

R_{FBOUT2} = 23.2kΩ

R_{DACO1} = 26.1kΩ

R_{DACO2} = 124kΩ

C_{DACO} = 0.082µF

where:

V_{X3} = 14.27V

N_1 = 1.22

N_2 = 0.805

- With the output feedback network determined, use V_{MAX} and solve for the input resistor feedback network according to the following formulas:

$$R_{FBIN1} = 100k \bullet \left[\frac{1 + \left(\frac{4.47V}{V_{MAX} - 6V} \right)}{1 + \left(\frac{5.593V}{V_{MAX} - 6V} \right)} \right] \Omega$$

$$= 100k \bullet \left[\frac{1 + \left(\frac{4.47V}{53V - 6V} \right)}{1 + \left(\frac{5.593V}{53V - 6V} \right)} \right] \Omega$$

$$= 97,865\Omega$$

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The closest standard value for R_{FBIN1} is 97.6kΩ.

$$R_{DACI2} = 2.75 \bullet \left(\frac{R_{FBIN1}}{V_{MAX} - 6V} \right) \Omega$$

$$= 2.75 \bullet \left(\frac{97,865}{53V - 6V} \right) \Omega$$

$$= 5,726\Omega$$

Choose R_{DACI2} = 5.76kΩ which is the closest standard value.

$$R_{FBIN2} = \frac{1}{\left(\frac{1}{100k - R_{FBIN1}} \right) - \left(\frac{1}{R_{DACI2}} \right)} \Omega$$

$$= \frac{1}{\left(\frac{1}{100k - 97,865} \right) - \left(\frac{1}{5,726} \right)} \Omega$$

$$= 3,404\Omega$$

Choose R_{FBIN2} = 3.4kΩ which is the closest standard value.

$$R_{DACI1} = 0.2 \bullet R_{DACI2}\ \Omega$$

$$= 0.2 \bullet 5,726\Omega$$

$$= 1,145\Omega$$

Choose R_{DAC1} = 1.1kΩ which is the closest standard value.

$$C_{DACI} = \frac{1}{1000 \bullet R_{DACI1}} F$$

$$= \frac{1}{1000 \bullet 1,145} F$$

$$= 873nF$$

- Similar to the output feedback resistors, the final input feedback resistors were chosen to be standard values using an iterative process. The V_{X1} and V_{X2} equations in the Input Voltage Sensing and Modulation Network section were used to validate the selections:

  R_{FBIN1} = 93.1kΩ

  R_{FBIN2} = 3.24kΩ

  R_{DACI1} = 1.05kΩ

  R_{DACI2} = 5.49kΩ

  C_{DACI} = 1µF

  where:

  V_{X1} = 6V

  V_{X2} = 53V

- The 10A maximum charge current limit and 2.5A trickle charge current limit are set by choosing R_{SENSE2}, R_{IMON_OUT} and R_{IOW} using the following formulas:

$$R_{SENSE2} = \frac{0.0497}{I_{OUT(MAX)}} \Omega = \frac{0.0497}{10} \cong 5m\Omega$$

$$R_{IMON\_OUT} = \frac{1208}{I_{OUT(MAXS0)} \bullet R_{SENSE2}} \Omega$$

$$= \frac{1208}{2.5 \bullet 5m} \Omega$$

$$= 96.64k\Omega$$

where the nearest standard value is 97.6kΩ.

$$R_{IOW} = \frac{24.3k \bullet R_{IMON\_OUT}}{R_{IMON\_OUT} - 24.3k} \Omega$$

$$= \frac{24.3k \bullet 47.6k}{97.6k - 24.3k} \Omega$$

$$= 32,356\Omega$$

where the nearest standard value is also 32.4kΩ.

APPLICATIONS INFORMATION

- The input current limit is set by properly choosing R_{SENSE1}. In this example, the panel can deliver up to 5.4A. Choosing a margin of 30% yields:

$$R_{SENSE1} = \frac{0.0505}{I_{IN(MAX)}} = \frac{0.0505}{1.3 \bullet 5.4} = 7.2m\Omega$$

- To enable temperature compensated charging limits and allow a Stage 3 regulation voltage of 97.2% of Stage 2, use $V_{S3} / V_{S2} = 0.972$ in the following equation:

$$CHARGECFG1\% = \left[2.67 \bullet \left(\frac{V_{S3}}{V_{S2}} - 0.85\right) + 0.55\right] \bullet 100\%$$

$$CHARGECFG1\% = 87.6\%$$

Standard resistor values of 90.9kΩ (from CHARGECFG1 to ground) and 13kΩ (from AV_{DD} to CHARGECFG1) can be used to set CHARGECFG1.

- To set no time limits with a –20°C to 50°C valid battery temperature range requires CHARGECFG2 to be tied to AV_{DD}.
- For greater charging voltage accuracy, it is recommended that 0.1% tolerance resistors be used for the output feedback resistor network.
- Please reference the LT8705 data sheet for completing the remaining power portions of the LT8490.

APPLICATIONS INFORMATION

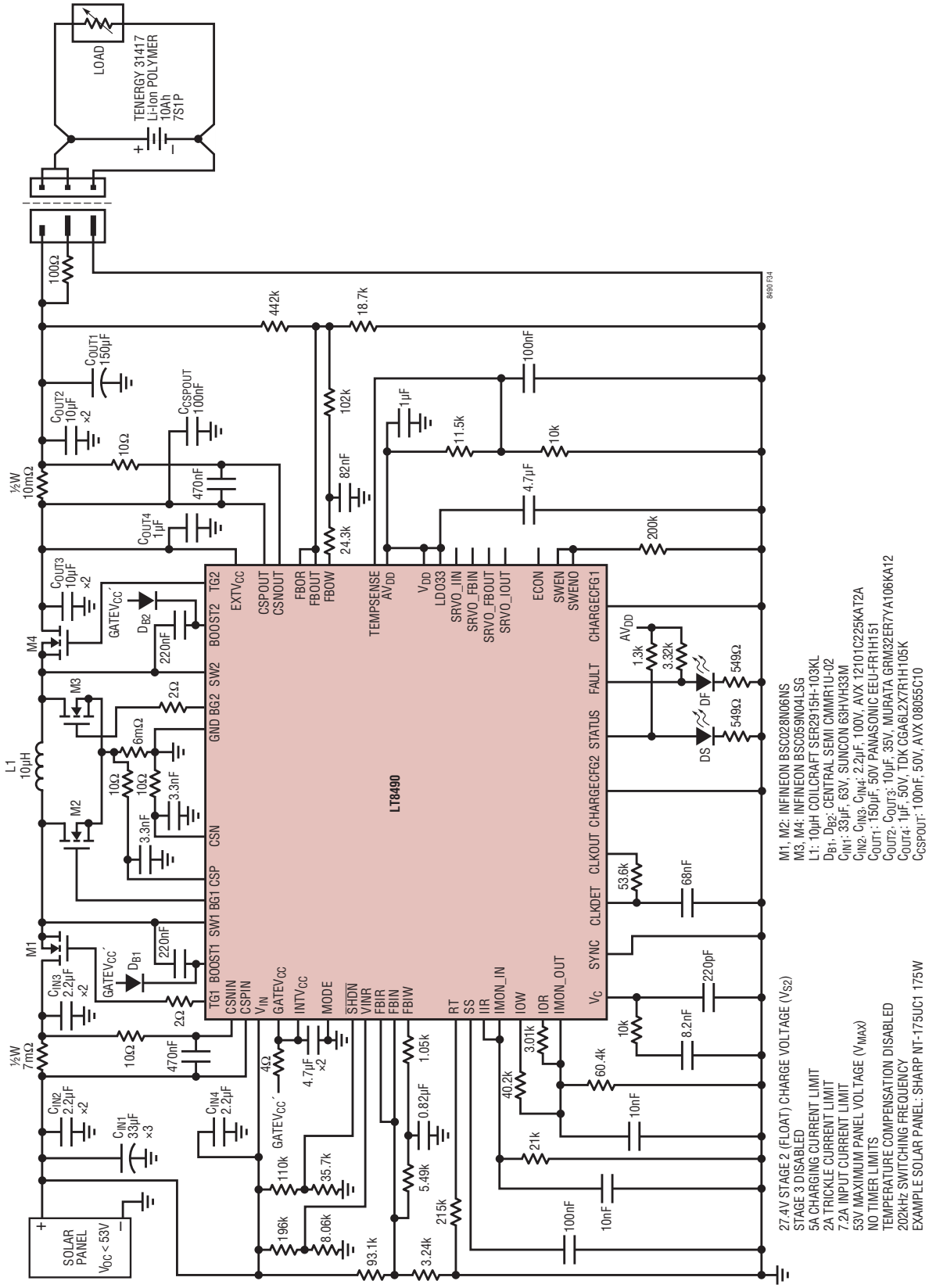
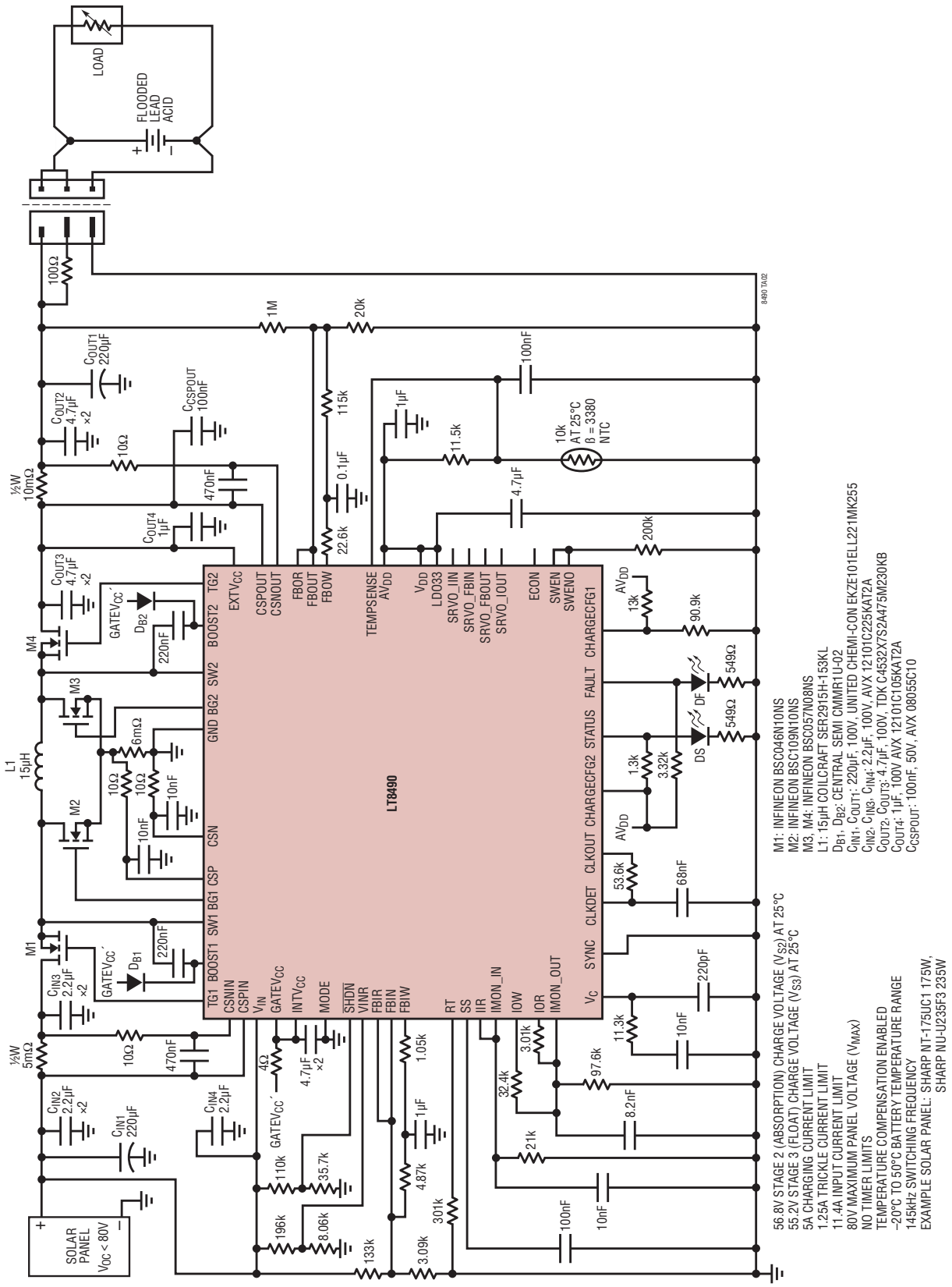


Figure 34. 27.4V Lithium-Ion Polymer Battery Charger

APPLICATIONS INFORMATION

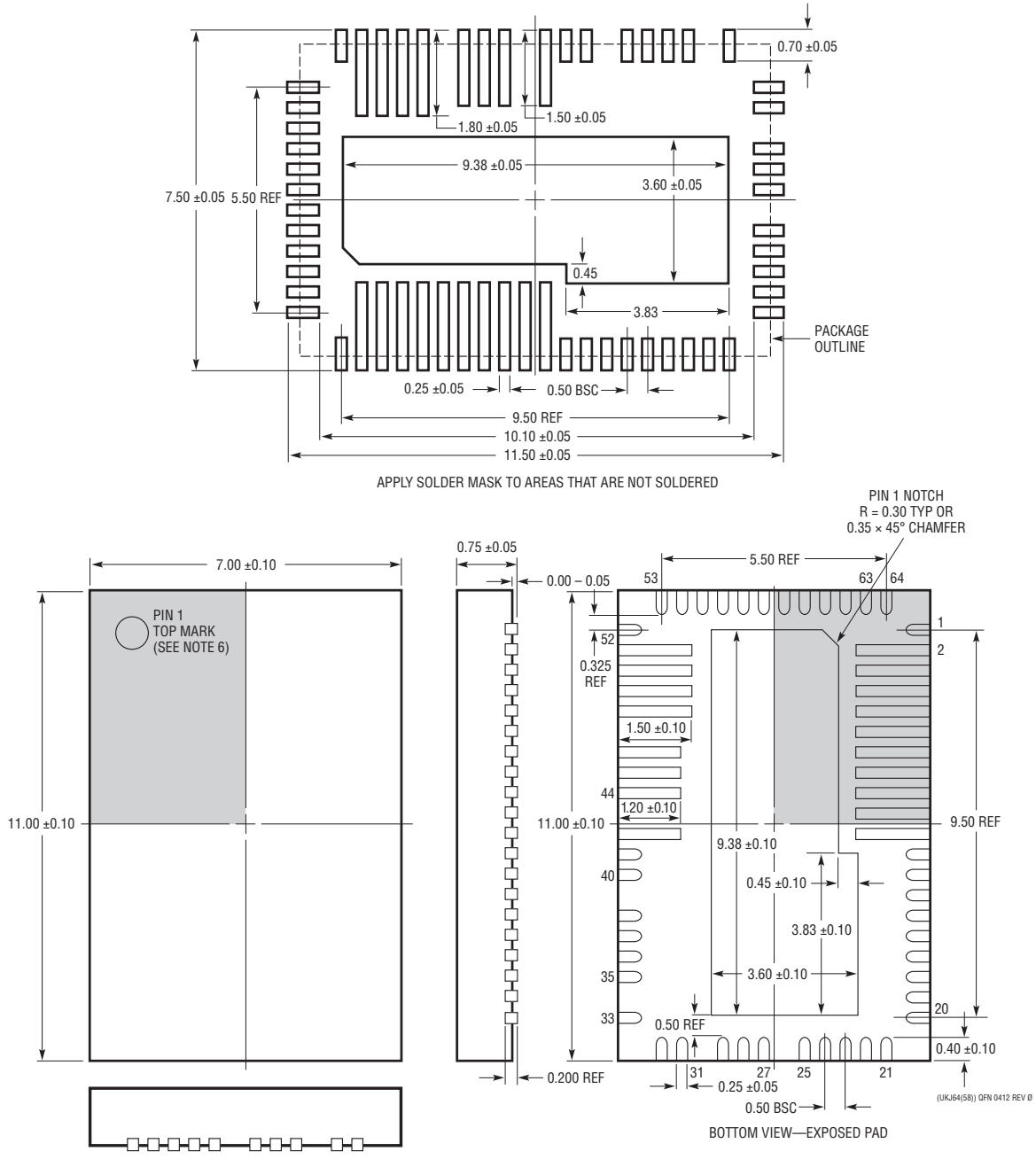
56.8V Lead-Acid Battery Charger (Four 12V Batteries in Series)



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT8490#packaging for the most recent package drawings.

UKJ Package
Variation: UKJ64(58)
64(58)-Lead Plastic QFN (7mm × 11mm)
(Reference LTC DWG # 05-08-1922 Rev Ø)



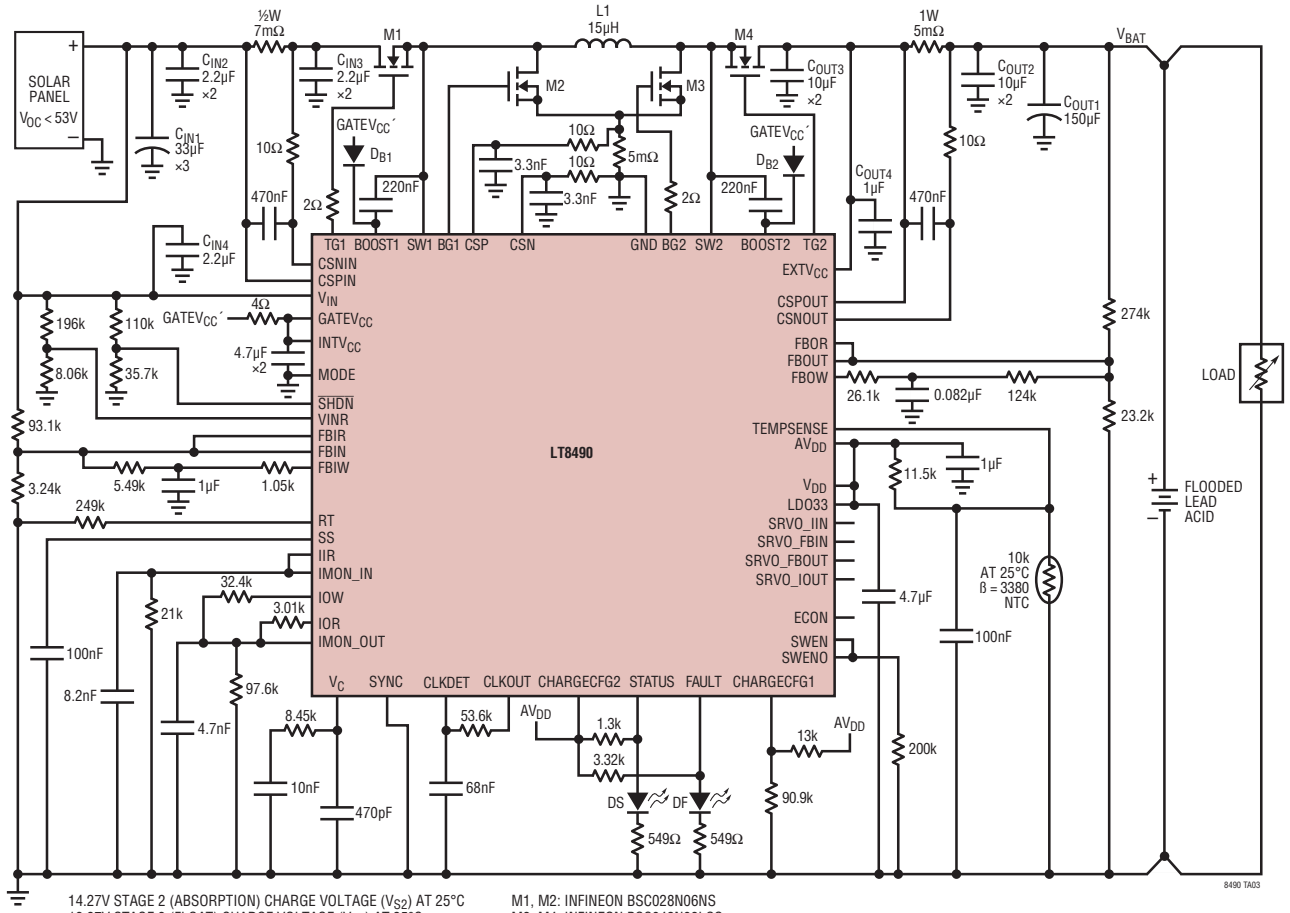
NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/15	Changed diode type symbol. Modified the Block Diagram.	1, 38, 39, 42 11

TYPICAL APPLICATION

14.2V Flooded Lead-Acid Battery Charger



14.27V STAGE 2 (ABSORPTION) CHARGE VOLTAGE (V_{S2}) AT 25°C
13.87V STAGE 3 (FLOAT) CHARGE VOLTAGE (V_{S3}) AT 25°C
10A CHARGING CURRENT LIMIT
2.5A TRICKLE CURRENT LIMIT
7.2A INPUT CURRENT LIMIT
53V MAXIMUM PANEL VOLTAGE (V_{MAX})
NO TIMER LIMITS
TEMPERATURE COMPENSATION ENABLED
–20°C TO 50°C BATTERY TEMPERATURE RANGE
175kHz SWITCHING FREQUENCY
EXAMPLE SOLAR PANEL: SHARP NT-175UC1 175W

M1, M2: INFINEON BSC028N06NS
M3, M4: INFINEON BSC042N03LSG
L1: 15µH COILCRAFT SER2915H-153KL
D_{B1}, D_{B2}: CENTRAL SEMI CMMR1U-02
C_{IN1}: 33µF, 63V, SUNCON 63HVH33M
C_{IN2}, C_{IN3}, C_{IN4}: 2.2µF, 100V, AVX 12101C225KAT2A
C_{OUT1}: 150µF, 35V NICHICON UPJ151MPD6TD
C_{OUT2}, C_{OUT3}: 10µF, 35V, MURATA GRM32ER7YA106KA12
C_{OUT4}: 1µF, 25V AVX 12063C105KAT2A

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3652/LT3652HV	Power Tracking 2A Battery Charger for Solar Power	V_{IN} Range = 4.95V to 32V (LT3652), 4.95V to 34V (HV), MPPC
LTC4000-1	High Voltage, High Current Controller for Battery Charger with MPPC	V_{IN} and V_{OUT} Range = 3V to 60V, MPPC
LTC4020	55V V_{IN}/V_{OUT} Buck-Boost Multi-Chemistry Battery Charging Controller	Li-Ion and Lead-Acid Algorithms, MPPC

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