SEPIC/Boost Converter with 2A, 70V Switch, 9µA Quiescent Current, POR and Watchdog Timer

FEATURES

- **Wide Input Voltage Range of ~1V to 60V (2.5V to 32V for Start-Up)**
- **Low Ripple Burst Mode® Operation**
  - **9µA I_Q at 12V_{IN} to 5.0V_{OUT}**
  - **Output Ripple (<10mV Typ.)**
- **Dual Supply Pins:**
  - **Improves Efficiency**
  - **Reduces Minimum Supply Voltage to ~1V after Start-Up to Extend Battery Life**
- **Integrated 2A/70V Power Switch**
- **Programmable Watchdog Timer Can Operate When V_{IN} Supply Is Removed**
- **Programmable Power-On Reset Timer (POR) with $\overline{RST}$ Functional for Input Supply Down to 1.3V**
- **FMEA Fault Tolerant in TSSOP Package**
- Fixed Frequency PWM, SEPIC/BOOST/FLYBACK Topologies
- Programmable Switching Frequency: 250kHz to 1.5MHz
- UVLO Programmable on SWEN and $\overline{RSTIN}$ Pins
- Soft-Start Programmable with One Capacitor
- Small 20-Lead QFN or 20-Lead TSSOP Packages

APPLICATIONS

- Automotive ECU Power
- Power for Portable Products
- Industrial Supplies

DESCRIPTION

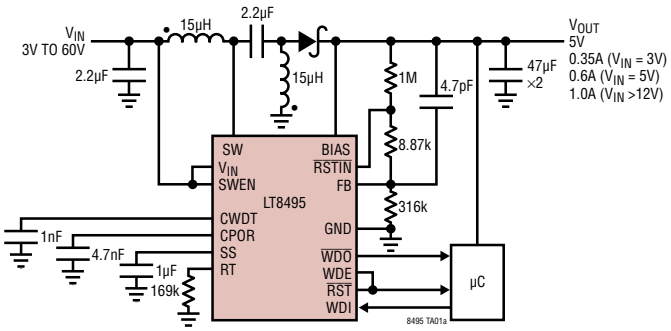
The LT®8495 is an adjustable frequency (250kHz to 1.5MHz) monolithic switching regulator with a power-on reset and watchdog timer. Quiescent current can be less than 9µA when operating and is ~0.3µA when SWEN, WDE and $\overline{RSTIN}$ are low. Configurable as a SEPIC, boost or flyback converter, the low ripple Burst Mode operation maintains high efficiency at low output current while keeping output ripple below 10mV. Dual supply pins (V_{IN} and BIAS) allow the part to automatically operate from the most efficient supply. Input supply voltage can be up to 60V for SEPIC topologies and up to 32V (with ride-through up to 60V) for boost and flyback topologies. After start-up, battery life is extended since the part can draw current from its output (BIAS) even when V_{IN} voltage drops below 2.5V.

The reset and watchdog timeout periods are independently adjustable using external capacitors. Using a resistor divider on the SWEN pin provides a programmable undervoltage lockout (UVLO) for the converter. A resistor divider connected to $\overline{RSTIN}$ provides UVLO control that asserts the $\overline{RST}$ pin.

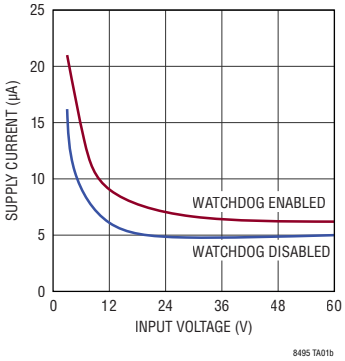
Additional features such as frequency foldback and soft-start are integrated. Fault tolerance in the TSSOP allows for adjacent pin shorts or an open without raising the output voltage above its programmed value. The LT8495 is available in 20-lead QFN and 20-lead TSSOP packages with exposed pads for low thermal resistance.

TYPICAL APPLICATION

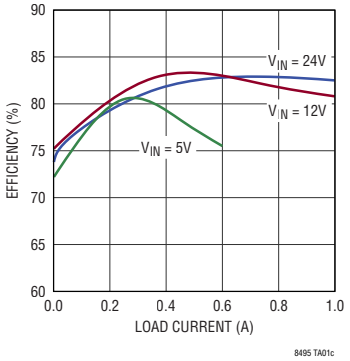
450kHz, 5V Output SEPIC Converter



No-Load Supply Current



Efficiency

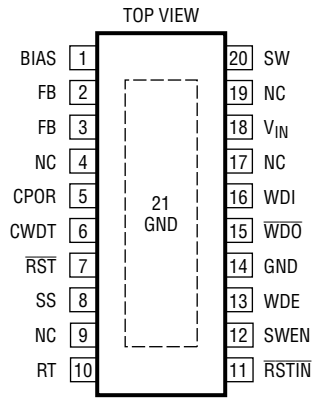


ABSOLUTE MAXIMUM RATINGS

(Note 1)

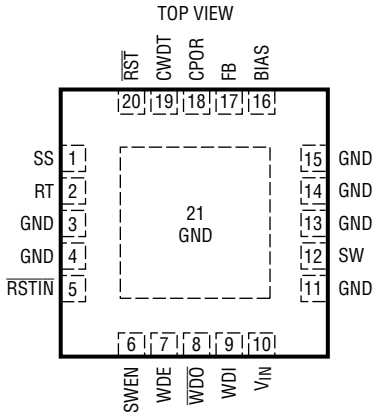
V_{IN}, BIAS Voltage 60V
SWEN, WDE, $\overline{RSTIN}$ Voltage 60V
FB Voltage 60V
SW Voltage 70V
WDI, $\overline{RST}$, $\overline{WDO}$ Voltage 6V
RT Voltage 6V
CPOR, CWDT, SS Voltage 3V
Operating Junction Temperature Range
LT8495E, LT8495I (Notes 2, 3) ..... –40°C to 125°C
LT8495H (Notes 2, 3) ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
FE Package ..... 300°C

PIN CONFIGURATION



FE PACKAGE
20-LEAD PLASTIC TSSOP

θ_{JA} = 38°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB



UF PACKAGE
20-LEAD (4mm × 4mm) PLASTIC QFN

θ_{JA} = 47°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LT8495#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8495EUF#PBF	LT8495EUF#TRPBF	8495	20-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C
LT8495IUF#PBF	LT8495IUF#TRPBF	8495	20-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C
LT8495EFE#PBF	LT8495EFE#TRPBF	LT8495FE	20-Lead Plastic TSSOP	–40°C to 125°C
LT8495IFE#PBF	LT8495IFE#TRPBF	LT8495FE	20-Lead Plastic TSSOP	–40°C to 125°C
LT8495HFE#PBF	LT8495HFE#TRPBF	LT8495FE	20-Lead Plastic TSSOP	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{SWEN} = 12V, V_{BIAS} = V_{WDE} = 5V, unless otherwise noted (Note 2).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum V_{IN} Operating Voltages	V_{BIAS} < 2.5V V_{BIAS} ≥ 2.5V	● ●		2.4	2.5 0	V V
Minimum BIAS Operating Voltages	V_{IN} < 2.5V V_{IN} ≥ 2.5V	● ●		2.4	2.5 0	V V
Power Switch Driver (PSD) Overvoltage Threshold (Note 4)	V_{IN} or BIAS Rising V_{IN} or BIAS Falling	● ●	32.1 32	34 33.9	36.5 36.4	V V
Power Switch Driver (PSD) Overvoltage Threshold Hysteresis (Note 4)				100		mV
Quiescent Current from V_{IN}	V_{SWEN} = 0V, V_{WDE} = 0V, $V_{\overline{RSTIN}}$ = 0V V_{SWEN} = 5V, V_{WDE} = 0V, V_{FB} = $V_{\overline{RSTIN}}$ = 1.25V V_{SWEN} = 5V, V_{WDE} = 5V, V_{FB} = $V_{\overline{RSTIN}}$ = 1.25V V_{SWEN} = 5V, V_{WDE} = 0V, V_{FB} = $V_{\overline{RSTIN}}$ = 1.25V (LT8495E, LT8495I) (LT8495H) V_{SWEN} = 5V, V_{WDE} = 5V, V_{FB} = $V_{\overline{RSTIN}}$ = 1.25V (LT8495E, LT8495I) (LT8495H)	 ● ● ● ●		0.3 3.0 3.1 3.0 3.0 3.1 3.1	0.9 4.8 4.9 6.2 8.0 6.3 8.0	µA µA µA µA µA µA µA
Quiescent Current from BIAS	V_{SWEN} = 0V, V_{WDE} = 0V, $V_{\overline{RSTIN}}$ = 0V V_{SWEN} = 5V, V_{WDE} = 0V, V_{FB} = $V_{\overline{RSTIN}}$ = 1.25V V_{SWEN} = 5V, V_{WDE} = 5V, V_{FB} = $V_{\overline{RSTIN}}$ = 1.25V V_{SWEN} = 5V, V_{WDE} = 0V, V_{FB} = $V_{\overline{RSTIN}}$ = 1.25V (LT8495E, LT8495I) (LT8495H) V_{SWEN} = 5V, V_{WDE} = 5V, V_{FB} = $V_{\overline{RSTIN}}$ = 1.25V (LT8495E, LT8495I) (LT8495H)	 ● ● ● ●		0.07 1.7 6.0 1.7 1.7 6.0 6.0	0.5 2.8 8.5 4.0 11 10.0 15.5	µA µA µA µA µA µA µA
BIAS to V_{IN} Comparator Threshold	V_{BIAS}-V_{IN}, V_{BIAS} Rising, V_{IN} = 12V V_{BIAS}-V_{IN}, V_{BIAS} Falling, V_{IN} = 12V Hysteresis (Rising-Falling Threshold)	● ● ●	0.55 0.17 0.20	0.90 0.37 0.53	1.2 0.57 0.80	V V V
Feedback Voltage		●	1.178	1.202	1.230	V
FB Pin Bias Current (Note 7)	V_{FB} = 1.202V			0.1	20	nA
FB Voltage Line Regulation	5V ≤ V_{IN} ≤ 32V, V_{BIAS} = 5V 5V ≤ V_{IN} ≤ 32V, V_{BIAS} = 0V			0.2 0.2	10 10	m%/V m%/V
Minimum Switch Off-Time				70		ns
Minimum Switch On-Time				95		ns
Switching Frequency	R_T = 68.1k R_T = 324k	● ●	0.92 219	1.0 250	1.06 280	MHz kHz
Switch Current Limit at Min. Duty Cycle (Note 5)		●	2.1	2.55	2.95	A
Switch Current Limit at Max. Duty Cycle (Note 6)		●	1.3	1.85	2.4	A
Switch V_{CESAT}	I_{SW} = 1.2A			340		mV
Switch Leakage Current (Note 7)	V_{SW} = 12V, V_{SWEN} = 0V			0.01	1	µA
Soft-Start Charging Current (Note 7)	V_{SS} = 100mV	●	5.2	8.2	12.2	µA
SWEN Pin Current (Note 7)	V_{SWEN} = 1.2V V_{SWEN} = 5V V_{SWEN} = 12V			0 35 240	25 200 550	nA nA nA
SWEN Rising Voltage Threshold		●	0.9	1	1.1	V
SWEN Voltage Hysteresis				30		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{SWEN} = 12V, V_{BIAS} = V_{WDE} = 5V, unless otherwise noted (Note 2).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{RSTIN}$ Pin Current (Note 7)	$V_{\overline{RSTIN}}$ = 1.2V $V_{\overline{RSTIN}}$ = 5V $V_{\overline{RSTIN}}$ = 12V			0 35 240	25 200 550	nA nA nA
$\overline{RSTIN}$ Threshold as % of V_{FB} Regulation Voltage		●	86	92	97	%
$\overline{RSTIN}$ Low to $\overline{RST}$ Asserted (t_{UV})	Step $V_{\overline{RSTIN}}$ from 1.3V to 0.9V	●	8	23	60	µs
Watchdog Timeout and Reset Delay Period (t_{RST}) (Note 8)	C_{POR} = 4700pF, Watchdog Timeout Not Occurring at Same Time as the Reset Delay	●	8.5	9.5	11.85	ms
Watchdog Upper Boundary (t_{WDU}) (Note 8)	C_{WDT} = 1000pF	●	14.9	16.7	20.9	ms
Watchdog Lower Boundary (t_{WDL}) (Note 8)	C_{WDT} = 1000pF	●	580	650	812	µs
$\overline{RST}$ Output Voltage Low	I_{SINK} = 1.25mA I_{SINK} = 100µA, V_{BIAS} = 1.3V, V_{IN} = 0V I_{SINK} = 100µA, V_{IN} = 1.3V, V_{BIAS} = 0V	● ● ●		33 15 15	150 150 150	mV mV mV
$\overline{RST}$ Leakage Current	$V_{\overline{RSTIN}}$ = 1.2V, $V_{\overline{RST}}$ = 5V (LT8495E, LT8495I) $V_{\overline{RSTIN}}$ = 1.2V, $V_{\overline{RST}}$ = 5V (LT8495H)	● ●		0 0	0.3 1.0	µA µA
$\overline{WDO}$ Output Voltage Low	I_{SINK} = 1.25mA	●		120	420	mV
$\overline{WDO}$ Leakage Current	$V_{\overline{WDO}}$ = 5V	●		0	0.25	µA
WDI Pin Current	V_{WDI} = 5V			0	0.1	µA
WDI Input Rising Threshold		●	0.4	0.8	1.25	V
WDI Voltage Hysteresis				58		mV
WDI Input Pulse Width		●	300			ns
WDE Pin Current (Note 7)	V_{WDE} = 1.2V V_{WDE} = 5V V_{WDE} = 12V			0 35 240	25 200 550	nA nA nA
WDE Rising Voltage Threshold		●	0.9	1	1.1	V
WDE Voltage Hysteresis				30		mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. Voltages are with respect to GND pin unless otherwise noted.

Note 2: The LT8495E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8495I is guaranteed to meet performance specifications from –40°C to 125°C junction temperature. The LT8495H is guaranteed over the full –40°C to 150°C operating junction temperature range. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating range when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: See Power Supplies and Operating Limits in the Applications Information section for more details.

Note 5: Current limit guaranteed by design and/or correlation to static test. Slope Compensation reduces current limit at higher duty cycles.

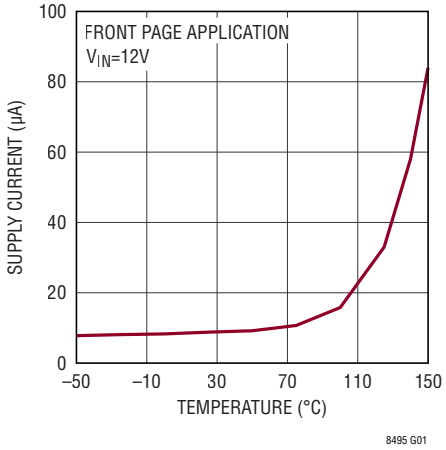
Note 6: Max duty cycle current limit measured at 1MHz switching frequency.

Note 7: Polarity specification for all currents into pins is positive. All voltages are referenced to GND unless otherwise specified.

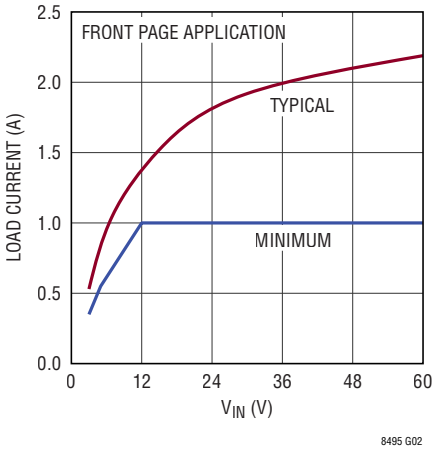
Note 8: This specification is guaranteed for only the exact capacitance as listed in the conditions. Variation of the capacitance from the exact listed value will cause proportional variation to t_{RST}, t_{WDU} and t_{WDL}.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

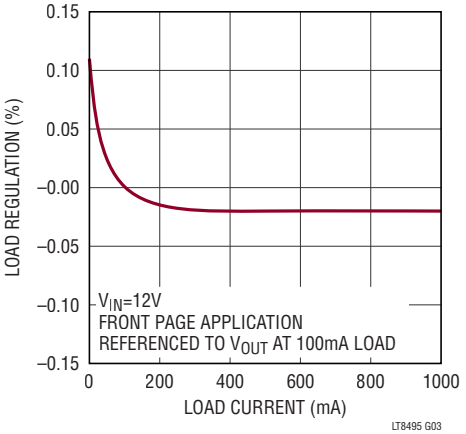
No Load Supply Current



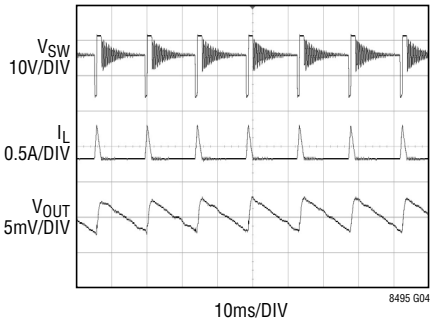
Maximum Load Current



Load Regulation

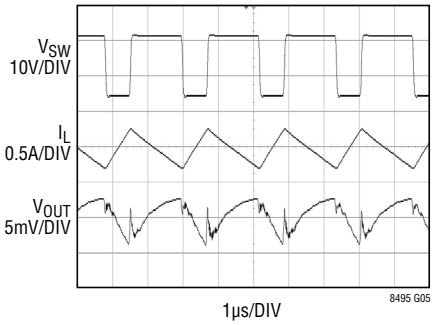


Switching Waveforms, Burst Mode Operation



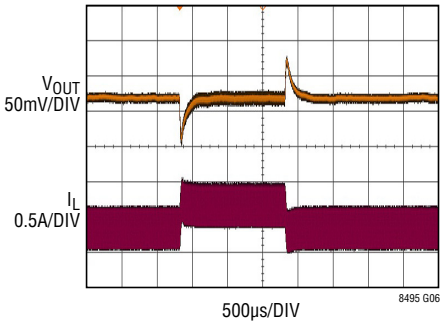
FRONT PAGE APPLICATION
V_{IN} = 12V
V_{OUT} = 5V
I_{LOAD} = 20mA

Switching Waveforms, Full Frequency Continuous Operation



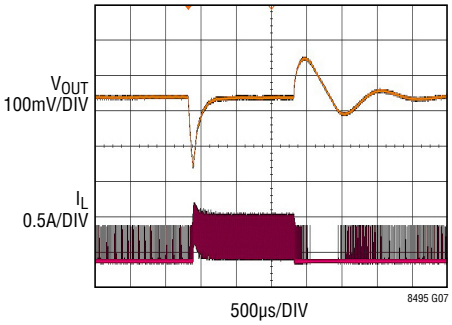
FRONT PAGE APPLICATION
V_{IN} = 12V
V_{OUT} = 5V
I_{LOAD} = 0.5A

Transient Load Response; Load Current Is Stepped from 300mA to 500mA



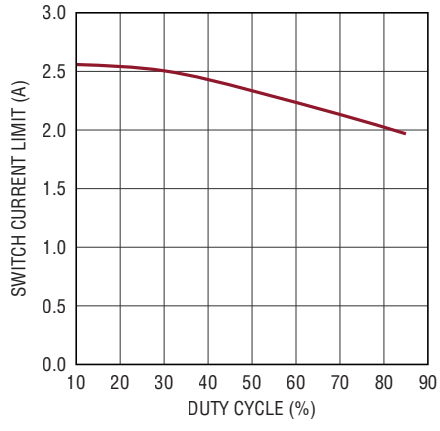
FRONT PAGE APPLICATION
V_{IN} = 12V
V_{OUT} = 5V

Transient Load Response; Load Current Is Stepped from 20mA (Burst Mode Operation) to 220mA

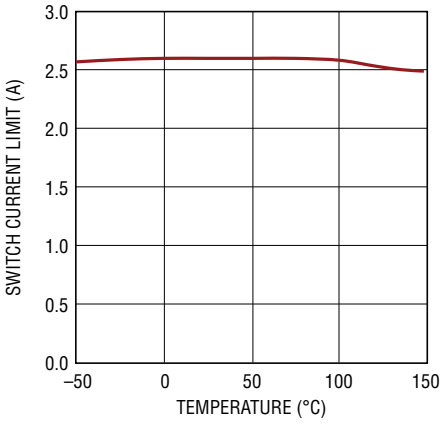


FRONT PAGE APPLICATION
V_{IN} = 12V
V_{OUT} = 5V

Switch Current Limit at 500kHz

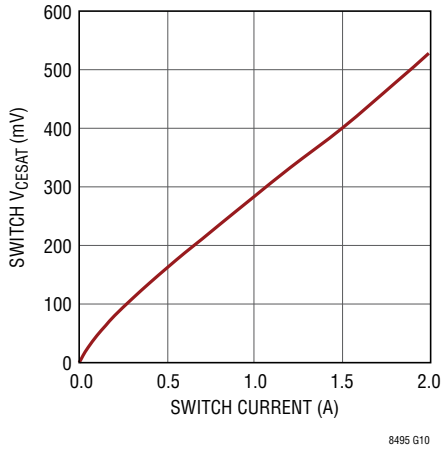


Switch Current Limit at Minimum Duty Cycle

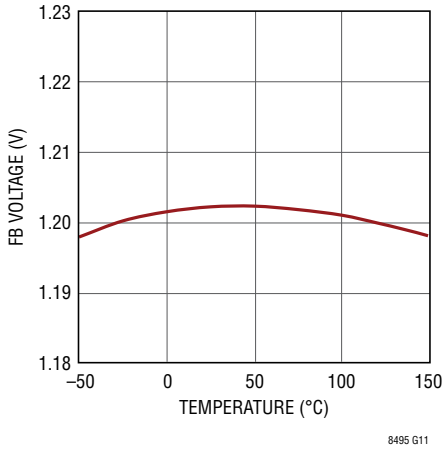


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

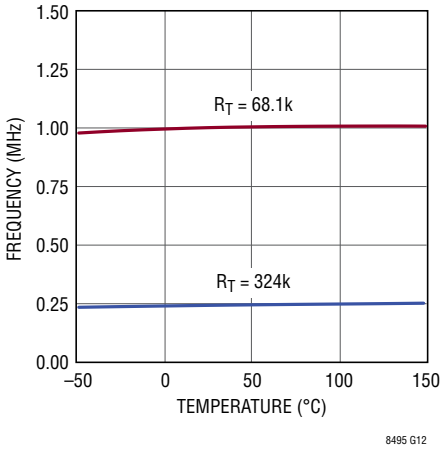
Switch V_{CESAT}



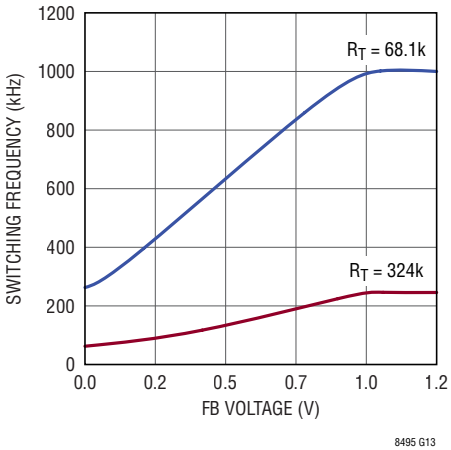
Feedback Voltage



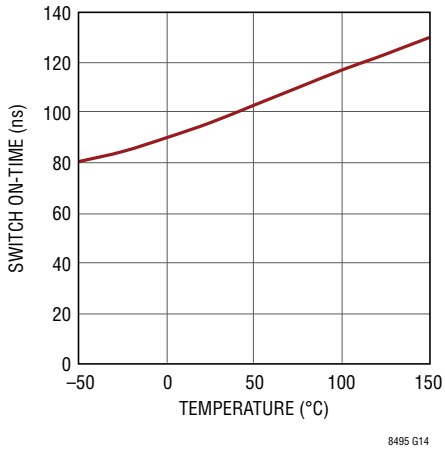
Oscillator Frequency



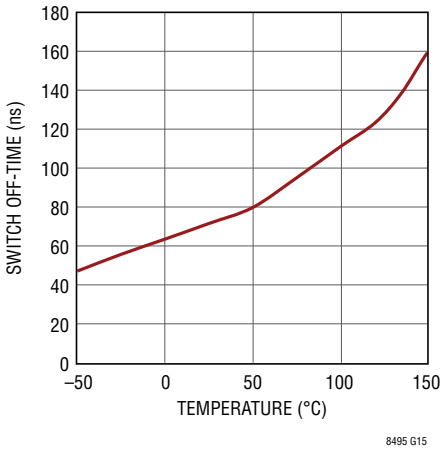
Frequency Foldback



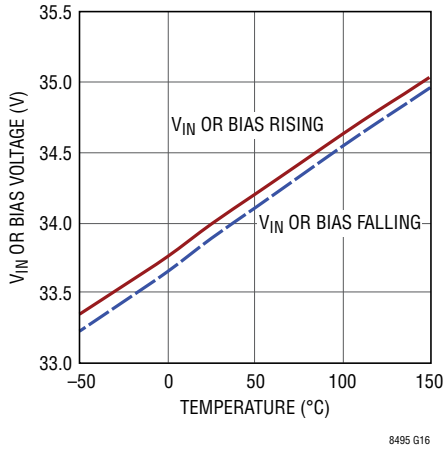
Minimum Switch On-Time



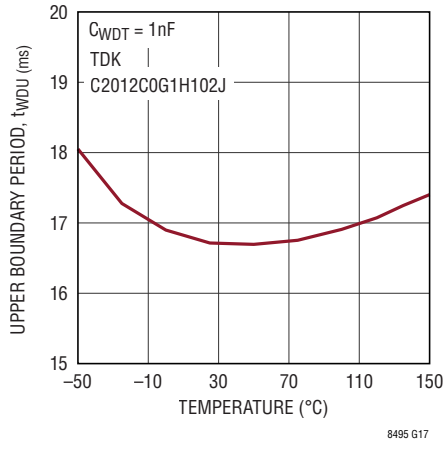
Minimum Switch Off-Time



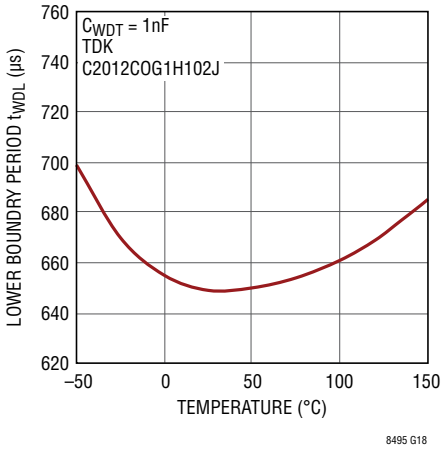
Overvoltage Lockout



Watchdog Upper Boundary Period

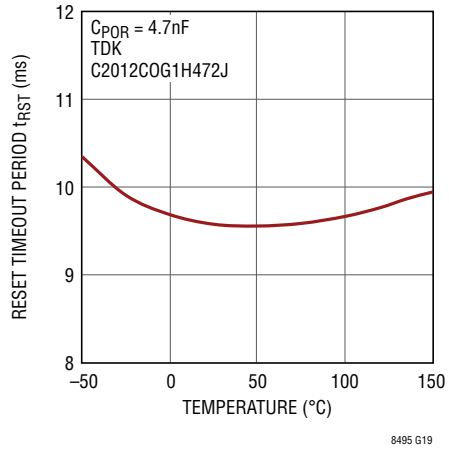


Watchdog Lower Boundary Period



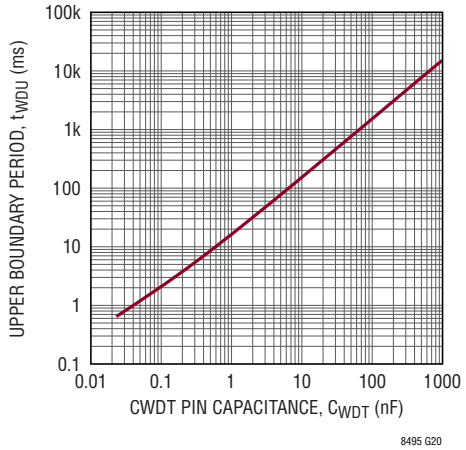
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Reset Timeout Period



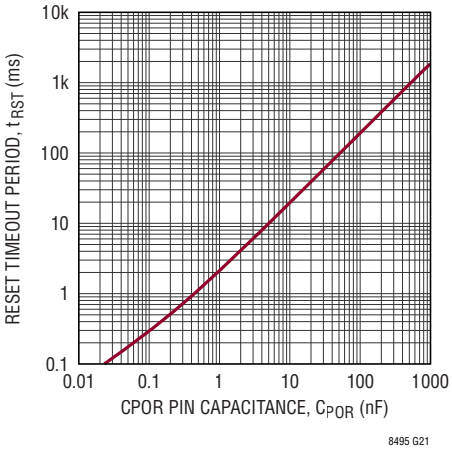
8495 G19

Watchdog Upper Boundary Period vs Capacitance



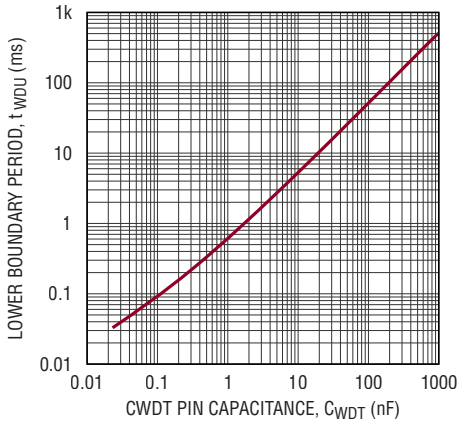
8495 G20

Reset Timeout Period vs Capacitance



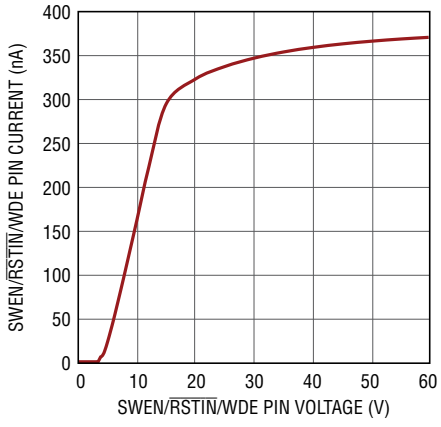
8495 G21

Watchdog Lower Boundary Period vs Capacitance



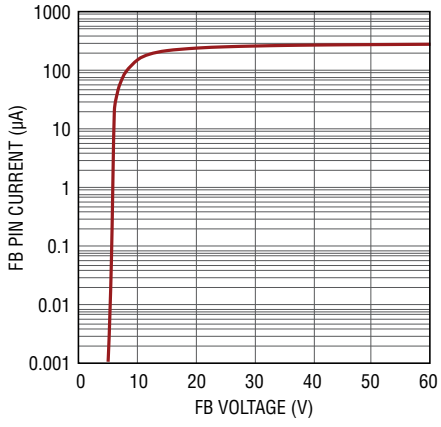
8495 G22

SWEN/$\overline{\text{RSTIN}}$/WDE Pin Current



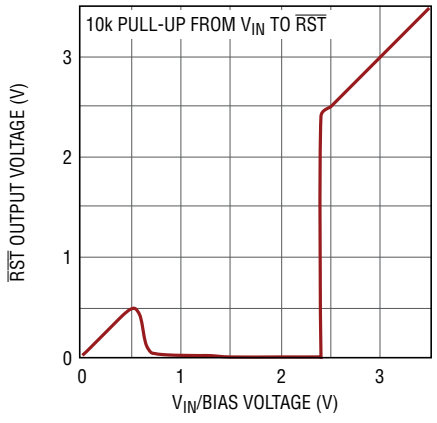
8495 G23

FB Pin Current



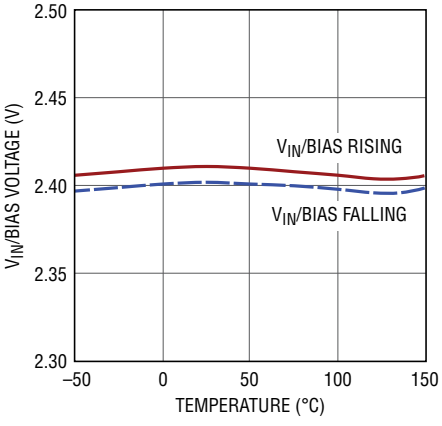
8495 G24

$\overline{\text{RST}}$ Output Voltage vs Supply Voltage



8495 G25

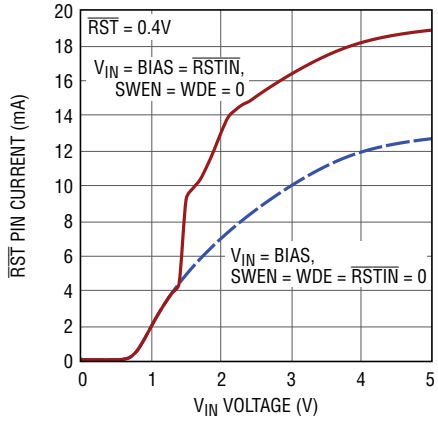
Internal UVLO



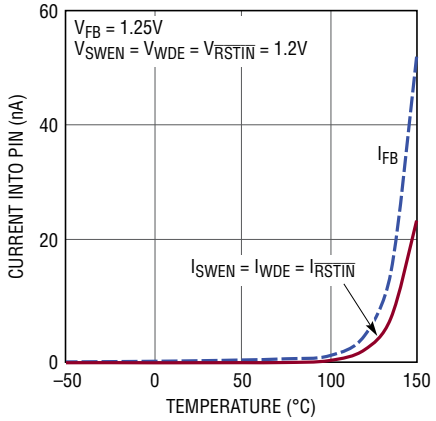
8495 G26

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

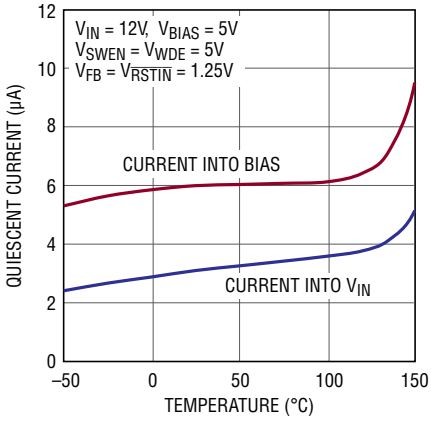
$\overline{RST}$ Pin Current vs Supply Voltage



Pin Current



Quiescent Current



PIN FUNCTIONS (QFN/TSSOP)

SS (Pin 1/Pin 8): Soft-Start Pin. Place a soft-start capacitor on this pin. Upon start-up, the SS pin will be charged by a (nominally) 256k resistor to about 2.1V.

RT (Pin 2/Pin 10): Oscillator Frequency Set Pin. Place a resistor from this pin to ground to set the internal oscillator frequency. Minimize capacitance on this pin. See the Applications Information section for more details.

GND (Pins 3, 4, 11, 13, 14, 15, Exposed Pad 21/Pin 14, Exposed Pad 21): Ground. Solder all pins and the exposed pad directly to the local ground plane. The exposed pad metal of the package provides both electrical contact to ground and good thermal contact to the printed circuit board.

NC (Pins 4, 9, 17, 19, TSSOP only): No Connects: These pins are not connected to internal circuitry and must be left floating to ensure fault tolerance.

$\overline{\text{RSTIN}}$ (Pin 5/Pin 11): Reset Input Reference. Connect a resistor divider to $\overline{\text{RSTIN}}$ to set the threshold voltage for asserting $\overline{\text{RST}}$. The $\overline{\text{RSTIN}}$ voltage is compared to an internal 1.1V reference. $\overline{\text{RSTIN}}$ voltages lower than the reference cause $\overline{\text{RST}}$ to assert low.

SWEN (Pin 6/Pin 12): Switch Enable Detect Pin. This pin enables/disables the switching regulator and soft-start. A resistor divider can be connected to SWEN to perform an undervoltage lockout function.

WDE (Pin 7/Pin 13): Watchdog Timer Enable Pin. Drive above 1.1V to enable the watchdog timer function. When WDE is low, the $\overline{\text{WDO}}$ output driver is disabled causing the pin to be high impedance.

$\overline{\text{WDO}}$ (Pin 8/Pin 15): Watchdog Out. Active low, open-drain output. $\overline{\text{WDO}}$ asserts low if WDE is enabled and the microcontroller fails to drive the WDI pin of the LT8495 with the appropriate signal.

WDI (Pin 9/Pin 16): Watchdog Timer Input Pin. This pin receives the watchdog signal from a microcontroller. If the appropriate signal is not received, $\overline{\text{WDO}}$ will pulse low for a period equal to the reset delay timer period (t_{RST}).

V_{IN} (Pin 10/Pin 18): Supply Input Pin. This pin is typically connected to the input of the DC/DC converter. Must be locally bypassed.

SW (Pin 12/Pin 20): Switch Pin. This is the collector of the internal NPN power switch. Minimize trace area connected to this pin to minimize EMI.

BIAS (Pin 16/Pin 1): Supply Input Pin. This pin is typically connected to the output of the DC/DC converter in cases where V_{IN} can be higher than V_{OUT}. Must be locally bypassed.

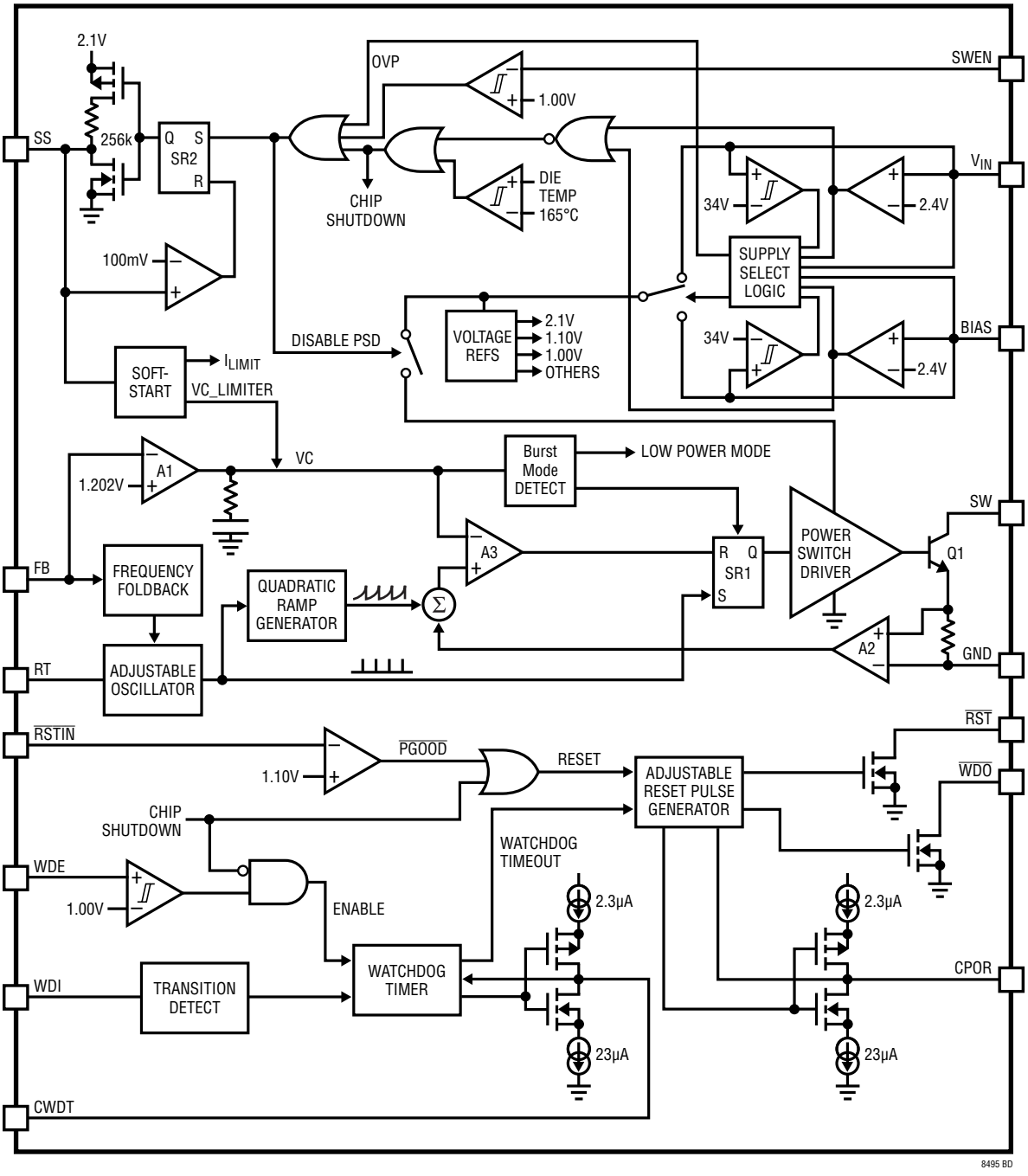
FB (Pin 17/Pins 2, 3): Output Voltage Feedback Pin. The LT8495 regulates the FB pin to 1.202V. Connect a resistor divider between the output, FB and GND to set the regulated output voltage.

CPOR (Pin 18/Pin 5): $\overline{\text{WDO}}$ and $\overline{\text{RST}}$ Active Delay Period Programming Pin. Attach an external capacitor (C_{POR}) to GND to set the period (t_{RST}). See the Applications Information section for more information.

CWDT (Pin 19/Pin 6): Watchdog Timer Programming Pin. Place a capacitor (C_{WDT}) between this pin and ground to adjust the watchdog timer upper (t_{WDU}) and lower (t_{WDL}) boundary periods. See the Applications Information section for more information.

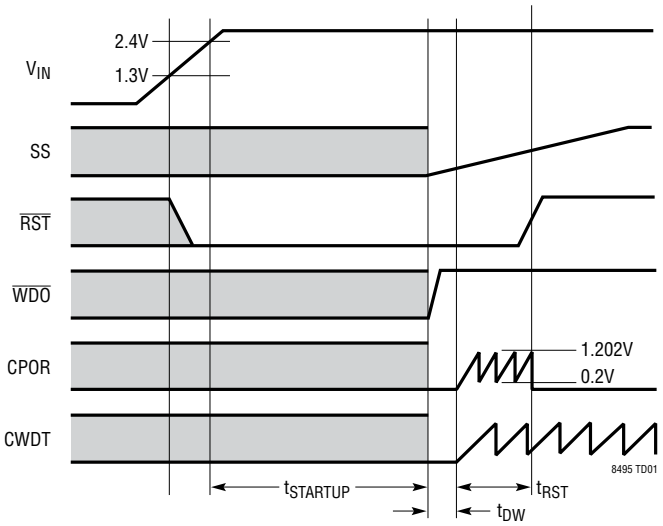
$\overline{\text{RST}}$ (Pin 20/Pin 7): Active Low, Open-Drain Reset. Asserts low when $\overline{\text{RSTIN}}$ is less than ~1.1V (see Electrical Characteristics). After $\overline{\text{RSTIN}}$ rises, $\overline{\text{RST}}$ will remain asserted low for the period (t_{RST}) set by the capacitor on the CPOR pin.

BLOCK DIAGRAM

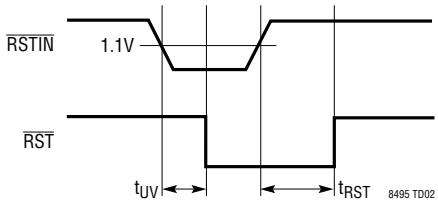


TIMING DIAGRAMS

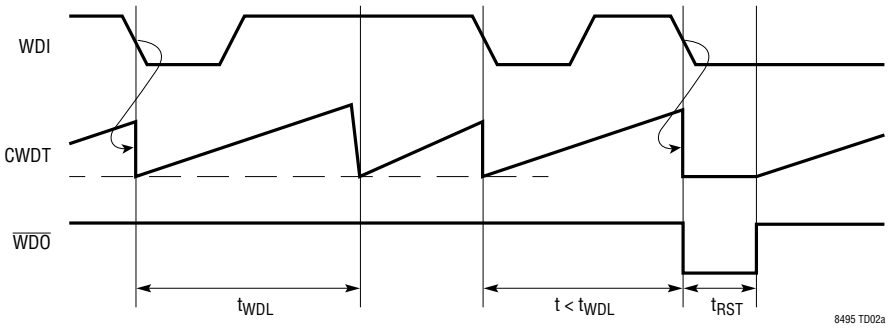
Start-Up Timing



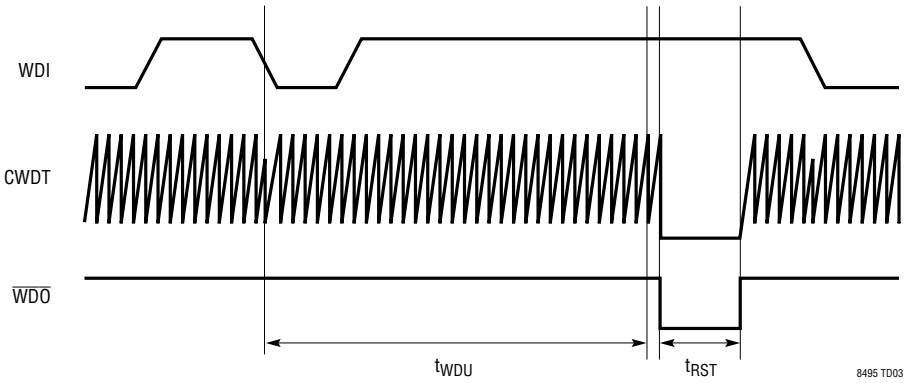
RSTIN Timing



Watchdog Timing, Lower Boundary



Watchdog Timing, Upper Boundary



$t_{STARTUP}$ = TIME REQUIRED TO START UP THE CHIP, APPROXIMATELY 1ms
t_{DW} = TIME REQUIRED TO START UP THE WATCHDOG OR POR TIMER, APPROXIMATELY 200µs
t_{UV} = TIME REQUIRED TO ASSERT $\overline{RST}$ LOW AFTER $\overline{RSTIN}$ GOES BELOW ITS THRESHOLD, APPROXIMATELY 23µs
t_{RST} = PROGRAMMED RESET PERIOD
t_{WDU} = WATCHDOG UPPER BOUNDARY PERIOD, APPROXIMATELY 31 RAMPING CYCLES ON CWDT PIN
t_{WDL} = WATCHDOG LOWER BOUNDARY PERIOD, APPROXIMATELY 1 RAMPING CYCLE ON CWDT PIN

OPERATION

The LT8495 is a constant-frequency, current mode SEPIC/boost/flyback regulator with power-on reset and a watchdog timer. Operation can be best understood by referring to the Block Diagram. The switching regulation, watchdog timer and reset detection functions are controlled by the SWEN, WDE and $\overline{\text{RSTIN}}$ pins respectively. If all three pins are grounded, the part enters shutdown with minimal current drawn from the V_{IN} and BIAS sources. If any of these three pins are driven above their respective thresholds, this part is turned on.

Switching Regulator Operation

In the Block Diagram, the adjustable oscillator, with frequency set by the external R_T resistor, enables an RS latch, turning on the internal power switch. An amplifier and comparator monitor the switch current flowing through an internal sense resistor, turning the switch off when this current reaches a level determined by the voltage at VC. An error amplifier adjusts the VC voltage by measuring the output voltage through an external resistor divider tied to the FB pin. If the error amplifier's output voltage (VC) increases, more current is delivered to the output; if the VC voltage decreases, less current is delivered. An active clamp on the VC voltage provides current limit. An internal regulator provides power to the control circuitry.

In order to improve efficiency, the NPN power switch driver (see Block Diagram) supplies NPN base current from whichever of V_{IN} and BIAS has the lower supply voltage. However, if either of them is below 2.4V or above 34V (typical values), the power switch draws current from the other pin. If both supply pins are below 2.4V or above 34V then switching activity is stopped.

To further optimize efficiency, the LT8495 automatically enters Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the V_{IN}/BIAS pin supply currents to be less than 3µA to 6µA typically (see Electrical Characteristics table).

Start-Up Operation

Several functions are provided to enable a very clean start-up for the LT8495.

- First, the SWEN pin voltage is monitored by an internal voltage reference to give a precise turn-on threshold. An external resistor divider can be connected from the input power supply to the SWEN pin to provide a user-programmable undervoltage lock-out function.
- Second, the soft-start circuitry provides for a gradual ramp-up of the switch current. When the part is brought out of shutdown, the external SS capacitor is first discharged, and then an integrated 256k resistor pulls the SS pin up to ~2.1V. By connecting an external capacitor to the SS pin, the voltage ramp rate on the pin can be set. Typical values for the soft-start capacitor range from 100nF to 1µF.
- Finally, the frequency foldback circuit reduces the maximum switching frequency when the FB pin is below 1V. This feature reduces the minimum duty cycle that the part can achieve thus allowing better control of the switch current during start-up.

Power-On Reset and Watchdog Timer Operation

The LT8495 has a power-on reset (POR) circuit and a reset timer to assert the $\overline{\text{RST}}$ pin for a minimum amount of time. After initial power up the open-drain $\overline{\text{RST}}$ pin is asserted low for a programmable reset delay time (see the Timing Diagrams). During normal operation, the $\overline{\text{RST}}$ pin can also be asserted when either the $\overline{\text{RSTIN}}$ pin is below its threshold or the chip enters shutdown due to an abnormal condition. After the chip exits shutdown and the $\overline{\text{RSTIN}}$ pin rises above its threshold, the $\overline{\text{RST}}$ pin is released after the reset delay time which is programmable through the CPOR pin.

The watchdog timer typically monitors a microcontroller's activity. The watchdog timer can be enabled or disabled by applying a logic signal to the WDE pin. When enabled, the watchdog timer requires successive negative edges on the WDI pin to happen within a programmed time window to keep $\overline{\text{WDO}}$ from pulsing low. Therefore, if the time between the two negative WDI edges is too short or too long, the $\overline{\text{WDO}}$ pin will be pulsed low. When the $\overline{\text{WDO}}$ pin pulls low, a reset timer keeps the $\overline{\text{WDO}}$ pin low for a delay programmed by the CPOR pin. The $\overline{\text{WDO}}$ pin will go high again after the reset timer expires or the chip shuts down (see the Timing Diagrams). The window periods can be set through the CWDT pin.

APPLICATIONS INFORMATION

Low Ripple Burst Mode Operation

To enhance efficiency at light loads, the LT8495 regulator enters low ripple Burst Mode operation keeping the output capacitor charged to the proper voltage while minimizing the input quiescent current. During Burst Mode operation, the LT8495 regulator delivers single-cycle bursts of current to the output capacitor with each followed by a sleep period where the output power is delivered to the load by the output capacitor. The quiescent currents of V_{IN}/BIAS are reduced to less than 3µA to 6µA typically during the sleep time (see Electrical Characteristics table).

As the load current decreases towards a no-load condition, the frequency of single current pulses decreases (see Figure 1), therefore the percentage of time that the LT8495 operates in sleep mode increases, resulting in reduced average input current and thus high efficiency even at very low loads.

By maximizing the time between pulses, the LT8495 quiescent current is minimized. Therefore, to optimize the quiescent current performance at light loads, the current in the feedback resistor divider and the reverse current in the external diode must be minimized, as these appear to the output as load currents. More specifically, during the sleep time, the boost converter has the reverse diode leakage current conducting from output to input, while the SEPIC converter has leakage current conducting from output to ground. Use the largest possible feedback resistors and a low leakage Schottky diode in applications with ultralow Q current.

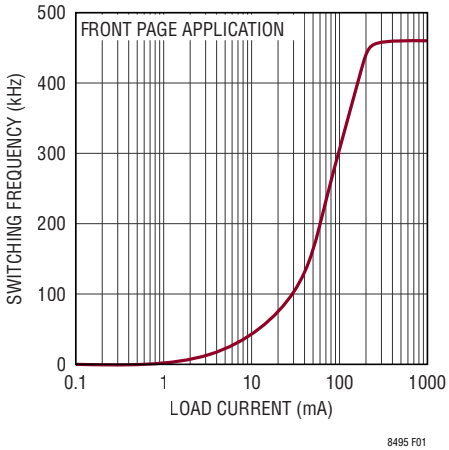


Figure 1. Switching Frequency in Burst Mode Operation

In Burst Mode operation, the burst frequency and the charge delivered with each pulse will not change with output capacitance. Therefore, the output voltage ripple will be inversely proportional to the output capacitance. In a typical application with a 47µF output capacitor, the output ripple is about 10mV and with two 47µF output capacitors the output ripple is about 5mV (see Switching Waveforms, Burst Mode Operation in Typical Performance Characteristics section). The output voltage ripple can continue to be decreased by increasing the output capacitance.

At higher output loads the LT8495 regulator runs at the frequency programmed by the R_T resistor and operates as a standard current mode regulator. The transition between high current mode and low ripple Burst Mode operation is seamless, and will not disturb the output voltage.

Chip Enable Pins

The SWEN, WDE and $\overline{\text{RSTIN}}$ pins are used to enable various portions of the LT8495. The lowest current state is when all three pins are at 0V which disables all functions of the LT8495. Raising any of these pins above their respective input threshold voltages (see Electrical Characteristics section) activates the core circuits of the LT8495. Start-up of the LT8495 core circuits typically requires about 1ms (see the Timing Diagram). See the sections Enabling the Switching Regulator, Watchdog Timer, and Reset Conditions for further details about SWEN, WDE and $\overline{\text{RSTIN}}$ respectively.

Enabling the Switching Regulator

The SWEN pin is used to enable or disable the switching regulator. This pin operates independently of the watchdog enable (WDE) and the $\overline{\text{RST}}$ control input ($\overline{\text{RSTIN}}$). The rising threshold of SWEN is typically 1V, with 30mV of hysteresis. The switching regulator is disabled by driving the SWEN pin below this threshold which deactivates the NPN power switch. The switching regulator is enabled by

APPLICATIONS INFORMATION

driving SWEN above its threshold. Before active switching begins, the soft-start capacitor is quickly discharged then slowly charged causing a gradual start-up of the regulator. SWEN can be connected to V_{IN} if "always on" operation is desired, although some current will flow into the SWEN pin (see Typical Performance Characteristics) increasing overall bias current of the system. Also, a resistor divider can be connected to SWEN to create an undervoltage lockout function (see Undervoltage Lockouts) for more information.

Setting the Output Voltage

The output voltage is programmed with a resistor divider from output to the FB pin (R2) and from the FB pin to ground (R1). Choose the 1% resistors according to:

$$R2 = R1\left(\frac{V_{OUT}}{1.202} - 1\right)$$

Note that choosing larger resistors decreases the quiescent current of the application circuits. In low load applications, choosing larger resistors is more critical since the part enters Burst Mode operation with lower quiescent current.

Power Switch Duty Cycle

In order to maintain loop stability and deliver adequate current to the load, the power NPN (Q1 in the Block Diagram) cannot remain "on" for 100% of each clock cycle. The maximum allowable duty cycle is given by:

$$DC_{MAX} = \frac{T_P - \text{Minimum Switch Off-Time}}{T_P} \bullet 100\%$$

where T_P is the clock period and the Minimum Switch Off-Time (found in the Electrical Characteristics) is typically 70ns.

Conversely, the power NPNs (Q1 in the Block Diagram) cannot remain "off" for 100% of each clock cycle, and will turn on for a minimum time (Minimum Switch On-Time) when in regulation. This Minimum Switch On-Time governs the minimum allowable duty cycle given by:

$$DC_{MIN} = \frac{\text{Minimum Switch On-Time}}{T_P} \bullet 100\%$$

where T_P is the clock period and Minimum Switch On-Time (found in the Electrical Characteristics) is typically 95ns.

The application should be designed such that the operating duty cycle (DC) is between DC_{MIN} and DC_{MAX}. Normally, DC rises with higher V_{OUT} and lower V_{IN}.

Duty cycle equations for both boost and SEPIC topologies are given below, where V_D is the diode forward voltage drop and V_{CESAT} is typically 340mV at 1.2A.

For the boost topology:

$$DC \cong \frac{V_{OUT} - V_{IN} + V_D}{V_{OUT} + V_D - V_{CESAT}}$$

For the SEPIC topology:

$$DC \cong \frac{V_{OUT} + V_D}{V_{IN} + V_{OUT} + V_D - V_{CESAT}}$$

The LT8495 can be used in configurations where the duty cycle is higher than DC_{MAX}, but it must be operated in the discontinuous conduction mode or Burst Mode operation so that the effective duty cycle is reduced.

Setting the Switching Frequency

The LT8495 uses a constant frequency PWM architecture that can be programmed to switch from 250kHz to 1.5MHz by using a resistor tied from the RT pin to ground. Table 1 shows the necessary R_T values for various switching frequencies.

Table 1. Switching Frequency vs R_T Value

SWITCHING FREQUENCY (MHz)	R_T VALUE (kΩ)
0.25	324
0.4	196
0.6	124
0.8	88.7
1.0	68.1
1.2	54.9
1.4	45.3
1.5	41.2

APPLICATIONS INFORMATION

Inductor Selection

General Guidelines: The high frequency operation of the LT8495 allows for the use of small surface mount inductors. For high efficiency, choose inductors with high frequency core material, such as ferrite, to reduce core losses. To improve efficiency, choose inductors with more volume for a given inductance. The inductor should have low DCR (copper wire resistance) to reduce I^2R losses, and must be able to handle the peak inductor current without saturating. Note that in some applications, the current handling requirements of the inductor can be lower, such as in the SEPIC topology when using uncoupled inductors, where each inductor only carries a fraction of the total switch current. Molded chokes or chip inductors usually do not have enough core area to support peak inductor currents in the 2A to 3A range. To minimize radiated noise, use a toroidal or shielded inductor. Note that the inductance of shielded types will drop more as current increases, and will saturate more easily.

Minimum Inductance: Although there can be a trade-off with efficiency, it is often desirable to minimize board space by choosing smaller inductors. When choosing an inductor, there are two conditions that limit the minimum inductance; (1) providing adequate load current, and (2) avoidance of subharmonic oscillation. Choose an inductance that is high enough to meet both of these requirements.

Adequate Load Current: Small value inductors result in increased ripple currents and thus, due to the limited peak switch current, decrease the average current that can be provided to a load (I_{OUT}). In order to provide adequate load current, L should be at least:

$$L > \frac{DC \bullet V_{IN}}{2(f)\left(I_{LIM} - \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet \eta}\right)}$$

For boost topologies, or:

$$L > \frac{DC \bullet V_{IN}}{2(f)\left(I_{LIM} - \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet \eta} - I_{OUT}\right)}$$

for the SEPIC topologies.

where:

L = L1||L2 for uncoupled SEPIC topology

DC = switch duty cycle (see previous section)

I_{LIM} = switch current limit, typically about 2.35A at 50% duty cycle (see the Typical Performance Characteristics section)

η = power conversion efficiency (typically 85% to 90% for boost and 80% to 85% for SEPIC at high currents)

f = switching frequency

Negative values of L indicate that the output load current I_{OUT} exceeds the switch current limit capability of the LT8495.

Avoiding Subharmonic Oscillations: The internal slope compensation circuit of LT8495 helps prevent the subharmonic oscillations that can occur when the duty cycle is greater than 50%, provided that the inductance exceeds a minimum value. In applications that operate with duty cycles greater than 50%, the inductance must be at least:

$$L > \frac{(V_{IN} - V_{CESAT}) \bullet (2DC - 1)}{0.76 \bullet (1.5 \bullet DC + 1) \bullet f \bullet (1 - DC)}$$

for boost and coupled inductor SEPIC, or:

$$L1||L2 > \frac{(V_{IN} - V_{CESAT}) \bullet (2DC - 1)}{0.76 \bullet (1.5 \bullet DC + 1) \bullet f \bullet (1 - DC)}$$

for the uncoupled inductor SEPIC topologies.

Maximum Inductance: Excessive inductance can reduce current ripple to levels that are difficult for the current comparator (A2 in the Block Diagram) to cleanly discriminate, thus causing duty cycle jitter and/or poor regulation. The maximum inductance can be calculated by:

$$L_{MAX} = \frac{V_{IN} - V_{CESAT}}{I_{MIN(RIPPLE)}} \bullet \frac{DC}{f}$$

where L_{MAX} is L1||L2 for uncoupled SEPIC topologies and $I_{MIN(RIPPLE)}$ is typically 150mA.

APPLICATIONS INFORMATION

Current Rating: Finally, the inductor(s) must have a rating greater than its peak operating current to prevent inductor saturation resulting in efficiency loss.

In steady state, the peak and average input inductor currents (continuous conduction mode only) is given by:

$$I_{L1(PEAK)} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet \eta} + \frac{V_{IN} \bullet DC}{2 \bullet L1 \bullet f}$$

$$I_{L1(AVG)} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet \eta}$$

for the boost and uncoupled inductor SEPIC topology.

For uncoupled SEPIC topologies, the peak and average currents of the output inductor L2 is given by:

$$I_{L2(PEAK)} = I_{OUT} + \frac{V_{OUT} \bullet (1-DC)}{2 \bullet L2 \bullet f}$$

$$I_{L2(AVG)} = I_{OUT}$$

For the coupled inductor SEPIC:

$$I_{L(PEAK)} = I_{OUT} \bullet \left[1 + \frac{V_{OUT}}{V_{IN} \bullet \eta}\right] + \frac{V_{IN} \bullet DC}{2 \bullet L \bullet f}$$

$$I_{L(AVG)} = I_{OUT} \bullet \left[1 + \frac{V_{OUT}}{V_{IN} \bullet \eta}\right]$$

Note: Inductor current can be higher during load transients. It can also be higher during short circuit and start-up if inadequate soft-start capacitance is used. Thus, $I_{L(PEAK)}$ may be higher than the switch current limit of 2.95A, and the RMS inductor current is approximately equal to $I_{L(AVG)}$. Choose an inductor having sufficient saturation current and RMS current ratings.

Capacitor Selection

Low ESR (equivalent series resistance) capacitors should be used at the output to minimize the output ripple voltage. Multilayer ceramic capacitors are an excellent choice, as they have an extremely low ESR and are available in very small packages. X5R or X7R dielectrics are preferred, as these materials retain their capacitance over wider voltage and temperature ranges. Always use a capacitor with a sufficient voltage rating. Many capacitors rated at 2.2µF to 20µF, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired output voltage. Solid tantalum or OS-CON capacitors can be used, but they will occupy more board area than a ceramic and will have a higher ESR with greater output ripple.

Ceramic capacitors also make a good choice for the input decoupling capacitor, which should be placed as closely as possible to the V_{IN} and BIAS pins of the LT8495. A 2.2µF to 4.7µF input capacitor is sufficient for most applications.

Audible Noise

Ceramic capacitors are small, robust and have very low ESR. However, due to their piezoelectric nature, ceramic capacitors can sometimes create audible noise when used with the LT8495. During Burst Mode operation, the LT8495 regulator's switching frequency depends on the load current, and at very light loads the regulator can excite the ceramic capacitor at audio frequencies, generating audible noise. Since LT8495 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output.

Diode Selection

The diode used in boost or SEPIC topologies conducts current only during switch off-time. During switch on-time, the diode has reverse voltage across it. The peak reverse voltage is equal to V_{OUT} in the boost topology and equal to (V_{OUT} + V_{IN}) in the SEPIC topology. Use a diode with a reverse voltage rating greater than the peak reverse voltage.

An additional consideration is the reverse leakage current. The leakage current appears to the output as load current and affects the efficiency, most noticeably, under light load conditions. In Burst Mode operation, after the inductor current vanishes, the reverse voltage across the boost diode is approximately equal to $V_{OUT} - V_{IN}$ in the boost topology and V_{OUT} in the SEPIC topology. The percentage of time that the diode is reverse biased increases as load current decreases.

Schottky diodes that have larger forward voltages often have less leakage, so a trade-off exists between light load and high load efficiency. Also the Schottky diodes with larger reverse bias ratings may have less leakage at a given output voltage, therefore, superior leakage performance can be

APPLICATIONS INFORMATION

achieved at the expense of diode size. Finally, keep in mind that the leakage current of a power Schottky diode goes up exponentially with junction temperature. Therefore, the Schottky diode must be selected with care to avoid excessive increase in light load supply current at high temperatures.

Soft-Start

The LT8495 contains a soft-start circuit to limit peak switch currents during start-up. High start-up current is inherent in switching regulators since the feedback loop is saturated due to V_{OUT} being far from its final value. The regulator tries to charge the output capacitor as quickly as possible, which results in large peak currents. The start-up current can be limited by connecting an external capacitor (typically 100nF to 1µF) to the SS pin. This capacitor is slowly charged to ~2.1V by an internal 256k resistor once the part is activated. SS pin voltages below ~0.8V reduce the internal current limit. Thus, the gradual ramping of the SS voltage also gradually increases the current limit as the capacitor charges. This, in turn, allows the output capacitor to charge gradually toward its final value while limiting the start-up current. When the switching regulator shuts down the soft-start capacitor is automatically discharged to ~100mV or less before charging resumes, thus assuring that the soft-start occurs after every reactivation of the switching regulation.

Power Supplies and Operating Limits

The LT8495 draws supply current from the V_{IN} and BIAS pins. The largest supply current draw occurs when the switching regulator is enabled (SWEN is high) and the power switch is toggling on and off. Under light load conditions the switching regulator enters Burst Mode operation where the power switch toggles infrequently and the input current is significantly reduced (see the Low Ripple Burst Mode Operation section).

Power Switch Driver (PSD) Operating Range: The NPN power switch is driven by a power switch driver (PSD) as shown in the Block Diagram. The driver must be powered by a supply (V_{IN} or BIAS) that is above the minimum operating voltage and below the PSD overvoltage threshold. These voltages are typically 2.4V and 34V respectively (see Electrical Characteristics).

If neither V_{IN} nor BIAS is within this operating range, the PSD and the switching regulator are automatically disabled. Voltages up to 60V are not harmful to the PSD, however, as discussed, switching regulation is automatically disabled when neither V_{IN} nor BIAS is in the valid operating range. See Table 2 for some example operating conditions.

Reset and Watchdog Operating Voltage Limits: The reset circuits operate properly as long as either V_{IN} or BIAS is above 1.3V (see Reset Conditions section). The watchdog timer operates properly when either V_{IN} or BIAS is between 2.5V and 60V. The table below gives some example operating conditions.

Table 2: Operating Condition Examples

V_{IN} (V)	BIAS (V)	RESET CIRCUITS	WATCHDOG	SWITCHING REGULATOR
0	1.3	X		
1.3	0	X		
1	40	X	X	
40	40	X	X	
1	30	X	X	X
12	40	X	X	X

Automatic Power Supply Selection: In order to minimize power loss, the LT8495 draws as much of its required current as possible from the lowest suitable voltage supply (V_{IN} or BIAS) in accordance with the requirements described in the previous two sections. This selection is automatic and can change as V_{IN} and/or BIAS voltages change.

The LT8495 compares the V_{IN} and BIAS voltages to determine which is lower. The comparator has an offset and hysteresis as shown in the Electrical Characteristics section. The voltage comparison happens continuously when the power switch is toggling. The result of the latest comparison is latched inside the LT8495 when switching stops. If the power switch is not toggling, the LT8495 uses the last V_{IN} vs BIAS comparison to determine which supply is lower. After initial power up or any thermal lockout the LT8495 always concludes that V_{IN} is the lower supply voltage until subsequent voltage comparisons can be made while the power switch is toggling.

BIAS Connection for SEPIC Converters: For SEPIC converters, where V_{IN} can be above or below V_{OUT}, BIAS is typically connected to V_{OUT} which improves efficiency when

APPLICATIONS INFORMATION

V_{IN} voltage is higher than V_{OUT}. Connecting BIAS to V_{OUT} in a SEPIC topology also allows the switching regulator to operate with V_{IN} above 34V (typical switch driver overvoltage threshold) in cases where V_{OUT} is regulated below the PSD overvoltage threshold. Finally, connecting BIAS to V_{OUT} also allows the converter to operate from V_{IN} voltages less than 2.5V after V_{OUT} rises within the PSD operating range. This can be very useful in battery powered applications since the battery voltage drops as it discharges.

BIAS Connection for Boost Converters: For boost converters, BIAS is typically connected to V_{OUT} or to ground. Connecting BIAS to V_{OUT} allows the converter to operate with $V_{IN} < 2.5V$ after V_{OUT} has risen within the PSD operating range. However, during no load conditions on V_{OUT}, despite V_{IN} being selected as the primary input supply, the overall power loss will be slightly elevated due to the small amount of current still being drawn from the higher voltage BIAS pin. To minimize boost converter power loss during no load conditions, connect BIAS instead to ground.

For boost applications with V_{OUT} higher than the PSD operating range, the BIAS pin should not typically be connected to V_{OUT}. The LT8495 will never draw the majority of its current from BIAS due to the excessive voltage, therefore this connection does not help to improve efficiency. Alternative choices for the BIAS pin connection are ground or another supply that is within the PSD operating range.

Maximum V_{IN} for Boost Converters: V_{IN} cannot generally be higher than V_{OUT} in boost topologies because of the DC path from V_{IN} to V_{OUT} though the inductor and the output diode. If V_{IN} must be higher than V_{OUT}, then the inductor must be powered by a separate supply that is always below V_{OUT}. Otherwise a SEPIC topology can be used.

Also, the LT8495 will not operate in a boost topology with V_{IN} voltages above the PSD operating range unless BIAS is connected to an alternative supply within the valid operating range.

V_{IN}/BIAS Ramp Rate: While initially powering a switching converter application, the V_{IN}/BIAS ramp rate should be limited. High V_{IN}/BIAS ramp rates can cause excessive inrush currents in the passive components of the converter. This can lead to current and/or voltage overstress and may damage the passive components or the chip. Ramping rates less than 500mV/µs, depending on component parameters, will generally prevent these issues. Also, be careful to avoid hot plugging. Hot plugging occurs when an active voltage supply is "instantly" connected or switched to the input of the converter. Hot plugging results in very fast input ramp rates and is not recommended. Finally, for more information, refer to Linear Application Note 88, which discusses voltage overstress that can occur when inductive source impedance is hot plugged to an input pin bypassed by ceramic capacitors.

Watchdog Timer

The LT8495 includes an adjustable watchdog timer that can monitor a microcontroller activity. If a code execution error occurs, the watchdog timer can detect this and pull the open drain $\overline{WDO}$ pin low. $\overline{WDO}$ can be connected to $\overline{RST}$ or to another input of the microcontroller to reset or interrupt the microcontroller. Note that the pull-up resistor must be connected to $\overline{WDO}$ for proper operation. This resistor is often already integrated in the microcontroller.

The watchdog circuitry monitors negative edges on the WDI pin. The WDI pin's negative going pulses are restricted to appear inside a programmed time window to prevent $\overline{WDO}$ from going low. During a code execution error, the microcontroller will generate WDI pulses that are either too fast or too slow which will cause $\overline{WDO}$ to assert low and force the microcontroller to reset the program (see the Timing Diagram section).

While monitoring WDI, if the time between any two falling edges is shorter than the watchdog lower boundary, t_{WDL} (see Figure 2), or longer than the watchdog upper boundary, t_{WDU} (see Figure 3), $\overline{WDO}$ is pulled down for a programmable period of t_{RST} (see Reset Conditions section).

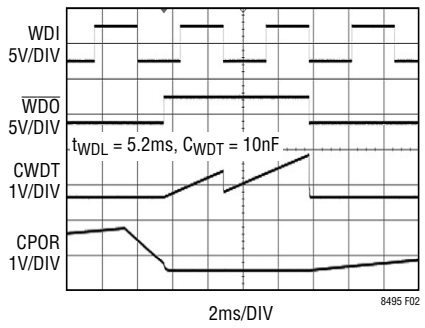


Figure 2. Window Watchdog Waveforms

APPLICATIONS INFORMATION

Thus, the WDI period should be higher than t_{WDL}, and lower than t_{WDU} to keep $\overline{WDO}$ high under normal conditions. $\overline{WDO}$ also pulls low if no negative WDI edge occurs during the watchdog upper boundary period.

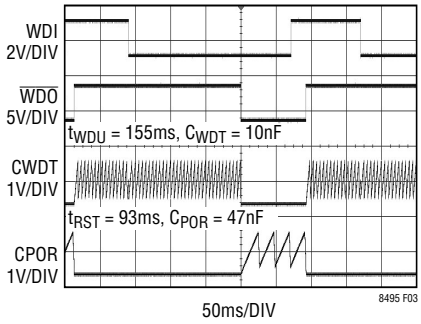


Figure 3. Timeout Watchdog Waveforms

Selecting the Watchdog Timing Capacitor: The watchdog timeout period is adjustable and can be optimized for software execution. The watchdog upper and lower boundary timeout periods (t_{WDU} and t_{WDL}) are adjusted by connecting a capacitor, C_{WDT}, between the CWDT pin and ground. t_{WDU} is typically 30 • t_{WDL} for large C_{WDT} values (greater than about 50nF). For lower values this ratio reduces as shown in Figure 6.

To program the t_{WDU} and t_{WDL} periods, see the Watchdog Upper and Lower Boundary Periods vs Capacitance graphs in the Typical Characteristics section to select C_{WDT}. The required capacitor value can also be calculated from a given watchdog timeout period by using the following equation:

$$C_{WDT} = K_1 \bullet t_{WDU}$$

Where C_{WDT} is the external capacitor value in nF, t_{WDU} is the upper boundary period in ms, and K1 is their ratio with typical values shown in Figure 4. K1 can be approximated as 0.065nF/ms for upper boundaries greater than 50ms.

In addition, the following equation can be used to calculate the watchdog lower boundary period for a given C_{WDT} capacitor value.

$$t_{WDL} = K2 \bullet C_{WDT}$$

Where t_{WDL} is the lower boundary in ms, C_{WDT} is the external capacitance in nF, and K2 is their ratio with typical values shown in Figure 5. K2 can be approximated as 0.52ms/nF for C_{WDT} values greater than 10nF.

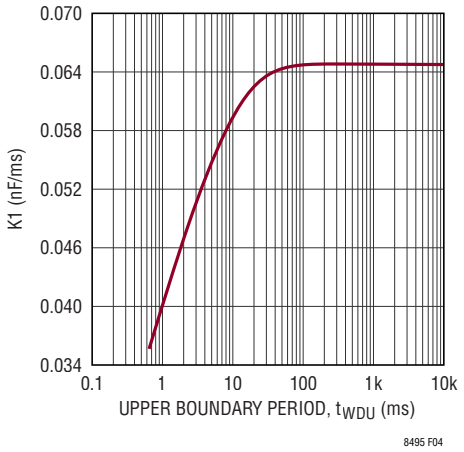


Figure 4. Watchdog Upper Boundary Parameter

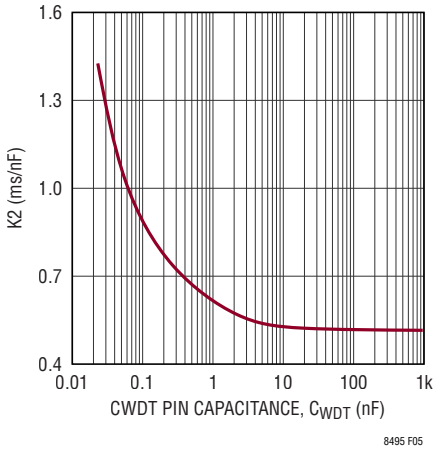


Figure 5. Watchdog Lower Boundary Parameter

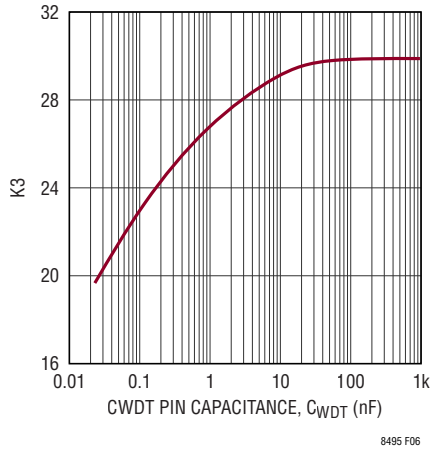


Figure 6. Upper and Lower Boundary Ratio

APPLICATIONS INFORMATION

The watchdog lower boundary period (t_{WDL}) has a fixed relationship to t_{WDU} for a given C_{WDT} capacitance. The t_{WDL} period is related to t_{WDU} by the following relationship:

$$t_{WDU} = K3 \bullet t_{WDL}$$

where K3 is the ratio between upper and lower boundary with typical values shown in Figure 6.

Leaving the CWDT pin unconnected will generate a minimum watchdog timeout of approximately 270µs. Maximum timeout is limited by the largest available low leakage capacitor. The Electrical Characteristics section indicates the guaranteed tolerance of the timeout period for a given capacitance. The accuracy of the timeout period will also be affected by capacitor leakage (the nominal charging current is 2.3µA) and capacitor tolerance. A low leakage ceramic capacitor is recommended.

Watchdog Timer Start-Up: There are several conditions when the WDI pin is not monitored by the watchdog timer. For each condition, the start-up or resumption of WDI pin monitoring occurs as described below:

- The watchdog timer is disabled during the POR or thermal lockout. After POR and thermal lockout are cleared, CWDT will begin ramping from 0V. The WDI edges are ignored while the CWDT charges from 0V to ~200mV.
- The watchdog is disabled when WDE is low. After WDE rises, CWDT may require 1µs to 100µs (typical) before starting to ramp up. The WDI edges are ignored until the CWDT charges from 0V to ~200mV.
- WDI edges are not monitored while $\overline{WDO}$ is asserted low. Four CPOR cycles are required before $\overline{WDO}$ is released and CWDT begins ramping up. The WDI edges are ignored until the CWDT charges from 0V to ~200mV.

If desired, the $\overline{RST}$ pin can be connected to WDE to enable the watchdog timer at about the same time $\overline{RST}$ is released. For the example shown in Figure 7, $\overline{RST}$ is connected to WDE. After the chip starts up, the output voltage ramps up towards 5V for the microcontroller supply. When V_{OUT} rises above 4.5V, and thus $\overline{RSTIN}$ rises above 1.1V, the $\overline{RST}$ and WDE pins will be held low for the additional period of t_{RST}. After t_{RST}, $\overline{RST}$ is released and WDE will pull high, thus enabling the microcontroller and the watchdog timer at about the same time.

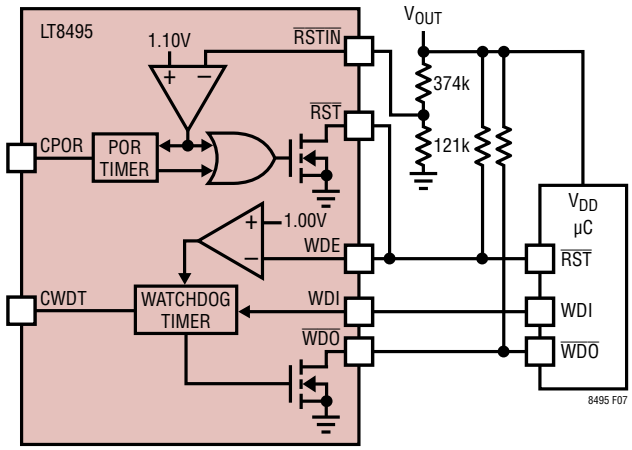


Figure 7. Watchdog Monitoring

Reset Conditions

The LT8495 has three reset conditions as described below. All of these conditions can cause the open-drain $\overline{RST}$ pin to pull low, as long as either V_{IN} or BIAS is above 1.3V. A pull-up resistor can be connected to the $\overline{RST}$ pin so that it can be used as a reset for an external microcontroller or other devices. An adjustable timer delays the release of $\overline{RST}$ by t_{RST} to ensure adequate reset duration for the external devices.

The three reset conditions are as follows:

- **POR:** The $\overline{RST}$ pin is asserted if V_{IN} and BIAS are both below 2.4V (typical). This is the power-on reset condition which causes $\overline{RST}$ to assert upon initial power up of the LT8495 (see Timing Diagrams). Under this condition the switching regulator and watchdog timer are disabled and the C_{WDT}, C_{POR}, and SS capacitors are discharged to ground.
- **Thermal Lockout:** An overtemperature condition on the LT8495 die will cause the $\overline{RST}$ pin to assert low. See High Temperature Considerations section for additional information. This condition disables the switching regulator, the watchdog timer and discharges the C_{WDT}, C_{POR}, and SS capacitors to ground. See Thermal Lockout section for additional information.

APPLICATIONS INFORMATION

- **$\overline{\text{RSTIN}}$ Undervoltage Lockout:** The open-drain $\overline{\text{RST}}$ pin is asserted low if the $\overline{\text{RSTIN}}$ input is below the 1.1V typical threshold (see Electrical Characteristics). This function enables the use of an external resistor divider to configure an under voltage detection circuit. This reset condition has no effect on the switching regulator or the watchdog timer. See the Undervoltage Lockouts section for more information.

A programmable timer delays the release of $\overline{\text{RST}}$ by t_{RST} after all of the above reset conditions are no longer met. Before releasing $\overline{\text{RST}}$, the external C_{POR} capacitor ramps up and down for four cycles creating the t_{RST} delay (see Figure 8). To program the t_{RST} period, see the Reset Timeout Period vs Capacitance graphs in the Typical Characteristics section to select C_{POR}. The required capacitor value can also be calculated from a given reset timeout period by using the following equation:

$$C_{POR} = K4 \bullet t_{RST}$$

where C_{POR} is the external capacitor value in nF. t_{RST} is the reset timeout period in ms, and K4 is their ratio with typical values shown in Figure 9, K4 can be approximated as 0.51nF/ms for reset timeout periods greater than 15ms. As described previously, this same timer is used to determine how long $\overline{\text{WDO}}$ is asserted low during a watchdog timeout.

As an example, to create a 9.5ms t_{RST} timeout period, choose a C_{POR} capacitor value of 4.7nF. Leaving the C_{POR} pin unconnected will generate a t_{RST} period of approximately 40µs. The maximum period is limited by the largest available low leakage capacitor. The Electrical Characteristics section indicates the guaranteed tolerance of the timeout period for a given capacitance. The accuracy of the timeout period will also be affected by capacitor leakage (the nominal charging current is 2.3µA) and capacitor tolerance. A low leakage ceramic capacitor is recommended.

As discussed previously, $\overline{\text{WDO}}$ is asserted low for a period of t_{RST} after a watchdog error occurs. This period is measured by counting four cycles on the CPOR pin in the same way that the reset delay is measured. If a watchdog timeout occurs at the same time as the reset delay period, the watchdog takes priority in the counter. Therefore, $\overline{\text{WDO}}$ is always asserted low for four cycles of the CPOR pin, while the $\overline{\text{RST}}$ delay may be extended beyond four cycles to a maximum of six cycles, thus increasing t_{RST} by up to 50%.

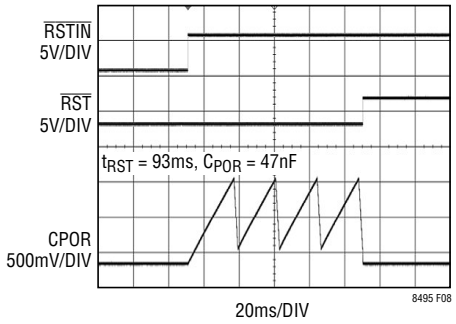


Figure 8. Reset Timer Waveforms

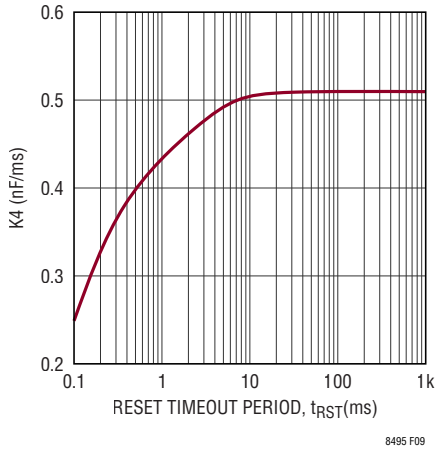


Figure 9. Reset Timer Parameter

Finally note that the t_{RST} delay on the $\overline{\text{RST}}$ pin does not affect the switching regulator or watchdog timer. The switching regulator and/or watchdog timer will start right after the part is no longer in the POR or thermal lockout condition.

Undervoltage Lockouts

Undervoltage lockout (UVLO) functions can be implemented using the SWEN and/or $\overline{\text{RSTIN}}$ pins. An undervoltage lockout can shut down appropriate circuitry to prevent undesired operation when input and/or output voltages are too low.

APPLICATIONS INFORMATION

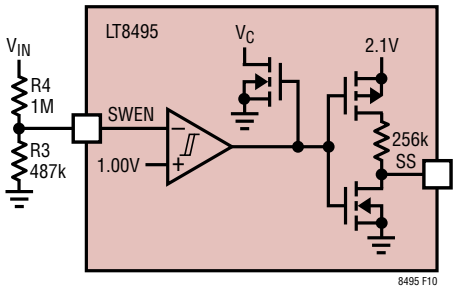


Figure 10. V_{IN} Undervoltage Lockout

Input UVLO: Connecting a resistor divider from V_{IN} to SWEN (see Figure 10) implements an input undervoltage lockout circuit. SWEN has an accurate rising threshold of 1.0V with 30mV of hysteresis (typical–see Electrical Specifications). By connecting a resistor divider from V_{IN} to SWEN, the LT8495 will be programmed to disable the switching regulator when V_{IN} drops below a desired threshold. Typically, this threshold is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The input UVLO prevents the regulator from operating at source voltages where the problems might occur.

As shown in Figure 10, by connecting a resistor divider from V_{IN} to SWEN, the falling undervoltage lockout threshold is set to:

$$V_{IN(UVLO)} = \frac{R3+R4}{R3} \bullet 0.97V$$

From the previous equation, the resistor divider shown in Figure 10 gives the V_{IN} pin a falling undervoltage lockout threshold of 2.96V. When V_{IN} is below this threshold, the switching regulation is disabled and the SS pin starts to discharge. After choosing the value of R3, for example, R4 can be calculated using:

$$R4 = R3 \bullet \left(\frac{V_{IN(UVLO)}}{0.97} - 1 \right) \Omega$$

Output UVLO: Connecting the $\overline{RST}$ and $\overline{RSTIN}$ pins as shown in Figures 11 and 12 implements an output undervoltage lock out (UVLO) circuit. This circuit resets V_{OUT} powered devices when V_{OUT} is below a desired voltage by asserting the open drain $\overline{RST}$ pin low. Note that a pull-up resistor is required on the $\overline{RST}$ pin, but might already be integrated in the µC. There is typically a 23µs delay from the $\overline{RSTIN}$ pin falling edge until $\overline{RST}$ is asserted low (see Electrical Characteristics section) for glitch immunity of the $\overline{RSTIN}$ pin. After $\overline{RSTIN}$ rises above its threshold, $\overline{RST}$ continues to be asserted low for a delayed time programmable by the CPOR pin capacitor.

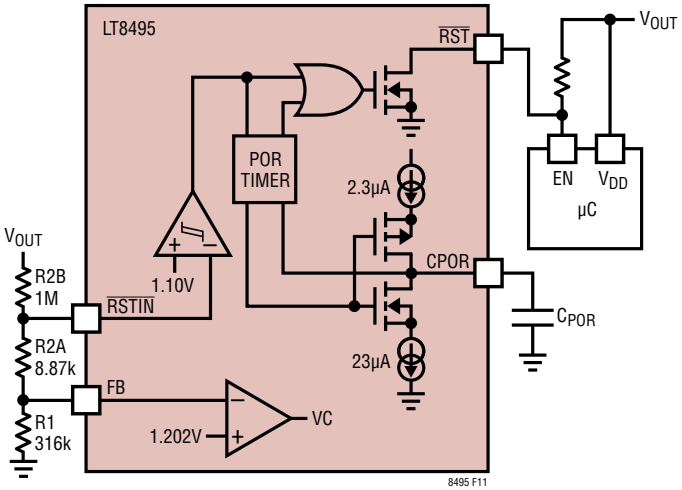


Figure 11. $\overline{RSTIN}$ Reset Lockout

As shown in Figure 12, the R2 resistor (calculated in the Setting the Output Voltage section) is divided into two resistors, R2A & R2B to implement the UVLO function. Next, the following equations are used to calculate their values.

$$R2A = R1 \bullet \left(\frac{92\%}{UVLO\%_{NOM}} - 1 \right)$$

$$R2B = R2 - R2A$$

where $UVLO\%_{NOM}$ is the desired nominal UVLO threshold voltage as a percentage of the nominal V_{OUT}. $UVLO\%_{NOM}$ is recommended to be 89.5% or less for most applications. Continue reading for more information about selecting $UVLO\%_{NOM}$.

APPLICATIONS INFORMATION

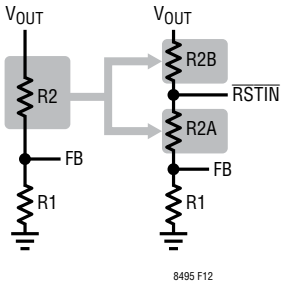


Figure 12. $\overline{\text{RSTIN}}$ Pin Connection Options

When choosing UVLO%$_{NOM}$, consider that the transient response to V_{OUT} load current steps may cause undershoot of V_{OUT}. Excessive V_{OUT} undershoot can cause $\overline{\text{RSTIN}}$ to drop below the comparator threshold and activate $\overline{\text{RST}}$. The following equation includes the maximum $\overline{\text{RSTIN}}$ comparator threshold (97% of the FB reference - see Electrical Characteristics) to show what the maximum UVLO threshold can be.

$$UVLO\%_{MAX} = UVLO\%_{NOM} \bullet \frac{97}{92}$$

For example, when choosing UVLO%$_{NOM}$ = 89.5%, UVLO%$_{MAX}$ = 94.36% of V_{OUT}. Therefore the $\overline{\text{RST}}$ pin may assert if V_{OUT} undershoots more than 5.64% below its steady-state regulated voltage. Choose a lower UVLO%$_{NOM}$ if more margin is required.

In addition, the choice of UVLO%$_{NOM}$ affects the minimum possible V_{OUT} voltage before $\overline{\text{RST}}$ is asserted.

$$UVLO\%_{MIN} = UVLO\%_{NOM} \bullet \frac{86}{92}$$

For example, when using UVLO%$_{NOM}$ = 89.5%, UVLO%$_{MIN}$ = 83.66% of V_{OUT}. Therefore the $\overline{\text{RST}}$ pin may not assert unless V_{OUT} is 16.34% below its nominal value. Note that in terms of absolute V_{OUT} UVLO voltage one must also consider the tolerance of the FB regulation voltage and the R1, R2A and R2B resistor tolerances.

In the example shown in Figure 11, V_{OUT} is regulated to 5V. For a desired UVLO% of 89.5%, the calculated R1, R2A, and R2B values are 316k, 8.87k, and 1M respectively.

POR UVLO: When both V_{IN} and BIAS are too low for proper LT8495 operation (typically <2.4V), the switching regulator and watchdog timers are disabled. For more information see the Reset Conditions section.

High Temperature Considerations

For higher ambient temperatures, care should be taken in the layout of the PCB to ensure good heat sinking of the LT8495. The exposed pad on the bottom of the package must be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will spread heat dissipated by the LT8495. Placing additional vias can reduce thermal resistance further. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating. Power dissipation within the LT8495 is estimated by calculating the total power loss from an efficiency measurement and subtracting the diode loss, FB resistor loss and inductor loss. The die temperature is calculated by multiplying the LT8495 power dissipation by the thermal resistance from junction to ambient.

The power switch and its driver dissipate the most power in the LT8495 (see Block Diagram). Higher switch current, duty cycle and output voltage result in higher die temperature. Power loss in the Power Switch Driver also increases with higher input supply voltage. The PSD is supplied by the lowest suitable voltage on V_{IN} and BIAS. Connecting BIAS to a low voltage supply, often V_{OUT}, can reduce the maximum die temperature of the LT8495 (see Automatic Power Supply Selection section).

Also note that leakage current into the SWEN, RSTIN, WDE, and FB pins increases at high junction temperatures (see Typical Performance Characteristics). The potential leakage current should be considered when choosing high value resistors connected to those pins.

Thermal Lockout: If the die temperature reaches approximately 165°C, the part will go into thermal lockout and the chip will be reset. The part will be enabled again when the die temperature has dropped by ~5°C (nominal). See the Reset Conditions section for more details about the chip's state during thermal lockout

Fault Tolerance

The LT8495 is designed to tolerate single fault condition in the TSSOP package. Shorting two adjacent pins together or leaving one single pin floating does not raise V_{OUT} or cause damage to the LT8495 regulator.

APPLICATIONS INFORMATION

Table 3 and Table 4 show the effects that result from shorting adjacent pins and from a floating pin, respectively. The NC pins must be left floating to ensure fault tolerance. For the best fault tolerance to inadvertent adjacent pin shorts, the BIAS pin must be tied to something higher than 1.230V or to the output to avoid overvoltage during a short from FB to BIAS.

Table 3. Effects of Pin Shorts (TSSOP)

PIN NAMES	PIN #	EFFECT ON OUTPUT
FB-BIAS	1-2	Output voltage will fall to approximately 1.202V if BIAS is connected to the output.
CPOR-CWDT	5-6	No effect on output.
CWDT-$\overline{RST}$	6-7	No effect on output.
$\overline{RST}$-SS	7-8	No effect or output will fall below regulation.
$\overline{RSTIN}$-SWEN	11-12	No effect on output.
SWEN-WDE	12-13	No effect on output.
WDE-GND	13-14	No effect on output.
GND-$\overline{WDO}$	14-15	No effect on output.
$\overline{WDO}$-WDI	15-16	No effect on output.

Table 4.Effects of Floating Pins (TSSOP)

PIN NAME	PIN #	EFFECT ON OUTPUT
BIAS	1	Depending on the V_{IN} voltage and the circuit topology, floating this pin will degrade device performance or the output will fall below regulation.
FB	2-3	No effect if the other FB pad is soldered.
CPOR	5	No effect on output.
CWDT	6	No effect on output.
$\overline{RST}$	7	No effect on output.
SS	8	No effect after part has started. Can potentially lead to an increase of inrush current during start-up.
RT	10	Output may fall below regulation.
$\overline{RSTIN}$	11	No effect on output.
SWEN	12	Enable state of the pin becomes undefined. Output will not exceed regulation voltage.
WDE	13	No effect on output.
GND	14	No effect if Exposed Pad is soldered.
$\overline{WDO}$	15	No effect on output.
WDI	16	No effect on output.
V_{IN}	18	Depending on the BIAS voltage and the circuit topology, floating this pin will degrade device performance or the output will fall below regulation.
SW	10	Output will fall below regulation voltage.
Exposed Pad	21	Output maintains regulation, but potential degradation of device performance.

Layout Hints

As with all high frequency switchers, when considering layout, care must be taken to achieve optimal electrical, thermal and noise performance. One will not get advertised performance with a careless layout. For maximum efficiency, switch rise and fall times are typically in the 5ns to 10ns range. To prevent noise, both radiated and conducted, the high speed switching current paths, shown in Figures 13 & 14, must be kept as short as possible. This is implemented in the suggested PCB layouts in Figures 15 & 16. Shortening this path will also reduce the parasitic trace inductance. At switch-off, this parasitic inductance produces a flyback spike across the LT8495 switch. When operating at higher currents and output voltages, with poor layout, this spike can generate voltages across the LT8495 that may exceed its absolute maximum rating. A ground plane should also be used under the switcher circuitry to prevent interplane coupling and overall noise. The FB components should be kept as far away as practical from the switch node. The ground for these components should be separated from the switch current path. Failure to do so can result in poor stability or subharmonic oscillation.

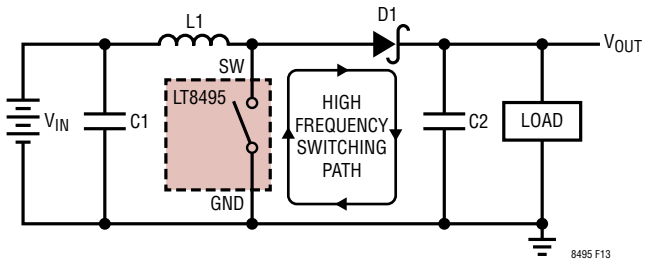


Figure 13. High Speed Chopped Switching Path for Boost Topology

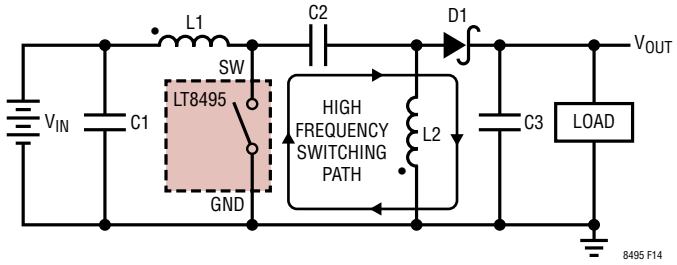


Figure 14. High Speed Chopped Switching Path for SEPIC Topology

APPLICATIONS INFORMATION

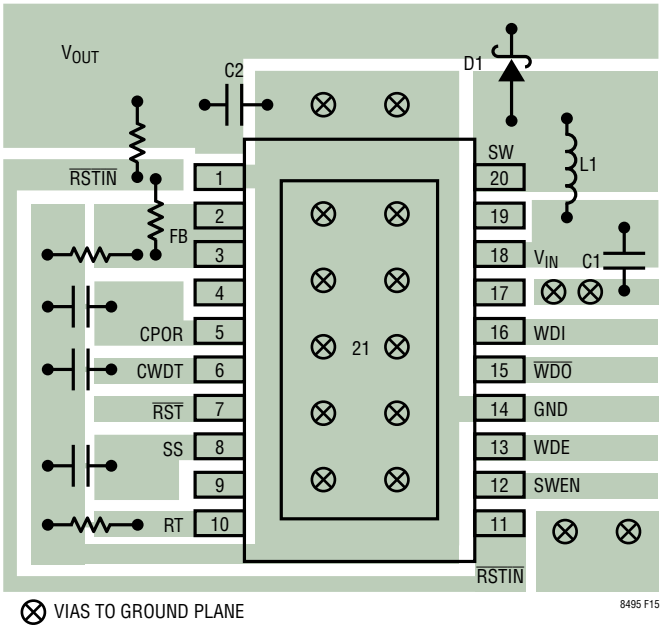


Figure 15. Suggested Component Placement for Boost Topology. Pin 21 (Exposed Pad) Must Be Soldered Directly to the Local Ground Plane for Adequate Thermal Performance. Multiple Vias to Additional Ground Planes Will Improve Thermal Performance

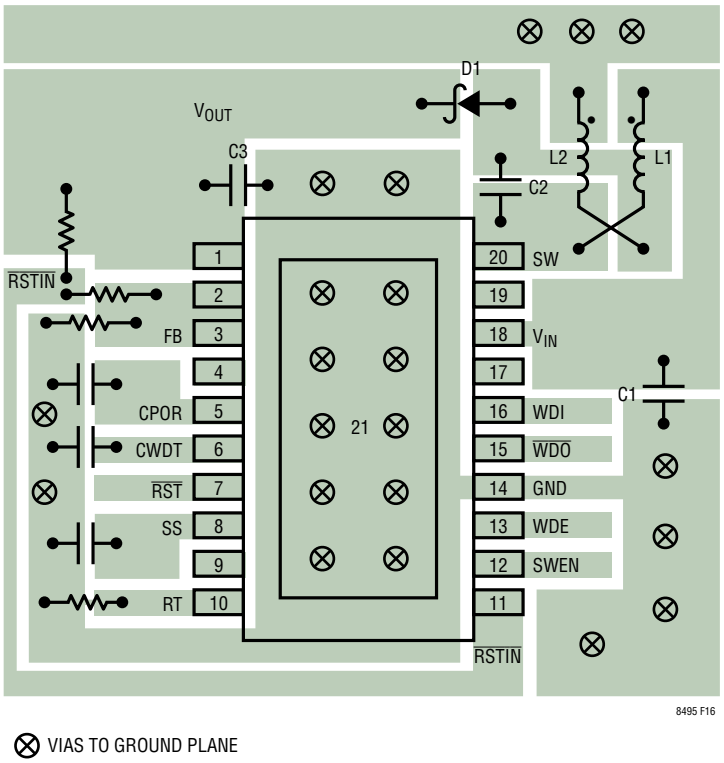
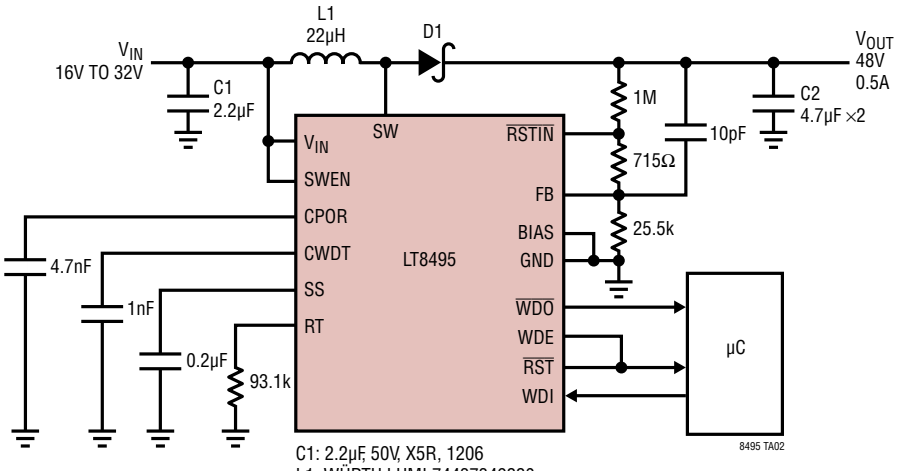


Figure 16. Suggested Component Placement for SEPIC Topology. Pin 21 (Exposed Pad) Must Be Soldered Directly to the Local Ground Plane for Adequate Thermal Performance. Multiple Vias to Additional Ground Planes Will Improve Thermal Performance

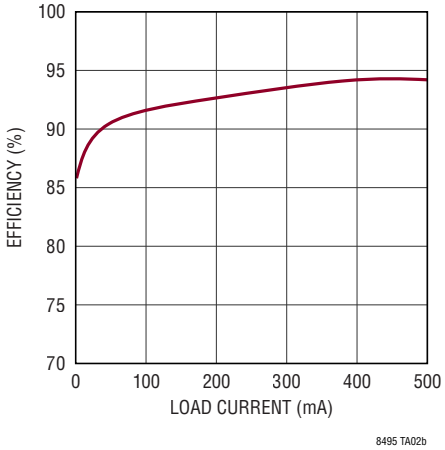
TYPICAL APPLICATIONS

750kHz, 16V to 32V Input, 48V Output, 0.5A Boost Converter

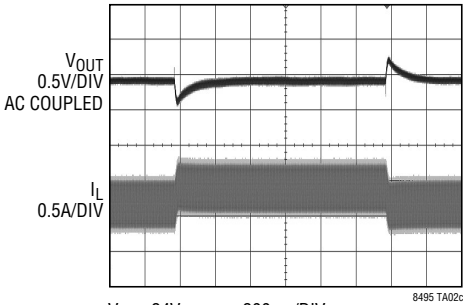


C1: 2.2µF, 50V, X5R, 1206
L1: WÜRTH LHMI 74437349220
D1: ONSEMI MBRA2H100
C2: 4.7µF, 100V, X7R, 1210

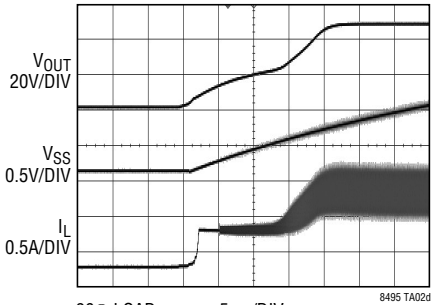
Efficiency, V_{IN} = 24V



Transient Response with 400mA to 500mA to 400mA Output Load Step

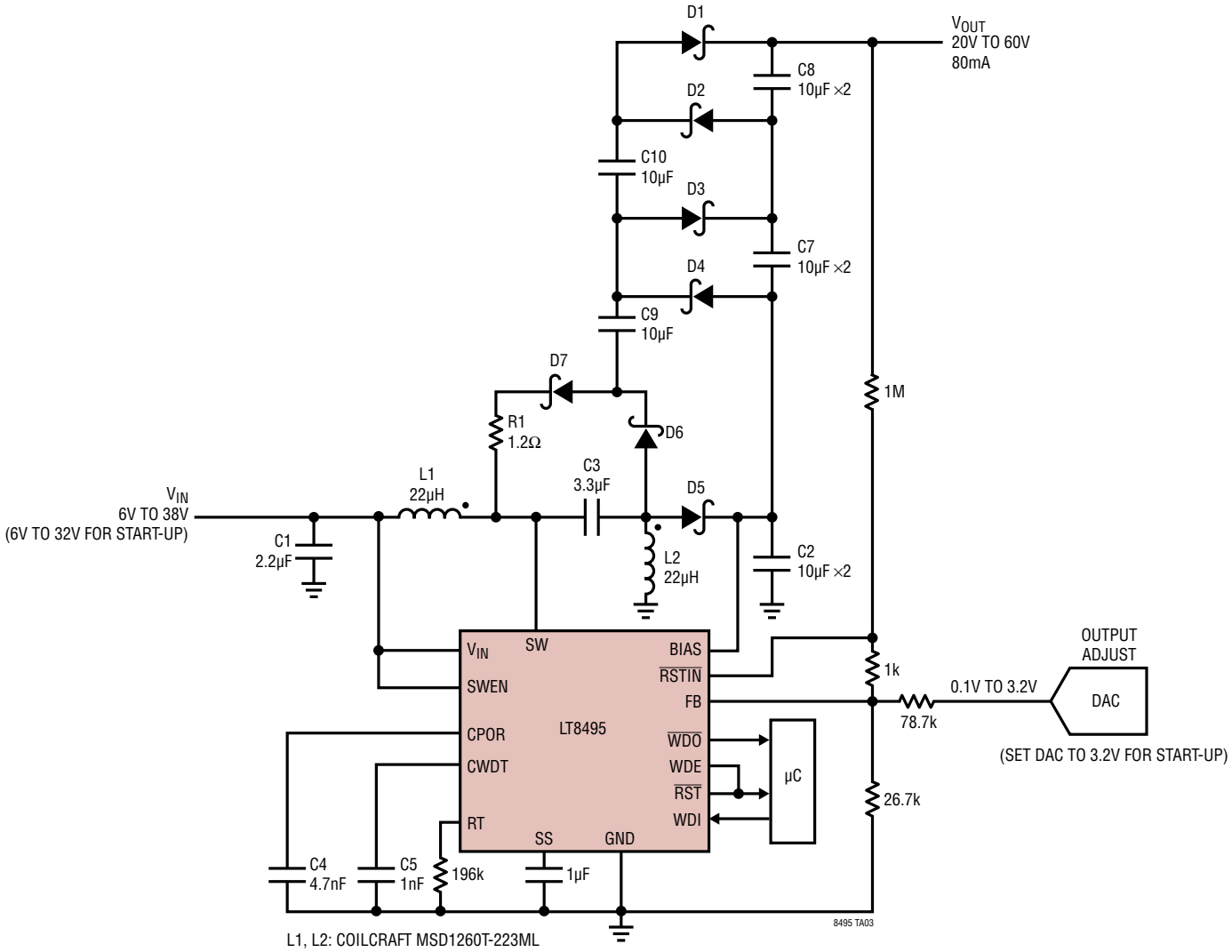


Start-Up Waveforms



TYPICAL APPLICATIONS

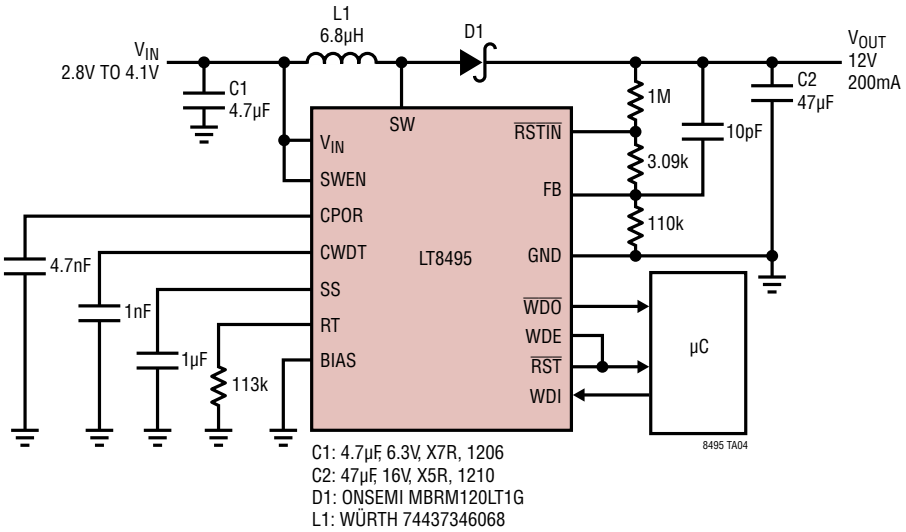
Wide Input and Output Range SEPIC Converter with Charge Pump Switches at 400kHz



L1, L2: COILCRAFT MSD1260T-223ML
C1: 2.2µF, 50V, X5R,1206
C3: 3.3µF, 100V, X7R, 1210
C2, C7-C10: TAIYO YUDEN GMK325C7106KMHT, 10µF, 35V, X7S, 1210
C4: 4.7nF, 25V, NP0, 0603
C5: 1nF, 25V, NP0, 0603
D1-D4: FAIRCHILD MBR0540
D5-D7: ON-SEMI MBRA2H100
R1: 1.2Ω, 0.5W, SMD, 2010

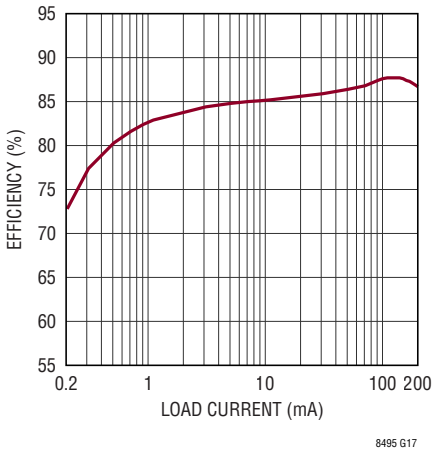
TYPICAL APPLICATIONS

Li-Ion to 12V, Low Q Current Boost @ 650kHz



C1: 4.7µF, 6.3V, X7R, 1206
C2: 47µF, 16V, X5R, 1210
D1: ONSEMI MBRM120LT1G
L1: WÜRTH 74437346068

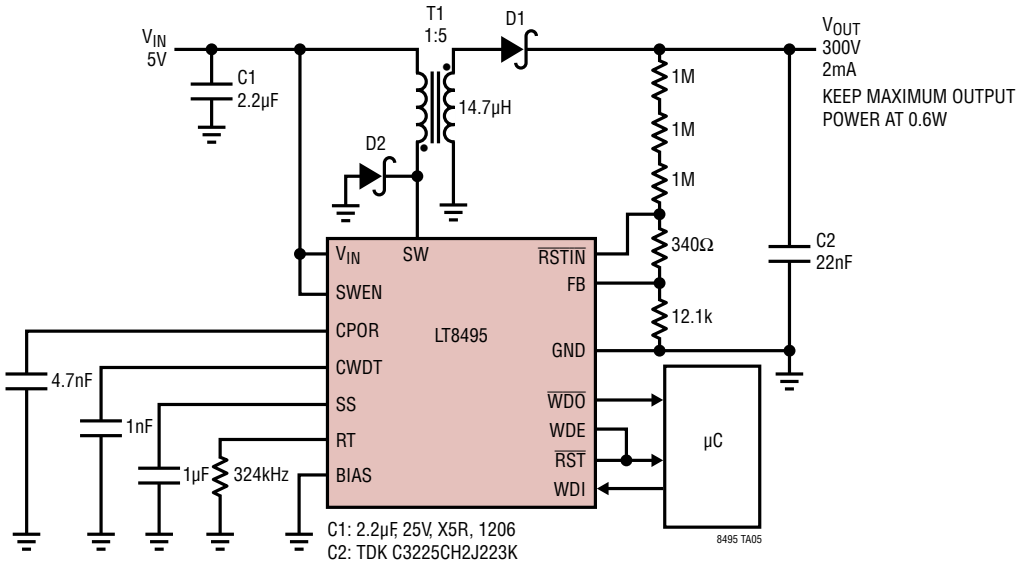
Efficiency, V_{IN} = 3.3V



TYPICAL APPLICATIONS

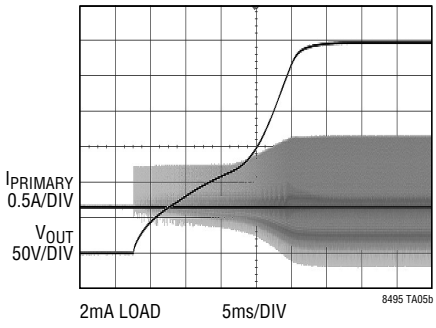
Low Q Current, 5V to 300V, 250kHz Flyback Converter

Danger High Voltage! Operation by High Voltage Trained Personnel Only

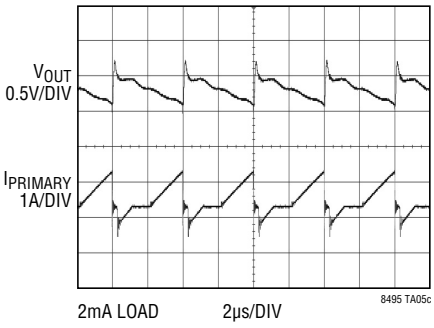


C1: 2.2µF, 25V, X5R, 1206
C2: TDK C3225CH2J223K
D1: VISHAY GSD2004S DUAL DIODE CONNECTED IN SERIES
D2: ONSEMI MBRA2H100
T1: WE –FLEX TRANSFORMER 749196121

Start-Up Waveforms

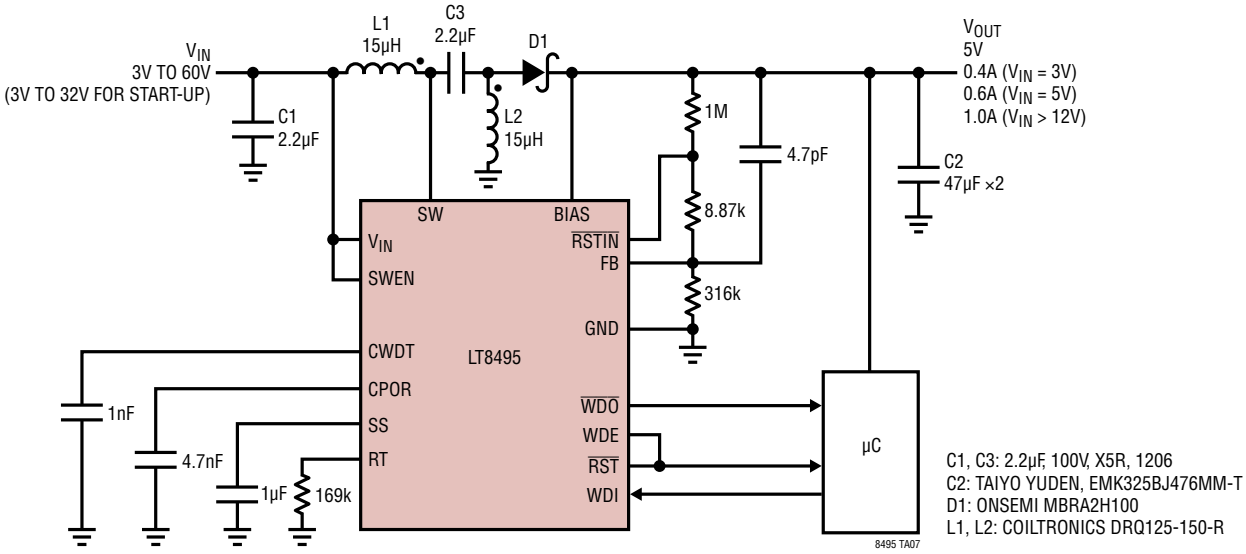


Switching Waveforms



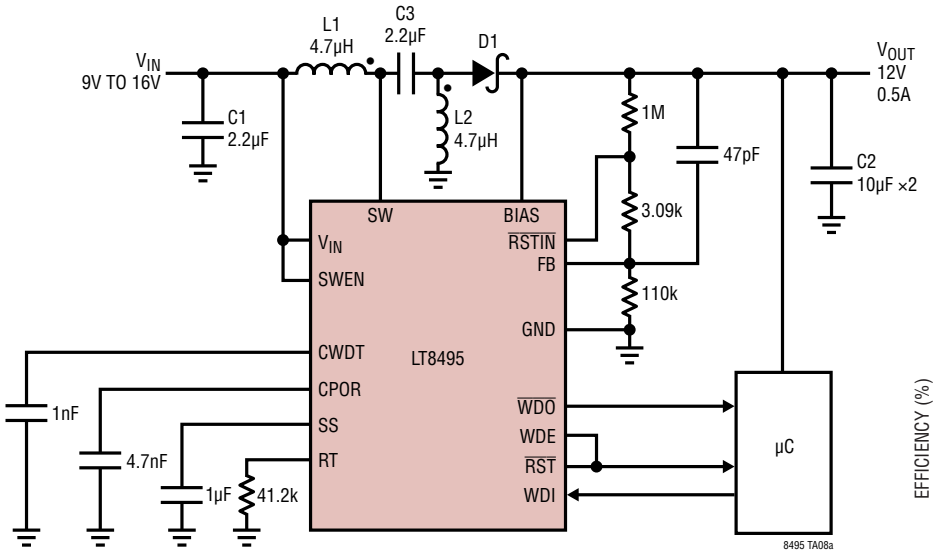
TYPICAL APPLICATIONS

450kHz, 5V Output SEPIC Converter
(Same as Front Page Application)



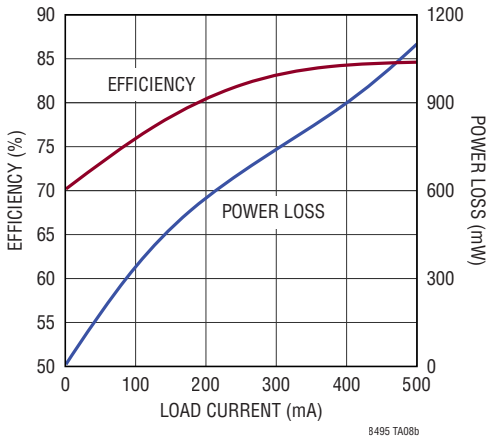
C1, C3: 2.2µF, 100V, X5R, 1206
C2: TAIYO YUDEN, EMK325BJ476MM-T
D1: ONSEMI MBRA2H100
L1, L2: COILTRONICS DRQ125-150-R

1.5MHz, 12V Output SEPIC Converter



C1, C3: 2.2µF, 50V, X5R, 1206
C2: TAIYO YUDEN, TMK325BJ106MM
D1: CENTRAL SEMI CMMSH2-40
L1, L2: COILTRONICS DRQ74-4R7

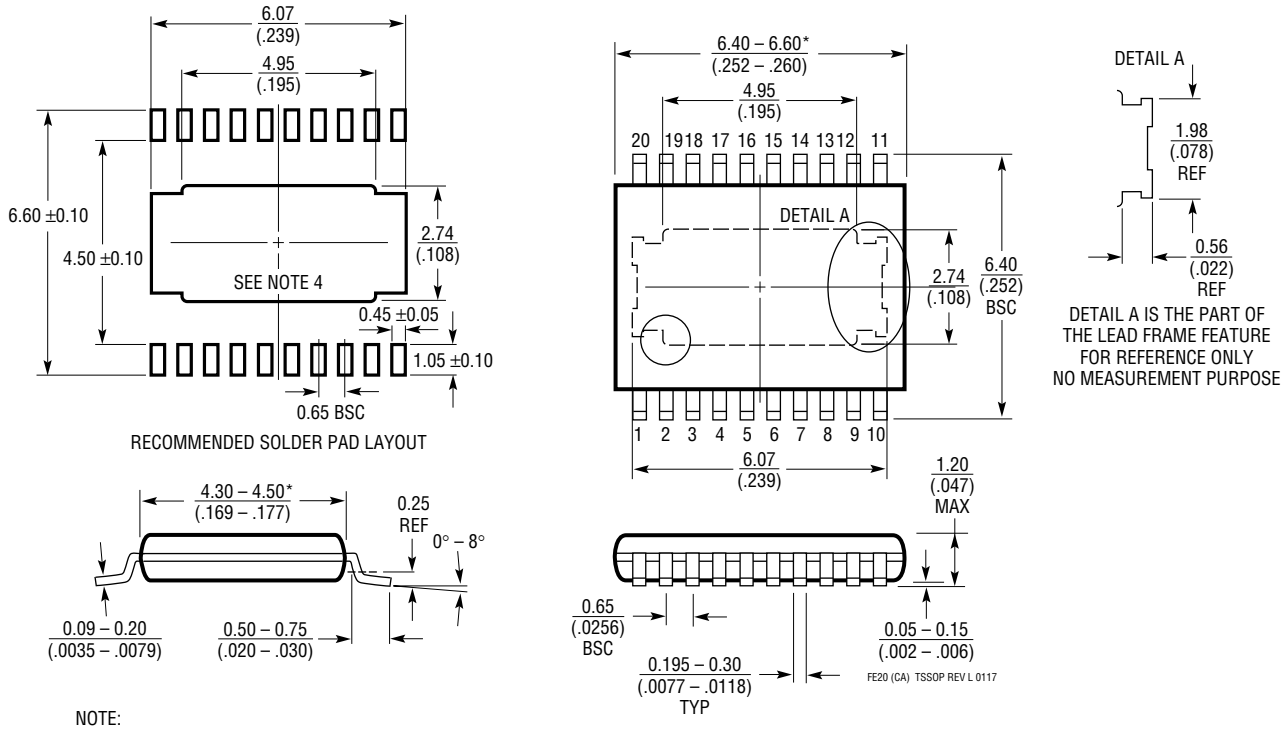
Efficiency, V_{IN} = 12V



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT8495#packaging for the most recent package drawings.

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev L)
Exposed Pad Variation CA



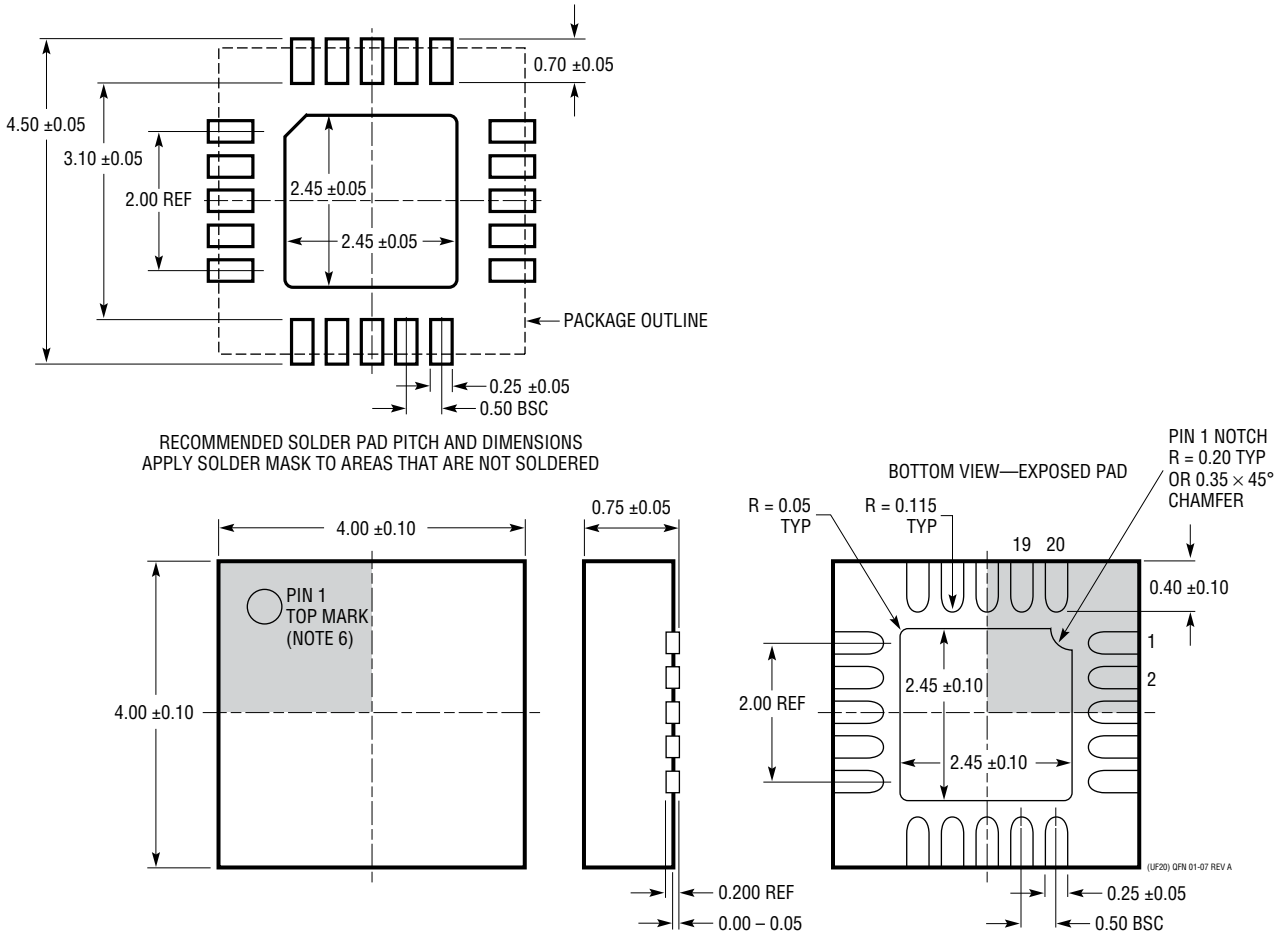
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT8495#packaging for the most recent package drawings.

UF Package
20-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1710 Rev A)



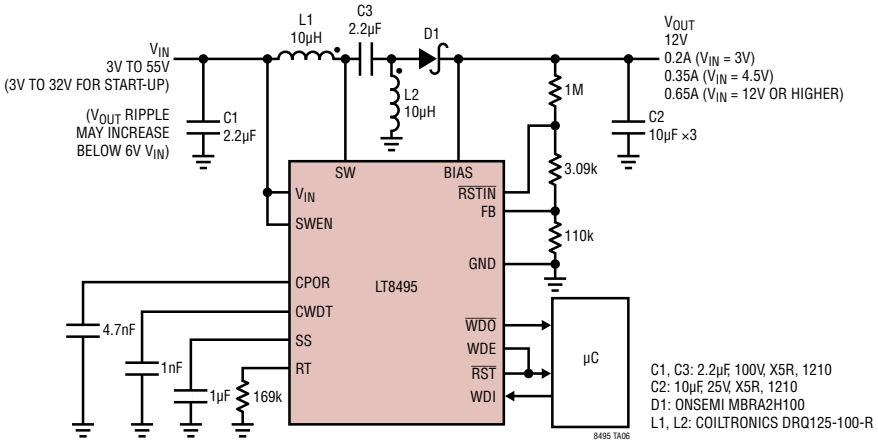
NOTE:
1. DRAWING IS PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-1)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

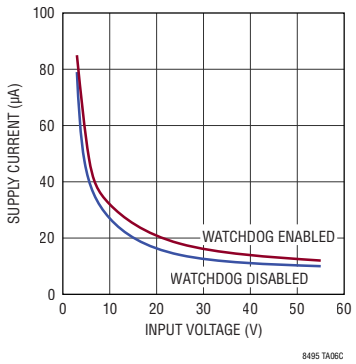
REV	DATE	DESCRIPTION	PAGE NUMBER
A	07/15	Added QFN package option.	1
		Added QFN package option and H-Grade option in TSSOP.	2, 3, 4, 9
		Clarified Quiescent Current specifications.	3
		Clarified RST Leakage Current specifications.	4
		Added Pin Current and Quiescent Current graphs.	8
		Clarified Pin Functions for QFN package.	9
		Clarified leakage current characteristics in High Temperature Considerations.	23
		Added new Typical Applications.	30
B	06/17	Clarified Input Conditions on Top Typical Application	30, 34

TYPICAL APPLICATIONS

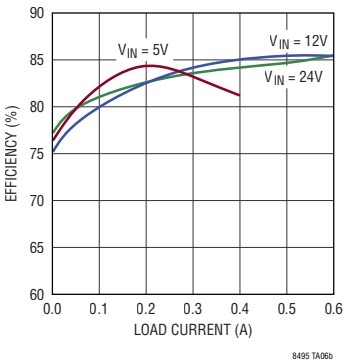
450kHz, Wide Input Range 12V Output SEPIC Converter



No Load Supply Current



Efficiency



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8494	70V, 2A Boost/SEPIC 1.5MHz High Efficiency DC/DC Converter	$V_{IN(MIN)}$ = 2.5V, $V_{IN(MAX)}$ = 32V, $V_{OUT(MIN)}$ = 70V, I_Q = 9µA, I_{SD} = <1µA, 4mm × 4mm QFN-20, TSSOP-20E Packages
LT3580	42V, 2A Boost/Inverting 2.5MHz High Efficiency DC/DC Converter	V_{IN}: 2.5V to 32V, $V_{OUT(MAX)}$ = ±40V, I_Q = 1mA, I_{SD} < 1µA, 3mm × 3mm DFN-8, MSOP-8E Packages
LT8580	65V, 1A Boost/Inverting DC/DC Converter	V_{IN}: 2.55V to 40V, $V_{OUT(MAX)}$ = ±60V, I_Q = 1.2mA, I_{SD} < 1µA, 3mm × 3mm DFN-8, MSOP-8E Packages
LT8570/LT8570-1	65V, 500mA/250mA Boost/Inverting DC/DC Converter	$V_{IN(MIN)}$ = 2.55V, $V_{IN(MAX)}$ = 40V, $V_{OUT(MIN)}$ = ±60V, I_Q = 1.2mA, I_{SD} = <1µA, 3 × 3 DFN-8, MSOP-8E Package
LT8582	40V, Dual 3A, 2.5MHz High Efficiency Boost Converter	V_{IN}: 2.5V to 40V, $V_{OUT(MAX)}$ = ±40V, I_Q = 2.8µA, I_{SD} < 1µA, 7mm × 4mm DFN-24 Package
LT8471	40V, Dual 3A, Multitopology High Efficiency DC/DC Converter	V_{IN}: 2.6V to 50V, $V_{OUT(MAX)}$ = ±45V, I_Q = 2.4mA, I_{SD} < 1µA, TSOP-20E Package
LT3581	40V, 3.3A, 2.5MHz High Efficiency Boost Converter	V_{IN}: 2.5V to 40V, $V_{OUT(MAX)}$ = ±40V, I_Q = 1mA, I_{SD} < 1µA, 4mm × 3mm DFN-14, MSOP-16E Packages
LT8582	40V, Dual 3A Boost, Inverter, SEPIC, 2.5MHz High Efficiency Boost Converter	V_{IN}: 2.5V to 40V, $V_{OUT(MAX)}$ = ±40V, I_Q = 2.1mA, I_{SD} < 1µA, 7mm × 4mm DFN-24 Package
LT3579/LT3579-1	40V, 3.3A Boost, Inverter, SEPIC, 2.5MHz High Efficiency Boost Converter	V_{IN}: 2.5V to 40V, $V_{OUT(MAX)}$ = ±40V, I_Q = 1mA, I_{SD} < 1µA, 4mm × 5mm QFN-20, TSSOP-20E Packages

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