Bipolar Output Synchronous Controller with Seamless Four Quadrant Operation

FEATURES

- **Bipolar Output Cleanly Transitions Through 0V**
- **Output Can Source or Sink Current for Any Output Voltage**
- **CTRL Pin Externally Sets Output Voltage**
- **Wide Input Range: 4.5V to 80V**
- **Power Good Indication Pin (PG)**
- Switching Frequency Up to 750kHz
- Can Be Synchronized to an External Clock
- High Gain EN Pin Accepts Slowly Varying Input Signals
- 20-Lead TSSOP Exposed Pad Package

APPLICATIONS

- Four Quadrant Power Supplies
- Bidirectional Current Sources
- High Power, Low Frequency Signal Amplification
- Test and Measurement
- Electronic Window Tinting

DESCRIPTION

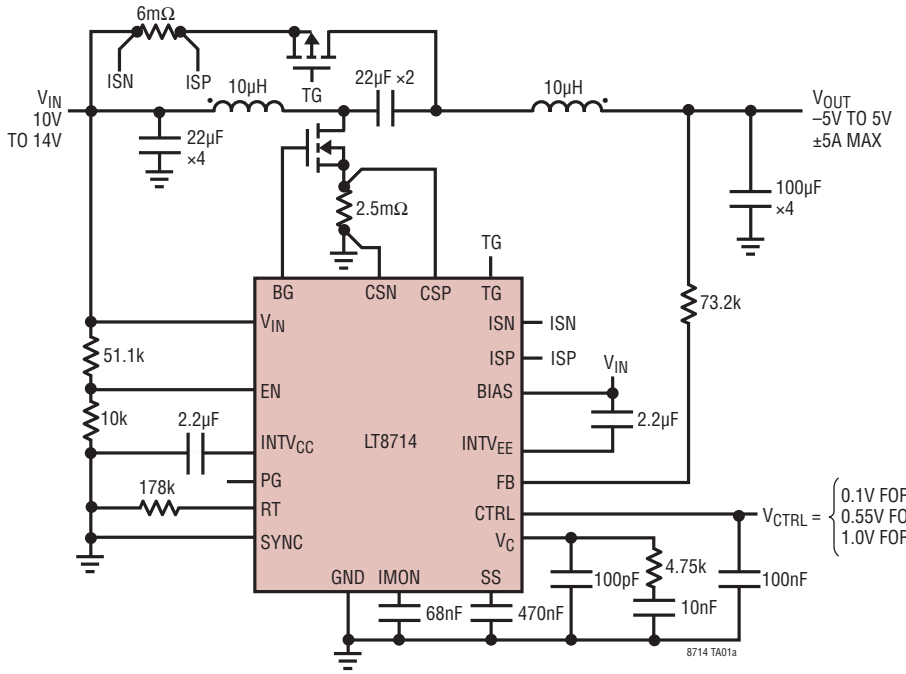
The LT®8714 is a synchronous PWM DC/DC controller designed for a four quadrant output converter. The output voltage cleanly transitions through zero volts with sourcing and sinking output current capability.

The LT8714 is ideal for regulating to positive, negative, or zero volts when configured for the novel four quadrant topology. Applications include four quadrant power supplies, high power bidirectional current sources, active loads, and high power, low frequency signal amplification. In addition, the LT8714 incorporates a power good feature to let the user know if V_{OUT} is above or below its target regulation voltage.

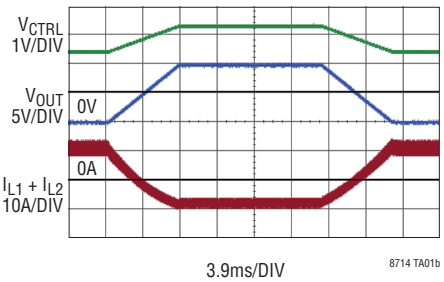
The LT8714's switching frequency range can be programmed between 100kHz and 750kHz via a resistor from the RT pin to GND. A SYNC pin is also provided if the user would like to synchronize the part to an external clock. Additional features such as current limiting and soft-start are included. The LT8714 is available in a 20-lead TSSOP package.

TYPICAL APPLICATION

200kHz, –5V to 5V Output from a 10V to 14V Input



V_{OUT} Cleanly Transitions from –5V to 5V (V_{IN} = 12V)

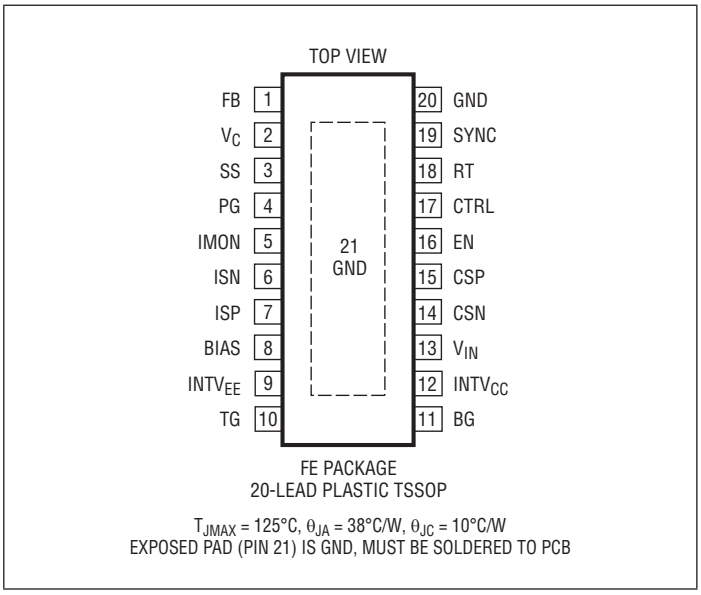


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} Voltage ..... –0.3V to 80V
BIAS Voltage ..... –0.3V to 80V
EN Voltage ..... –0.3V to 80V
BG Voltage ..... Note 5
TG Voltage ..... Note 5
RT Voltage ..... –0.3V to 5V
SS Voltage ..... –0.3V to 3V
FB Voltage ..... –0.3V to 5V
V_C Voltage ..... –0.3V to 2V
SYNC Voltage ..... –0.3V to 5.5V
PG Voltage ..... –0.3V to 7V
PG Current ..... ±1mA
CTRL Voltage ..... –0.3V to 5V
$INTV_{CC}$ Voltage ..... –0.3V to 7V
$INTV_{EE}$ Voltage ..... Note 5
CSP Voltage ..... –0.3V to 2V
CSN Voltage ..... –0.3V to 2V
ISP Voltage ..... ISN – 0.4V to ISN + 2V
ISN Voltage ..... –0.3V to 80V
IMON Voltage ..... –0.3V to 2.5V
Operating Junction Temperature Range
LT8714E ..... –40°C to 125°C
LT8714I ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



FE PACKAGE
20-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 38°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8714EFE#PBF	LT8714EFE#TRPBF	LT8714FE	20-Lead Plastic TSSOP Exposed Pad	–40°C to 125°C
LT8714IFE#PBF	LT8714IFE#TRPBF	LT8714FE	20-Lead Plastic TSSOP Exposed Pad	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications for each channel are at T_A = 25°C. V_{IN} = 12V, V_{EN} = 12V, V_{BIAS} = 12V, unless otherwise noted (Note 2).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Operating Input Voltage		●		4.25	4.5	V
Quiescent Current, I_{VIN}	Not Switching, V_{BIAS} = 7.5V			4	5.5	mA
Quiescent Current in Shutdown	V_{EN} = 0V			0	1	µA
EN Chip Enable Thresholds	EN Rising	●	1.22	1.3	1.38	V
	EN Falling	●	1.18	1.26	1.34	V
EN Chip Enable Hysteresis				44		mV
EN Input Voltage Low	Shutdown Mode	●			0.3	V
EN Pin Bias Current	V_{EN} = 3V			44	60	µA
	V_{EN} = 1.3V			12.7	15.2	µA
	V_{EN} = 0V			0	0.1	µA
SS Charge Current	V_{SS} = 50mV, Current Flowing Out of SS pin	●	7	10.1	13.8	µA
SS Low Detection Voltage	Part Exiting Undervoltage Lockout	●	18	50	82	mV
SS Voltage to Enable Switching	SS Rising		0.75	1.0	1.21	V
	SS Falling		0.65	0.92	1.15	V
SS Hysteresis				80		mV
Low Dropout Regulators, I_{INTVCC} and I_{INTVEE}						
$INTV_{CC}$ Voltage	I_{INTVCC} = 10mA	●	6.2	6.3	6.4	V
$INTV_{CC}$ Undervoltage Lockout	$INTV_{CC}$ Rising	●	3.88	4	4.12	V
	$INTV_{CC}$ Falling	●	3.5	3.73	3.95	V
$INTV_{CC}$ Undervoltage Lockout Hysteresis				270		mV
$INTV_{CC}$ Dropout Voltage	V_{IN} = 6V, I_{INTVCC} = 10mA			255		mV
$INTV_{CC}$ Load Regulation	V_{IN} = 12V, I_{INTVCC} = 0mA to 80mA			–0.44	–2	%
$INTV_{CC}$ Line Regulation	10V ≤ V_{IN} ≤ 80V, I_{INTVCC} = 10mA			–0.005	–0.03	%/V
$INTV_{CC}$ Maximum External Load Current					5	mA
$INTV_{EE}$ Voltage, $V_{BIAS} – V_{INTVEE}$	I_{INTVEE} = 10mA	●	6.03	6.18	6.33	V
$INTV_{EE}$ Undervoltage Lockout, $V_{BIAS} – V_{INTVEE}$	$V_{BIAS} – V_{INTVEE}$ Rising	●	3.24	3.42	3.6	V
	$V_{BIAS} – V_{INTVEE}$ Falling	●	2.94	3.22	3.48	V
$INTV_{EE}$ Undervoltage Lockout Hysteresis, $V_{BIAS} – V_{INTVEE}$				200		mV
I_{INTVEE} Dropout Voltage, V_{INTVEE}	V_{BIAS} = 6V, I_{INTVEE} = 10mA			0.75		V
Control Loops (Refer to Block Diagram to Locate Amplifiers)						
Current Limit Voltage, $V_{CSP} – V_{CSN}$	V_{FB} = 1.4V, CTRL = 1.1V, Minimum Duty Cycle	●	60.5	66	71.5	mV
	V_{FB} = 1.4V, CTRL = 1.1V, Maximum Duty Cycle	●	40	47	56	mV
	V_{FB} = 0.1V, CTRL = 1.1V, Minimum Duty Cycle	●	–23	–32	–41	mV
	V_{FB} = 0.1V, CTRL = 1.1V, Maximum Duty Cycle	●	–38	–51	–65	mV
FB Regulation Voltage	CTRL = 1.1V	●	1.092	1.102	1.112	V
	CTRL = 0.1V	●	0.092	0.102	0.112	V
	CTRL = 0V	●	0	0.0167	0.033	V
FB Pin Bias Current at FB Regulation. (Note 6)	CTRL = 1.1V	●	66.4	68.3	70.2	µA
	CTRL = 0.1V	●	–67.7	–69.7	–71.7	µA
	CTRL = 0V	●	–77.6	–81.6	–85	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications for each channel are at T_A = 25°C. V_{IN} = 12V, V_{EN} = 12V, V_{BIAS} = 12V, unless otherwise noted (Note 2).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
FB Internal Voltage, V1	I_{FB} = 0.0µA	●	0.597	0.6065	0.616	V
FB Internal Resistance, R1		●	7.1	7.25	7.4	kΩ
FB Amp Transconductance, EA1	ΔI_{VC} = 2µA			200		µmhos
FB Amp Voltage Gain, EA1				108		V/V
FB Line Regulation	4.5V ≤ V_{IN} ≤ 80V		–0.02	–0.001	0.02	%/V
Output Current Sense Regulation Voltage, $V_{ISP} – V_{ISN}$	V_{ISN} = 80V, V_{FB} = 1.4V, CTRL = 1.1V	●	46	50	54	mV
	V_{ISN} = 5V, V_{FB} = 1.4V, CTRL = 1.1V	●	46	50	54	mV
IMON Regulation Voltage, EA2	V_{FB} = 1V	●	1.184	1.208	1.233	V
Output Current Sense Amp Transconductance, A7	ΔI_{IMON} = 10µA			1000		µmhos
Output Current Sense Amp Voltage Gain, A7				12.14		V/V
Output Current Sense Amp Input Dynamic Range, A7	Negative Input Range	●	–55.5	–49.5	–43.5	mV
	Positive Input Range		500			mV
IMON Amp Transconductance, EA2	ΔI_{VC} =2µA, V_{FB} = 1.4V, CTRL=1.1V			160		µmhos
IMON Amp Voltage Gain, EA2	V_{ISN} = 12V, V_{FB} = 1.4V, CTRL = 1.1V			70		V/V
Valley Inductor Current Limit, $V_{ISP} – V_{ISN}$	V_{ISN} = 80V	●	–220	–300	–380	mV
	V_{ISN} = 12V	●	–220	–300	–380	mV
Oscillator						
Switching Frequency, f_{OSC}	R_T = 46.4k	●	640	750	860	kHz
	R_T = 357k	●	85	100	115	kHz
Switching Frequency Range	Free-Running or Synchronizing	●	100		750	kHz
SYNC High Level for Sync		●	1.5			V
SYNC Low Level for Sync		●			0.4	V
SYNC Clock Pulse Duty Cycle	V_{SYNC} = 0V to 3V		20		80	%
Recommended Min SYNC Ratio f_{SYNC}/f_{OSC}				3/4		
Gate Drivers, BG and TG						
BG Rise Time	C_{BG} = 3300pF (Note 3)			24		ns
BG Fall Time	C_{BG} = 3300pF (Note 3)			21		ns
TG Rise Time	C_{TG} = 3300pF (Note 3)			15		ns
TG Fall Time	C_{TG} = 3300pF (Note 3)			16		ns
BG and TG Non-Overlap Time	TG Rising to BG Rising, C_{BG} = C_{TG} = 3300pF (Note 3)		80	140	220	ns
	BG Falling to TG Falling, C_{BG} = C_{TG} = 3300pF (Note 3)		45	90	150	ns
BG Minimum On-Time	C_{BG} = C_{TG} = 3300pF		150		420	ns
BG Minimum Off-Time	C_{BG} = C_{TG} = 3300pF		100		480	ns
TG Minimum On-Time	C_{BG} = C_{TG} = 3300pF		0		150	ns
TG Minimum Off-Time	C_{BG} = C_{TG} = 3300pF		290		770	ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications for each channel are at T_A = 25°C. V_{IN} = 12V, V_{EN} = 12V, V_{BIAS} = 12V, unless otherwise noted (Note 2).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Good Indicator, PG						
PG Overvoltage Threshold, V_{FB} – CTRL	V_{FB} Rising, 0.1V ≤ CTRL ≤ 1.1V	●	75	114	155	mV
	V_{FB} Falling, 0.1V ≤ CTRL ≤ 1.1V	●	20	60	100	mV
PG Undervoltage Threshold, V_{FB} – CTRL	V_{FB} Rising, 0.1V ≤ CTRL ≤ 1.1V	●	–100	–60	–20	mV
	V_{FB} Falling, 0.1V ≤ CTRL ≤ 1.1V	●	–155	–114	–75	mV
PG Power Good Hysteresis for Overvoltage or Undervoltage				54		mV
PG Output Voltage Low	100µA into PG Pin, V_{FB} = 1.4V, CTRL = 1.1V	●		9	50	mV
PG Leakage Current	V_{PG} = 7V, V_{FB} = 1.1V, CTRL = 1.1V			0.01	1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT8714E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LT8714I is guaranteed over the full –40°C to 125°C operating junction temperature range.

Note 3: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

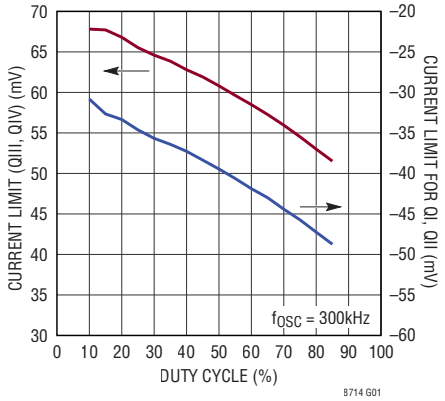
Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation over the specified maximum operating junction temperature may impair device reliability.

Note 5: Do not apply a positive or negative voltage or current source to the BG, TG, and $INTV_{EE}$ pins, otherwise permanent damage may occur.

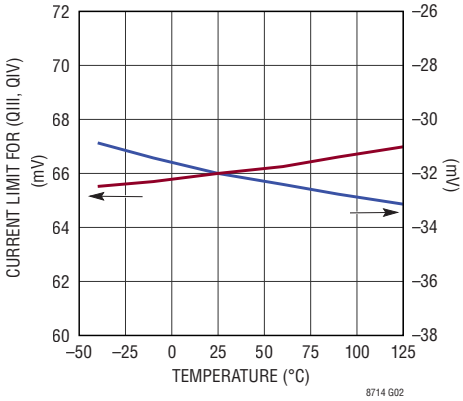
Note 6: Negative FB current is defined as current flowing out of the FB pin. Positive FB current is defined as current flowing into the FB pin.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

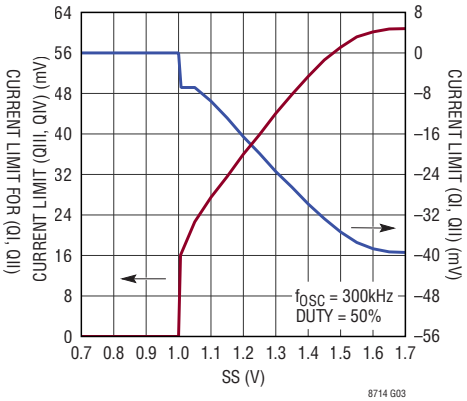
Max Current Limit vs Duty Cycle (CSP – CSN)



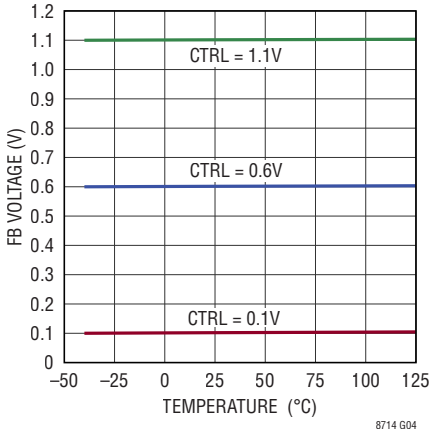
Max Current Limit vs Temperature (CSP – CSN)



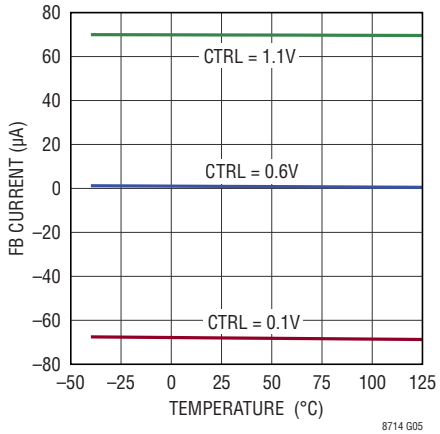
Max Current Limit vs Soft-Start (CSP – CSN)



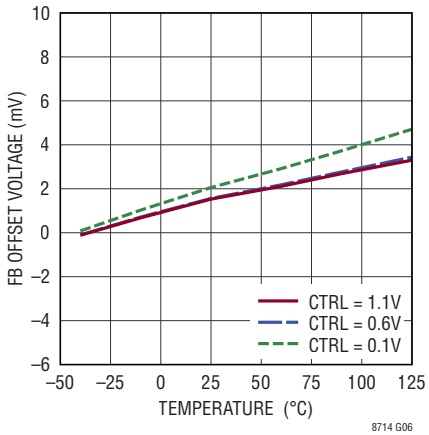
FB Regulation Voltage vs Temperature



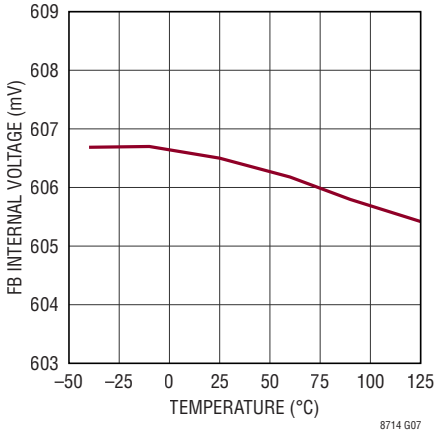
FB Regulation Current vs Temperature



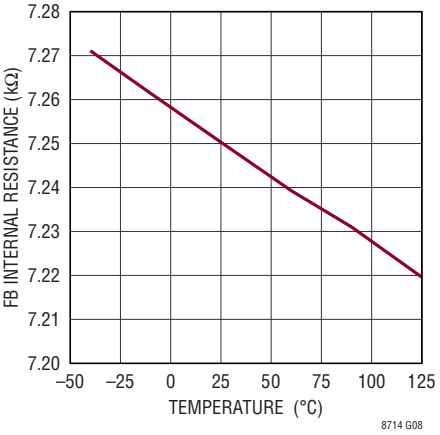
FB Offset Voltage vs Temperature (V_{FB} – CTRL)



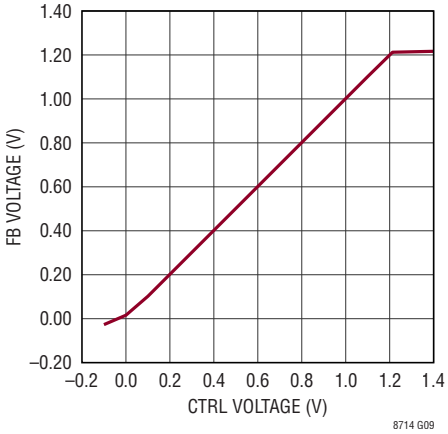
FB Internal Voltage vs Temperature



FB Internal Resistance vs Temperature



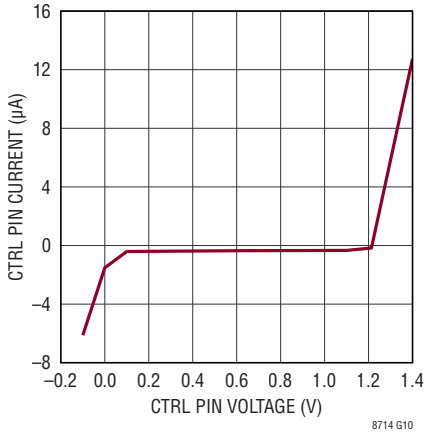
FB Voltage vs CTRL Voltage



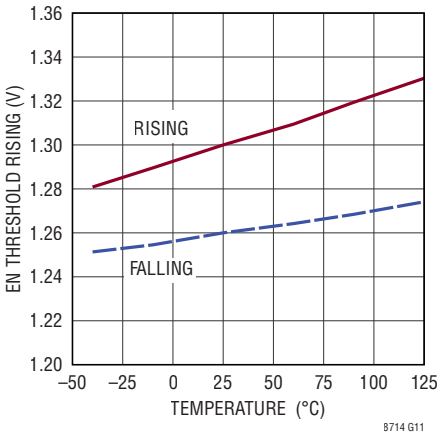
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

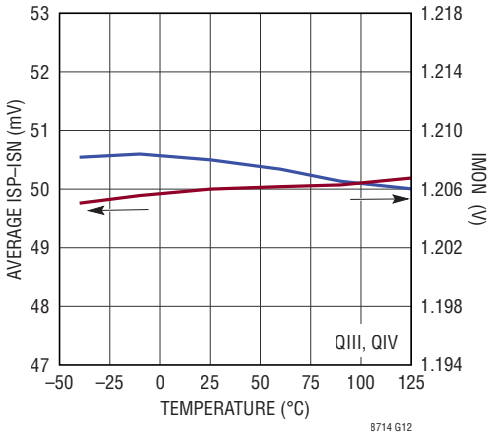
CTRL Pin Current vs CTRL Pin Voltage



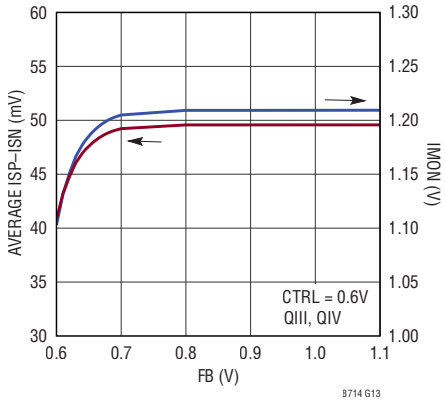
EN Threshold vs Temperature



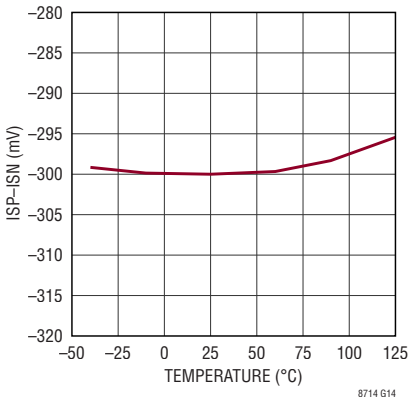
Output Current Sense Regulation Voltage (ISP – ISN and IMON)



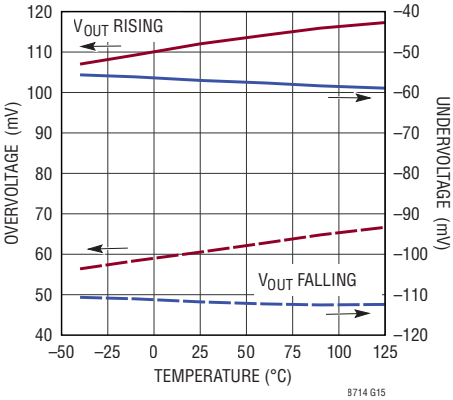
Output Current Sense Regulation Voltage vs FB (ISP – ISN and IMON)



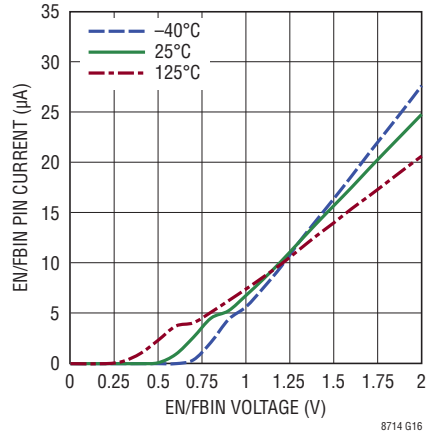
Valley Current Limit Thresholds (ISP – ISN)



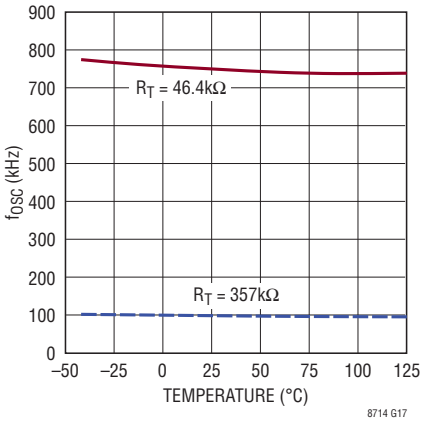
Power Good Thresholds vs Temperature (V_{FB} – CTRL)



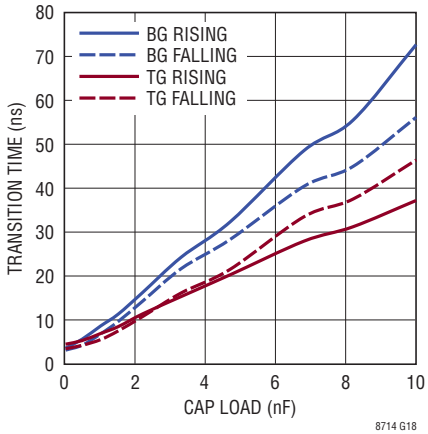
EN Pin Current (0V to 2V) vs Temperature



Oscillator Frequency vs Temperature

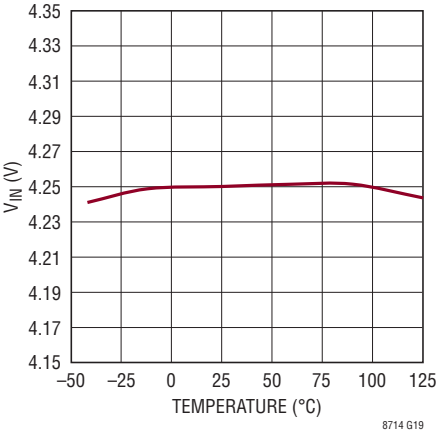


BG and TG Transition Time

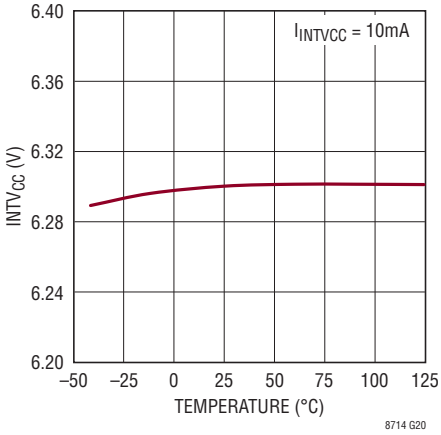


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

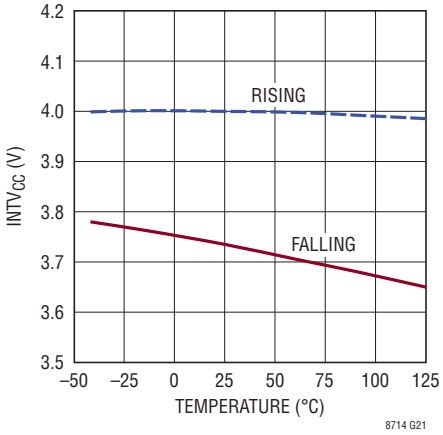
Minimum Operating Input Voltage



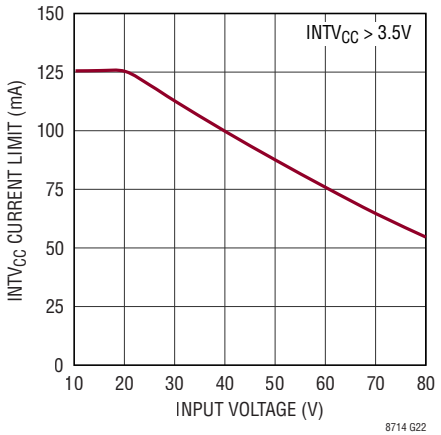
$INTV_{CC}$ vs Temperature



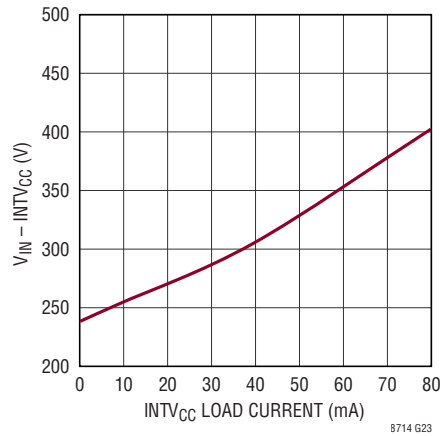
$INTV_{CC}$ UVLO vs Temperature



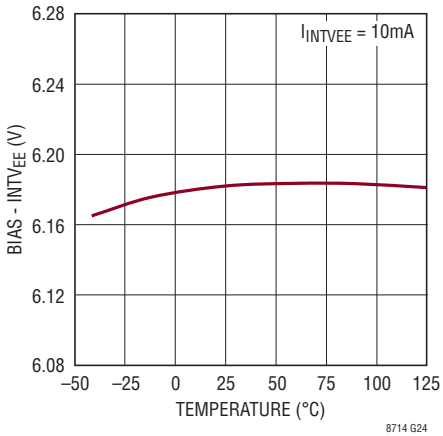
$INTV_{CC}$ Current Limit vs V_{IN}



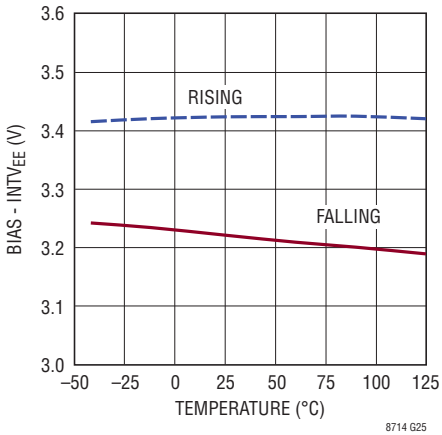
$INTV_{CC}$ Dropout



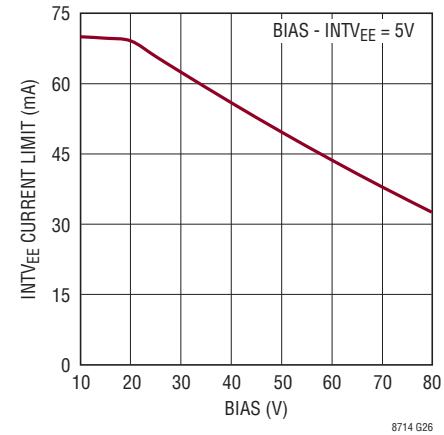
$INTV_{EE}$ vs Temperature



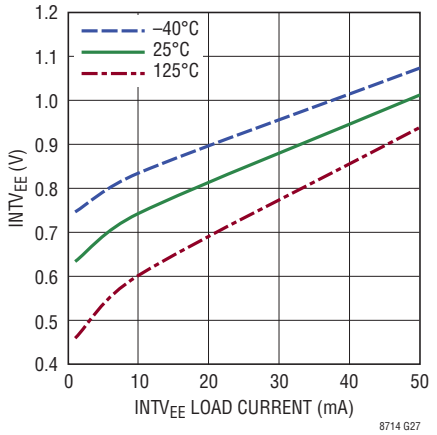
$INTV_{EE}$ UVLO vs Temperature



$INTV_{EE}$ Current Limit vs BIAS



$INTV_{EE}$ Dropout (BIAS = 6V)



PIN FUNCTIONS

FB (Pin 1): Feedback Pin. For the four quadrant converter, tie a resistor from the FB pin to V_{OUT} according to the following equation:

$$R_{FB} = 7250\Omega \bullet \left(\frac{V_{OUT} - V_{CTRL}}{V_{CTRL} - 0.6065} \right)$$

V_C (Pin 2): Error Amplifier Output Pin. Tie external compensation network to this pin.

SS (Pin 3): Soft-Start Pin. Place a soft-start capacitor here that is greater than 5× the IMON capacitor. Upon start-up, the SS pin will be charged by a (nominally) 260k resistor to ~2.7V. During an overtemperature or UVLO condition, the SS pin will be quickly discharged to reset the part. Once these conditions are clear, the part will attempt to restart.

PG (Pin 4): Power Good Pin. The PG pin functions as an active high Power Good pin. Power is good when V_{FB} is within ±60mV of V_{CTRL}. A pull-up resistor or some other form of pull-up network is needed on this pin to use this feature. See the Block Diagram and Applications section for more information.

IMON (Pin 5): Output Current Sense Monitor Output Pin. Outputs a voltage that is proportional to the voltage seen across the ISP and ISN pins.

$$V_{IMON} = 12.14 \bullet (V_{ISP-ISN} + 49.9mV)$$

Since the voltage across the ISP and ISN pins is AC, a filtering capacitor is needed on the IMON pin to average out the ISP and ISN voltage. Recommended capacitor values range from 10nF to 100nF. A 49.9mV offset is added to the amplifier, so when the average ISP – ISN voltage is 0V, the IMON voltage is 606mV. When the average voltage across the ISP and ISN pins is 50mV, the IMON pin will output 1.208V. Do not resistively load down this pin.

ISN and ISP (Pins 6 and 7): Output Current Sense Negative and Positive Input Pins Respectively. Kelvin connect ISN and ISP pins to a sense resistor to limit the output current. The commanded NFET current will limit the voltage difference across the sense resistor to 50mV (typical).

BIAS (Pin 8): Top Gate Driver Supply Pin. The BIAS pin sets the top rail for the TG gate driver. Connect this pin to the converter's input voltage source V_{IN} and bypass locally.

$INTV_{EE}$ (Pin 9): 6.18V-Below-BIAS Regulator Pin. Must be locally bypassed with a minimum capacitance of 2.2µF to BIAS. This pin sets the bottom rail for the TG gate driver. The TG gate driver can begin switching when BIAS – $INTV_{EE}$ exceeds 3.42V (typical).

TG (Pin 10): PFET Gate Drive Pin. Low and high levels are BIAS – $INTV_{EE}$ and BIAS respectively.

BG (Pin 11): NFET Gate Drive Pin. Low and high levels are GND and $INTV_{CC}$ respectively.

$INTV_{CC}$ (Pin 12): 6.3V Input LDO Regulator Pin. Must be locally bypassed with a minimum capacitance of 2.2µF to GND. A maximum of 5mA external load can connect to the $INTV_{CC}$ pin. The undervoltage lockout on $INTV_{CC}$ is 4V (typical). The gate driver, BG, can begin switching when $INTV_{CC}$ exceeds 4V (typical).

V_{IN} (Pin 13): Input Supply Pin. Must be locally bypassed. The minimum voltage for the part to operate is 4.5V (typical).

CSN and CSP (Pins 14 and 15): NFET Current Sense Negative and Positive Input Pins Respectively. Kelvin connect these pins to a sense resistor to limit the NFET switch current. The maximum positive sense voltage at low duty cycle is 66mV (typical). The maximum negative sense voltage at low duty cycles is –32mV (typical).

PIN FUNCTIONS

EN (Pin 16): Enable Pin. In conjunction with the UVLO (undervoltage lockout) circuit, this pin is used to enable/disable the chip and restart the soft-start sequence. Drive below 0.3V to disable the chip with very low quiescent current. Drive above 1.3V (typical) to activate the chip and restart the soft-start sequence. See the Block Diagram and Applications section for more information. Do not float this pin.

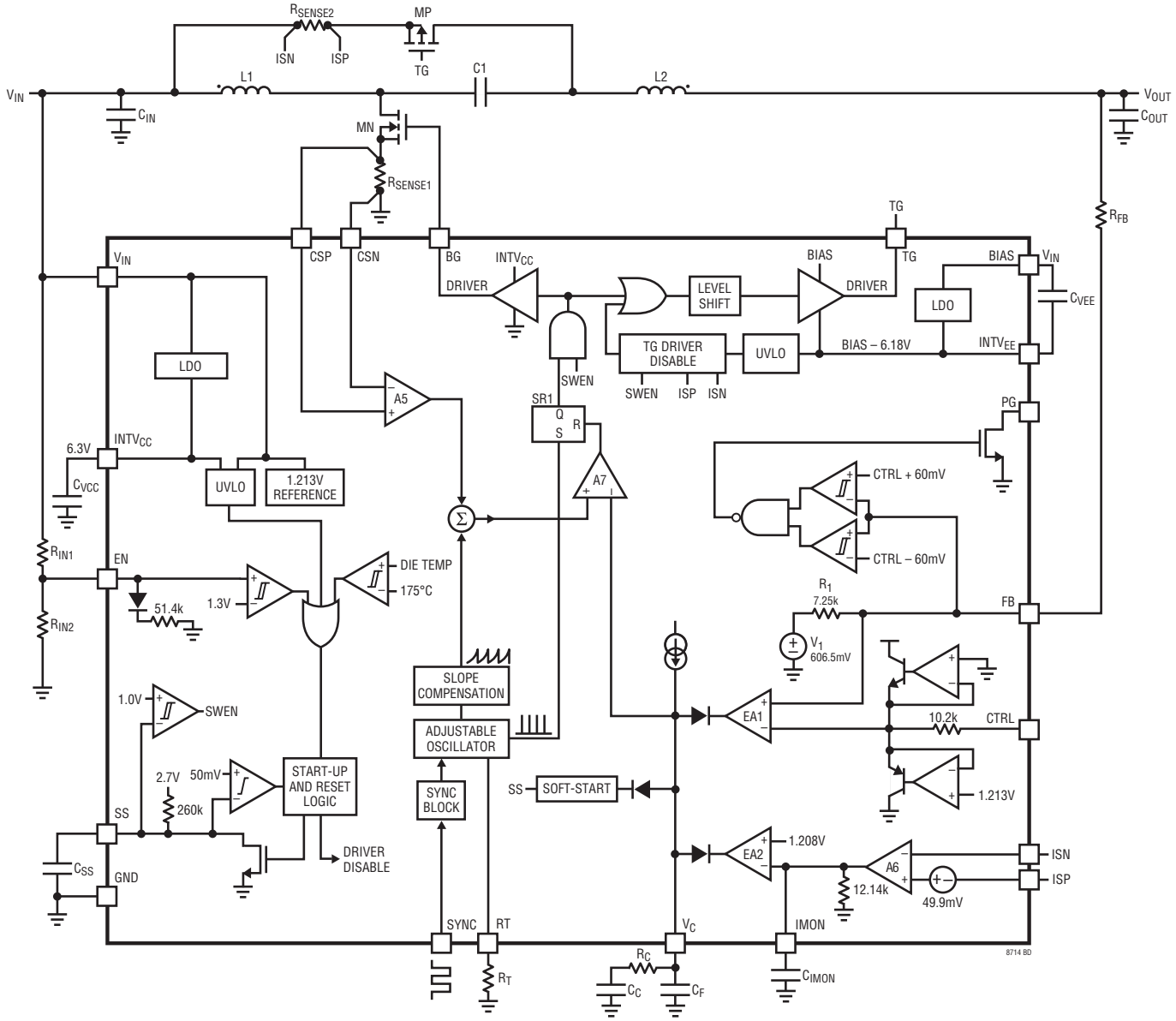
CTRL (Pin 17): Output Voltage Control Pin. The CTRL pin sets the regulation voltage for V_{FB}. The CTRL pin accepts voltages from 0.1 to 1.1V. In the event that the CTRL pin is driven above 1.213V, the voltage at FB regulates to ≈1.213V. Likewise, if the CTRL pin is driven below 0V, the voltage at FB regulates to ≈0V.

RT (Pin 18): Timing Resistor Pin. Adjusts the LT8714's switching frequency. Place a resistor from this pin to ground to set the frequency to a fixed free-running level. Do not float this pin.

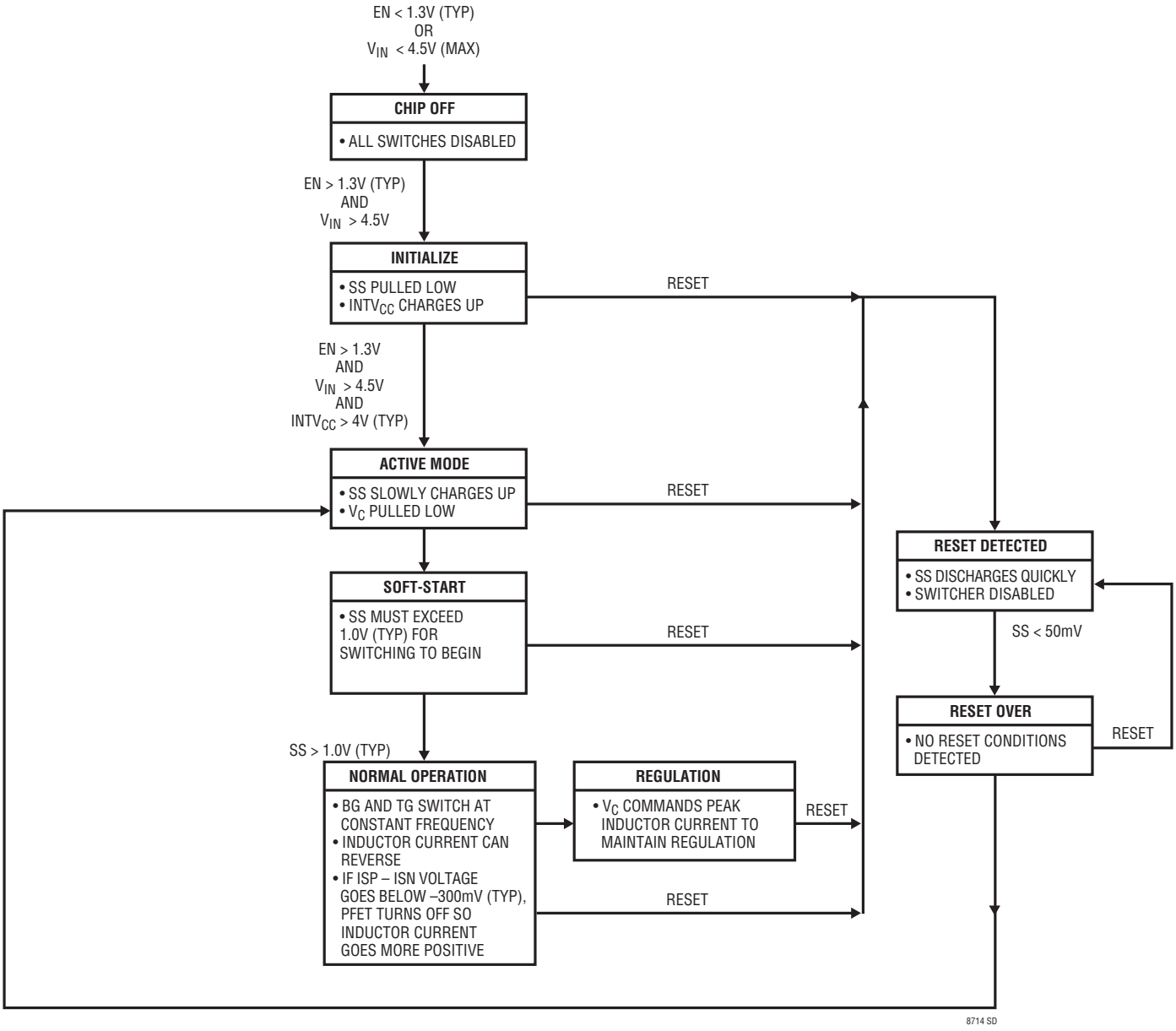
SYNC (Pin 19): To synchronize the switching frequency to an outside clock, simply drive this pin with a clock. The high voltage level of the clock must be between 1.5V and 5V, and the low level must be less than 0.4V. Drive this pin to less than 0.4V to revert to the internal free-running clock. See the Applications Information section for more information.

GND (Pin 20 and Exposed Pad Pin 21): Ground. Must be soldered directly to local ground plane.

BLOCK DIAGRAM



STATE DIAGRAM



REGULATION = OUTPUT VOLTAGE (FB)
OUTPUT CURRENT (ISP-ISN AND IMON)

RESET = UVLO ON V_{IN} (< 4.5V (MAX))
UVLO ON $INTV_{CC}$ (< 4V (TYP))
EN < 1.3V (TYP)
OVERTEMPERATURE (T_J > 175°C (TYP))

OPERATION

OPERATION – FOUR QUADRANT OVERVIEW

Four quadrant operation means that a device can operate as a power source and as a load irrespective of the voltage polarity. To illustrate this concept, please refer to Figures 1 and 2.

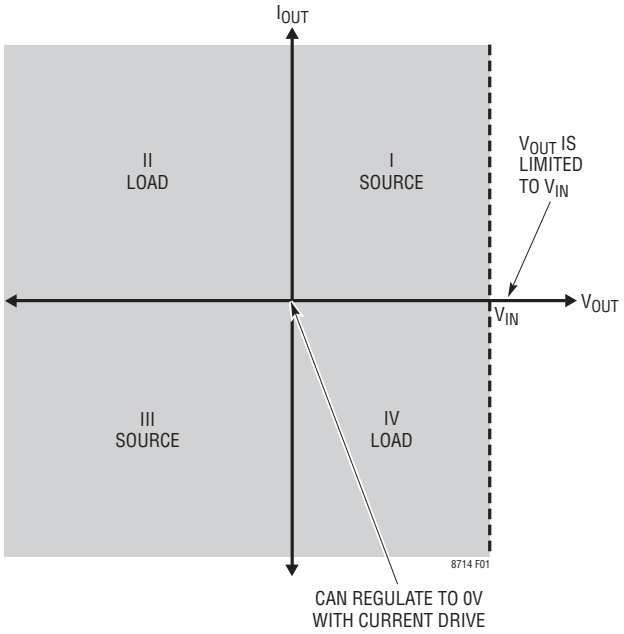


Figure 1. Four Quadrant Operation Overview

From the graph and current flow diagrams, we can have positive output voltage and positive output current, positive output voltage and negative output current, negative output voltage and positive output current, and negative output voltage and negative output current. Quadrants I and III transfer power from V_{IN} to V_{OUT}. Quadrants II and IV transfer power from V_{OUT} back to V_{IN}.

The maximum positive output voltage of the four quadrant converter is limited to V_{IN}.

OPERATION – LT8714 OVERVIEW

The LT8714 uses a constant-frequency, current mode control scheme to provide excellent line and load regulation for the four quadrant converter. The part's undervoltage lockout (UVLO) function and soft-start provide a controlled start up sequence. In addition, synchronous switching makes high efficiency and high output current applications possible. Please refer to the Block Diagram and the State Diagram for the following description of the part's operation.

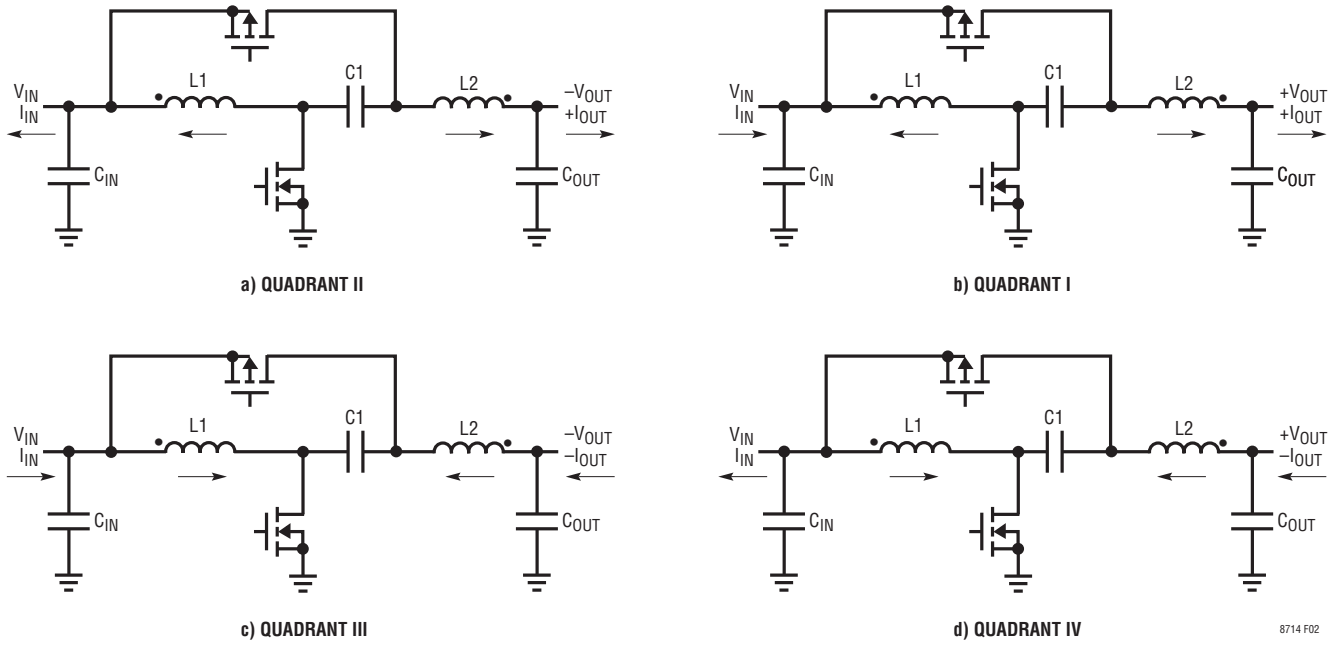


Figure 2. Four Quadrant Topology Current Flow

OPERATION

OPERATION – START-UP

Several functions are provided to enable a very clean start-up of the LT8714.

Precise Turn-On Voltage

The EN pin has a single voltage level for enabling the internal rails to operate the part. To activate a soft-start cycle and allow switching to commence, take the EN pin above 1.3V (typical). This comparator has 44mV of hysteresis to protect against glitches and slow ramping. Taking the EN pin below 0.3V shuts down the chip, resulting in extremely low quiescent current. See Figure 3 below that illustrates the different chip modes for different EN pin voltages.

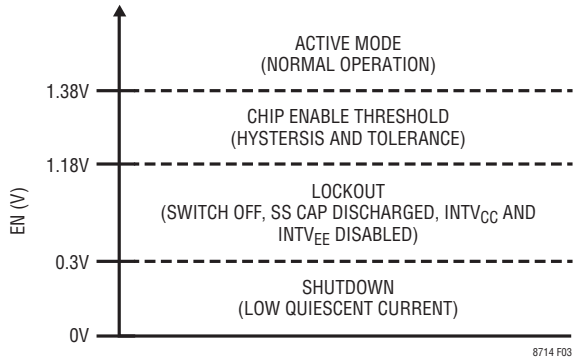


Figure 3. Chip EN Thresholds

Undervoltage-Lockout (UVLO)

The LT8714 has internal UVLO circuitry that disables the chip when V_{IN} < 4.5V (max) or $INTV_{CC}$ < 4V (typical). The EN pin can also be used to create a configurable UVLO. See the Applications section for more information.

Soft-Start of Switch Current

The soft-start circuitry provides for a gradual ramp-up of the switch current (refer to Commanded Switch Current vs. SS in Typical Performance Characteristics). When the part is brought out of shutdown, the external SS capacitor is first discharged which resets the states of the logic circuits in the chip. Once $INTV_{CC}$ comes out of UVLO (> 4V typical) and the chip is in active mode, an integrated 260k resistor pulls the SS pin to ~2.7V at a ramp rate set by the external capacitor connected to the pin. Typical values for the soft-start capacitor range from 100nF to 1µF. The soft-start capacitor should also be at least 5× greater than the external capacitor connected to the IMON pin to avoid start-up issues.

OPERATION – REGULATION

Use the Block Diagram when stepping through the following description of the LT8714 operating in regulation. The LT8714 has 2 modes of regulation:

1. Output Voltage (via FB pin)
2. Output Current (via ISP, ISN, and IMON pins)

Both of these regulation loops control the peak commanded current through the external NFET, MN. The output current regulation loop, however, regulates the peak NFET current in Quadrants III and IV.

At the start of each oscillator cycle, the SR latch (SR1) is set, which first turns off the external PFET, MP, and then turns on the external NFET, MN. The NFET's source current flows through an external current sense resistor (R_{SENSE1}) generating a voltage proportional to the NFET switch current. This voltage is then amplified by A5 and added to a stabilizing ramp. The resulting sum is fed into the positive terminal of the PWM comparator A7. When the voltage on the positive input of A7 exceeds the voltage on the negative input (V_C pin), the SR latch is reset, turning off the NFET and then turning on the PFET. The voltage on the V_C pin is controlled by one or both regulation loops. For simplicity, each mode of regulation will be described independently so that only one of the modes of regulation is in command of the LT8714.

Output Voltage Regulation

A single external resistor is used to set the target output voltage. See the Pin Functions section for selecting the feedback resistor for a desired output voltage. The V_C pin voltage (negative input of A7) is set by EA1, which is simply an amplified difference between the FB pin voltage and the CTRL pin voltage. In this manner, the error amplifier sets the correct peak current level to maintain output voltage regulation.

OPERATION

Output Current Regulation (Quadrants III and IV)

An external sense resistor connected between the ISP and ISN pins (R_{SENSE2}) sets the maximum sinking output current of the converter when placed in the source of the PFET, MP. A built-in 49.9mV offset is added to the voltage seen across R_{SENSE2}. The offset voltage and the sensed voltage are then amplified and is output to the IMON pin. An external capacitor must be placed from IMON to ground to filter the amplified chopped voltage that's sensed across R_{SENSE2}. The voltage at the IMON pin is fed into the negative input of the IMON error amplifier, EA3. The V_C pin voltage is set by EA3, which is simply an amplified difference between the IMON pin voltage and the 1.208V reference voltage. In this manner, the IMON error amplifier sets the correct peak current level to maintain output sinking current regulation.

OPERATION – RESET CONDITIONS

The LT8714 has 2 reset cases. When the part is in reset, the SS pin is pulled low and both power switches, MN and MP, are forced off. Once all of the reset conditions are gone, the part is allowed to begin a soft-start sequence and switching can commence. Each of the following events can cause the LT8714 to be in reset:

1. UVLO
   a. V_{IN} is < 4.5V (maximum)
   b. $INTV_{CC}$ < 4V (typical)
2. Die Temperature > 175°C

OPERATION – POWER SWITCH CONTROL

The main power switch is the external NFET (MN in Block Diagram) and the synchronous power switch is the external PFET (MP in Block Diagram). A non-overlap time of ~140ns and ~90ns on the rising and falling edges respectively is added (see Electrical Characteristics) to prevent cross conduction. Figure 4 shows the BG and TG (BIAS – TG) signals.

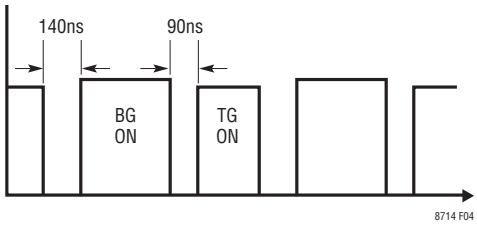


Figure 4. Synchronous Switching

OPERATION – POWER GOOD (PG PIN)

The PG pin is an open-drain pin that functions as an active high Power Good pin. Power is good when the FB voltage is within ±60mV of the CTRL pin voltage. The PG comparators have 54mV of hysteresis to reject glitches.

OPERATION – LDO REGULATORS ($INTV_{CC}$ AND $INTV_{EE}$)

The $INTV_{CC}$ LDO regulates to 6.3V (typical) and is used as the top rail for the BG gate driver. The $INTV_{CC}$ regulator also has safety features to limit the power dissipation in the internal pass device and also to prevent it from damage if the pin is shorted to ground. The UVLO threshold on $INTV_{CC}$ is 4V (typical), and the LT8714 will be in reset until the LDO comes out of UVLO.

The $INTV_{EE}$ regulator regulates to 6.18V (typical) below the BIAS pin voltage. The BIAS and $INTV_{EE}$ voltages are used for the top and bottom rails of the TG gate driver respectively. Just like the $INTV_{CC}$ regulator, the $INTV_{EE}$ regulator has a safety feature to limit the power dissipation in the internal pass device.

APPLICATIONS INFORMATION

FOUR QUADRANT CONVERTER COMPONENT SELECTION

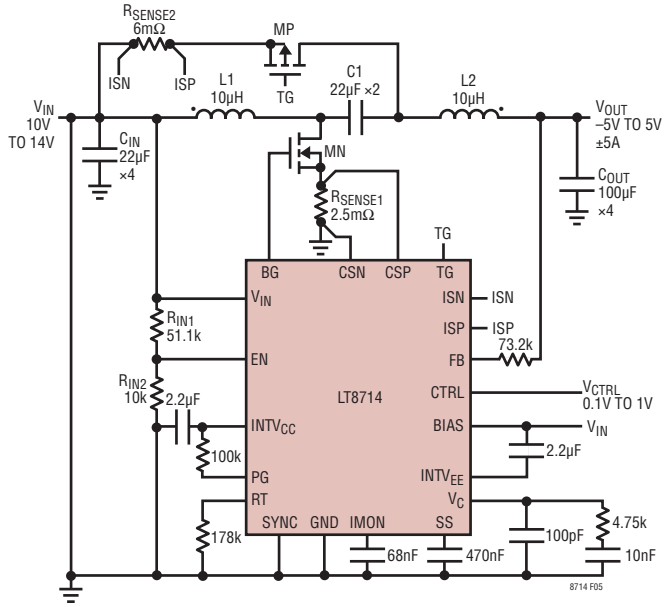


Figure 5. Four Quadrant Converter—The Component Values Given are Typical Values for a 200kHz, –5V to 5V/±5A Output from a 10V to 14V Input

For a desired output current and output voltage over a given input voltage range, Table 1 is a step-by-step set of equations to calculate component values for the LT8714 when operating as a four quadrant power supply. Refer to the Appendix section for further information on the design equations presented in Table 1.

Variable Definitions:

$V_{IN(MIN)}$ = Minimum Input Voltage

$V_{IN(MAX)}$ = Maximum Input Voltage

$V_{OUT(POS)}$ = Max Positive Output Voltage

$V_{OUT(NEG)}$ = Max Negative Output Voltage

I_{OUT} = Output Current of Converter

f = Switching Frequency

DC_{MAX} = Duty Cycle at $V_{IN(MIN)}$ and $V_{OUT(NEG)}$

DC_{MIN} = Duty Cycle at $V_{IN(MIN)}$ and $V_{OUT(POS)}$

V_{CSPN}+ = Current Limit Voltage at DC_{MAX}

V_{CSPN}– = Current Limit Voltage at DC_{MIN}

Table 1. Four Quadrant Converter Design Equations

	Parameters/Equations
Step 1: Inputs	Pick V_{IN}, V_{OUT}, I_{OUT}, and f to calculate equations below.
Step 2: DC_{MAX}	$DC_{MAX}=\frac{V_{IN(MIN)}-V_{OUT(NEG)}}{2V_{IN(MIN)}-V_{OUT(NEG)}}$, $DC_{MIN}=\frac{V_{IN(MIN)}-V_{OUT(POS)}}{2V_{IN(MIN)}-V_{OUT(POS)}}$
Step 3: V_{CSPN}	See Max Current Limit vs Duty Cycle plot in Typical Performance Characteristics to find V_{CSPN} at DC_{MAX}.
Step 4: R_{SENSE1}	$R_{SENSE1^+}=0.63\bullet\frac{V_{CSPN^+}}{I_{OUT}}\bullet(1-DC_{MAX})$ $R_{SENSE1^-}=0.63\bullet\frac{V_{CSPN^-}}{I_{OUT}}\bullet(1-DC_{MIN})$ $R_{SENSE1}=MIN(R_{SENSE1^+},R_{SENSE1^-})$
Step 5: R_{SENSE2}	$R_{SENSE2}=\frac{50m}{1.6\bullet I_{OUT}}$
Step 6: L	$L_{TYP}=\frac{R_{SENSE1}\bullet V_{IN(MIN)}}{12.5m\bullet f}\bullet DC_{MAX}$ (1) $L_{MIN}=-\frac{R_{SENSE1}}{40m\bullet f\bullet DC_{MAX}}\bullet V_{OUT(NEG)}$ (2) $L_{MAX}=\frac{R_{SENSE1}\bullet V_{IN(MIN)}}{3m\bullet f}\bullet DC_{MIN}$ (3) • Solve equations 1, 2 and 3 for a range of L values. • The minimum value of the L range is the higher of L_{TYP} and L_{MIN}. The maximum of the L value range is L_{MAX}. • L = L1 = L2 for coupled inductors • L = L1 || L2 for uncoupled inductors
Step 7: C1 (Note 2)	$C1\geq\frac{I_{OUT}}{0.05\bullet V_{IN(MIN)}}\bullet\frac{DC_{MAX}}{f}, V_{RATING}>V_{IN}+\lvert V_{OUT}\rvert$
Step 8: C_{OUT}	$C_{OUT}\geq\left(\frac{4\bullet V_{IN(MAX)}}{8\bullet L\bullet f^2\bullet 0.005\bullet V_{OUT(NEG)}}\right)\bullet\left(\frac{V_{IN(MAX)}-V_{OUT(NEG)}}{2\bullet V_{IN(MAX)}-V_{OUT(NEG)}}\right)$
Step 9: C_{IN}	$C_{IN}\geq\frac{I_{OUT}}{0.005\bullet V_{IN(MIN)}\bullet f}\bullet DC_{MAX}$
Step 10: C_{IMON}	$C_{IMON}\geq\frac{100\mu A\bullet DC_{MAX}}{0.005\bullet f}$
Step 11: R_{FB}	$R_{FB}=7250\Omega\bullet\frac{V_{OUT}-V_{CTRL}}{V_{CTRL}-0.6065}$
Step 12: R_T	$R_T=\frac{35{,}880}{f}-1$; f in kHz and R_T in kΩ

NOTE 1: The final values for C_{OUT} and C_{IN} may deviate from the above equations in order to obtain desired load transient performance for a particular application. The C_{OUT} and C_{IN} equations assume zero ESR, so increase the capacitance accordingly based on the combined ESR.

NOTE 2: See the Appendix section for sizing C1 when using single inductors.

APPLICATIONS INFORMATION

SETTING THE OUTPUT VOLTAGE REGULATION

The LT8714 output voltage is set by connecting an external resistor (R_{FB}) from the converter's output, V_{OUT}, to the FB pin. The equation below determines R_{FB}:

$$R_{FB} = 7250\Omega \bullet \frac{V_{OUT} - V_{CTRL}}{V_{CTRL} - 0.6065}$$

$$V_{CTRL} = \frac{V_{OUT} + 83.7\mu A \bullet R_{FB}}{(1 + R_{FB}/7.25k)}$$

To set the output voltage, follow the three steps listed in the order below:

1. Select the highest magnitude V_{OUT} voltage (positive or negative) for the application.
2. Select the desired CTRL pin voltage (0.1V to 1.1V) for the highest magnitude V_{OUT} voltage.
3. Substitute the selected V_{OUT} voltage and CTRL pin voltage into the equation above to size R_{FB}. (Note that for negative values of R_{FB}, the selected CTRL voltage needs to be reduced).

Example 1: 10V to 14V Input → –5V to 5V Output

1. $V_{OUT} = -5V$.
2. For negative output voltages, CTRL < 0.6065. Select CTRL = 0.1V.
3. $R_{FB} = 7250\Omega \bullet \frac{-5V - 0.1V}{0.1V - 0.6065V} = 73k$; use 73.2k
4. $V_{CTRL} = \frac{5 + 83.7\mu A \bullet 73.2k}{(1 + 73.2k/7.25k)} = 1.003V$ for $V_{OUT} = 5V$

Example 2: 10V to 14V Input → –1V to 6V Output

1. $V_{OUT} = 6V$.
2. For positive output voltages, CTRL > 0.6065. Select CTRL = 1.1V.
3. $R_{FB} = 7250\Omega \bullet \frac{6V - 1.1V}{1.1V - 0.6065V} = 72k$; use 73.2k
4. $V_{CTRL} = \frac{-1 + 83.7\mu A \bullet 73.2k}{(1 + 73.2k/7.25k)} = 0.462V$ for $V_{OUT} = -1V$

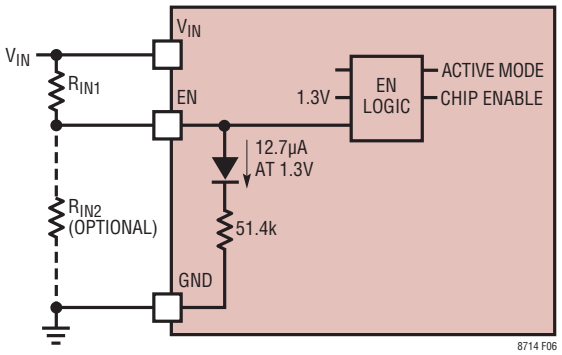


Figure 6. Enable Threshold

SETTING THE MINIMUM START-UP VOLTAGE

By connecting a resistor divider between V_{IN}, EN, and GND, a minimum input startup voltage can be set. To set the minimum input voltage, use Figure 6 as a guide.

The resistor R_{IN2} is optional, but it is recommended to increase the accuracy of the enable threshold. For increased accuracy, set $R_{IN2} \leq 10k\Omega$. To size R_{IN1} for a desired start up voltage, use the following equation below:

$$V_{IN\_START\text{-}UP} = 12.7\mu A \bullet R_{IN1} + 1.3V\left(1 + \frac{R_{IN1}}{R_{IN2}}\right)$$

OUTPUT CURRENT MONITORING AND LIMITING (R_{SENSE2} AND ISP – ISN AND IMON PINS)

The LT8714 has an output current monitor circuit that can be used to monitor and/or limit output current in Quadrants III and IV, but not in I or II. The current monitor circuit works as shown in Figure 7. If it is not desirable to monitor and limit the output current, simply connect the IMON pin to ground, tie ISP and ISN to V_{IN}, and remove R_{SENSE2}.

The current through R_{SENSE2} is sensing the current through MP which is turning on and off every clock cycle. Since the current through R_{SENSE2} is chopped, a filter capacitor connected from the IMON pin to ground is needed to filter the voltage at the IMON pin before heading to EA3. Below is the equation to calculate the required IMON pin capacitor.

$$C_{IMON} > \frac{100\mu A \bullet DC}{5mV \bullet f}$$

where DC is the duty cycle of the converter's application, and f is the switching frequency. To prevent start-up issues,

APPLICATIONS INFORMATION

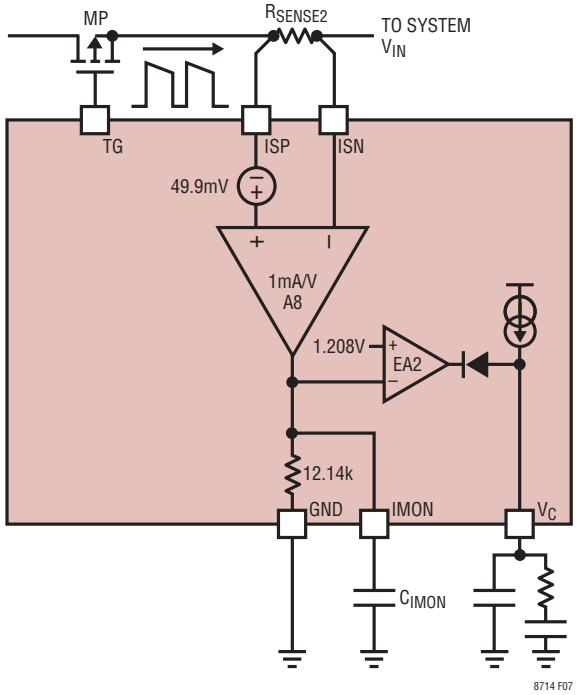


Figure 7. Output Current Monitor and Control

the IMON capacitor should charge up faster than the SS capacitor. It is recommended to size the SS capacitor at least 5× greater than the IMON capacitor.

Output Current Monitoring

The voltage at the IMON pin is an amplified version of the voltage seen across the ISP and ISN pins. Below are the equations relating the R_{SENSE2} current to the IMON pin voltage. Assume the current through R_{SENSE2} is steady state and that its time average current is approximately equal to the converter's sinking output current:

$$V_{IMON} = 12.14 \bullet (I_{RSENSE2(AVE)} \bullet R_{SENSE2} + 49.9mV)$$

$$I_{OUT} \approx I_{RSENSE2(AVE)} = \frac{\frac{V_{IMON}}{12.14} - 49.9mV}{R_{SENSE2}}$$

Output Current Limiting (Quadrants III and IV)

As shown in Figure 7, IMON voltages exceeding 1.208V (typical) causes the V_C voltage to reduce, thus limiting the inductor current. This voltage on IMON corresponds to an average voltage of 50mV across R_{SENSE2}. Below is the equation for selecting the R_{SENSE2} resistor for limiting the sinking output current for Quadrants III and IV in steady state:

$$R_{SENSE2} = \frac{50mV}{I_{OUT(LIMIT)}}$$

If it is not desirable to limit the output current in Quadrants III and IV, size R_{SENSE2} by setting $I_{OUT(LIMIT)}$ ~60% higher than the maximum output current of the converter.

SWITCH CURRENT LIMIT (R_{SENSE1} AND CSP – CSN PINS)

The external current sense resistor (R_{SENSE1}) sets the maximum peak current though the external NFET switch (MN). The maximum voltage across R_{SENSE1} is 66mV (typical) and minimum voltage is –32mV at very low switch duty cycles. The use of internal slope-compensation decreases the current limit as the duty cycle increases (see the Max Current Limit vs. Duty Cycle (CSP – CSN) plot in the Typical Performance Characteristics). The equations below give the positive and negative switch current limits for a given duty cycle and current sense resistor (find $V_{CSPN}+$ and $V_{CSPN}–$ in the operating duty cycle in the plot mentioned):

$$I_{SW+} = \frac{V_{CSPN+}}{R_{SENSE1}}$$

$$I_{SW-} = \frac{V_{CSPN-}}{R_{SENSE1}}$$

To provide a desired load current for any given application, R_{SENSE1} must be sized appropriately. The switch current will be at its highest when the input voltage is at the lowest

APPLICATIONS INFORMATION

of its range. The equations below calculates R_{SENSE1} for four quadrant operation:

$$R_{SENSE1^+} = \frac{0.74 \bullet V_{CSPN^+} \bullet \left(1 - \frac{i_{RIPPLE}}{2}\right)}{\left(\frac{I_{OUT}}{1 - DC}\right) + \left(\frac{|V_{OUT} \bullet I_{OUT}|}{V_{IN}}\right) \bullet \left(\frac{1}{\eta} - 1\right)}$$

$$R_{SENSE1^-} = \frac{0.74 \bullet V_{CSPN-} \bullet \left(1 - \frac{i_{RIPPLE}}{2}\right)}{\left(\frac{I_{OUT}}{1 - DC}\right) + \left(\frac{|V_{OUT} \bullet I_{OUT}|}{V_{IN}}\right) \bullet \left(\frac{1}{\eta} - 1\right)}$$

where:

η = Converter Efficiency (assume ~90% for Quadrants I and IV and ~80% for Quadrants II and III)

V_{CSPN}+ = Max Positive Current Limit Voltage (see Max Current Limit vs. Duty Cycle (CSP – CSN) plot in the Typical Performance Characteristics)

V_{CSPN}– = Max Negative Current Limit Voltage (see Max Current Limit vs. Duty Cycle (CSP – CSN) plot in the Typical Performance Characteristics)

I_{OUT} = Converter Output Current

DC_{MAX} = Switching Duty Cycle at Minimum V_{IN} and most negative V_{OUT}

DC_{MIN} = Switching Duty Cycle at Minimum V_{IN} and most positive V_{OUT}

i_{RIPPLE} = Peak-to-Peak Inductor Ripple Current Percentage at Minimum V_{IN} (recommended to use 25%)

CURRENT SENSE FILTERING

Certain applications may require filtering of the inductor current sense signals due to excessive switching noise that can appear across R_{SENSE1} and/or R_{SENSE2}. Higher operating voltages, higher values of R_{SENSE}, and more capacitive MOSFETs will all contribute additional noise across R_{SENSE} when MOSFETs transition. The CSP/CSN and/or the ISP/ISN sense signals can be filtered by adding one of the RC networks shown below in Figures 8 and 9.

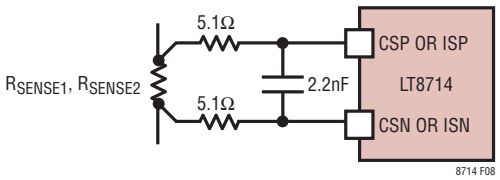


Figure 8. Differential RC Filter on CSP/CSN and/or ISP/ISN Pins

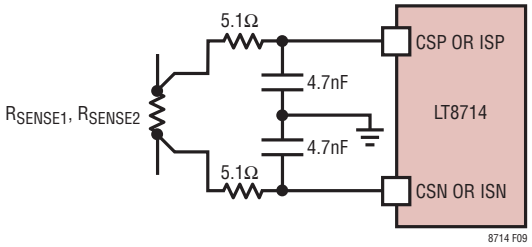


Figure 9. Differential and Common Mode RC Filter on CSP/CSN and/or ISP/ISN Pins

The filter shown in Figure 8 filters out differential noise, whereas the filter in Figure 9 filters out the differential and common mode noise at the expense of an additional capacitor and approximately twice the capacitance value. It is recommended to Kelvin the ground connection directly to the paddle of the LT8714 if using the filter in Figure 9. The filter network should be placed as close as possible to the LT8714. Resistors greater than 10Ω should be avoided as this can increase the offset voltages at the CSP/CSN and ISP/ISN pins. The RC product should be kept less than 30ns, which is simply the total series R (5.1Ω + 5.1Ω in this case) times the equivalent capacitance seen across the sense pins (2.2nF for Figure 8 and 2.35nF for Figure 9).

SWITCHING FREQUENCY

The LT8714 uses a constant frequency architecture between 100kHz and 750kHz. The frequency can be set using the internal oscillator or can be synchronized to an external clock source. Selection of the switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage. For high power applications, consider operating at lower frequencies to minimize MOSFET heating from switching losses. The switching frequency can be set by placing an

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appropriate resistor from the RT pin to ground and tying the SYNC pin low. The frequency can also be synchronized to an external clock source driven into the SYNC pin. The following sections provide more details.

Oscillator Timing Resistor (R_T)

The operating frequency of the LT8714 can be set by the internal free-running oscillator. When the SYNC pin is driven low (< 0.4V), the frequency of operation is set by a resistor from the R_T pin to ground. The oscillator frequency is calculated using the following formula:

$$f = \frac{35{,}880}{(R_T + 1)}$$

where f is in kHz and R_T is in kΩ. Conversely, R_T (in kΩ) can be calculated from the desired frequency (in kHz) using:

$$R_T = \frac{35{,}880}{f} - 1$$

Clock Synchronization

An external source can set the operating frequency of the LT8714 by providing a digital clock signal into the SYNC pin (R_T resistor still required). The LT8714 will operate at the SYNC clock frequency. The LT8714 will revert to its internal free-running oscillator clock when the SYNC pin is driven below 0.4V for a few free-running clock periods.

Driving SYNC high for an extended period of time effectively stops the operating clock and prevents latch SR1 from becoming set (see Block Diagram). As a result, the switching operation of the LT8714 will stop.

The duty cycle of the SYNC signal must be between 20% and 80% for proper operation. Also, the frequency of the SYNC signal must meet the following two criteria:

1. SYNC may not toggle outside the frequency range of 100kHz to 750kHz unless it is stopped below 0.4V to enable the free-running oscillator.
2. The SYNC frequency can always be higher than the free-running oscillator frequency (as set by the R_T resistor), f_{OSC}, but should not be less than 25% below f_{OSC}.

After SYNC begins toggling, it is recommended that switching activity is stopped before the SYNC pin stops toggling. Excess negative inductor current can result when SYNC stops toggling as the LT8714 transitions from the external SYNC clock source to the internal free-running oscillator clock. Switching activity can be stopped by driving the EN pin low.

LDO REGULATORS

The LT8714 has two linear regulators to run the BG and TG gate drivers. The $INTV_{CC}$ LDO regulates 6.3V (typical) above ground, and the $INTV_{EE}$ regulator regulates 6.18V (typical) below the BIAS pin.

$INTV_{CC}$ LDO Regulator

The $INTV_{CC}$ LDO is used as the top rail for the BG gate driver. An external capacitor greater than 2.2µF must be placed from the $INTV_{CC}$ pin to ground. The UVLO threshold on $INTV_{CC}$ is 4V (typical), and the LT8714 will be in reset until the LDO comes out of UVLO.

Overcurrent protection circuitry typically limits the maximum current draw from the LDO to 125mA. When $INTV_{CC}$ is below ~3.5V during start-up or an overload condition, the typical current limit is reduced to 25mA. If V_{IN} is greater than 20V (typical), then the current limit of the LDO reduces linearly with V_{IN} to limit the maximum power in the $INTV_{CC}$ pass device. See the $INTV_{CC}$ Current Limit vs. V_{IN} plot in the Typical Performance Characteristics. If the die temperature exceeds 175°C (typical), the current limit of the LDO drops to 0.

Power dissipated in the $INTV_{CC}$ LDO should be minimized to improve efficiency and prevent overheating of the LT8714. The current limit reduction with input voltage circuit helps prevent the part from overheating, but these guidelines should be followed. The maximum current drawn through the $INTV_{CC}$ LDO occurs under the following conditions:

1. Large (capacitive) MOSFETs being driven at high frequencies.
2. The converter's switch voltage ($2 \bullet V_{IN} - V_{OUT}$) is high, thus requiring more charge to turn the MOSFET gates on and off.

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In general, use appropriately sized MOSFETs and lower the switching frequency for higher voltage applications to keep the $INTV_{CC}$ current at a minimum.

$INTV_{EE}$ LDO Regulator

The BIAS and $INTV_{EE}$ voltages are used for the top and bottom rails of the TG gate driver respectively. An external capacitor greater than 2.2µF must be placed between the BIAS and $INTV_{EE}$ pins. The TG pin can begin switching after the $INTV_{EE}$ regulator comes out of UVLO. Overcurrent protection circuitry typically limits the maximum current draw from the regulator to 65mA. If BIAS is greater than 20V (typical), then the current limit of the regulator reduces linearly with BIAS to limit the maximum power in the $INTV_{EE}$ pass device. See the $INTV_{EE}$ Current Limit vs. BIAS plot in the Typical Performance Characteristics.

The same thermal guidelines from the $INTV_{CC}$ LDO Regulator section apply to the $INTV_{EE}$ regulator as well.

LAYOUT GUIDELINES FOR THE FOUR QUADRANT CONVERTER

General Layout Guidelines

- To optimize thermal performance, solder the exposed pad of the LT8714 to the ground plane with multiple vias around the pad connecting to additional ground planes.
- High speed switching path (see specific topology below for more information) must be kept as short as possible.
- The FB, V_C, IMON, and R_T components should be placed as close to the LT8714 as possible, while being far away as practically possible from switching nodes. The ground for these components should be separated from the switch current path.
- Place bypass capacitors for the V_{IN} and BIAS pins (C_{VIN} and C_{BIAS}) as close as possible to the LT8714.
- Place bypass capacitors for the $INTV_{CC}$ and $INTV_{EE}$ pins (C_{VCC} and C_{VEE}) as close as possible to the LT8714.
- The load should connect directly to the positive and negative terminals of the output capacitor for best load regulation.

Four Quadrant Topology Specific Layout Guidelines

Keep the length of high speed switching path governing C_{IN}, R_{SENSE1}, MN, C1, MP, R_{SENSE2}, and ground return as short as possible to minimize parasitic inductive spikes at the switch node during switching.

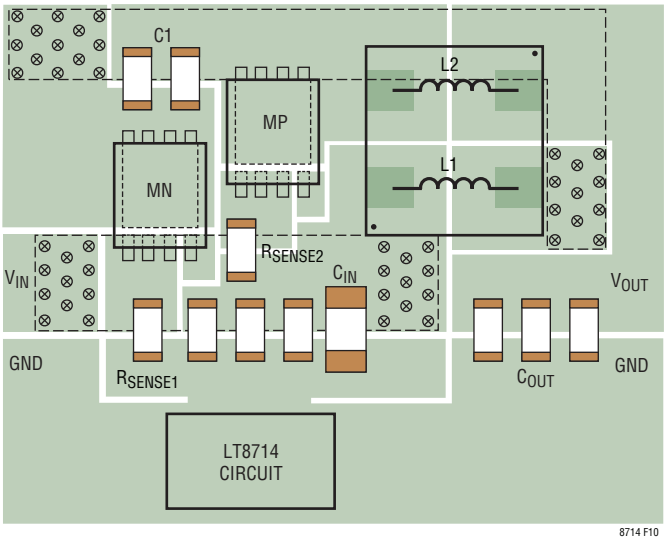

Figure 10: Suggested Component Placement for the Four Quadrant Converter

Current Sense Resistor Layout Guidelines

- Route the CSP/CSN and ISP/ISN lines differentially (close together) from the chip to the current sense resistor as shown in Figure 11.
- For the most accurate current sensing, make an inner cut out in the sense resistor foot print so that the kelvin connection does not introduce any additional offset on the CSP – CSN or ISP – ISN pins.

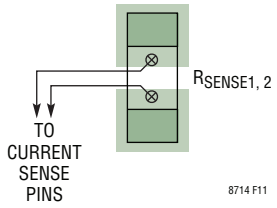

Figure 11: Suggested Routing and Connections of CSP/CSN and ISP/ISN Lines

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THERMAL CONSIDERATIONS

Overview

The primary components on the board that dissipate the most power and produce the most heat are the power switches, MN and MP, the power inductor, sense resistors, and the LT8714 IC. It is imperative that a good thermal path be provided for these components to dissipate the heat generated within the packages. This can be accomplished by taking advantage of the thermal pads on the underside of the packages. It is recommended that multiple vias in the printed circuit board be used to conduct heat away from each of these components and into a copper plane with as much area as possible. For the case of the power switches, the copper area of the drain connections shouldn't be too big as to create a large EMI surface that can radiate noise around the board.

Power MOSFET Loss and Thermal Calculations

The LT8714 requires two external power MOSFETs, an NFET switch for the BG gate driver and a PFET switch for the TG gate driver. Important parameters for estimating the power dissipation in the MOSFETs are:

1. On-Resistance (R_{DSON})
2. Gate-to-Drain Charge (Q_{GD})
3. Body Diode Forward Voltage (V_{BD})
4. V_{DS} of the FETs during their "Off-Time"
5. Switch Current (I_{SW})
6. Switching Frequency (f)

The power loss in each power switch has a DC and AC term. The DC term is when the power switch is fully on, and the AC term is when the power switch is transitioning from on-off or off-on.

The following applies for both the NFET and PFET power switches. For the four quadrant topology, the average current through each MOSFET (I_{SW}) during its on-time is:

$$I_{SW} \approx \frac{I_{OUT}}{(1-DC)} + \frac{|V_{OUT} \bullet I_{OUT}|}{4V_{IN}}$$

The $|V_{DS}|$ voltage during the off-time is approximately $2V_{IN} - V_{OUT}$. During the non-overlap time of the gate drivers, the inductor current flows through the body diode of either the NFET or PFET, depending on the polarity of I_{OUT}. Below are the equations for the power loss in MN and MP.

For Quadrants I and II:

$$P_{MOSFET} = P_{I^2R} + P_{SWITCHING}$$

$$P_{MP} = I_P{}^2 \bullet R_{DSON} + V_{DS} \bullet I_P \bullet f \bullet t_{RF}$$

$$P_{MN} = I_N{}^2 \bullet R_{DSON} + V_{BD} \bullet \left(\frac{I_{PK}}{1.6} + I_{VY} \right) \bullet f \bullet 140ns$$

$$I_{PK} = I_{SW} + \frac{i_{RIPPLE}}{2}; \quad I_{VY} = I_{SW} - \frac{i_{RIPPLE}}{2}$$

$$I_N = \sqrt{DC \bullet \left(I_{SW}{}^2 + \frac{i_{RIPPLE}{}^2}{12} \right)}$$

$$I_P = \sqrt{(1-DC) \bullet \left(I_{SW}{}^2 + \frac{i_{RIPPLE}{}^2}{12} \right)}$$

$$P_{RR-N} \approx V_{DS} \bullet Q_{RR-N} \bullet f$$

For Quadrants III and IV:

$$P_{MOSFET} = P_{I^2R} + P_{SWITCHING}$$

$$P_{MN} = I_N{}^2 \bullet R_{DSON} + V_{DS} \bullet I_N \bullet f \bullet t_{RF}$$

$$P_{MP} = I_P{}^2 \bullet R_{DSON} + V_{BD} \bullet \left(\frac{I_{PK}}{1.6} + I_{VY} \right) \bullet f \bullet 140ns$$

$$I_{PK} = I_{SW} + \frac{i_{RIPPLE}}{2}; \quad I_{VY} = I_{SW} - \frac{i_{RIPPLE}}{2}$$

$$I_N = \sqrt{DC \bullet \left(I_{SW}{}^2 + \frac{i_{RIPPLE}{}^2}{12} \right)}$$

$$I_P = \sqrt{(1-DC) \bullet \left(I_{SW}{}^2 + \frac{i_{RIPPLE}{}^2}{12} \right)}$$

$$P_{RR-P} \approx V_{DS} \bullet Q_{RR-P} \bullet f$$

where:

f = Switching Frequency

I_N = NFET RMS Current

I_P = PFET RMS Current

t_{RF} = Average of the rise and fall times of the NFET's drain voltage

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I_{PK} = Peak inductor current

I_{VY} = Valley inductor current

i_{RIPPLE} = Inductor ripple current

DC = Switch duty cycle (see Power Switch Duty Cycle section in Appendix)

V_{BD} = NFET or PFET body diode forward voltage at

I_{SW} = Switch current in the NFET or PFET

P_{RR-N} = NFET body diode reverse recovery power loss

P_{RR-P} = PFET body diode reverse recovery power loss

Q_{RR-N} = Reverse recovery charge stored in the junction capacitance of the NFET body diode

Q_{RR-P} = Reverse recovery charge stored in the junction capacitance of the PFET body diode

Typical values for t_{RF} are 10 to 40ns depending upon the MOSFET capacitance and drain voltage. In general, the lower the Q_{GD} of the MOSFET, the faster the rise and fall times of its drain voltage. For best calculations, measure the rise and fall times in the application.

Body diode reverse recovery power loss is dependent on many factors and can be difficult to quantify in an application. In general, this power loss is split between the NFET and PFET by a ratio and increases with higher V_{DS} and/or higher switching frequency.

Chip Power and Thermal Calculations

Power dissipation in the LT8714 chip comes from three primary sources: $INTV_{CC}$ and $INTV_{EE}$ LDOs providing gate drive to the BG and TG pins and additional input quiescent current. The average current through each LDO is determined by the gate charge of the power switches, MN and MP, and the switching frequency. Below are the equations for calculating the chip power loss followed by an example. For the four quadrant converter, BIAS is always tied to V_{IN}, so all of the chip power comes from V_{IN}. V_{IN} primarily supplies the chip Q current, and power for both the BG and TG gate drivers. Below are the chip power equations for the four quadrant converter:

$$P_{VCC} = 1.04 \bullet Q_{MN} \bullet f \bullet V_{IN}$$
$$P_{VEE1} = Q_{MP} \bullet f \bullet V_{IN}$$
$$P_{VEE2} = 3.15mA \bullet (1 - DC) \bullet V_{IN}$$
$$P_{Q} = 4mA \bullet V_{IN}$$

where:

f = Switching frequency

DC = Switch duty cycle (see Power Switch Duty Cycle section in Appendix)

Q_{MN} = Total gate charge of NFET power switch (MN) at $6.3V_{GS}$

Q_{MP} = Total gate charge of PFET power switch (MP) at $6.18V_{SG}$

Chip Power Calculations Example

Table 2 calculates the power dissipation of the LT8714 for a 200kHz, 10V to 14V to ±5V/±5A application when V_{IN} is 12V. From P_{CHIP} in Table 2, the die junction temperature can be calculated using the appropriate thermal resistance and worst-case ambient temperature:

$$T_J = T_A + \theta_{JA} \bullet P_{CHIP}$$

where T_J = die junction temperature, T_A = ambient temperature and θ_{JA} is the thermal resistance from the silicon junction to the ambient air.

The published θ_{JA} value is 38°C/W for the TSSOP Exposed Pad package. In practice, lower θ_{JA} values are realizable if board layout is performed with appropriate grounding (accounting for heat sinking properties of the board) and other considerations listed in the Layout Guidelines section. For instance, a θ_{JA} value of ~22°C/W was consistently achieved when board layout was optimized as per the suggestions in the Layout Guidelines section.

THERMAL LOCKOUT

If the die temperature reaches ~175°C, the part will go into reset, so the power switches turn off and the soft-start capacitor will be discharged. The LT8714 will come out of reset when the die temperature drops by ~5°C (typical).

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Table 2. Power Calculations Example for a 200kHz, 10V to 14V to ±5V/±5A. (V_{IN} = 12V, V_{OUT} = –5V, MN = BSC093N04LSG and MP = STL60P4LLF6 ×2)

DEFINITION OF VARIABLES	EQUATION	DESIGN EXAMPLE	VALUE
DC = Switch Duty Cycle	$DC \cong \frac{V_{IN} - V_{OUT}}{2V_{IN} - V_{OUT}}$	$DC \cong \frac{12V - (-5V)}{2 \bullet 12V - (-5V)}$	$DC \cong 58.6\%$
P_{VCC} = $INTV_{CC}$ LDO Power Driving the BG Gate Driver Q_{MN} = NFET Total Gate Charge at V_{GS} = 6.3V f = Switching Frequency	$P_{VCC} = 1.04 \bullet Q_{MN} \bullet f \bullet V_{IN}$	$P_{VCC} = 1.04 \bullet 12nC \bullet 200kHz \bullet 12V$	P_{VCC} = 30mW
P_{VEE1} = $INTV_{EE}$ LDO Power Driving the TG Gate Driver Q_{MP} = PFET Total Gate Charge at V_{SG} = 6.18V	$P_{VEE1} = Q_{MP} \bullet f \bullet V_{IN}$	$P_{VEE1} = 2 \bullet 44nC \bullet 200kHz \bullet 12V$	P_{VEE1} = 211.2mW
P_{VEE2} = Additional TG Gate Driver Power Loss	$P_{VEE2} = 3.15mA \bullet (1 - DC) \bullet V_{IN}$	$P_{VEE2} = 3.15mA \bullet (1 - 0.586) \bullet 12V$	P_{VEE2} = 15.65mW
P_Q = Chip Bias Loss	$P_Q = 4mA \bullet V_{IN}$	$P_Q = 4mA \bullet 12V$	P_Q = 48mW
			P_{CHIP} = 304.85mW

APPENDIX

POWER SWITCH DUTY CYCLE

In order to maintain loop stability and deliver adequate current to the load, the external power NFET (MN in the Block Diagram) cannot remain "on" or "off" for 100% of each clock cycle.

For Quadrants I and II, the maximum allowable duty cycle is given by:

$$DC_{MAX} = \frac{T_P - MinOnTime_{TG}}{T_P} \bullet 100\%$$

where T_P is the clock period and $MinOnTime_{TG}$ (found in the Electrical Characteristics) is a max of 150ns.

The minimum duty cycle is given by:

$$DC_{MIN} = \frac{MinOffTime_{TG}}{T_P} \bullet 100\%$$

Where $MinOffTime_{TG}$ = 770ns.

For Quadrants III and IV, the maximum allowable duty cycle is given by:

$$DC_{MAX} = \frac{T_P - MinOffTime_{BG}}{T_P} \bullet 100\%$$

where T_P is the clock period and $MinOffTime_{BG}$ (found in the Electrical Characteristics) is a max of 480ns.

The minimum duty cycle is given by:

$$DC_{MIN} = \frac{MinOnTime_{BG}}{T_P} \bullet 100\%$$

where T_P is the clock period and $MinOnTime_{BG}$ (found in the Electrical Characteristics) is a max of 420ns.

The application should be designed such that the operating duty cycle is between DC_{MIN} and DC_{MAX} for both positive and negative output voltages.

The duty cycle equation for the four quadrant converter is given below where V_{ON_MP} is the voltage drop across the external power PFET (MP) when it is "on", and V_{ON_MN} is the voltage drop across the external power NFET (MN) when it is "on".

For the four quadrant converter:

$$DC \cong \frac{V_{IN} - V_{OUT} + V_{ON\_MP}}{2V_{IN} - V_{OUT} + V_{ON\_MP} - V_{ON\_MN}}$$

INDUCTOR SELECTION

For high efficiency, choose inductors with high frequency core material, such as ferrite, to reduce core losses. Also to improve efficiency, choose inductors with more volume for a given inductance. The inductor should have low DCR (copper-wire resistance) to reduce I^2R losses, and must be able to handle the peak inductor current without saturating. Molded chokes or chip inductors do not have enough core area to support peak inductor currents in the 5A to 15A range. To minimize radiated noise, use a toroidal or shielded inductor. See Table 3 for a list of inductor manufacturers.

Table 3. Inductor Manufacturers

Coilcraft	MSS1278, XAL1010, MSD1583 and MSD1278 Series	www.coilcraft.com
Cooper Bussmann	DR127, DRQ127, and HCM1104 Series	www.cooperbussmann.com
Vishay	IHLP Series	www.vishay.com
Wurth	WE-DCT Series WE-CFWI Series 6.8µH, 74485540680 8.2µH,74485540820 10µH, 74485540101	www.we-online.com

Minimum Inductance

Although there can be a trade-off between efficiency and size, it is often desirable to minimize board space by choosing smaller inductors. When choosing an inductor, there are three conditions that limit the minimum inductance: (1) providing adequate load current, (2) avoiding subharmonic oscillation, and (3) supplying minimum ripple current to avoid false tripping of the current comparator.

APPENDIX

Adequate Load Current

Small value inductors result in increased ripple currents and thus, due to the limited peak switch current, decrease the average current that can be provided to the load. In order to provide adequate load current, L should be at least:

$$L \geq \frac{V_{IN} \bullet DC}{2 \bullet f \bullet \left(\frac{V_{CSPN}}{R_{SENSE1}} - \frac{I_{OUT}}{(1-DC)} - \frac{|V_{OUT} \bullet I_{OUT}|}{4V_{IN}} \right)}$$

where:

L = $L_1 = L_2$ for coupled inductors

L = $L_1 \,||\, L_2$ for uncoupled inductors

DC = Switch duty cycle (see previous section)

V_{CSPN} = Current limit voltage at the operating switch duty cycle (see Max Current Limit vs Duty Cycle (CSP – CSN) plot in the Typical Performance Characteristics)

R_{SENSE1} = Current sense resistor connected across the CSP – CSN pins (see Block Diagram)

f = Switching frequency

I_{OUT} = Maximum output current

Negative values of L indicate that the output load current, I_{OUT}, exceeds the switch current limit capability of the converter. Decrease R_{SENSE1} to increase the switch current limit.

Avoiding Sub-Harmonic Oscillations

The LT8714's internal slope compensation circuit will prevent sub-harmonic oscillations that can occur when the duty cycle is greater than 50%, provided that the inductance exceeds a minimum value. In applications that operate with duty cycles greater than 50%, the inductance must be at least:

$$L_{MIN} \geq -\frac{R_{SENSE1}}{40m \bullet f \bullet DC} \bullet V_{OUT}$$

where:

$L_{MIN} = L_1 = L_2$ for coupled inductors

$L_{MIN} = L_1 \,||\, L_2$ for uncoupled inductors

Maximum Inductance

Excessive inductance can reduce ripple current to levels that are difficult for the current comparator (A5 in the Block Diagram) to cleanly discriminate, thus causing duty cycle jitter and/or poor regulation. The maximum inductance can be calculated by:

$$L_{MAX} \leq \frac{V_{IN} \bullet R_{SENSE1} \bullet DC}{3m \bullet f}$$

where:

$L_{MAX} = L_1 = L_2$ for coupled inductors

$L_{MAX} = L_1 \,||\, L_2$ for uncoupled inductors

Inductor Current Rating

The inductor(s) must have a rating greater than their peak operating current to prevent inductor saturation, which would result in efficiency losses. The maximum inductor current (considering start-up and steady-state conditions) is given by:

$$I_{L\_PK\_POS} = \frac{66mV - 16mV \bullet DC^2}{R_{SENSE1}} + \frac{V_{IN} \bullet 100ns}{L}$$

$$I_{L\_VY\_NEG} = \frac{-32mV - 16mV \bullet DC^2}{R_{SENSE1}} + \frac{V_{IN} \bullet 190ns}{L} - \frac{V_{IN} \bullet DC}{L \bullet f}$$

$$I_{L1,MAX} = I_{L\_MAX} - I_{L2,MAX}$$

$$I_{L2,MAX} = I_{L\_MAX} \bullet (1-DC)$$

where:

$I_{L\_PK\_POS}$ = Sum of the peak inductor currents for Quadrants III and IV

$I_{L\_VY\_NEG}$ = Sum of the peak inductor currents for Quadrants I and II

APPENDIX

I_{L_MAX} = Peak or valley current in L1 + L2

I_{L1_MAX} = Peak or valley current in L1

I_{L2_MAX} = Peak or valley current in L2

Note that these equations offer conservative results for the required inductor current ratings. The current ratings could be lower for applications with light loads, and if the SS capacitor is sized appropriately to limit inductor currents at start-up.

Coupling Network for Tightly Coupled Inductors

The capacitor C1 that is connected between the two inductor windings is called the DC link or flying capacitor. Its purpose is to serve as a floating voltage source that virtually connects the input side and output side of the converter.

The most optimal value for C1 is given in the equation:

$$C1 \geq \frac{I_{OUT}}{0.05 \bullet V_{IN(MIN)}} \bullet \frac{DC_{MAX}}{f}$$

No RC damping network is needed across C1.

Coupling Network for Single Inductors

Two discrete inductors shown in Figure 12 maybe used instead of a coupled inductor with a few requirements.

1. Size the flying capacitor C1 according to the equation:

$$C1 \geq \frac{I_{OUT}}{0.25 \bullet V_{IN(MIN)}} \bullet \frac{DC_{MAX}}{f}$$

2. Calculate C_{DAMP}

$$C_{DAMP} > 2 \bullet C1$$

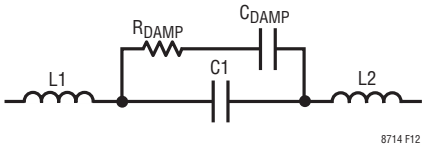


Figure 12. RC Damp Network for Discrete Inductors

3. Calculate R_{DAMP}

$$R_{DAMP} \approx \sqrt{\frac{L1+L2}{C1}}$$

It should be noted that the value calculated for C1 is a starting point. The value of C1 is a trade-off between transient stability and power dissipation in R_{DAMP}. As C1 increases, the power dissipated in R_{DAMP} reduces, but transient performance may be worse. The application should be evaluated and C1 may need to be adjusted to achieve optimal performance.

Coupling Network for Loosely Coupled Inductors

An RC damp network maybe required even if using coupled inductors to damp out the resonance between the leakage inductances of L1 and L2, and capacitor C1.

In this case, calculate C_{DAMP} as before for single inductors. To calculate R_{DAMP}, replace L1 and L2 with L_{LK1} and L_{LK2}, which can be found in the manufacture's data sheet

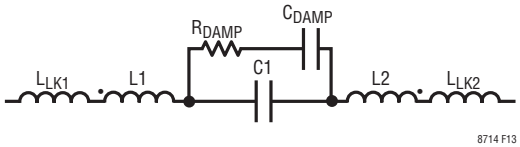


Figure 13. RC Damp Network for Coupled Inductors

or contacting the inductor's manufacturer.

1. Size the flying capacitor C1 according to the equation:

$$C1 \geq \frac{I_{OUT}}{0.25 \bullet V_{IN(MIN)}} \bullet \frac{DC_{MAX}}{f}$$

2. Calculate C_{DAMP}

$$C_{DAMP} > 2 \bullet C1$$

3. Calculate R_{DAMP}

$$R_{DAMP} \approx \sqrt{\frac{L_{LK1}+L_{LK2}}{C1}}$$

APPENDIX

It should be noted that the value calculated for C1 is a starting point. The value of C1 is a trade-off between transient stability and power dissipation in R_{DAMP}. As C1 increases, the power dissipated in R_{DAMP} reduces, but transient performance may be worse. The application should be evaluated and C1 may need to be adjusted to achieve optimal performance.

INPUT AND OUTPUT CAPACITOR SELECTION

Input and output capacitance is necessary to suppress voltage ripple caused by discontinuous current moving in and out of the regulator. A parallel combination of capacitors is typically used to achieve high capacitance and low ESR (equivalent series resistance). Tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Capacitors with low ESR and high ripple current ratings, such as OS-CON and POSCAP are also available.

Ceramic capacitors should be placed near the regulator input and output to suppress high frequency switching noise. A minimum 1µF ceramic capacitor should also be placed from V_{IN} to GND and from BIAS to GND as close to the LT8714 pins as possible. Due to their excellent low ESR characteristics, ceramic capacitors can significantly reduce ripple voltage and help reduce power loss in the higher ESR bulk capacitors. X5R or X7R dielectrics are preferred, as these materials retain their capacitance over wide voltage and temperature ranges. Many ceramic capacitors, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired operating voltage.

Input Capacitor, C_{IN}

The input capacitor, C_{IN}, carries the high frequency chopped current and must be sized appropriately. Below is the equation for calculating the capacitance of C_{IN} for 0.5% input voltage ripple:

$$C_{IN} \geq \frac{I_{OUT}}{0.005 \bullet V_{IN} \bullet f} \bullet DC$$

where:

DC = Switch duty cycle (see Power Switch Duty Cycle section)

f = Switching frequency

The worst case for the input capacitor (largest capacitance needed) is when the input voltage is at its lowest because the duty cycle is the highest. Keep in mind that the voltage rating of the input capacitor needs to be greater than the maximum input voltage. This equation calculates the capacitance value during steady-state operation and may need to be adjusted for desired transient response. Also, this assumes no ESR, so the input capacitance may need to be larger depending on the equivalent ESR of the input capacitor(s).

Output Capacitor, C_{OUT}

The output capacitor, C_{OUT}, sees the inductor ripple current. Below is the equation for calculating the capacitance of C_{OUT} for 0.5% output voltage ripple:

$$C_{OUT} \geq \frac{V_{IN} \bullet DC}{8 \bullet L \bullet f^2 \bullet 0.005 \bullet V_{OUT}}$$

where:

DC = Switch duty cycle (see Power Switch Duty Cycle section)

L = Inductance Value

f = Switching frequency

The worst case for the output capacitor (largest capacitance needed) is when the output regulation voltage is at its most negative value. This equation calculates the capacitance value during steady-state operation and may need to be adjusted for desired transient response. Also, this assumes no ESR, so the output capacitance may need to be larger depending on the equivalent ESR of the output capacitor(s). See Table 4 for a list of ceramic capacitor manufacturers.

APPENDIX

Table 4. Ceramic Capacitor Manufacturers

TDK	www.tdk.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com

POWER MOSFET SELECTION

The LT8714 requires two external power MOSFETs, an NFET switch for the BG gate driver and a PFET switch for the TG gate driver. It is important to select MOSFETs for optimizing efficiency. For choosing an NFET and PFET, the important device parameters are:

1. Breakdown Voltage (BV_{DSS})
2. Gate Threshold Voltage (V_{GSTH})
3. On-Resistance (R_{DSON})
4. Total Gate Charge (Q_G)
5. Turn-Off Delay Time ($t_{D(OFF)}$)
6. Package has Exposed Paddle

The drain-to-source breakdown voltage of the NFET and PFET power MOSFETs must exceed:

$$BV_{DSS} > 2V_{IN} - V_{OUT}$$

If operating close to the BV_{DSS} rating of the MOSFET, check the leakage specifications on the MOSFET because leakage can decrease the efficiency of the converter.

The gate to source voltage affects the on-resistance and total gate charge of the FETs. In general, power MOSFET on-resistance and total gate charge go hand-in-hand and are typically inversely proportional to each other; the lower the on-resistance, the higher total gate charge. Choose MOSFETs with an on-resistance to give a voltage drop to be less than 300mV at the peak current. At the same time, choose MOSFETs with a lower total gate charge to reduce LT8714 power dissipation and MOSFET switching losses.

It should be noted that for high input to output voltage applications, reverse recovery loss can be a noticeable power loss term in both FETs due to four quadrant operation of the LT8714. In these applications, it may be beneficial to put a Schottky diode in parallel with both FET's to shunt the internal body diodes. Note that the Schottky diode forward drop must be smaller than the body diode forward voltage.

The turn-off delay time ($t_{D(OFF)}$) of available NFETs is generally smaller than that of available PFETs. However, the delay time of both FETs should be checked for a given application due to four quadrant operation of the LT8714. The turn-off delay time of the PFET as specified by the data sheet must be less than ~140ns. The turn-off delay time of the NFET as specified by the data sheet must be less than ~90ns. If the turn-off delay times as specified by the data sheets of both FETs are longer than the respective non-overlap times, the FETs may still be good to use. To verify, measure the NFET and PFET turn-off delay times directly at the gate pin of both FETs.

The NFET and PFET gate-to-source drive is approximately 6.3V and 6.18V respectively, so logic level MOSFETs are required. The BG gate driver can begin switching when the $INTV_{CC}$ voltage exceeds ~4V. To prevent possible damage to the NFET, ensure that the selected NFET is in the triode region of operation with 4V of gate-to-source drive. The TG gate driver can begin switching when the BIAS to $INTV_{EE}$ voltage exceeds ~3.45V, so it is optimal that the PFET be in the linear mode of operation with 3.45V of gate-to-source drive.

Finally, both the NFET and PFET power MOSFETs should be in a package with an exposed paddle for the drain connection to be able to dissipate heat. The on-resistance of MOSFETs is proportional to temperature, so it's more efficient if the MOSFETs are running "cool" with the help of the exposed paddle. See Table 5 for a list of power MOSFET manufacturers and Table 6 for a list of recommended PFET's.

Table 5. Power MOSFET (NFET and PFET) Manufacturers

Fairchild Semiconductor	www.fairchildsemi.com
On-Semiconductor	www.onsemi.com
Vishay	www.vishay.com
Diodes Inc.	www.diodes.com
Infineon	www.infineon.com
ST Microelectronics	www.st.com

APPENDIX

Table 6. Recommended PFETs

20V	SI7635DP, SI7633DP	www.vishay.com
30V	SI7101DN, SI7143DP	www.vishay.com
40V	FDD4141, SI7463ADP, SIS443DN, SI7611DN STL604PLLF6	www.fairchildsemi.com, www.vishay.com www.st.com
60V	SI7465DP, SUD19P06-60, SUD50P06-15 STL42P6LLF6	www.vishay.com www.st.com
100V	FDMC86139P, SI7113DN	www.fairchildsemi.com, www.vishay.com

COMPENSATION – ADJUSTMENT

To compensate the feedback loop of the LT8714, a series resistor-capacitor network in parallel with an optional single capacitor should be connected from the V_C pin to GND. For most applications, choose a series capacitor in the range of 1nF to 10nF with 4.7nF being a good starting value. The optional parallel capacitor should range in value from 47pF to 220pF with 100pF being a good starting value. The compensation resistor, R_C, is usually in the range of 5kΩ to 50kΩ. A good technique to compensate a new application is to use a 100kΩ potentiometer in place of the series resistor R_C. With the series and parallel capacitors at 4.7nF and 100pF respectively, adjust the potentiometer while observing the transient response and the optimum value for R_C can be found. The series capacitor can be reduced or increased from 4.7nF to speed up the converter or slow down the converter, respectively. For the circuit in Figure 5, a 10nF series cap was used. Figures 14 to 16 illustrate the process of tuning R_C for the circuit of Figure 5 with a load current stepped between 1A and 3.5A with an input voltage of 10V. Figure 14 shows the transient response with R_C equal to 1.04kΩ. The phase margin is poor as evidenced by the excessive ringing in the output voltage and inductor current. In Figure 15, the value of R_C is increased to 2.74kΩ, which results in a more damped response. Figure 16 shows the results when R_C is increased further to 4.75kΩ. The transient response is nicely damped and the compensation procedure is complete.

Note the load transient plots shown are for Quadrant I. The R_C value may need to be adjusted to find a balance to ensure stability in all four quadrants.

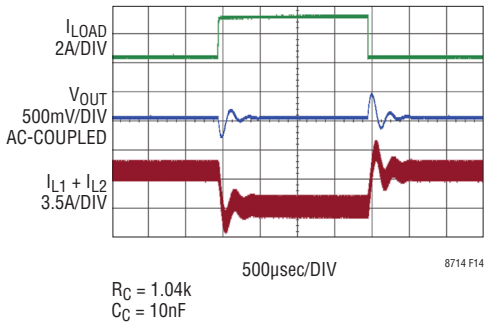


Figure 14: Transient Response Shows Excessive Ringing

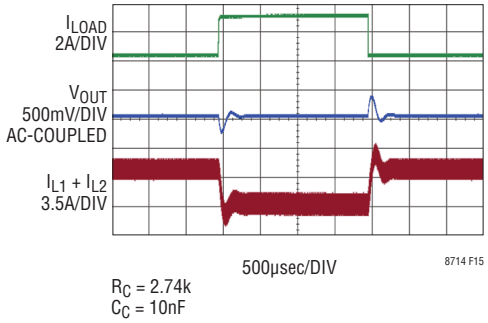


Figure 15: Transient Response Is Improved

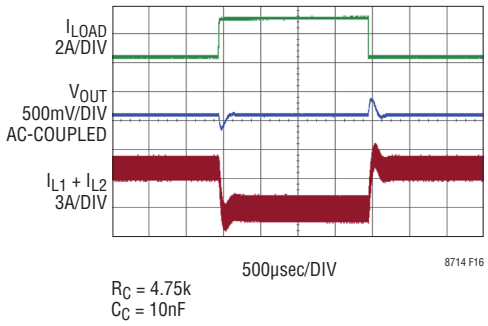
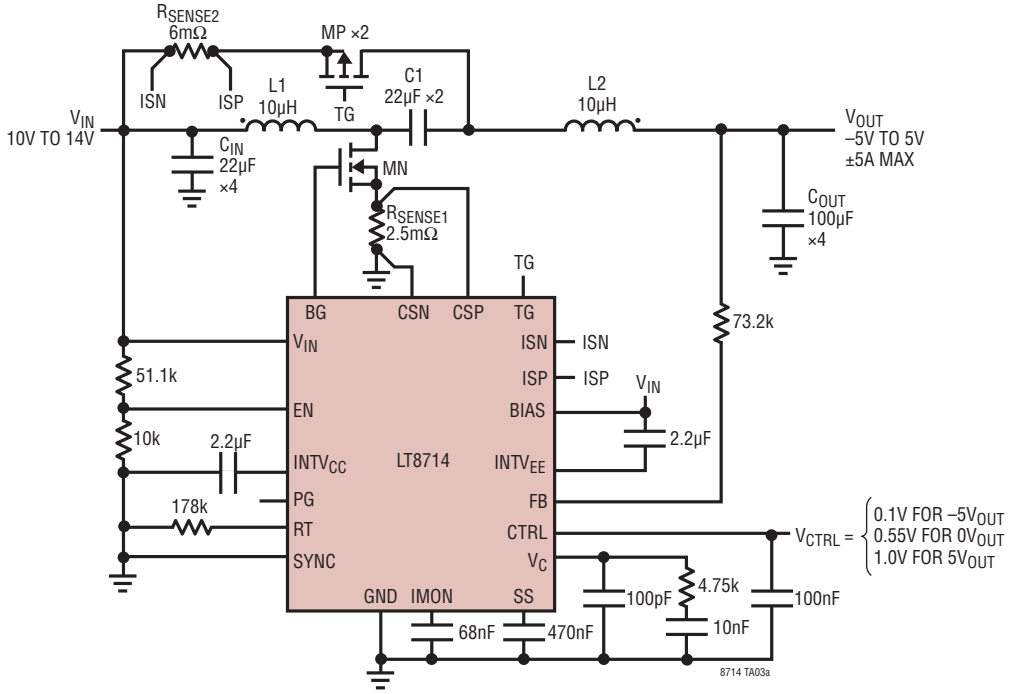


Figure 16: Transient Response Is Well Damped

TYPICAL APPLICATIONS

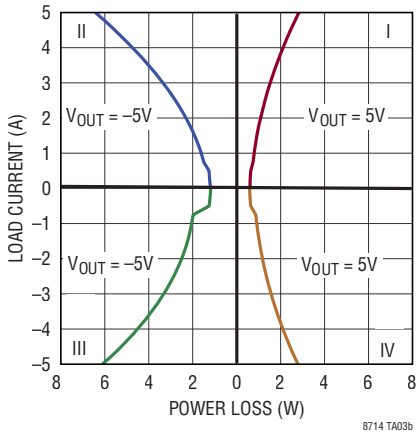
200kHz, 10V to 14V Input Generates a –5V to 5V Output that Delivers –5A to 5A of Output Current



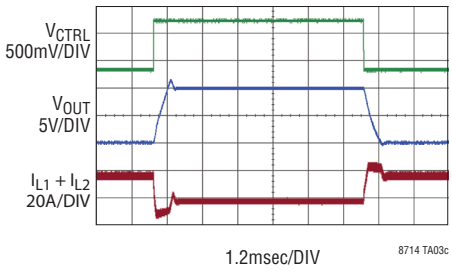
L1, L2: WURTH 10µH WE-CFWI 74485540101
MN: INFINEON BSC093N04LSG
MP: STMICRO STL60P4LLF6

C_{IN}, C1: 22µF, 25V, 1812, X7R
C_{OUT}: 100µF, 16V, 1210, X5R
R_{SENSE1}: 2.5mΩ, 2512
R_{SENSE2}: 6mΩ, 2512

Power Loss in Each Quadrant (V_{IN} = 12V)

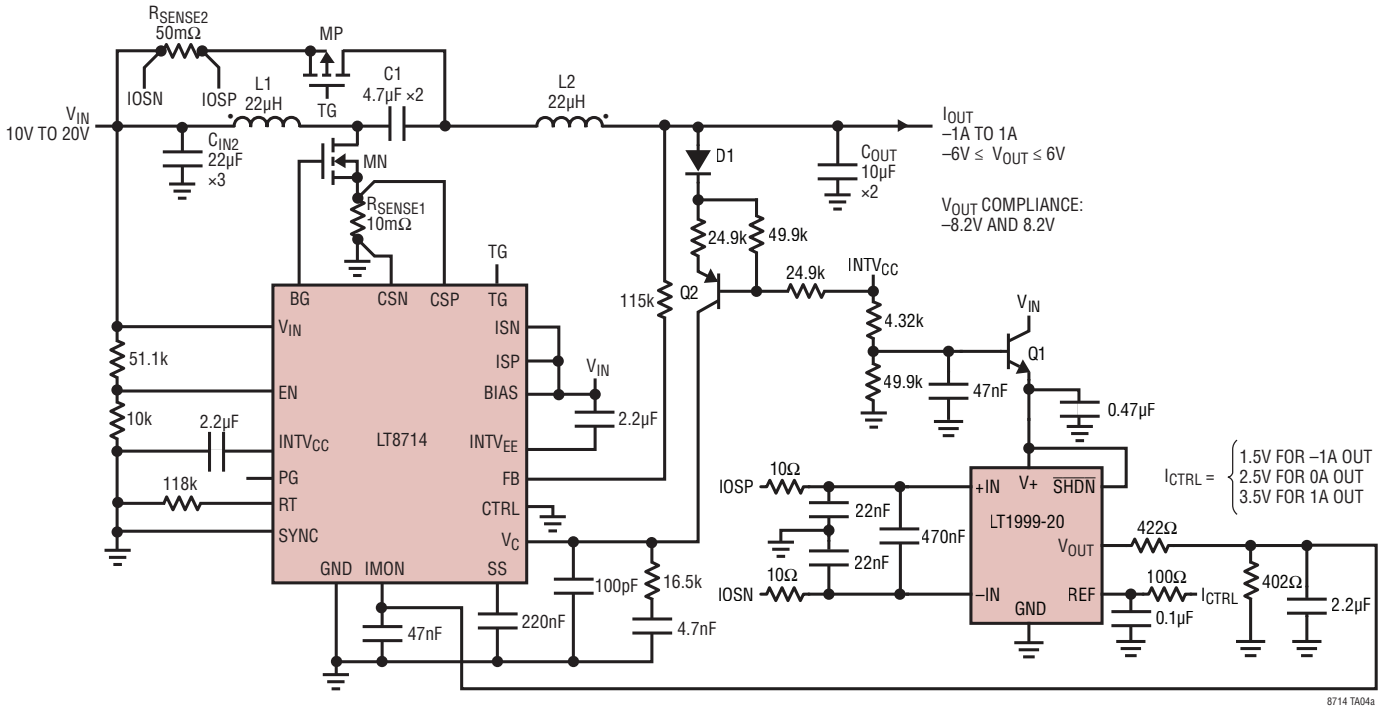


V_{CTRL} Step from 0.1V to 1V to 0.1V (R_{LOAD} = 1Ω)



TYPICAL APPLICATIONS

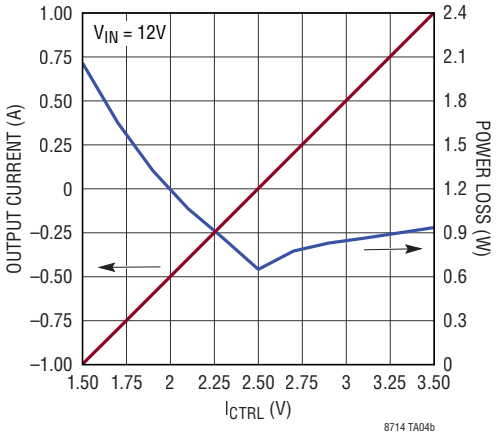
300kHz, Bidirectional 1A Current Source



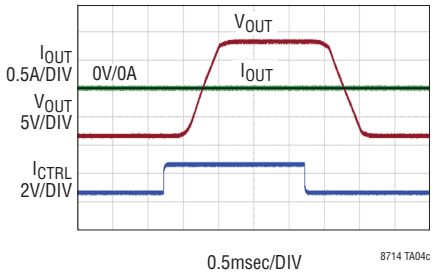
L1, L2: COILCRAFT 22µH MSD1278-223ML
MN: FAIRCHILD FDMC86570L
MP: STMICRO STL42P6LLF6
Q1: CENTRAL SEMI CMST3904
Q2: CENTRAL SEMI CMST3906
D1: CENTRAL SEMI CMDD4448

C_{IN}: 22µF, 25V, 1812, X7R
C1: 4.7µF, 50V, 1210, X7R
C_{OUT}: 10µF, 16V, 1210, X7R
R_{SENSE1}: 10mΩ, 1206
R_{SENSE2}: 50mΩ, 2512

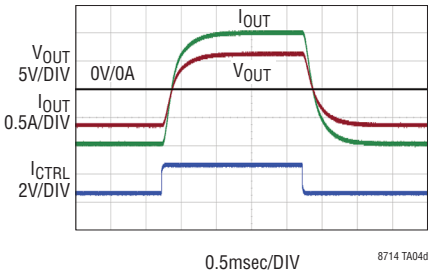
Output Current and Power Loss vs I_{CTRL} (R_{LOAD} = 6Ω)



I_{CTRL} Step from 1.5V to 3.5V to 1.5V at V_{IN} = 12V (No Load)

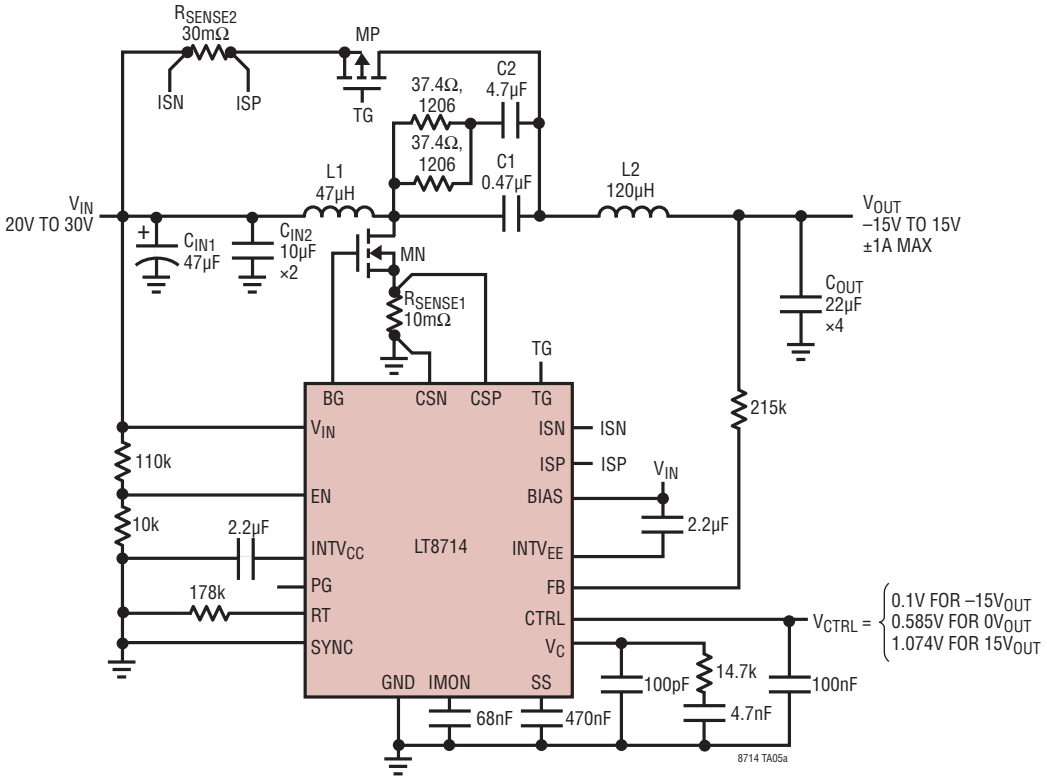


I_{CTRL} Step from 1.5V to 3.5V to 1.5V at V_{IN} = 12V (R_{LOAD} = 6Ω)



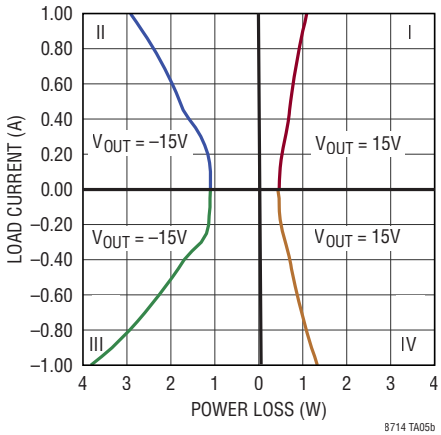
TYPICAL APPLICATIONS

200kHz, 20V to 30V Input Generates a –15V to 15V Output that Delivers –1A to 1A of Output Current

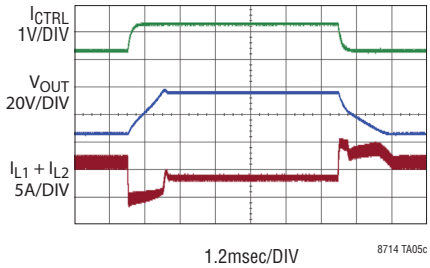


L1: COILCRAFT 47µH MSS1278T-473KL
L2: COILCRAFT 120µH MSS1278T-124KL
MN: FAIRCHILD FDMC86102
MP: FAIRCHILD FDMC86139P
C_{IN1}: 47µF, 50V AVX TCJE476M035R0055
C_{IN2}: 10µF, 50V, 1210, X7S
C1: 0.47µF, 100V, 1812, X7R
C2: 4.7µF, 100V, 1812, X7R
C_{OUT}: 22µF, 25V, 1812, X7R
R_{SENSE1}: 10mΩ, 2512
R_{SENSE2}: 30mΩ, 2512

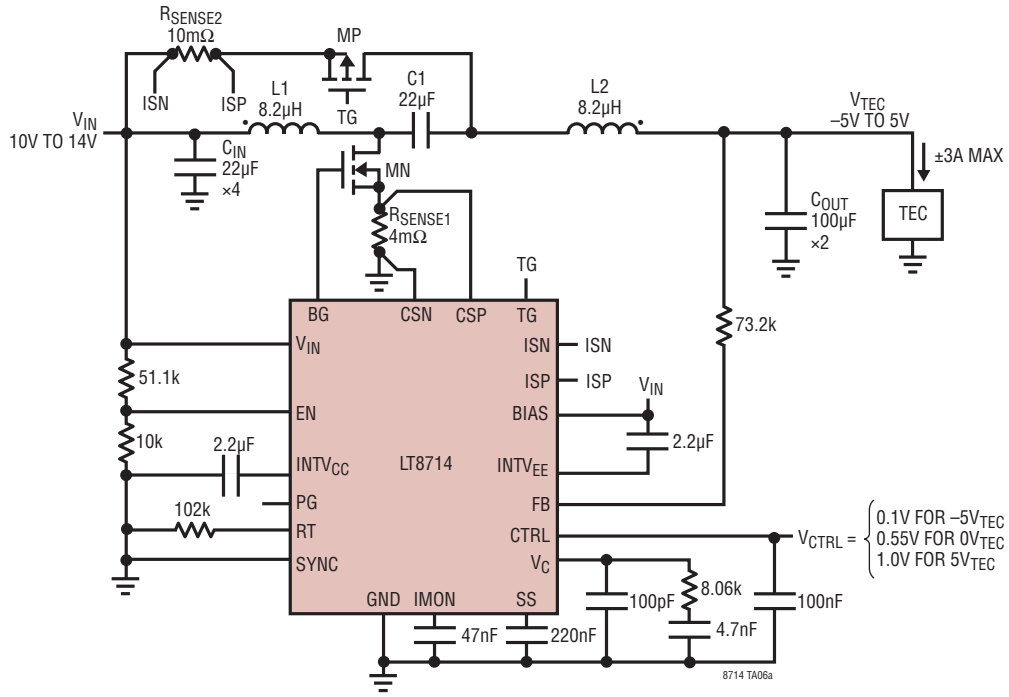
Power Loss in Each Quadrant (V_{IN} = 24V)



V_{CTRL} Step from 0.1V to 1V to 0.1V at V_{IN} = 24V (R_{LOAD} = 20Ω)



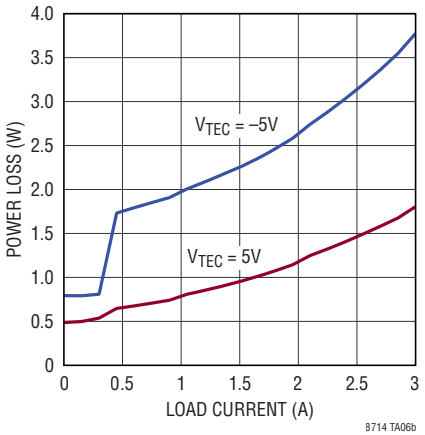
350kHz, Four Quadrant Converter, Drives a 3A TEC from a 10V to 14V Input



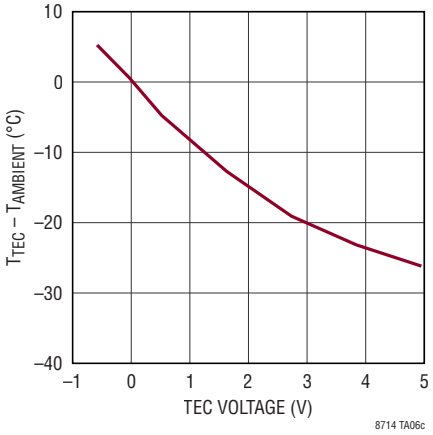
L1, L2: WURTH 8.2µH WE-CFWI 74485540820
MN: INFINEON BSC093N04LSG
MP: STMICRO STL60P4LLF6

C_{IN}, C1: 22µF, 25V, 1812, X7R
C_{OUT}: 100µF, 6.3V, 1812, X5R
R_{SENSE1}: 4mΩ, 2012
R_{SENSE2}: 10mΩ, 2512

Power Loss vs Load Current (V_{IN} = 12V)



TEC Temp vs TEC Voltage (V_{IN} = 12V)*

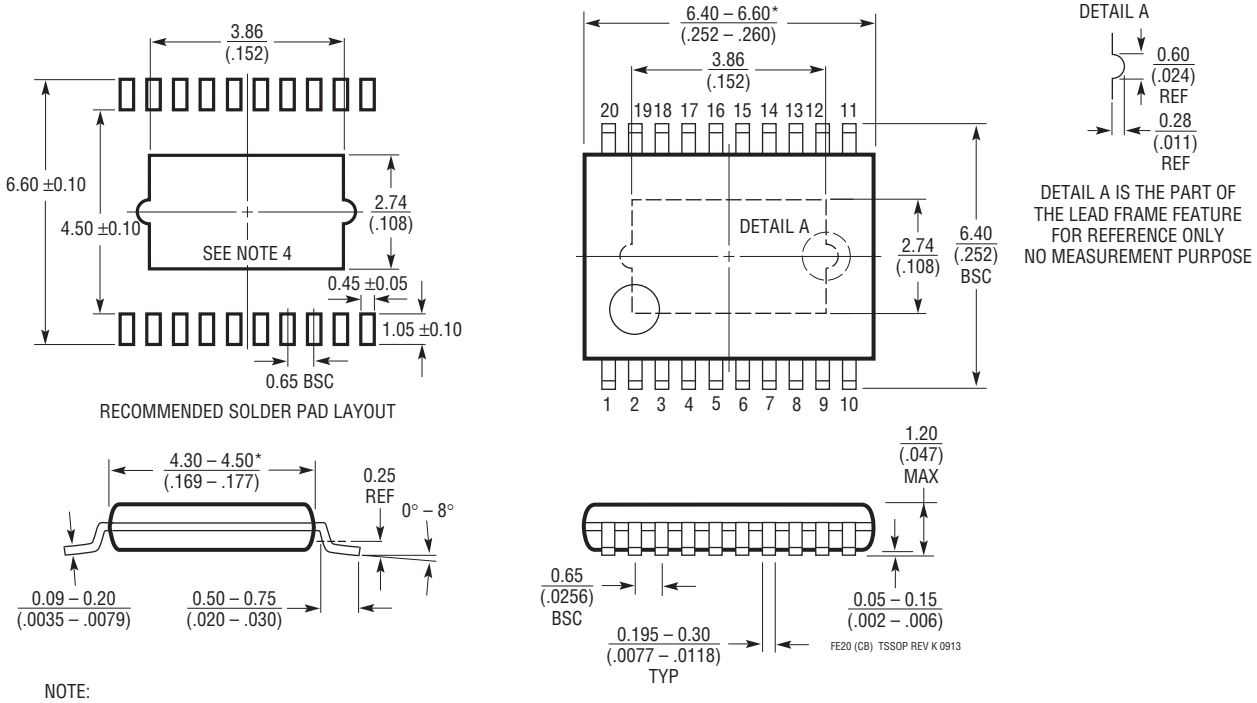


*TEC = LAIRD DA-011-05-02-00-00
FAN DRIVE TO 5V

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT8714#packaging for the most recent package drawings.

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev K)
Exposed Pad Variation CB

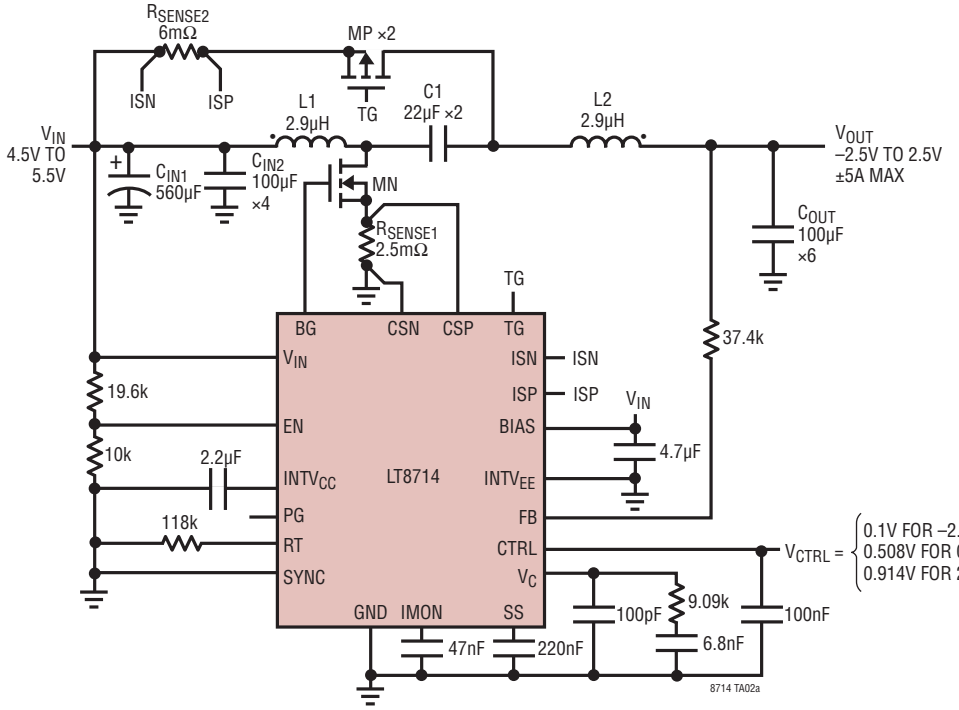


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

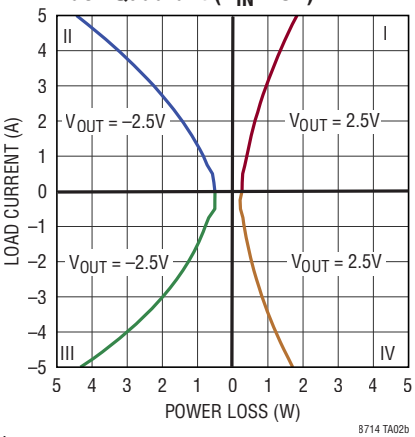
TYPICAL APPLICATION

300kHz, 5V Input Generates a –2.5V to 2.5V Output that Delivers –5A to 5A of Output Current

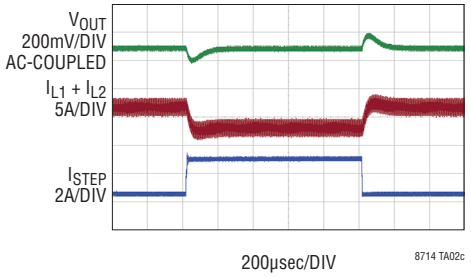


L1, L2: WURTH 2.9µH WE-CFWI 74485540290
MN: VISHAY SiRA12DP
MP: VISHAY Si7625DN
C_{IN1}: OSCON 560µF, 10V 10SEQP560M
C_{IN2}, C_{OUT}: 100µF, 6.3V, 1812, X5R
C1: 22µF, 25V, 1812, X7R
R_{SENSE1}: 2.5mΩ, 2512
R_{SENSE2}: 6mΩ, 2512

Power Loss vs Load Current in Each Quadrant (V_{IN} = 5V)



1.5A to 4A Load Step (QI, V_{OUT} = 2.5V)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3757A	Boost, Flyback, SEPIC and Inverting Controller	2.9V ≤ V_{IN} ≤ 40V, 100kHz to 1MHz Programmable Operating Frequency, 3mm × 3mm DFN-10 and MSOP-10E
LT3758A	Boost, Flyback, SEPIC and Inverting Controller	5.5V ≤ V_{IN} ≤ 100V, 100kHz to 1MHz Programmable Operating Frequency, 3mm × 3mm DFN-10 and MSOP-10E
LT3957A	Boost, Flyback, SEPIC and Inverting Converter with 5A, 40V Switch	3V ≤ V_{IN} ≤ 40V, 100kHz to 1MHz Programmable Operating Frequency, 5mm × 6mm QFN
LT3958	Boost, Flyback, SEPIC and Inverting Converter with 3.3A, 84V Switch	5V ≤ V_{IN} ≤ 80V, 100kHz to 1MHz Programmable Operating Frequency, 5mm × 6mm QFN
LT8705	80V V_{IN} and V_{OUT} Synchronous 4-Switch Buck-Boost DC/DC Controller	2.8V ≤ V_{IN} ≤ 80V, 100kHz to 400kHz Programmable Operating Frequency, 5mm × 7mm QFN-38 and TSSOP-38
LT8709	Negative Input Synchronous Multi-Topology DC/DC Control	–80V ≤ V_{IN} ≤ –4.5V, Up to 400kHz Programmable Operating Frequency, TSSOP-20
LT8710	Synchronous SEPIC/Inverting/Boost Controller with Output Current Control	4.5V ≤ V_{IN} ≤ 80V, 100kHz to 1MHz Programmable Operating Frequency, TSSOP-20

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