Low Power, 8th Order Progressive Elliptic, Lowpass Filter

FEATURES

- 8th Order Elliptic Filter in SO-8 Package
- Operates from Single 3.3V to ±5V Power Supplies
- –20dB at $1.2f_{CUTOFF}$
- –52dB at $1.4f_{CUTOFF}$
- –70dB at $2f_{CUTOFF}$
- Wide Dynamic Range
- $110\mu V_{RMS}$ Wideband Noise
- 3.8mA Supply Current with ±5V Supplies
- 2.5mA Supply Current with Single 5V Supply
- 2mA Supply Current with Single 3.3V Supply

APPLICATIONS

- Telecommunication Filters
- Antialiasing Filters

DESCRIPTION

The LTC®1069-1 is a monolithic 8th order lowpass filter featuring clock-tunable cutoff frequency and 2.5mA power supply current with a single 5V supply. An additional feature of the LTC1069-1 is operation with a single 3.3V supply.

The cutoff frequency (f_{CUTOFF}) of the LTC1069-1 is equal to the clock frequency divided by 100. The gain at f_{CUTOFF} is –0.7dB and the typical passband ripple is ±0.15dB up to $0.9f_{CUTOFF}$. The stopband attenuation of the LTC1069-1 features a progressive elliptic response reaching 20dB attenuation at $1.2f_{CUTOFF}$, 52dB attenuation at $1.4f_{CUTOFF}$ and 70dB attenuation at $2f_{CUTOFF}$.

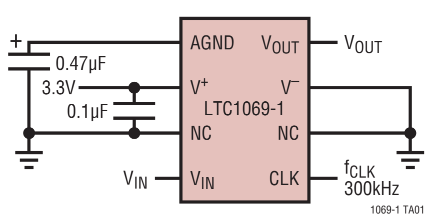
With ±5V supplies, the LTC1069-1 cutoff frequency can be clock-tuned up to 12kHz; with a single 5V supply, the maximum cutoff frequency is 8kHz.

The low power feature of the LTC1069-1 does not penalize the device's dynamic range. With ±5V supplies and an input range of $0.3V_{RMS}$ to $2.5V_{RMS}$, the signal-to-(noise + THD) ratio is ≥70dB. The wideband noise of the LTC1069-1 is $110\mu V_{RMS}$. *Other filter responses with lower power or higher speed can be obtained. Please contact LTC marketing for details.*

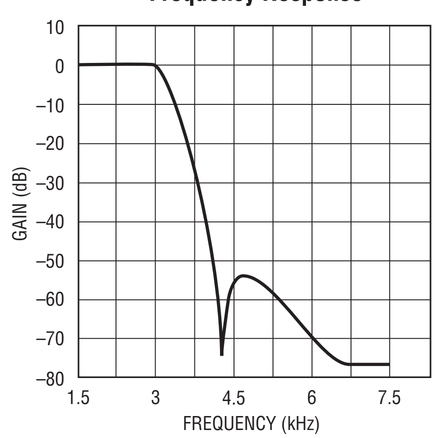
The LTC1069-1 is available in 8-pin PDIP and 8-pin SO packages.

TYPICAL APPLICATION

Single 3.3V Supply 3kHz Elliptic Lowpass Filter



Frequency Response



ABSOLUTE MAXIMUM RATINGS

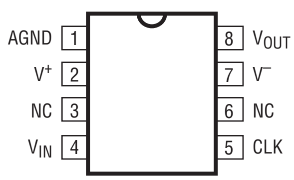
(Note 1)

Total Supply Voltage (V^+ to V^-) 12V
Maximum Voltage at
Any Pin .... (V^- – 0.3V) ≤ V ≤ (V+ + 0.3V)

Operating Temperature Range
LTC1069C-1 .... 0°C to 70°C
LTC1069I-1 .... –40°C to 85°C
Storage Temperature Range................... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

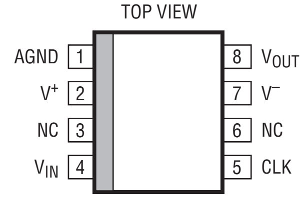
PIN CONFIGURATION

TOP VIEW



N8 PACKAGE
8-LEAD PLASTIC DIP
T_{JMAX} = 110°C, θ_{JA} = 100°C/W

TOP VIEW



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC1069-1CN8#PBF		LTC1069-1	8-Lead Plastic DIP	0°C to 70°C
LTC1069-1IN8#PBF		LTC1069-1	8-Lead Plastic DIP	–40°C to 85°C
LTC1069-1CS8#PBF	LTC1069-1CS8#TRPBF	10691	8-Lead Plastic SO	0°C to 70°C
LTC1069-1IS8#PBF	LTC1069-1IS8#TRPBF	10691I	8-Lead Plastic SO	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. f_{CUTOFF} is the filter's cutoff frequency and is equal to f_{CLK}/100. The f_{CLK} signal level is TTL or CMOS (clock rise or fall time ≤ 1µs), V_S = 3.3V to ±5V, R_L = 10k, unless otherwise noted. All AC gains are measured relative to the passband gain.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Gain (f_{IN} ≤ 0.25f_{CUTOFF})	V_S = ±5V, f_{CLK} = 500kHz f_{TEST} = 1.25kHz, V_{IN} = 1V_{RMS}	 ●	–0.30 –0.35	0.2	0.70 0.75	dB dB
	V_S = 3.3V, f_{CLK} = 200kHz f_{TEST} = 0.5kHz, V_{IN} = 0.5V_{RMS}	 ●	–0.30 –0.35	0.2	0.70 0.75	dB dB

ELECTRICAL CHARACTERISTICS

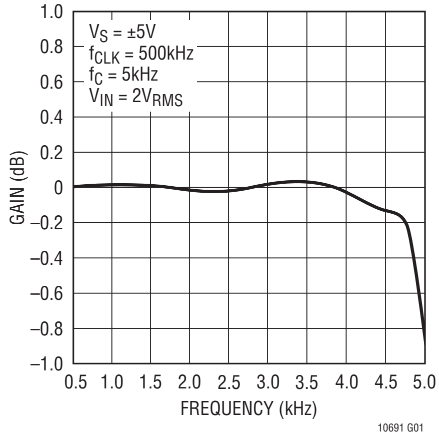
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. f_{CUTOFF} is the filter's cutoff frequency and is equal to f_{CLK}/100. The f_{CLK} signal level is TTL or CMOS (clock rise or fall time ≤ 1µs), V_S = 3.3V to ±5V, R_L = 10k, unless otherwise noted. All AC gains are measured relative to the passband gain.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gain at $0.50f_{CUTOFF}$	V_S = ±5V, f_{CLK} = 500kHz		–0.10	–0.03	0.10	dB
	f_{TEST} = 2.5kHz, V_{IN} = $1V_{RMS}$	●	–0.11		0.11	dB
	V_S = 3.3V, f_{CLK} = 200kHz		–0.10	–0.03	0.10	dB
	f_{TEST} = 1kHz, V_{IN} = $0.5V_{RMS}$	●	–0.11		0.11	dB
Gain at $0.75f_{CUTOFF}$	V_S = ±5V, f_{CLK} = 500kHz		–0.20	0.04	0.20	dB
	f_{TEST} = 3.75kHz, V_{IN} = $1V_{RMS}$	●	–0.25		0.25	dB
	V_S = 3.3V, f_{CLK} = 200kHz		–0.20	0.04	0.20	dB
	f_{TEST} = 1.5kHz, V_{IN} = $0.5V_{RMS}$	●	–0.25		0.25	dB
Gain at $0.90f_{CUTOFF}$	V_S = ±5V, f_{CLK} = 500kHz		–0.20	–0.01	0.20	dB
	f_{TEST} = 4.5kHz, V_{IN} = $1V_{RMS}$	●	–0.25		0.25	dB
	V_S = 3.3V, f_{CLK} = 200kHz		–0.20	–0.01	0.20	dB
	f_{TEST} = 1.8kHz, V_{IN} = $0.5V_{RMS}$	●	–0.25		0.25	dB
Gain at $0.95f_{CUTOFF}$	V_S = ±5V, f_{CLK} = 500kHz		–0.30	–0.05	0.30	dB
	f_{TEST} = 4.75kHz, V_{IN} = $1V_{RMS}$	●	–0.35		0.35	dB
	V_S = 3.3V, f_{CLK} = 200kHz		–0.30	–0.04	0.30	dB
	f_{TEST} = 1.9kHz, V_{IN} = $0.5V_{RMS}$	●	–0.35		0.35	dB
Gain at f_{CUTOFF}	V_S = ±5V, f_{CLK} = 500kHz		–1.25	–0.70	–0.25	dB
	f_{TEST} = 5.0kHz, V_{IN} = $1V_{RMS}$	●	–1.35		–0.15	dB
	V_S = 3.3V, f_{CLK} = 200kHz		–1.25	–0.61	–0.25	dB
	f_{TEST} = 2.0kHz, V_{IN} = $0.5V_{RMS}$	●	–1.35		–0.15	dB
Gain at $1.25f_{CUTOFF}$	V_S = ±5V, f_{CLK} = 500kHz		–30	–27	–25	dB
	f_{TEST} = 6.25kHz, V_{IN} = $1V_{RMS}$	●	–31		–24	dB
	V_S = 3.3V, f_{CLK} = 200kHz		–30	–27	–25	dB
	f_{TEST} = 2.5kHz, V_{IN} = $0.5V_{RMS}$	●	–31		–24	dB
Gain at $1.50f_{CUTOFF}$	V_S = ±5V, f_{CLK} = 500kHz		–58	–53	–50	dB
	f_{TEST} = 7.5kHz, V_{IN} = $1V_{RMS}$	●	–59		–49	dB
	V_S = 3.3V, f_{CLK} = 200kHz		–58	–53	–50	dB
	f_{TEST} = 3kHz, V_{IN} = $0.5V_{RMS}$	●	–59		–49	dB
Output DC Offset (Input at AGND)	V_S = ±5V, f_{CLK} = 500kHz			30	150	mV
	V_S = 4.75V, f_{CLK} = 400kHz			20		mV
	V_S = 3.3V, f_{CLK} = 200kHz			15	100	mV
Output Voltage Swing	V_S = ±5V	●	–3.25	±4.0	3.25	V
	V_S = 4.75V	●	–1.50	±1.7	1.25	V
	V_S = 3.3V	●	–0.70	±0.9	0.60	V
Power Supply Current	V_S = ±5V, f_{CLK} = 500kHz	●		3.8	5.5	mA
	V_S = 4.75V, f_{CLK} = 400kHz	●		2.5	4.5	mA
	V_S = 3.3V, f_{CLK} = 200kHz	●		2.0	3.5	mA
Maximum Clock Frequency	V_S = ±5V			1.2		MHz
	V_S = 4.75V			0.8		MHz
	V_S = 3.3V			0.5		MHz
Input Frequency Range			0		f_{CLK}/2	MHz
Input Resistance			30	43	70	kΩ
Operating Power Supply Voltage			±1.57		±5.5	V

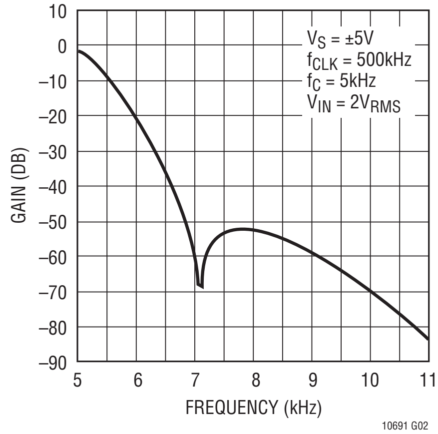
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

TYPICAL PERFORMANCE CHARACTERISTICS

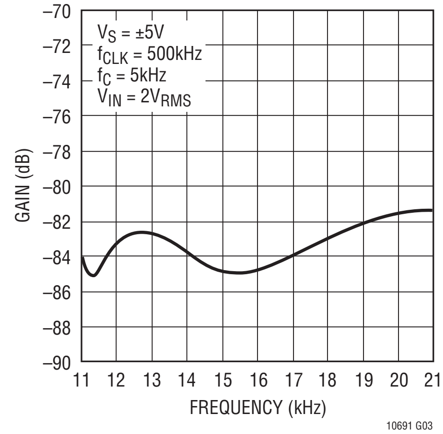
Passband Gain vs Frequency



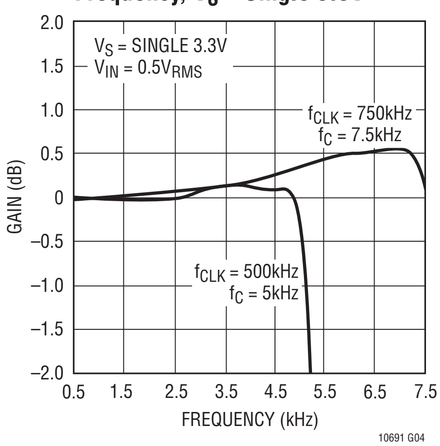
Transition Band Gain vs Frequency



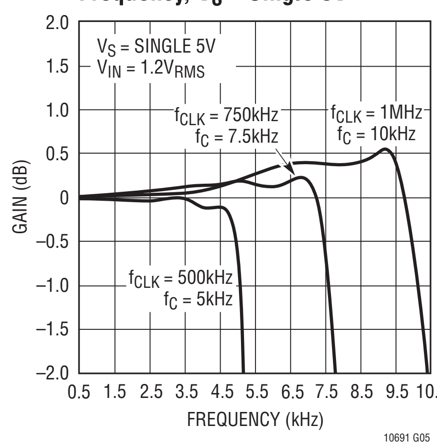
Stopband Gain vs Frequency



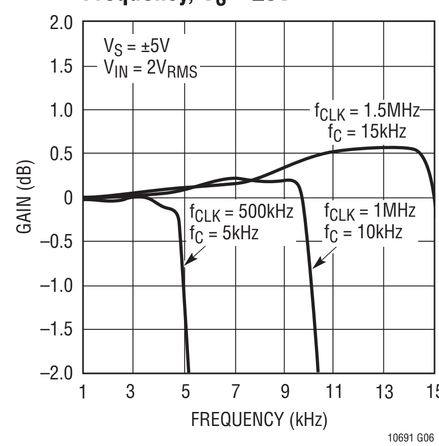
Passband Gain vs Clock Frequency, V_S = Single 3.3V



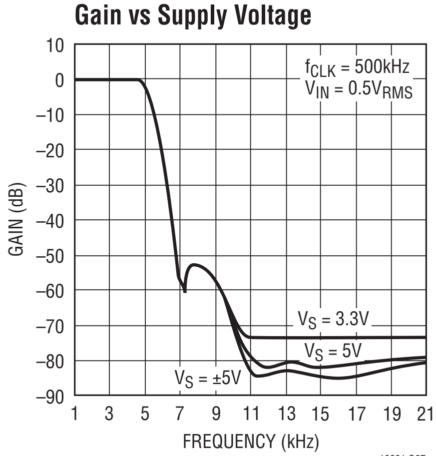
Passband Gain vs Clock Frequency, V_S = Single 5V



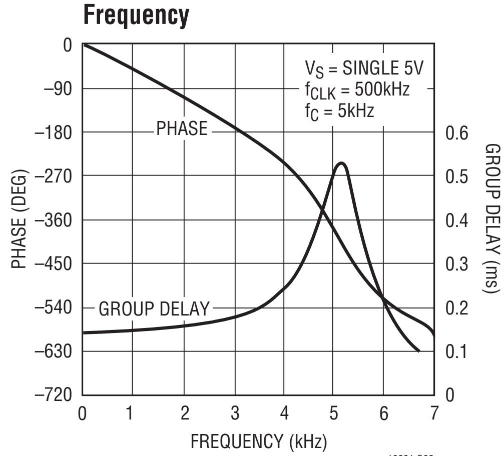
Passband Gain vs Clock Frequency, V_S = ±5V



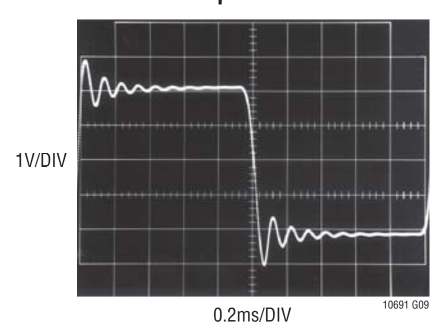
Gain vs Supply Voltage



Phase and Group Delay vs Frequency



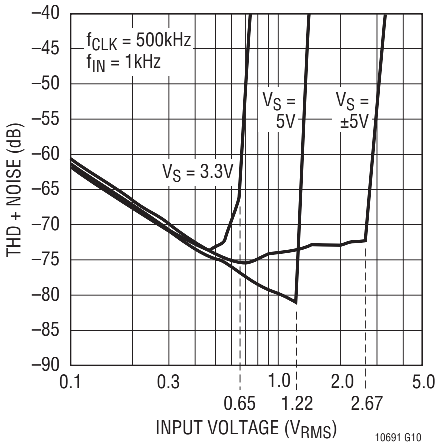
Transient Response



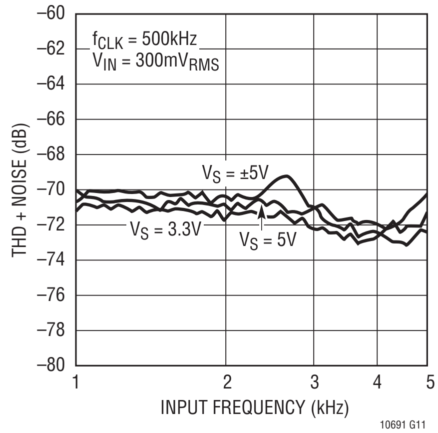
V_S = ±5V
f_{CLK} = 1MHz
f_{IN} = 500Hz
$4V_{P-P}$ SQUARE WAVE

TYPICAL PERFORMANCE CHARACTERISTICS

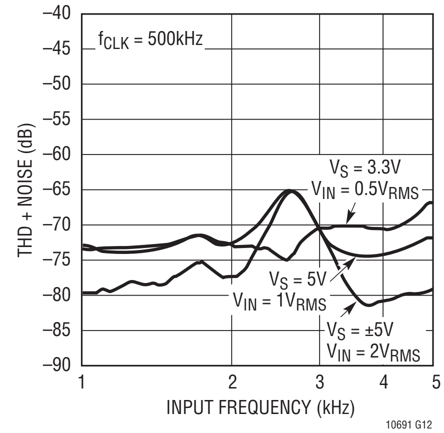
Dynamic Range THD + Noise vs V_{IN} (V_{RMS})



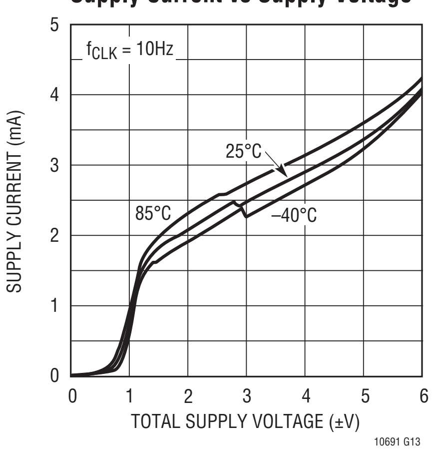
THD + Noise vs Frequency



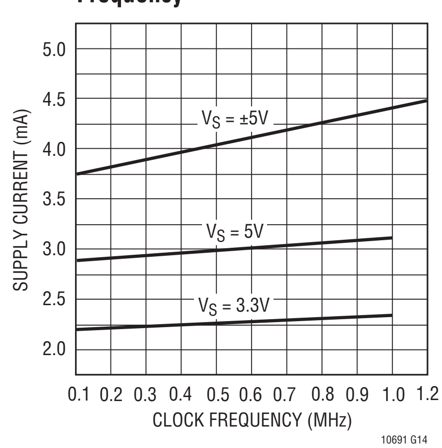
THD + Noise vs Frequency



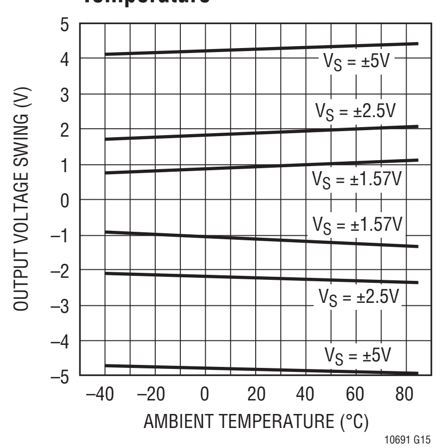
Supply Current vs Supply Voltage



Supply Current vs Clock Frequency



Output Voltage Swing vs Temperature



PIN FUNCTIONS

AGND (Pin 1): Analog Ground. The quality of the analog signal ground can affect the filter performance. For either single or dual supply operation, an analog ground plane surrounding the package is recommended. The analog ground plane should be connected to any digital ground at a single point. For dual supply operation Pin 1 should be connected to the analog ground plane.

For single supply operation Pin 1 should be bypassed to the analog ground plane with a 0.47μF or larger capacitor. An internal resistive divider biases Pin 1 to 1/2 the total power supply. Pin 1 should be buffered if used to bias other ICs. Figure 1 shows the connections for single supply operation.

V^+, $V^–$ (Pins 2, 7): Power Supply Pins. The V^+ (Pin 2) and the $V^–$ (Pin 7) should be bypassed with a 0.1μF capacitor to an adequate analog ground. The filter's power supplies should be isolated from other digital or high voltage analog supplies. A low noise linear supply is recommended. Using switching power supplies will lower the signal-to-noise ratio of the filter. Unlike previous monolithic filters, the power supplies can be applied at any order, that is, the positive supply can be applied before the negative supply and vice versa. Figure 2 shows the connection for dual supply operation.

NC (Pins 3, 6): No Connection. Pins 3 and 6 are not connected to any internal circuitry; they should be preferably tied to ground.

V_{IN} (Pin 4): Filter Input Pin. The filter input pin is internally connected to the inverting input of an op amp through a 43k resistor.

CLK (Pin 5): Clock Input Pin. Any TTL or CMOS clock source with a square wave output and 50% duty cycle (±10%) is an adequate clock source for the device. The power supply for the clock source should not necessarily be the filter's power supply. The analog ground of the filter should be connected to clock's ground at a single point only. Table 1 shows the clock's low and high level threshold value for a dual or a single supply operation. A pulse generator can be used as a clock source provided the high level ON time is greater than 0.42μs (V_S = ±5V). Sine waves less than 100kHz are not recommended for clock signal because excessive slow clock rise or fall times generate internal clock jitter. The maximum clock rise or fall is 1μs. The clock signal should be routed from the right side of the IC package to avoid coupling into any input or output analog signal path. A 1k resistor between the clock source and the clock input pin (5) will slow down the rise and fall times of the clock to further reduce charge coupling, Figure 1.

Table 1. Clock Source High and Low Thresholds

POWER SUPPLY	HIGH LEVEL	LOW LEVEL
Dual Supply = ±5V	1.5V	0.5V
Single Supply = 10V	6.5V	5.5V
Single Supply = 5V	1.5V	0.5V
Single Supply = 3.3V	1.2V	0.5V

V_{OUT} (Pin 8): Filter Output Pin. Pin 8 is the output of the filter and it can source or sink 1mA. Driving coaxial cables or resistive loads less than 20k will degrade the total harmonic distortion of the filter. When evaluating the device's dynamic range, a buffer is required to isolate the filter's output from coax cables and instruments.

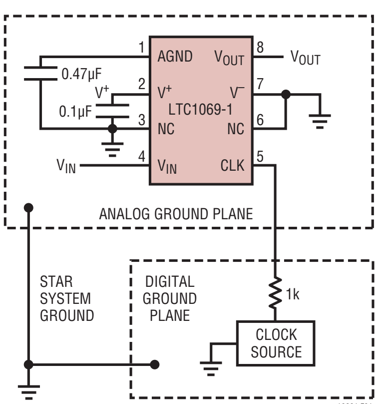


Figure 1. Connections for Single Supply Operation

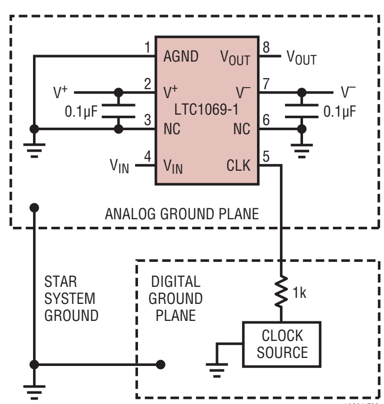


Figure 2. Connections for Dual Supply Operation

APPLICATIONS INFORMATION

Temperature Behavior

The power supply current of the LTC1069-1 has a positive temperature coefficient. The GBW product of its internal op amps is nearly constant and the speed of the device does not degrade at high temperatures. Figures 3a, 3b and 3c show the behavior of the maximum passband of the device for various supplies and temperatures. The filter, especially at ±5V supply, has a passband behavior which is nearly temperature independent.

Clock Feedthrough

The clock feedthrough is defined as the RMS value of the clock frequency and its harmonics that are present at the filter's output pin (8). The clock feedthrough is tested with the input pin (4) shorted to the AGND pin and depends on PC board layout and on the value of the power supplies. With proper layout techniques the values of the clock feedthrough are shown on Table 2.

Table 2. Clock Feedthrough

V_S	CLOCK FEEDTHROUGH
3.3V	$10\mu V_{RMS}$
5V	$40\mu V_{RMS}$
±5V	160µVRMS

Any parasitic switching transients during the rise and fall edges of the incoming clock are not part of the clock feedthrough specifications. Switching transients have frequency contents much higher than the applied clock; their amplitude strongly depends on scope probing techniques as well as grounding and power supply bypassing. The clock feedthrough can be reduced, if bothersome, by adding a single RC lowpass filter at the output pin (8) of the LTC1069-1.

Wideband Noise

The wideband noise of the filter is the total RMS value of the device's noise spectral density and determines the operating signal-to-noise ratio. Most of the wideband noise frequency contents lie within the filter passband. The wideband noise cannot be reduced by adding post filtering. The total wideband noise is nearly independent of the clock frequency and depends slightly on the power supply voltage (see Table 3). The clock feedthrough speci fications are not part of the wideband noise.

Table 3. Wideband Noise

V_S	WIDEBAND NOISE
3.3V	$100\mu V_{RMS}$
5V	$108\mu V_{RMS}$
±5V	$112\mu V_{RMS}$

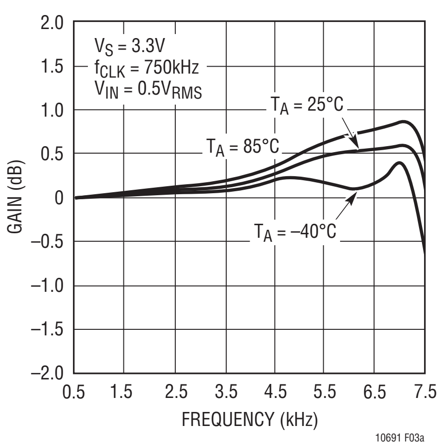


Figure 3a

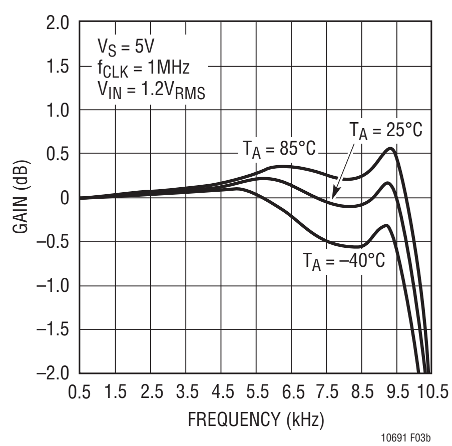


Figure 3b

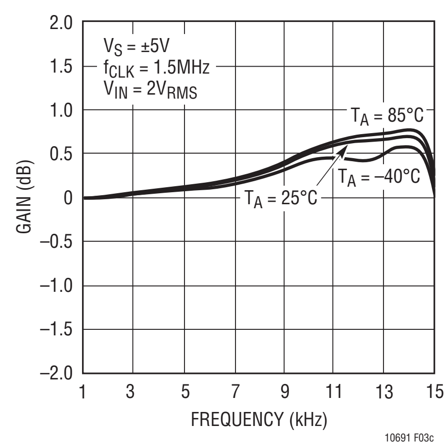


Figure 3c

APPLICATIONS INFORMATION

Aliasing

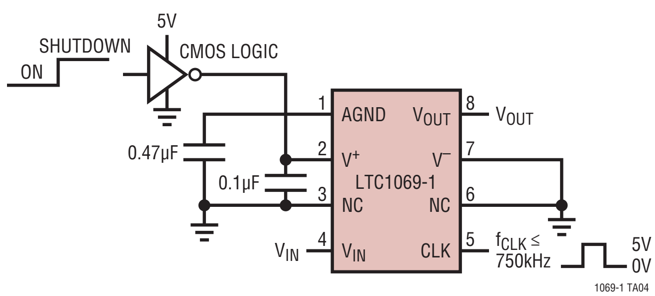
Aliasing is an inherent phenomenon of sampled data systems and it occurs for input frequencies approaching the sampling frequency. The internal sampling frequency of the LTC1069-1 is 100 times its cutoff frequency. For instance, if a 98kHz, $100mV_{RMS}$ signal is applied at the input of an LTC1069-1 operating with a 100kHz clock, a 2kHz, $28\mu V_{RMS}$ alias signal will appear at the filter output. Table 4 shows details.

Table 4. Aliasing (f_{CLK} = 100kHz)

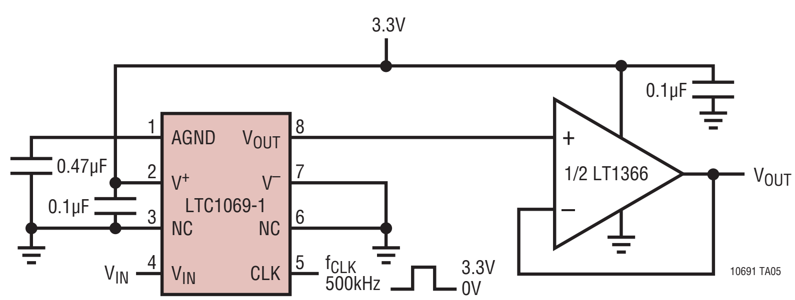
INPUT FREQUENCY ($V_{IN} = 1V_{RMS}$) (kHz)		OUTPUT LEVEL (Relative to Input) (dB)	OUTPUT FREQUENCY (Aliased Frequency) (kHz)
f_{CLK}/f_C = 100:1, f_{CUTOFF} = 1kHz			
96	(or 104)	–90.0	4.0
97	(or 103)	–86.0	3.0
98	(or 102)	–71.0	2.0
98.5	(or 101.5)	–56.0	1.5
99	(or 101)	–1.1	1.0
99.5	(or 100.5)	–0.21	0.5

TYPICAL APPLICATIONS

Single 5V Operation with Power Shutdown

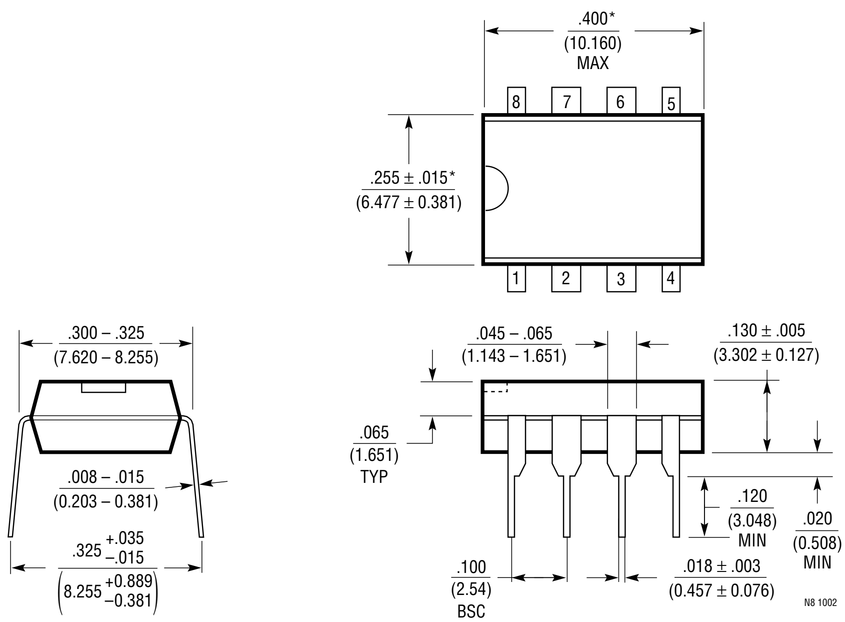


Single 3.3V Supply Operation with Output Buffer



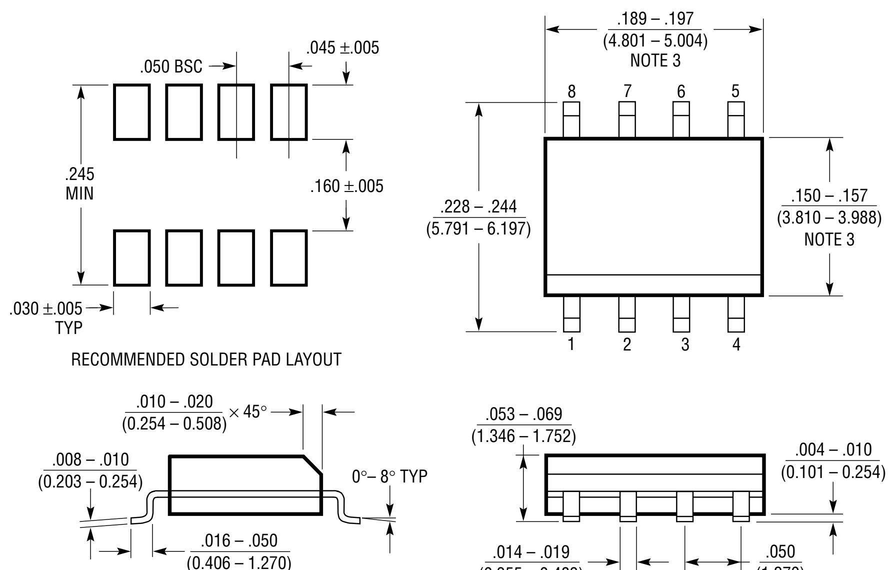
PACKAGE DESCRIPTION

N Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)

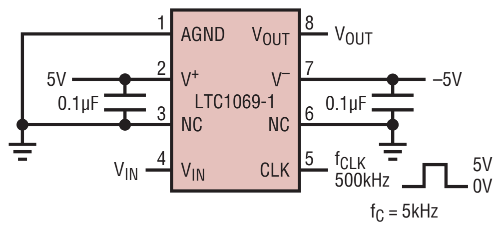


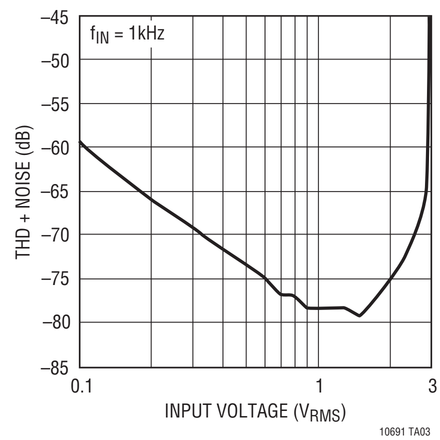
NOTE:
1. DIMENSIONS IN INCHES / (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

TYPICAL APPLICATION

Dual Supply Operation





RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1068	Very Low Noise, High Accuracy, Quad Universal Filter Building Block	User-Configurable, SSOP Package
LTC1069-6	Single Supply, Very Low Power, Elliptic LPF	50:1 f_{CLK}/f_C Ratio, 8-Pin SO Package
LTC1164-5	Low Power 8th Order Butterworth LPF	100:1 and 50:1 f_{CLK}/f_C Ratio
LTC1164-6	Low Power 8th Order Elliptic LPF	100:1 and 50:1 f_{CLK}/f_C Ratio
LTC1164-7	Low Power 8th Order Linear Phase LPF	100:1 and 50:1 f_{CLK}/f_C Ratio

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