LTC1565-31

## 650kHz Continuous Time, Linear Phase Lowpass Filter

## feATURES

- 7th Order, 650kHz Linear Phase Filter in an SO-8
- Differential Inputs and Outputs
- Operates on a Single 5 V or a $\pm 5 \mathrm{~V}$ Supply
- Low Offset: 5mV Typical
- 75dB THD and SNR
- 78dB SNR
- Shutdown Mode
- Requires No External Components
- Requires No External Clock Signal


## APPLICATIONS

- CDMA Basestations
- Data Communications
- Antialiasing Filters
- Smoothing or Reconstruction Filters
- Matched Filter Pairs
- Replacement for LC Filters


## DESCRIPTIOn

The LTC ${ }^{\circledR 1565-31}$ is a 7th order, continuous time, linear phase lowpass filter. The selectivity of the LTC1565-31, combined with its linear phase and dynamic range, make it suitable for filtering in data communications or data acquisition systems. The filter attenuation is 36 dB at $2 \times \mathrm{f}_{\text {CUTOFF }}$ and at least 72 dB for frequencies above $3 \times$ $f_{\text {CUTOFF }}$ Unlike comparable LC filters, the LTC1565-31 achieves this selectivity with a linear phase response in the passband.
With 5\% accuracy ofthe cutoff frequency, the LTC1565-31 can be used in applications requiring pairs of matched filters, such as transceiver I and Q channels. Furthermore, the differential inputs and outputs provide a simple interface for these wireless systems.
With a single 5 V supply and a $2 \mathrm{~V}_{\text {P-p }}$ input, the LTC1565-31 features an impressive spurious free dynamic range of 75 dB . The maximum signal-to-noise ratio is 78 dB and it is achieved with a $2.5 \mathrm{~V}_{\text {P-p }}$ input signal.
The LTC1565-31 features a shutdown mode where power supply current is typically less than $10 \mu \mathrm{~A}$.
For W-CDMA, 3G, CDMA 2000 and other cellular and noncellular cutoff frequencies or single-ended I/O, please contact LTC Marketing for additional information.
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## TYPICAL APPLICATION

Single 5V Supply, Differential 650kHz Lowpass Filter


Frequency Response


## LTC 1565-31

## ABSOLUTE MAXIMUM RATINGS

## PIn CONFIGURATIOn

## (Note 1)

Total Supply Voltage .............................................. 11V
Power Dissipation ............................................. 500 mW
Operating Temperature Range
LTC1565-31CS8.
LTC1565-31IS8 8....................................... $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ Storage Temperature Range ................. $-65^{\circ} \mathrm{C}$ to $150^{\circ} \mathrm{C}$ Lead Temperature (Soldering, 10 sec ) ................ $300^{\circ} \mathrm{C}$

| TOP VIEW |  |
| :---: | :---: |
| +10 1 | 8 +0ut |
| -12 2 | 7 -out |
| GND 3 | $6 \mathrm{v}^{+}$ |
| $\checkmark-4$ | 5 SHDN |
| S8 PACKAGE 8-LEAD PLASTIC SO |  |
| $\mathrm{T}_{\text {JMAX }}=150^{\circ} \mathrm{C}, \theta_{\mathrm{JA}}=80^{\circ} \mathrm{C} / \mathrm{W}$ (NOTE 4) |  |

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
| :--- | :--- | :--- | :--- | :--- |
| LTC1565-31CS8\#PBF | LTC1565-31CS8\#TRPBF | 156531 | 8 -Lead Plastic S0 | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ |
| LTC1565-31IS8\#PBF | LTC1565-31IS8\#TRPBF | 565311 | 8 -Lead Plastic S0 | $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ |

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.
For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS The • denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_{A}=25^{\circ} \mathrm{C} . \mathrm{V}_{S}=5 \mathrm{~V}, \mathrm{R}_{\mathrm{LOAD}}=10 \mathrm{k}$ from each output to AC ground, and Pin 5 open unless otherwise specified.

| PARAMETER | CONDITIONS |  | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Operating Supply Voltage |  |  | 4.75 |  | 11 | V |
| Filter Gain | $\mathrm{V}_{\mathrm{IN}}=1 \mathrm{~V}_{\mathrm{P}-\mathrm{P}} \mathrm{f}_{\mathrm{IN}}=25 \mathrm{kHz}$ <br> $\mathrm{f}_{\mathrm{IN}}=200 \mathrm{kHz}$ (Gain Relative to 25 kHz ) <br> $\mathrm{f}_{\mathrm{IN}}=300 \mathrm{kHz}$ (Gain Relative to 25 kHz ) <br> $\mathrm{f}_{\mathrm{IN}}=500 \mathrm{kHz}$ (Gain Relative to 25 kHz ) <br> $\mathrm{f}_{\mathrm{IN}}=650 \mathrm{kHz}$ (Gain Relative to 25 kHz ) <br> $\mathrm{f}_{\mathrm{IN}}=900 \mathrm{kHz}$ (Gain Relative to 25 kHz ) <br> $\mathrm{f}_{\mathrm{IN}}=1.3 \mathrm{MHz}$ (Gain Relative to 25 kHz ) <br> $\mathrm{f}_{\mathrm{IN}}=2.3 \mathrm{MHz}$ (Gain Relative to 25 kHz ) |  | $\begin{gathered} -0.3 \\ -0.2 \\ -0.7 \\ -2.2 \\ -4 \end{gathered}$ | $\begin{gathered} 0 \\ 0 \\ -0.4 \\ -1.6 \\ -3 \\ -11 \\ -36 \\ -72 \end{gathered}$ | $\begin{gathered} 0.3 \\ 0.1 \\ -0.1 \\ -0.95 \\ -2 \\ -7 \\ -31 \end{gathered}$ | $\begin{aligned} & \mathrm{dB} \\ & \mathrm{~dB} \\ & \mathrm{~dB} \\ & \mathrm{~dB} \\ & \mathrm{~dB} \\ & \mathrm{~dB} \\ & \mathrm{~dB} \\ & \mathrm{~dB} \end{aligned}$ |
| Filter Phase | $\begin{gathered} V_{I N}=1 V_{P-B} f_{I N}=25 \mathrm{kHz} \\ f_{I N}=200 \mathrm{kHz} \\ f_{I N}=300 \mathrm{kHz} \\ f_{I N}=500 \mathrm{kHz} \\ f_{I N}=600 \mathrm{kHz} \\ f_{I N}=650 \mathrm{kHz} \\ f_{I N}=900 \mathrm{kHz} \\ \hline \end{gathered}$ | $\bullet$ | $\begin{gathered} -162 \\ 34 \end{gathered}$ | $\begin{gathered} \hline-13 \\ -101 \\ -150 \\ 113 \\ 60 \\ 36 \\ -92 \end{gathered}$ | $\begin{gathered} -138 \\ 85 \end{gathered}$ | Deg Deg Deg Deg Deg Deg Deg |
| Phase Linearity | Ratio of 600 kHz Phase/300kHz Phase | $\bullet$ | 1.95 | 2 | 2.03 |  |
| Wideband Noise | Noise BW = DC to 2 ${ }^{\text {f Cutoff }}$ |  |  | 118 |  | $\mu \mathrm{V}_{\text {RMS }}$ |
| THD | $\mathrm{f}_{\mathrm{IN}}=100 \mathrm{kHz}, 1 \mathrm{~V}_{\text {P-p }}$ (Note 2) |  |  | 86 |  | dB |
| Filter Differential DC Swing | Maximum Difference Between Pins 7 and 8 $\begin{aligned} & V_{S}=5 \mathrm{~V} \\ & V_{S}= \pm 5 \mathrm{~V} \end{aligned}$ | $\bullet$ | $\begin{aligned} & \pm 1.4 \\ & \pm 2.2 \end{aligned}$ | $\begin{aligned} & \pm 1.7 \\ & \pm 2.3 \end{aligned}$ |  | V |
|  |  |  |  |  |  | 156531fa |
| $2$ |  |  |  |  | $T$ | $\operatorname{END}_{\text {Vology }}$ |

ELECTRICAL CHARACTERISTICS The odenotes the specifications which apply over the full operating temperature range, otherwise specifications are at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C} . \mathrm{V}_{\mathrm{S}}=5 \mathrm{~V}, \mathrm{R}_{\mathrm{LOAD}}=10 \mathrm{k}$ from each output to AC ground, and Pin 5 open unless otherwise specified.

| PARAMETER | CONDITIONS |  | MIN | TYP | MAX | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Input Bias Current |  |  | 0.1 | 0.3 | 0.6 | $\mu \mathrm{A}$ |
| Input Offset Current |  |  |  | $\pm 10$ |  | nA |
| Input Resistance | Common Mode, $\mathrm{V}_{\mathrm{IN}}=2.5 \mathrm{~V}$ Differential |  |  | $\begin{gathered} 75 \\ 145 \end{gathered}$ |  | $\mathrm{M} \Omega$ $\mathrm{M} \Omega$ |
| Input Capacitance |  |  |  | 3 |  | pF |
| Output DC Offset (Note 3) | $\begin{aligned} & V_{S}=5 \mathrm{~V} \\ & \left.V_{S}= \pm 5 \mathrm{~V} \text { (Note } 5\right) \end{aligned}$ |  |  | $\begin{aligned} & \pm 5 \\ & \pm 5 \end{aligned}$ | $\begin{aligned} & \pm 12 \\ & \pm 12 \end{aligned}$ | mV mV |
| Output DC Offset Drift | $\begin{aligned} & V_{S}=5 \mathrm{~V} \\ & V_{S}= \pm 5 \mathrm{~V} \end{aligned}$ |  |  | $\begin{aligned} & -400 \\ & -400 \end{aligned}$ |  | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ <br> $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| Ground Voltage (Pin 3) in Single Supply Applications | $V_{S}=5 \mathrm{~V}$ | $\bullet$ | 2.49 | 2.51 | 2.52 | V |
| $\overline{\overline{\text { SHDN }} \text { Pin Logic Thresholds }}$ | $\mathrm{V}_{\mathrm{S}}=5 \mathrm{~V}$, Minimum Logical " 1 " <br> $\mathrm{V}_{\mathrm{S}}=5 \mathrm{~V}$, Maximum Logical "0" |  | 3.3 |  | 4.2 | V |
|  | $\begin{aligned} & \mathrm{V}_{S}= \pm 5 \mathrm{~V} \text {, Minimum Logical "1" } \\ & \mathrm{V}_{S}= \pm 5 \mathrm{~V} \text {, Maximum Logical "0" } \end{aligned}$ | $\bullet$ | 2.4 |  | 2.9 | V |
| $\overline{\text { SHDN }}$ Pin Pull-Up Current | $\begin{aligned} & V_{S}=5 \mathrm{~V} \\ & V_{S}= \pm 5 \mathrm{~V} \end{aligned}$ |  |  | 5 9 |  | $\mu \mathrm{A}$ $\mu \mathrm{A}$ |
| Power Supply Current | $\begin{aligned} & V_{S}=5 \mathrm{~V} \\ & V_{S}= \pm 5 \mathrm{~V} \end{aligned}$ | $\bullet$ |  | $\begin{aligned} & 24 \\ & 25 \end{aligned}$ | $\begin{aligned} & 31 \\ & 33 \end{aligned}$ | mA mA |
| Power Supply Current in Shutdown Mode | Shutdown. Includes $\overline{\text { SHDN }}$ Pull-Up Current $\begin{aligned} & V_{S}=5 \mathrm{~V} \\ & V_{S}= \pm 5 \mathrm{~V} \end{aligned}$ | $\bullet$ |  | $\begin{gathered} 8 \\ 20 \end{gathered}$ | $\begin{aligned} & 16 \\ & 40 \end{aligned}$ | $\mu \mathrm{A}$ $\mu \mathrm{A}$ |

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
Note 2: Input and output voltages expressed as peak-to-peak numbers are assumed to be fully differential.

Note 3: Output DC offset is measured between Pin 8 and Pin 7 with Pin 1 and Pin 2 connected to Pin 3.
Note 4: Thermal resistance varies depending upon the amount of PC board metal attached to the device. $\theta_{\mathrm{JA}}$ is specified for a 3.8 square inch test board covered with 2 oz copper on both sides.
Note 5: Output DC offset measurements are performed by automatic test equipment approximately 0.5 seconds after application of power.

## TYPICAL PERFORMANCE CHARACTERISTICS

Frequency Response


Passband Gain and Delay vs Frequency


## LTC 1565-31

## TYPICAL PERFORMANCE CHARACTERISTICS



## PIn fUnCTIOnS

+IN, -IN (Pins 1, 2): Input Pins. Signals can be applied to either or both input pins. The typical DC gain from differential inputs (Pin 1 to Pin 2) to the differential outputs (Pin 8 to Pin 7) is $1.0 \mathrm{~V} / \mathrm{V}$. The input range is described in the Applications Information section.
GND (Pin 3): Ground. The ground pin is the reference voltage for the filter and is internally biased to one-half the total power supply voltage of the filter, maximizing the dynamic range of the filter. For single supply operation, the ground pin should be bypassed with a quality $0.1 \mu \mathrm{~F}$
ceramic capacitor to Pin 4. For dual supply operation, connect Pin 3 to a high quality DC ground. A ground plane should be used. A poor ground will increase noise and distortion.
The impedance seen at Pin 3 is $2.5 \mathrm{k} \Omega$ in normal mode. In shutdown, the pin is internally biased to the same levels as normal mode. The impedance in shutdown mode is typically $500 \mathrm{k} \Omega$ but varies with supply voltage and temperature.

## PIn functions

$\mathbf{V}^{-}, \mathbf{V}^{+}$(Pins 4, 6): Power Supply Pins. For a single 5V supply (Pin 4 grounded), a quality $0.1 \mu \mathrm{~F}$ ceramic bypass capacitor is required from the positive supply pin (Pin 6) to the negative supply pin (Pin 4). The bypass should be as close as possible to the IC. For dual supply applications (Pin 3 is grounded), bypass Pin 6 to Pin 3 and Pin 4 to Pin 3 with a quality $0.1 \mu \mathrm{~F}$ ceramic capacitor.
The maximum voltage difference between the ground pin (Pin 3) and the positive supply pin (Pin 6) should not exceed 5.5V.

SHDN (Pin 5): Shutdown. When the Pin 5 voltage is low, the LTC1565-31 goes into the current saving shutdown mode. Pin 5 has a $4 \mu$ A pull-up current. Leaving Pin 5 open will place the LTC1565-31 in its normal operating mode.
-OUT, +OUT (Pins 7, 8): Output Pins. Pins 7 and 8 are the filter differential output. Each pin can drive $1 \mathrm{k} \Omega$ or 300 pF loads. The common mode voltage at the output pins is the same as the voltage at Pin 3.

## BLOCK DIAGRAM



## APPLICATIONS InFORMATION

## Interfacing to the LTC1565-31

The difference between the voltages at Pin 1 and Pin 2 is the "differential input voltage." The average of the voltages at Pin 1 and Pin 2 is the "common mode input voltage." The difference between the voltages at Pin 7 and Pin 8 is the "differential output voltage." The average of the voltages at Pin 7 and Pin 8 is the "common mode output voltage." The input and output common mode voltages are independent. The input common mode voltage is set by the signal source, if DC coupled, or by the biasing network if AC coupled (Figures 1 and 2). The output common mode voltage is equal to the voltage of Pin 3, the GND pin. The GND pin is biased to one-half of the supply voltage by an internal resistive divider (see Block Diagram). To alter the common mode output voltage, Pin 3 can be driven with an external voltage source or resistor network. If external resistors are used, it is important to note that the internal 5 k resistors can vary $\pm 20 \%$ (their ratio only varies $\pm 1 \%$ ). The output can also be AC coupled.


DC COUPLED INPUT
$\mathrm{V}_{\text {IN }}($ COMMON MODE $)=\frac{\mathrm{V}_{\text {IN }}{ }^{+}+\mathrm{V}_{\text {IN }}-}{2}$
$V_{\text {OUT }}($ COMMON MODE $)=\frac{V_{\text {OUT }^{+}}+\mathrm{V}_{\text {OUT }^{-}}}{2}=\frac{\mathrm{V}^{+}}{2}$
Figure 1


AC COUPLED INPUT
$V_{\text {IN }}($ COMMON MODE $)=V_{\text {OUT }}($ COMMON MODE $)$

$$
=\frac{\mathrm{V}^{+}}{2}
$$

Figure 2

## Input Common Mode and Differential Voltage Range

The range of voltage each input can support while operating in its linear region is typically 0.8 V to 3.7 V for a single 5 V supply and -4.2 V to 3.2 V for $\mathrm{a} \pm 5 \mathrm{~V}$ supply. Therefore, the filter can accept a variety of common mode input voltages. Figures 3 and 4 show the THD of the filter versus common mode input voltage with a $2 V_{\text {p-p }}$ differential input signal.


1565-31 F03
Figure 3. THD vs Common Mode Input Voltage


1565-31 504
Figure 4. THD vs Common Mode Input Voltage
Figure 5 shows the THD and S/N ratio versus differential input voltage level for both a single 5 V supply and a $\pm 5 \mathrm{~V}$ supply. The common mode voltage of the input signal is one-half the total power supply voltage of the filter. The spurious free dynamic range, where the THD and S/N ratio are equal, is 75 dB to 76 dB when the differential input voltage level is $2 \mathrm{~V}_{\text {P-p }}$; that is, for a single 5 V supply, the

## APPLICATIONS INFORMATION



1565-31 F05
Figure 5. Dynamic Range Diff-In, Diff-Out
input voltages are Pin $1=2.5 \mathrm{~V} D \mathrm{DC} \pm 0.5 \mathrm{~V}$ and $\operatorname{Pin} 2=2.5 \mathrm{~V}$ DC $\pm 0.5 \mathrm{~V}$. Also note Figure 5 shows a 78 dB SNR ratio for higher THD levels.

As seen in Figures 3 and 4, the spurious free dynamic range can be optimized by setting the input common mode voltage slightly below one-half of the power supply voltage, i.e., 2 V for a single 5 V supply and -0.5 V for $\mathrm{a} \pm 5 \mathrm{~V}$ supply. Figure 6 shows the THD and SNR ratio versus differential input voltage level for both a single 5 V supply and a $\pm 5 \mathrm{~V}$ supply when the common mode input voltage is 2 V and -0.5 V respectively.

For best performance, the inputs should be driven differentially. For single-ended signals, connect the unused input to Pin 3 or a common mode reference.


1565-31 F06
Figure 6. THD vs $\mathrm{V}_{\mathrm{IN}}$ for a Common Mode Input Voltage 0.5V Below Mid Supply

## Output Common Mode and Differential Voltage Range

The output is a fully differential signal with a common mode level equal to the voltage at Pin 3. The specifications in the Electrical Characteristics table assume the inputs are driven differentially and the output is observed differentially. However, Pin 8 can be used as a single-ended output by simply floating Pin 7 . Pin 7 can be used as an inverting single-ended output by floating Pin 8. Using Pins 7 or 8 as single-ended outputs will decrease the performance.

The common mode output voltage can be adjusted by overdriving the voltage present on Pin 3 . The best performance is achieved using a common mode output voltage that is equal to mid supply (the default Pin 3 voltage). Figures 7 and 8 illustrate the THD versus output common mode voltage for a $2 V_{\text {P_p }}$ differential input voltage and a common mode input voltage that is 0.5 V below mid supply.


1565-31 F07
Figure 7. THD vs Common Mode Output Voltage


Figure 8. THD vs Common Mode Output Voltage

## LTC 1565-31

## APPLICATIONS INFORMATION

## Output Drive

Pin 7 and Pin 8 can drive a $1 \mathrm{k} \Omega$ or 300 pF load connected to AC ground with a $\pm 0.5 \mathrm{~V}$ signal (corresponding to a $2 V_{\text {P-p }}$ differential signal). For differential loads (loads connected from Pin 7 to Pin 8) the outputs can produce a $2 \mathrm{~V}_{\text {P-p }}$ differential signal across $2 \mathrm{k} \Omega$ or 150 pF . For smaller signal amplitudes the outputs can drive correspondingly larger loads.

## Noise

The wideband noise of the filter is the RMS value of the device's output noise spectral density. The wideband noise data is used to determine the operating signal-to-noise at a given distortion level. Most of the noise is concentrated
in the filter passband and cannot be removed with post filtering (Table 1). Table 2 lists the typical change in wideband noise with supply voltage.

Table 1. Wideband Noise vs Bandwidth, Single 5V Supply

| BANDWIDTH | TOTAL INTEGRATED NOISE |
| :--- | :--- |
| DC to $f_{\text {CUTOFF }}$ | $104 \mu \mathrm{~V}_{\text {RMS }}$ |
| DC to $2 \bullet f_{\text {CUTOFF }}$ | $118 \mu \mathrm{~V}_{\text {RMS }}$ |

Table 2. Wideband Noise vs Supply Voltage, $\mathrm{f}_{\text {Cutoff }}=650 \mathrm{kHz}$

| POWER SUPPLY | TOTAL INTEGRATED NOISE <br> DC TO $2 \bullet \mathrm{f}_{\text {CUTOFF }}$ |
| :--- | :--- |
| 5 V | $118 \mu \mathrm{~V}_{\mathrm{RMS}}$ |
| $\pm 5 \mathrm{~V}$ | $120 \mu \mathrm{~V}_{\mathrm{RMS}}$ |

## TYPICAL APPLICATIONS

Test Circuit for Single 5V Supply Operation


## TYPICAL APPLICATIONS

Single-Ended Input/Output Dual Supply Filter


A Fully Differential Filter with Adjustable Output Common Mode Voltage


## LTC 1565-31

## TYPICAL APPLICATIONS

Simple Pulse Shaping Circuit for Single 5V Operation, 1.25Mbps 2 Level Data



Simple Pulse Shaping Circuit for Single 5V Operation, 2Mbps (1Msps) 4 Level Data



## TYPICAL APPLICATIONS

Narrowband Cellular Basestation Receiver


PACKAGE DESCRIPTION

## S8 Package

8-Lead Plastic Small Outline (Narrow . 150 Inch)
(Reference LTC DWG \# 05-08-1610)


## LTC 1565-31

TYPICAL APPLICATION
Selective 620kHz CDMA Filter


Frequency Response


1565 TA12

## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
| :---: | :---: | :---: |
| LTC1560-1 | 1MHz/500kHz Continuous Time, Low Noise, Lowpass Elliptic Filter | $\mathrm{f}_{\text {CUTOFF }}=500 \mathrm{kHz}$ or 1 MHz |
| LTC1562/LTC1562-2 | Universal 8th Order Active RC Filters | $\begin{aligned} & \mathrm{f}_{\text {CUTOFF(MAX) }}=150 \mathrm{kHz}(\text { LTC1562 }), \\ & \mathrm{f}_{\text {CUTOFF(MAX) }}=300 \mathrm{kHz}(\text { LTC1562-2 }) \end{aligned}$ |
| LTC1563-2/LTC1563-3 | 4th Order Active RC Lowpass Filters | $\mathrm{f}_{\text {CUTOFF(MAX) }}=256 \mathrm{kHz}$ |
| LTC1569-6/LTC1569-7 | Self Clocked, 10th Order Linear Phase Lowpass Filters | $\begin{aligned} & \mathrm{f}_{\text {CLL }} / \mathrm{f}_{\text {CUTOFF }}=64 / 1, \mathrm{f}_{\text {CUTOFF(MAX }}=75 \mathrm{kHz} \text { (LTC1569-6) } \\ & \mathrm{f}_{\text {CLK }} / \mathrm{f}_{\text {CUTOFF }}=32 / 1, \mathrm{f}_{\text {CUTOFF(MAX) }}=300 \mathrm{kHz} \text { (LTC1569-7) } \end{aligned}$ |

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HMC882ALP5E HMC881ALP5E ADMV8420ACPZ ADMV8432ACPZ HMC881LP5ETR HMC882LP5ETR HMC1000LP5ETR
LTC1068IN\#PBF LTC1566-1IS8\#PBF LTC1569IS8-6\#PBF LTC1069-1CS8\#PBF

