Ultralow Power, Dual 10-Bit DAC in MSOP

FEATURES

- **Ultralow Power: 1.5µA (Typ) I_{CC} per DAC Plus 0.05µA Sleep Mode for Extended Battery Life**
- **Tiny: Two 10-Bit DACs in an 8-Lead MSOP—Half the Size of an SO-8**
- Wide 2.7V to 5.5V Supply Range
- Double Buffered for Simultaneous DAC Updates
- **Rail-to-Rail Voltage Outputs Drive 1000pF**
- Reference Range Includes Supply for Ratiometric 0V to V_{CC} Output
- Reference Input Impedance Is Code-Independent (7.1MΩ Typ)—Eliminates External Buffers
- 3-Wire Serial Interface with Schmitt Trigger Inputs
- Differential Nonlinearity: ±0.75LSB Max

APPLICATIONS

- Mobile Communications
- Portable Battery-Powered Instruments
- Remote or Inaccessible Adjustments
- Digitally Controlled Amplifiers and Attenuators
- Factory or Field Calibration

DESCRIPTION

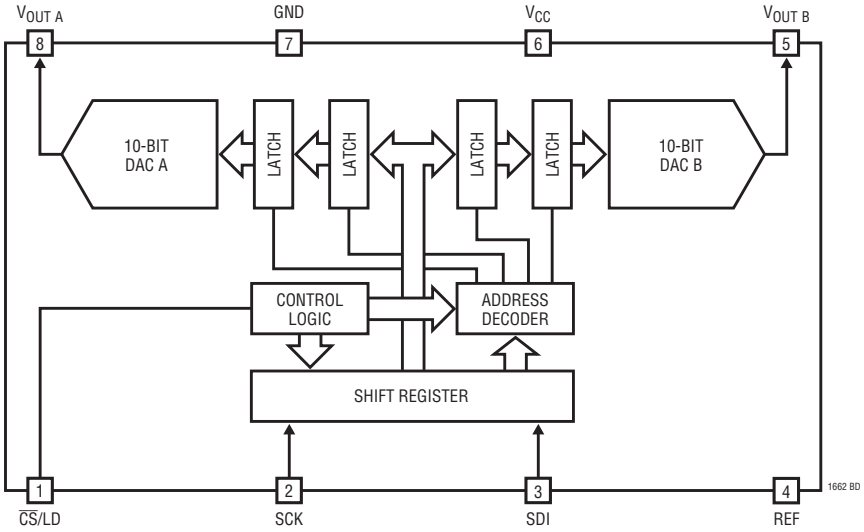
The LTC®1662 is an ultralow power, fully buffered voltage output, dual 10-bit digital-to-analog converter (DAC). Each DAC channel draws just 1.7µA (typ) total supply-plus-reference operating current, yet is capable of supplying DC output currents in excess of 1mA and reliably driving capacitive loads of up to 1000pF. A programmable sleep mode further reduces total operating current to 0.05µA.

Linear Technology's proprietary, inherently monotonic architecture provides excellent linearity and an exceptionally small external form factor. The double-buffered input logic provides simultaneous update capability and can be used to write to the DACs without interrupting sleep mode.

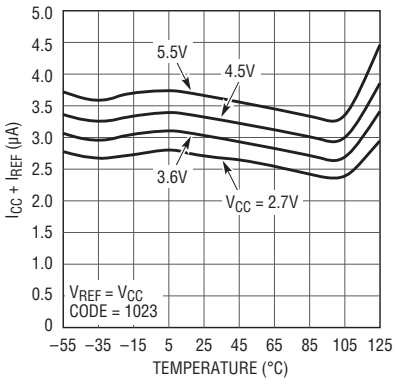
With its tiny operating current and exceptionally small size, the LTC1662 is ideal for use in the most power-constrained products. For most designs, there is no perceptible impact on the power budget; the LTC1662 draws many times less current than even a trimpot, while providing buffered, low impedance (0.5Ω typical, V_{CC} = 5V) rail-to-rail outputs.

The LTC1662 is pin and software compatible with the LTC1661 dual, 60µA 10-bit DAC. It is available in 8-pin MSOP and PDIP packages and is specified over the industrial temperature range.

BLOCK DIAGRAM



Total Supply-Plus-Reference Operating Current



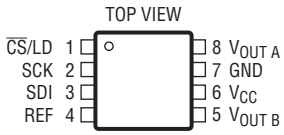
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} to GND ..... –0.3V to 7.5V
Logic Inputs to GND ..... –0.3V to 7.5V
$V_{OUT\ A}$, $V_{OUT\ B}$, REF to GND ..... –0.3V to (V_{CC} + 0.3V)
Maximum Junction Temperature ..... 125°C
Storage Temperature Range .....–65°C to 150°C

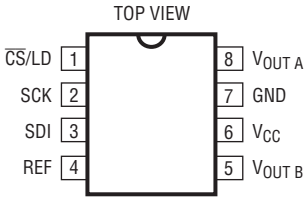
Operating Temperature Range
LTC1662C ..... 0°C to 70°C
LTC1662I ..... –40°C to 85°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PIN CONFIGURATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 150°C/W



N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 125°C, θ_{JA} = 100°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1662CMS8#PBF	LTC1662CMS8#TRPBF	LTKB	8-Lead Plastic MSOP	0°C to 70°C
LTC1662IMS8#PBF	LTC1662IMS8#TRPBF	LTKC	8-Lead Plastic MSOP	–40°C to 85°C
LTC1662CN8#PBF	LTC1662CN8#TRPBF	LTC1662CN8	8-Lead Plastic DIP	0°C to 70°C
LTC1662IN8#PBF	LTC1662IN8#TRPBF	LTC1662IN8	8-Lead Plastic DIP	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING**	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC1662CMS8	LTC1662CMS8#TR	LTKB	8-Lead Plastic MSOP	0°C to 70°C
LTC1662IMS8	LTC1662IMS8#TR	LTKC	8-Lead Plastic MSOP	–40°C to 85°C
LTC1662CN8	LTC1662CN8#TR	LTC1662CN8	8-Lead Plastic DIP	0°C to 70°C
LTC1662IN8	LTC1662IN8#TR	LTC1662IN8	8-Lead Plastic DIP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range ($T_A = T_{MIN}$ to T_{MAX}), otherwise specifications are at $T_A = 25°C$. $V_{CC} = 2.7V$ to $5.5V$, $V_{REF} \leq V_{CC}$, V_{OUT} unloaded unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Accuracy							
	Resolution		●	10			Bits
	Monotonicity	(Note 2)	●	10			Bits
DNL	Differential Nonlinearity	(Note 2)	●		±0.12	±0.75	LSB
INL	Integral Nonlinearity	(Note 2)	●		±0.8	±4	LSB
V_{OS}	Offset Error	$V_{CC} = 5V$, $V_{REF} = 4.096V$, Measured at Code 20	●		±5	±25	mV
V_{OS} TC	V_{OS} Temperature Coefficient				±15		µV/°C
GE	Gain Error	$V_{CC} = 5V$, $V_{REF} = 4.096V$	●		±1	±8	LSB
GE TC	Gain Error Temperature Coefficient				±12		µV/°C
PSR	Power Supply Rejection	$V_{REF} = 2.5V$			0.18		LSB/V
Reference Input							
	Input Voltage Range		●	0		V_{CC}	V
	Input Resistance	Active Mode Sleep Mode	●	3.9	7.1 2.5		MΩ GΩ
	Input Capacitance				10		pF
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	2.7		5.5	V
I_{CC}	Supply Current	$V_{CC} = 3V$ (Note 3) $V_{CC} = 5V$ (Note 3) $V_{CC} = 3V$ (Note 3) $V_{CC} = 5V$ (Note 3)	 ● ●		3.0 3.5	4.0 4.5 5.0 5.5	µA µA µA µA
	Sleep Mode Operating Current	Supply Plus Reference Current, $V_{CC} = V_{REF} = 5V$ (Note 3)	 ●		0.05	0.10 0.18	µA µA
DC Performance							
	Short-Circuit Current Low	$V_{OUT} = 0V$, $V_{CC} = V_{REF} = 5V$, Code = 1023 (Note 7)	●	5	12	70	mA
	Short-Circuit Current High	$V_{OUT} = V_{CC} = V_{REF} = 5V$, Code = 0 (Note 7)	●	3	10	80	mA
AC Performance							
	Voltage Output Slew Rate	Rising (Notes 4, 5) Falling (Notes 4, 5)			20 7		V/ms V/ms
	Voltage Output Settling Time	Rising $0.1V_{FS}$ to $0.9V_{FS}$ ±0.5LSB (Notes 4, 5) Falling $0.9V_{FS}$ to $0.1V_{FS}$ ±0.5LSB (Notes 4, 5)			0.40 0.75		ms ms
	Capacitive Load Driving				1000		pF
Digital I/O							
V_{IH}	Digital Input High Voltage	$V_{CC} = 2.7V$ to $5.5V$ $V_{CC} = 2.7V$ to $3.6V$	● ●	2.4 2.0			V V
V_{IL}	Digital Input Low Voltage	$V_{CC} = 4.5V$ to $5.5V$ $V_{CC} = 2.7V$ to $5.5V$	● ●			0.8 0.6	V V
I_{LK}	Digital Input Leakage	V_{IN} = GND to V_{CC}	●		±0.05	±1.0	µA
C_{IN}	Digital Input Capacitance				1.5		pF

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} = 4.5V to 5.5V							
t_1	SDI Setup	Relative to SCK Positive Edge	●	55			ns
t_2	SDI Hold	Relative to SCK Positive Edge	●	0			ns
t_3	SCK High Time	(Note 6)	●	30			ns
t_4	SCK Low Time	(Note 6)	●	30			ns
t_5	$\overline{CS}$/LD Pulse Width	(Note 6)	●	100			ns
t_6	LSB SCK High to $\overline{CS}$/LD High	(Note 6)	●	30			ns
t_7	$\overline{CS}$/LD Low to SCK High	(Note 6)	●	20			ns
t_9	SCK Low to $\overline{CS}$/LD Low	(Note 6)	●	0			ns
t_{11}	$\overline{CS}$/LD High to SCK Positive Edge	(Note 6)	●	20			ns
	SCK Frequency	Square Wave (Note 6)	●			16.7	MHz
V_{CC} = 2.7V to 5.5V							
t_1	SDI Setup	Relative to SCK Positive Edge (Note 6)	●	75			ns
t_2	SDI Hold	Relative to SCK Positive Edge (Note 6)	●	0			ns
t_3	SCK High Time	(Note 6)	●	50			ns
t_4	SCK Low Time	(Note 6)	●	50			ns
t_5	$\overline{CS}$/LD Pulse Width	(Note 6)	●	150			ns
t_6	LSB SCK High to $\overline{CS}$/LD High	(Note 6)	●	50			ns
t_7	$\overline{CS}$/LD Low to SCK High	(Note 6)	●	30			ns
t_9	SCK Low to $\overline{CS}$/LD Low	(Note 6)	●	0			ns
t_{11}	$\overline{CS}$/LD High to SCK Positive Edge	(Note 6)	●	30			ns
	SCK Frequency	Square Wave (Note 6)	●			10	MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Nonlinearity and monotonicity are defined and tested at V_{CC} = 5V, V_{REF} = 4.096V, from code 20 to code 1023. See Figure 2.

Note 3: Digital inputs at 0V or V_{CC}.

Note 4: Load is 10kΩ in parallel with 100pF.

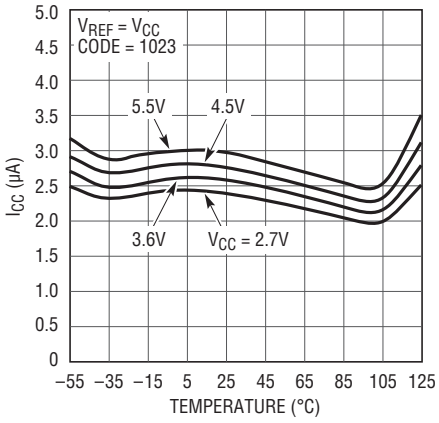
Note 5: V_{CC} = V_{REF} = 5V. DAC switched between 0.1V_{FS} and 0.9V_{FS}; i.e., codes k = 102 and k = 922.

Note 6: Guaranteed by design, not subject to test.

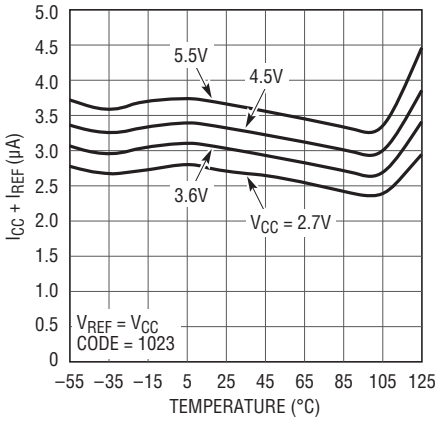
Note 7: One DAC output loaded.

TYPICAL PERFORMANCE CHARACTERISTICS

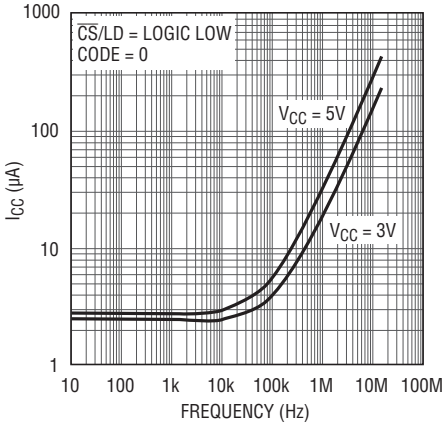
Supply Current vs Temperature



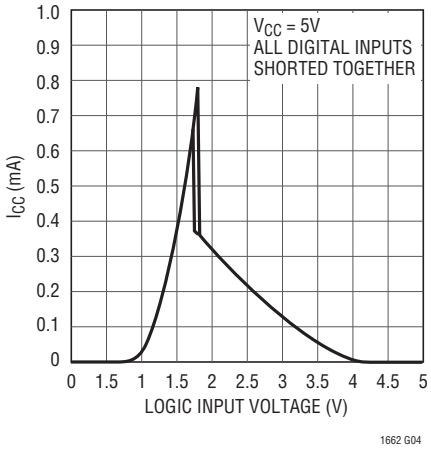
Total Supply-Plus-Reference Operating Current



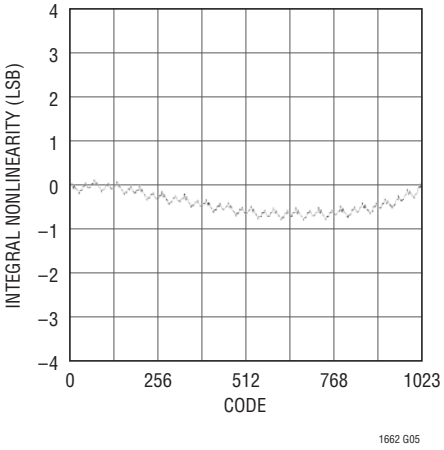
Supply Current vs Clock Frequency



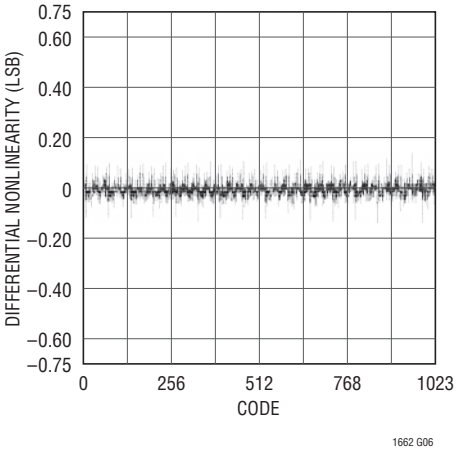
Supply Current vs Logic Input Voltage



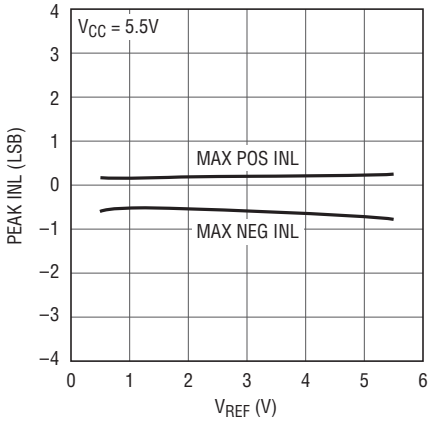
Integral Nonlinearity (INL)



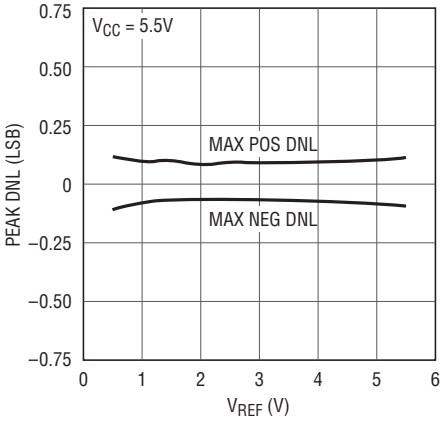
Differential Nonlinearity (DNL)



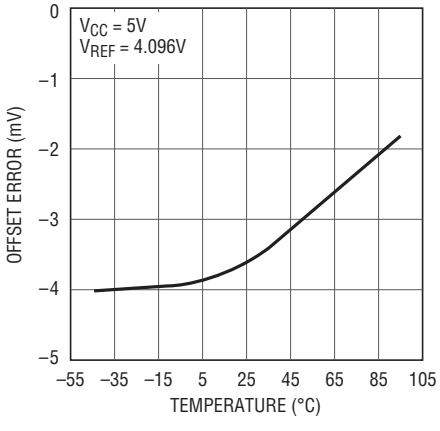
Integral Nonlinearity (INL) vs Reference Voltage



Differential Nonlinearity (DNL) vs Reference Voltage

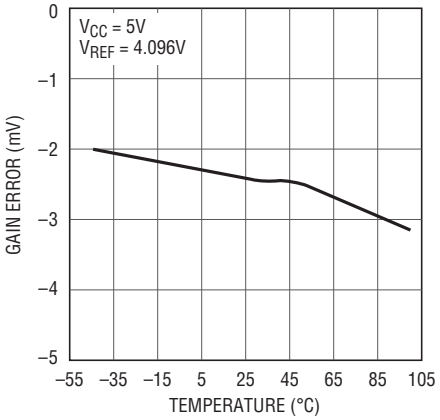


Offset Voltage vs Temperature

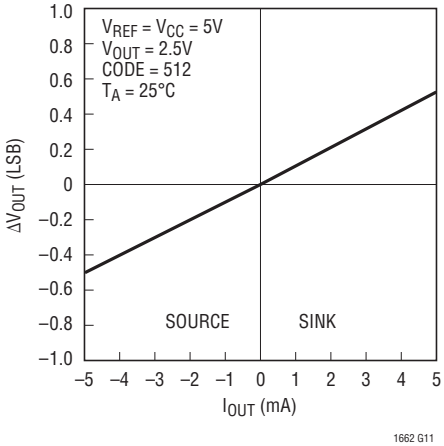


TYPICAL PERFORMANCE CHARACTERISTICS

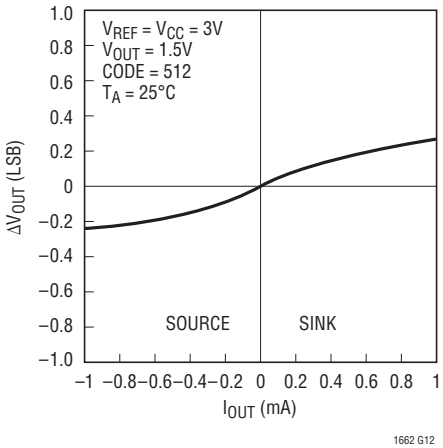
Gain Error vs Temperature



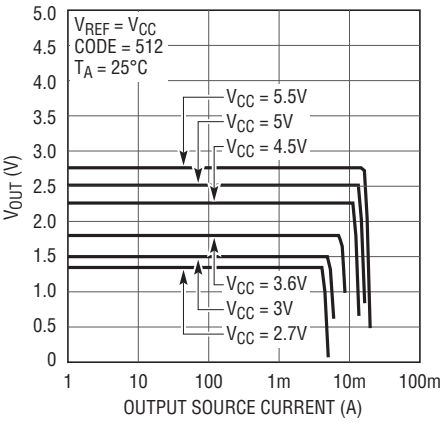
Load Regulation vs Output Current at 5V



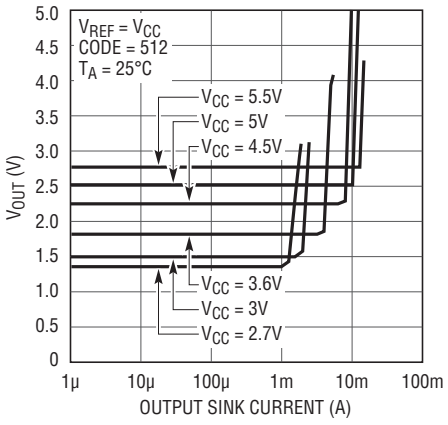
Load Regulation vs Output Current at 3V



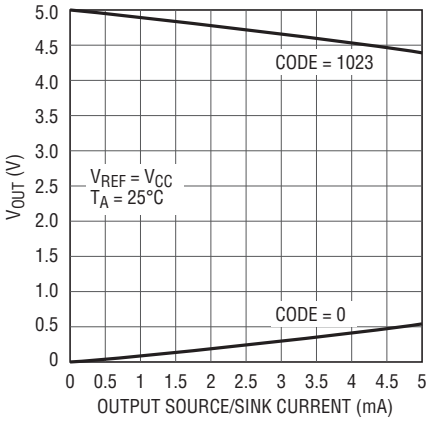
Output Amplifier Current Sourcing Capability (Mid-Scale)



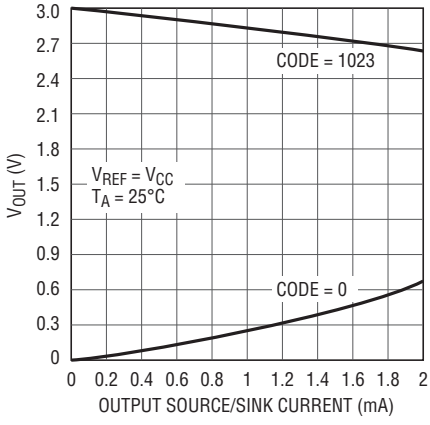
Output Amplifier Current Sinking Capability (Mid-Scale)



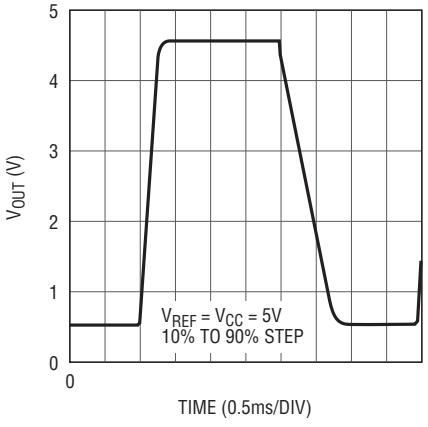
Max/Min Output Voltage vs Source/ Sink Output Current (V_{CC} = 5V)



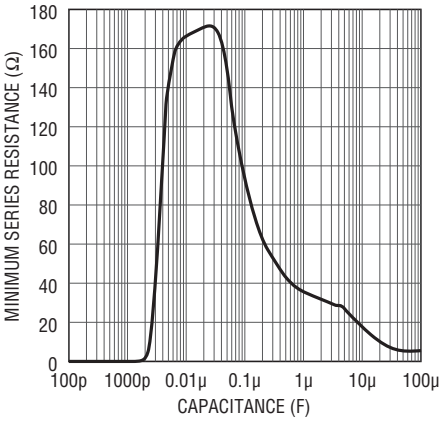
Max/Min Output Voltage vs Source/ Sink Output Current (V_{CC} = 3V)



Large-Signal Step Response



Output Minimum Series Resistance vs Load Capacitance



PIN FUNCTIONS

$\overline{CS}$/LD (Pin 1): Serial Interface Chip Select/Load Input. When $\overline{CS}$/LD is low, SCK is enabled for shifting data on SDI into the register. When $\overline{CS}$/LD is pulled high, SCK is disabled and the operation(s) specified in the control code, A3-A0, is (are) performed. CMOS and TTL compatible.

SCK (Pin 2): Serial Interface Clock Input. CMOS and TTL compatible.

SDI (Pin 3): Serial Interface Data Input. Input word data on the SDI pin is shifted into the 16-bit register on the rising edge of SCK. CMOS and TTL compatible.

REF (Pin 4): Reference Voltage Input. $0V \le V_{REF} \le V_{CC}$.

V_{OUTA}, V_{OUTB} (Pin 8, Pin 5): DAC Analog Voltage Outputs. The output range is

$$0 \le V_{OUTA}, V_{OUTB} \le V_{REF}\left(\frac{1023}{1024}\right)$$

V_{CC} (Pin 6): Supply Voltage Input. $2.7V \le V_{CC} \le 5.5V$.

GND (Pin 7): System Ground.

DEFINITIONS

Differential Nonlinearity (DNL): The difference between the measured change and the ideal 1LSB change for any two adjacent codes. The DNL error between any two codes is calculated as follows:

$$DNL = (\Delta V_{OUT} - LSB)/LSB$$

where ΔV_{OUT} is the measured voltage difference between two adjacent codes.

Full-Scale Error (FSE): The deviation of the actual full-scale voltage from ideal. FSE includes the effects of offset and gain errors (see Figure 2).

Gain Error (GE): The deviation from the slope of the ideal DAC transfer function, expressed in LSBs at full-scale.

Integral Nonlinearity (INL): The deviation from a straight line passing through the endpoints of the DAC transfer curve (endpoint INL). Because the output cannot go below zero, the linearity is measured between full-scale and the lowest code which guarantees the output will be greater than zero. The INL error at a given input code is calculated as follows:

$$INL = [V_{OUT} - V_{OS} - (V_{FS} - V_{OS})(code/1023)]/LSB$$

where V_{OUT} is the output voltage of the DAC measured at the given input code.

Least Significant Bit (LSB): The ideal voltage difference between two successive codes.

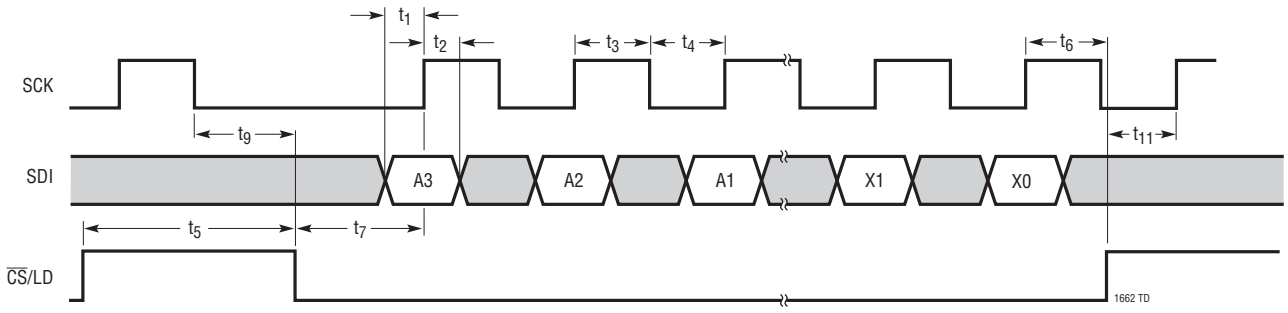
$$LSB = V_{REF}/1024$$

Resolution (n): Defines the number of DAC output states (2^n) that divide the full-scale range. Resolution does not imply linearity.

Voltage Offset Error (V_{OS}): Nominally, the voltage at the output when the DAC is loaded with all zeros. A single supply DAC can have a true negative offset, but the output cannot go below zero (see Figure 2).

For this reason, single supply DAC offset is measured at the lowest code that guarantees the output will be greater than zero.

TIMING DIAGRAM



OPERATION

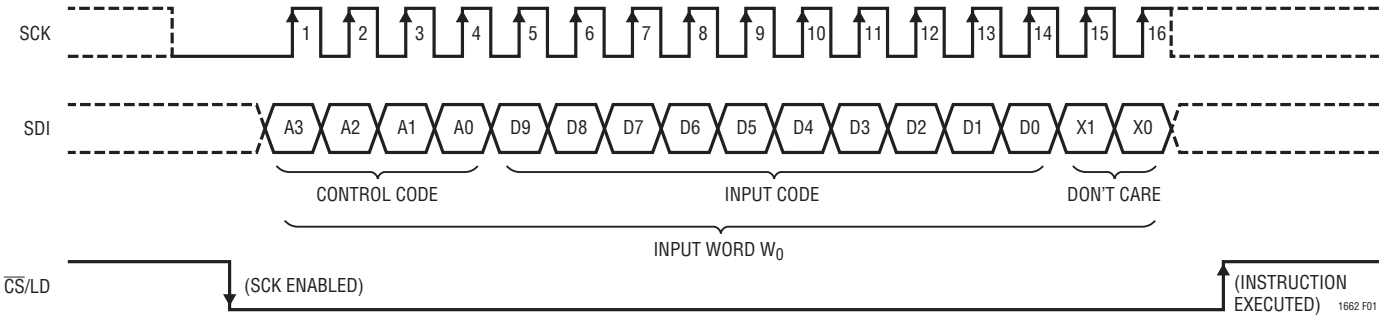


Figure 1. Register Loading Sequence

OPERATION

Table 1. DAC Control Functions

CONTROL				INPUT REGISTER STATUS	DAC REGISTER STATUS	POWER-DOWN STATUS (SLEEP/WAKE)	COMMENTS
A3	A2	A1	A0				
0	0	0	0	No Change	No Update	No Change	No Operation. Power-Down Status Unchanged (Part Stays In Wake or Sleep Mode)
0	0	0	1	Load DAC A	No Update	No Change	Load Input Register A with Data. DAC Outputs Unchanged. Power-Down Status Unchanged
0	0	1	0	Load DAC B	No Update	No Change	Load Input Register B with Data. DAC Outputs Unchanged. Power-Down Status Unchanged
1	0	0	0	No Change	Update Outputs	Wake	Load Both DAC Regs with Existing Contents of Input Regs. Outputs Update. Part Wakes Up
1	0	0	1	Load DAC A	Update Outputs	Wake	Load Input Reg A. Load DAC Regs with New Contents of Input Reg A and Existing Contents of Reg B. Outputs Update. Part Wakes Up
1	0	1	0	Load DAC B	Update Outputs	Wake	Load Input Reg B. Load DAC Regs with Existing Contents of Input Reg A and New Contents of Reg B. Outputs Update. Part Wakes Up
1	1	0	1	No Change	No Update	Wake	Part Wakes Up. Input and DAC Regs Unchanged. DAC Outputs Reflect Existing Contents of DAC Regs
1	1	1	0	No Change	No Update	Sleep	Part Goes to Sleep. Input and DAC Regs Unchanged. DAC Outputs Set to High Impedance State
1	1	1	1	Load DACs A, B with Same 10-Bit Code	Update Outputs	Wake	Load Both Input Regs. Load Both DAC Regs with New Contents of Input Regs. Outputs Update. Part Wakes Up

Note: All control codes other than those shown are undefined and not subject to test.

Transfer Function

The transfer function for the LTC1662 is:

$$V_{OUT(IDEAL)} = \left(\frac{k}{1024}\right) V_{REF}$$

where k is the decimal equivalent of the binary DAC input code D9-D0 and V_{REF} is the voltage at REF (Pin 4).

Power-On Reset

The LTC1662 actively clears the outputs to zero-scale when power is first applied, making system initialization consistent and repeatable.

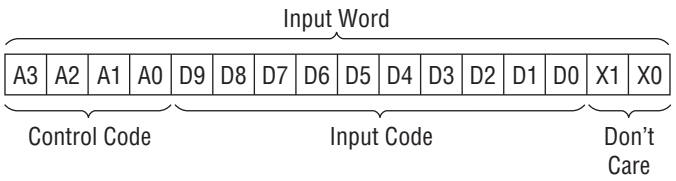
Power Supply Sequencing

The voltage at REF (Pin 4) should be kept within the range $-0.3V \le V_{REF} \le V_{CC} + 0.3V$ (see the Absolute Maximum Ratings). Particular care should be taken during power supply turn-on and turn-off sequences, when the voltage at V_{CC} (Pin 6) is in transition. If it is not possible to sequence the supplies, clamp the voltage at REF by connecting a Schottky diode between Pin 4 (anode) and Pin 6 (cathode).

Serial Interface

See Table 2. The 16-bit input word consists of the 4-bit control code, the 10-bit input code and two don't-care bits.

Table 2. LTC1662 Input Word



After the input word is loaded into the register (see Figure 1), it is internally converted from serial to parallel format. The parallel 10-bit-wide input code data path is then buffered by two latch registers.

OPERATION

The first of these, the input register, is used for loading new input codes. The second buffer, the DAC register, is used for updating the DAC outputs. Each DAC has its own 10-bit input register and 10-bit DAC register.

By selecting the appropriate 4-bit control code (see Table 1) it is possible to perform single operations, such as loading one DAC or changing power-down status (sleep/wake). In addition, some control codes perform two or more operations at the same time. For example, one such code loads DAC A, updates both outputs and Wakes the part up. The DACs can be loaded separately or together, but the outputs are always updated together.

Register Loading Sequence

See Figure 1. With $\overline{CS}$/LD held low, data on the SDI input is shifted into the 16-bit shift register on the positive edge of SCK. The 4-bit control code, A3-A0, is loaded first, then the 10-bit input code, D9-D0, ordered MSB to LSB in each case. Two don't-care bits, X1 and X0, are loaded last. When the full 16-bit input word has been shifted in, $\overline{CS}$/LD is pulled high, causing the system to respond according to Table 1. The clock is disabled internally when $\overline{CS}$/LD is high. Note: SCK must be low when $\overline{CS}$/LD is pulled low.

Sleep Mode

DAC control code 1110_b is reserved for the special sleep instruction (see Table 1). In this mode, static power consumption is greatly reduced. The reference input and analog outputs are set in a high impedance state and all DAC settings are retained in memory so that when sleep mode is exited, the outputs of DACs not updated by the Wake command are restored to their last active state.

Sleep mode is initiated by performing a load sequence using control code 1110_b (the DAC input code D9-D0 is ignored).

To save instruction cycles, the DACs may be prepared with new input codes during sleep (control codes 0001_b and 0010_b); then, a single command (1000_b) can be used both to wake the part and to update the output values.

Alternatively, one DAC may be loaded with a new input code during sleep; then with just one command, the other DAC is loaded, the part is awakened and both outputs are updated.

For example, control code 0001_b is used to load DAC A during sleep. Then control code 0101_b loads DAC B, wakes the part and simultaneously updates both DAC outputs.

Voltage Outputs

Each of the rail-to-rail output amplifiers contained in the LTC1662 can typically source or sink at least 1mA (V_{CC} = 5V). The outputs swing to within a few millivolts of either supply when unloaded and have an equivalent output resistance of 130Ω (typical) when driving a load to the rails. The output amplifiers are stable driving capacitive loads of up to 1000pF.

A small resistor placed in series with the output can be used to achieve stability for any load capacitance. Please see the Output Minimum Resistance vs Load Capacitance curve in the Typical Performance Characteristics section.

Rail-to-Rail Output Considerations

In any rail-to-rail DAC, the output swing is limited to voltages within the supply range.

If the DAC offset is negative, the output for the lowest codes limits at 0V as shown in Figure 2b.

Similarly, limiting can occur near full-scale when the REF pin is tied to V_{CC}. If $V_{REF} = V_{CC}$ and the DAC full-scale error (FSE = V_{OS} + GE) is positive, the output for the highest codes limits at V_{CC} as shown in Figure 2c. No full-scale limiting can occur if V_{REF} is less than V_{CC} – FSE.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

OPERATION

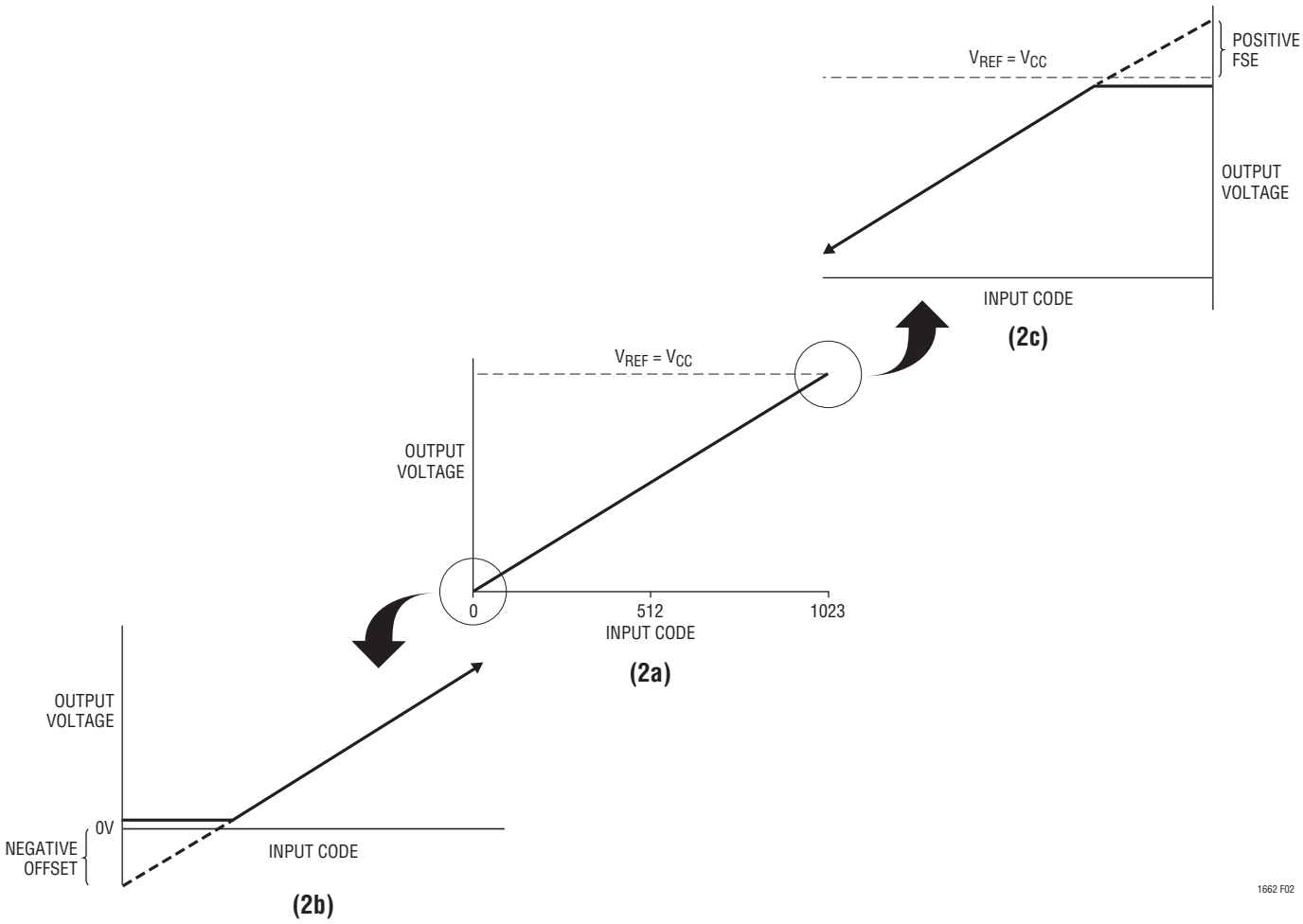
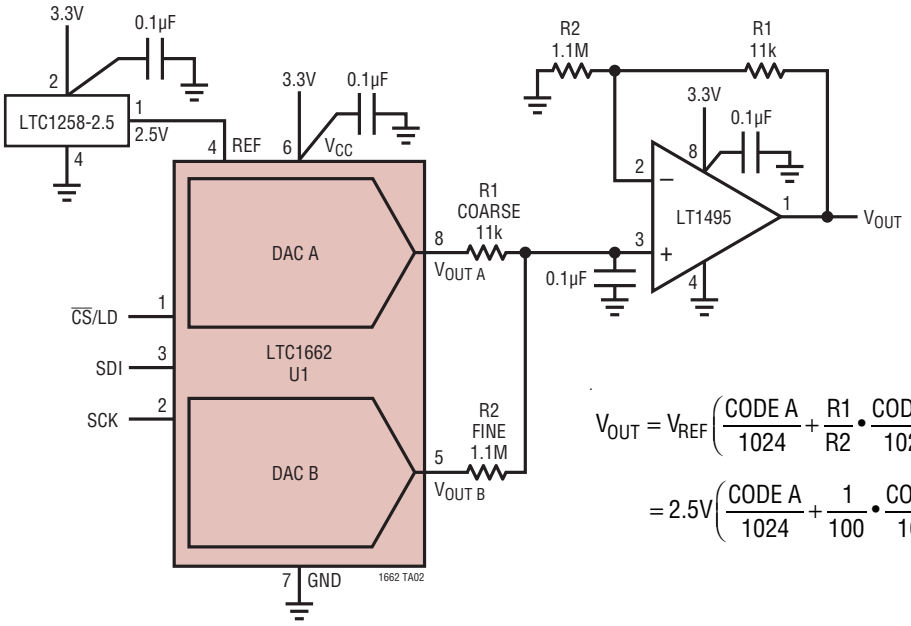


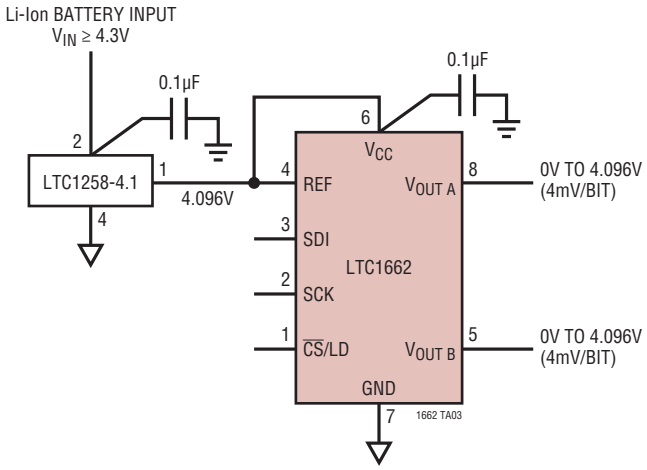
Figure 2. Effects of Rail-to-Rail Operation On a DAC Transfer Curve. (a) Overall Transfer Function (b) Effect of Negative Offset for Codes Near Zero-Scale (c) Effect of Positive Full-Scale Error for Input Codes Near Full-Scale When $V_{REF} = V_{CC}$

TYPICAL APPLICATIONS

Micropower Trim Circuit with Coarse/Fine Adjustment. Total Supply Current Is 9.5µA



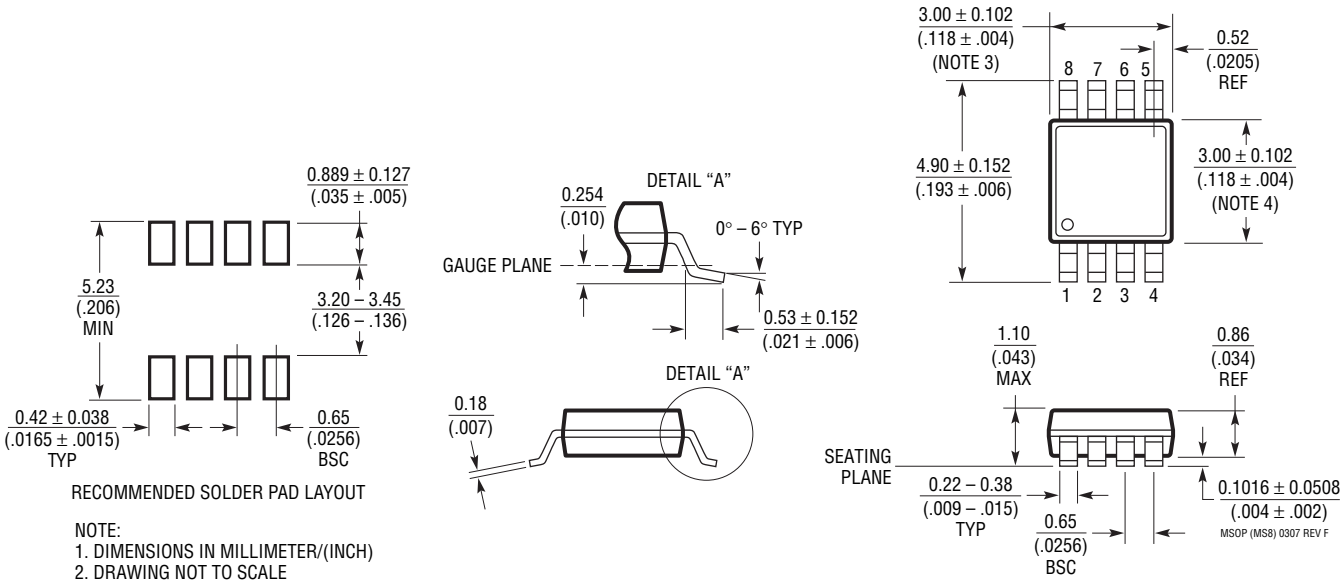
Using the LTC1258 and the LTC1662 in a Portable Application Powered by a Single Li-Ion Battery. Total Supply Current Is 8.2µA



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev F)

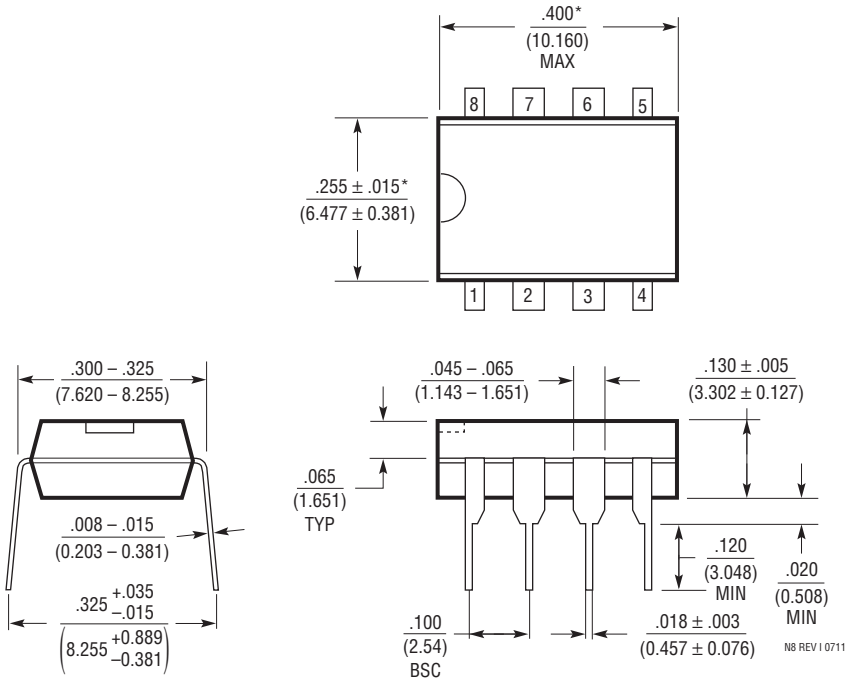


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

N Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510 Rev I)



NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

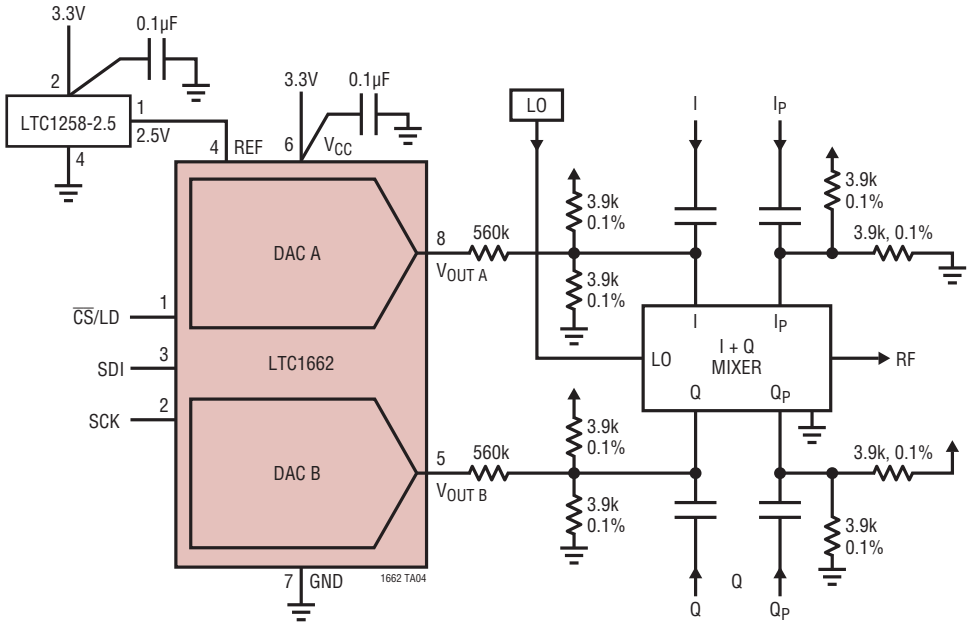
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/12	Removed Typical values in the Timing Characteristics section.	4
		Corrected Related Parts listing for the LTC1659.	16

TYPICAL APPLICATION

Ultralow Power DAC Optimizes Mixer Performance



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1661	Dual 10-Bit V_{OUT} DAC in 8-Lead MSOP Package	V_{CC} = 2.7V to 5.5V, 60µA per DAC, Rail-to-Rail Output
LTC1663	Single 10-Bit V_{OUT} DAC with 2-Wire Interface in SOT-23 Package	V_{CC} = 2.7V to 5.5V, Internal Reference, 60µA
LTC1664	Quad 10-Bit V_{OUT} DAC in 16-Pin Narrow SSOP	V_{CC} = 2.7V to 5.5V, 60µA per DAC, Rail-to-Rail Output
LTC1665/LTC1660	Octal 8-/10-Bit V_{OUT} DAC in 16-Pin Narrow SSOP	V_{CC} = 2.7V to 5.5V, 60µA per DAC, Rail-to-Rail Output
LTC1446/LTC1446L	Dual 12-Bit V_{OUT} DACs in SO-8 Package with Internal Reference	LTC1446: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1446L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1448	Dual 12-Bit V_{OUT} DAC in SO-8 Package	V_{CC} = 2.7V to 5.5V, External Reference Can Be Tied to V_{CC}
LTC1454/LTC1454L	Dual 12-Bit V_{OUT} DACs in SO-16 Package with Added Functionality	LTC1454: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1454L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1458/LTC1458L	Quad 12-Bit Rail-to-Rail Output DACs with Added Functionality	LTC1458: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1458L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1659	Single Rail-to-Rail 12-Bit V_{OUT} DAC in 8-Lead MSOP Package	V_{CC} = 2.7V to 5.5V, Low Power Multiplying V_{OUT} DAC. Output Swings from GND to REF. REF Input Can Be Tied to V_{CC}

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