LTC2600/LTC2610/LTC2620

Octal 16-/14-/12-Bit Rail-to-Rail DACs in 16-Lead SSOP

FEATURES

- **Smallest Pin-Compatible Octal DACs:**
  LTC2600: 16 Bits
  LTC2610: 14 Bits
  LTC2620: 12 Bits
- **Guaranteed 16-Bit Monotonic Over Temperature**
- Wide 2.5V to 5.5V Supply Range
- Low Power Operation: 250μA per DAC at 3V
- Individual Channel Power-Down to 1μA, Max
- Ultralow Crosstalk Between DACs (<10μV)
- High Rail-to-Rail Output Drive (±15mA, Min)
- Double-Buffered Digital Inputs
- Pin-Compatible 10-/8-Bit Versions (LTC1660/LTC1665)
- Tiny 16-Lead Narrow SSOP and 20-Lead 4mm × 5mm QFN Packages

APPLICATIONS

- Mobile Communications
- Process Control and Industrial Automation
- Instrumentation
- Automatic Test Equipment

DESCRIPTION

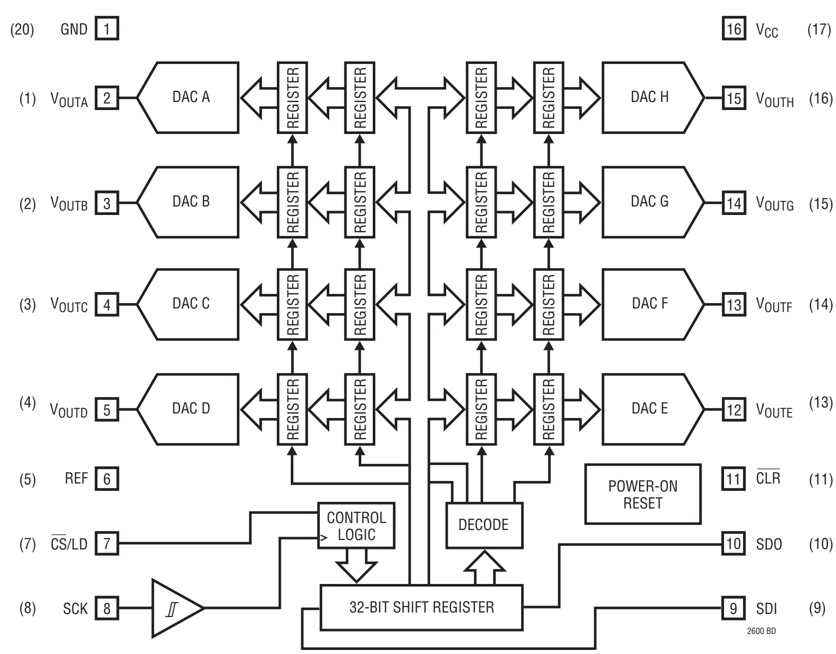
The LTC®2600/LTC2610/LTC2620 are octal 16-, 14- and 12-bit, 2.5V-to-5.5V rail-to-rail voltage-output DACs in 16-lead narrow SSOP and 20-lead 4mm × 5mm QFN packages. They have built-in high performance output buffers and are guaranteed monotonic.

These parts establish new board-density benchmarks for 16- and 14-bit DACs and advance performance standards for output drive, crosstalk and load regulation in single-supply, voltage-output multiples.

The parts use a simple SPI/MICROWIRE compatible 3-wire serial interface which can be operated at clock rates up to 50MHz. Daisychain capability and a hardware CLR function are included.

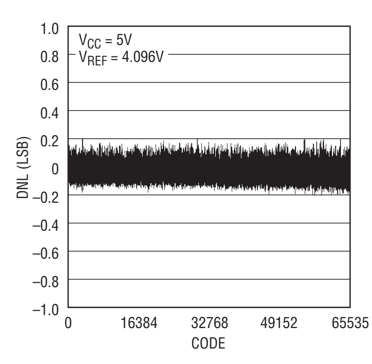
The LTC2600/LTC2610/LTC2620 incorporate a power-on reset circuit. During power-up, the voltage outputs rise less than 10mV above zero-scale; and after power-up, they stay at zero-scale until a valid write and update take place.

BLOCK DIAGRAM



NOTE: NUMBERS IN PARENTHESIS REFER TO THE UFD PACKAGE

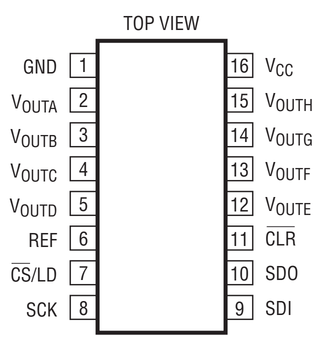
Differential Nonlinearity (LTC2600)



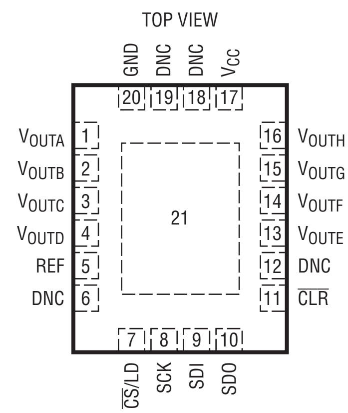
ABSOLUTE MAXIMUM RATINGS (Note 1)

Any Pin to GND .... –0.3V to 6V
Any Pin to V_{CC} .... –6V to 0.3V
Operating Temperature Range
  LTC2600C/LTC2610C/LTC2620C .... 0°C to 70°C
  LTC2600I/LTC2610I/LTC2620I............. –40°C to 85°C
Storage Temperature Range.................. –65°C to 150°C
Maximum Junction Temperature........................... 125°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PIN CONFIGURATION



GN PACKAGE
16-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 150°C/W



UFD PACKAGE
20-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2600CUFD#PBF	LTC2600CUFD#TRPBF	2600	20-Lead (4mm × 5mm) Plastic DFN	0°C to 70°C
LTC2600IUFD#PBF	LTC2600IUFD#TRPBF	2600	20-Lead (4mm × 5mm) Plastic DFN	–40°C to 85°C
LTC2600CGN#PBF	LTC2600CGN#TRPBF	2600	16-Lead Plastic SSOP	0°C to 70°C
LTC2600IGN#PBF	LTC2600IGN#TRPBF	2600I	16-Lead Plastic SSOP	–40°C to 85°C
LTC2610CUFD#PBF	LTC2610CUFD#TRPBF	2610	20-Lead (4mm × 5mm) Plastic DFN	0°C to 70°C
LTC2610IUFD#PBF	LTC2610IUFD#TRPBF	2610	20-Lead (4mm × 5mm) Plastic DFN	–40°C to 85°C
LTC2610CGN#PBF	LTC2610CGN#TRPBF	2610	16-Lead Plastic SSOP	0°C to 70°C
LTC2610IGN#PBF	LTC2610IGN#TRPBF	2610I	16-Lead Plastic SSOP	–40°C to 85°C
LTC2620CUFD#PBF	LTC2620CUFD#TRPBF	2620	20-Lead (4mm × 5mm) Plastic DFN	0°C to 70°C
LTC2620IUFD#PBF	LTC2620IUFD#TRPBF	2620	20-Lead (4mm × 5mm) Plastic DFN	–40°C to 85°C
LTC2620CGN#PBF	LTC2620CGN#TRPBF	2620	16-Lead Plastic SSOP	0°C to 70°C
LTC2620IGN#PBF	LTC2620IGN#TRPBF	2620I	16-Lead Plastic SSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.5V to 5.5V, V_{REF} ≤ V_{CC}, V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC2620 MIN	LTC2620 TYP	LTC2620 MAX	LTC2610 MIN	LTC2610 TYP	LTC2610 MAX	LTC2600 MIN	LTC2600 TYP	LTC2600 MAX	UNITS
DC Performance													
	Resolution		●	12			14			16			Bits
	Monotonicity	V_{CC} = 5V, V_{REF} = 4.096V (Note 2)	●	12			14			16			Bits
DNL	Differential Nonlinearity	V_{CC} = 5V, V_{REF} = 4.096V (Note 2)	●			±0.5			±1			±1	LSB
INL	Integral Nonlinearity	V_{CC} = 5V, V_{REF} = 4.096V (Note 2)	●		±0.75	±4		±3	±16		±12	±64	LSB
	Load Regulation	V_{REF} = V_{CC} = 5V, Mid-Scale I_{OUT} = 0mA to 15mA Sourcing I_{OUT} = 0mA to 15mA Sinking	 ● ●		 0.025 0.025	 0.125 0.125		 0.1 0.1	 0.5 0.5		 0.3 0.3	 2 2	 LSB/mA LSB/mA
		V_{REF} = V_{CC} = 2.5V, Mid-Scale I_{OUT} = 0mA to 7.5mA Sourcing I_{OUT} = 0mA to 7.5mA Sinking	 ● ●		 0.05 0.05	 0.25 0.25		 0.2 0.2	 1 1		 0.8 0.8	 4 4	 LSB/mA LSB/mA
ZSE	Zero-Scale Error	V_{CC} = 5V, V_{REF} = 4.096V Code = 0			1	9		1	9		1	9	mV
V_{OS}	Offset Error	V_{CC} = 5V, V_{REF} = 4.096V (Note 7)			±1	±9		±1	±9		±1	±9	mV
	V_{OS} Temperature Coefficient				±3			±3			±3		µV/°C
GE	Gain Error	V_{CC} = 5V, V_{REF} = 4.096V			±0.2	±0.7		±0.2	±0.7		±0.2	±0.7	%FSR
	Gain Temperature Coefficient				±6.5			±6.5			±6.5		ppm/°C

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.5V to 5.5V, V_{REF} ≤ V_{CC}, V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC2600/LTC2610/LTC2620 MIN	TYP	MAX	UNITS
PSR	Power Supply Rejection	V_{CC} = ±10%			–80		dB
R_{OUT}	DC Output Impedance	V_{REF} = V_{CC} = 5V, Mid-Scale; –15mA ≤ I_{OUT} ≤ 15mA V_{REF} = V_{CC} = 2.5V, Mid-Scale; –7.5mA ≤ I_{OUT} ≤ 7.5mA	● ●		0.025 0.030	0.15 0.15	Ω Ω
	DC Crosstalk (Note 4)	Due to Full-Scale Output Change (Note 5) Due to Load Current Change Due to Powering Down (per Channel)			±10 ±3.5 ±7.3		µV µV/mA µV
I_{SC}	Short-Circuit Output Current	V_{CC} = 5.5V, V_{REF} = 5.6V Code: Zero-Scale; Forcing Output to V_{CC} Code: Full-Scale; Forcing Output to GND	 ● ●	 15 15	 34 34	 60 60	 mA mA
		V_{CC} = 2.5V, V_{REF} = 5.6V Code: Zero-Scale; Forcing Output to V_{CC} Code: Full-Scale; Forcing Output to GND	 ● ●	 7.5 7.5	 18 24	 50 50	 mA mA
Reference Input							
	Input Voltage Range		●	0		V_{CC}	V
	Resistance	Normal Mode	●	11	16	20	kΩ
	Capacitance				90		pF
I_{REF}	Reference Current, Power-Down Mode	All DACs Powered Down	●		0.001	1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.5V to 5.5V, V_{REF} ≤ V_{CC}, V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC2600/LTC2610/LTC2620 MIN	TYP	MAX	UNITS
Power Supply							
V_{CC}	Positive Supply Voltage		●	2.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5V (Note 3) V_{CC} = 3V (Note 3) All DACs Powered Down (Note 3) V_{CC} = 5V All DACs Powered Down (Note 3) V_{CC} = 3V	● ● ● ●		2.6 2.0 0.35 0.10	4 3.2 1 1	mA mA μA μA
Digital I/O							
V_{IH}	Digital Input High Voltage	V_{CC} = 2.5V to 5.5V V_{CC} = 2.5V to 3.6V	● ●	2.4 2.0			V V
V_{IL}	Digital Input Low Voltage	V_{CC} = 4.5V to 5.5V V_{CC} = 2.5V to 5.5V	● ●			0.8 0.6	V V
V_{OH}	Digital Output High Voltage	Load Current = –100μA	●	V_{CC} – 0.4			V
V_{OL}	Digital Output Low Voltage	Load Current = +100μA	●			0.4	V
I_{LK}	Digital Input Leakage	V_{IN} = GND to V_{CC}	●			±1	μA
C_{IN}	Digital Input Capacitance	(Note 6)	●			8	pF

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.5V to 5.5V, V_{REF} ≤ V_{CC}, V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LTC2620 MIN	TYP	MAX	LTC2610 MIN	TYP	MAX	LTC2600 MIN	TYP	MAX	UNITS
AC Performance												
t_S	Settling Time (Note 8)	±0.024% (±1LSB at 12 Bits) ±0.006% (±1LSB at 14 Bits) ±0.0015% (±1LSB at 16 Bits)		7			7 9			7 9 10		 μs μs
	Settling Time for 1LSB Step (Note 9)	±0.024% (±1LSB at 12 Bits) ±0.006% (±1LSB at 14 Bits) ±0.0015% (±1LSB at 16 Bits)		2.7			2.7 4.8			2.7 4.8 5.2		μs μs μs
	Voltage Output Slew Rate			0.80			0.80			0.80		V/μs
	Capacitive Load Driving			1000			1000			1000		pF
	Glitch Impulse	At Mid-Scale Transition		12			12			12		nV • s
	Multiplying Bandwidth			180			180			180		kHz
e_n	Output Voltage Noise Density	At f = 1kHz At f = 10kHz		120 100			120 100			120 100		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
	Output Voltage Noise	0.1Hz to 10Hz		15			15			15		$μV_{P-P}$

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (See Figure 1) (Note 6)

SYMBOL	PARAMETER	CONDITIONS		LTC2600/LTC2610/LTC2620 MIN	TYP	MAX	UNITS
V_{CC} = 2.5V to 5.5V							
t_1	SDI Valid to SCK Setup		●	4			ns
t_2	SDI Valid to SCK Hold		●	4			ns
t_3	SCK High Time		●	9			ns
t_4	SCK Low Time		●	9			ns
t_5	$\overline{CS}$/LD Pulse Width		●	10			ns
t_6	LSB SCK High to $\overline{CS}$/LD High		●	7			ns
t_7	$\overline{CS}$/LD Low to SCK High		●	7			ns
t_8	SDO Propagation Delay from SCK Falling Edge	C_{LOAD} = 10pF V_{CC} = 4.5V to 5.5V V_{CC} = 2.5V to 5.5V	 ● ●			 20 45	 ns ns
t_9	$\overline{CLR}$ Pulse Width		●	20			ns
t_{10}	$\overline{CS}$/LD High to SCK Positive Edge		●	7			ns
	SCK Frequency	50% Duty Cycle	●			50	MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Linearity and monotonicity are defined from code kL to code 2N – 1, where N is the resolution and k_L is given by $k_L = 0.016(2^N/V_{REF})$, rounded to the nearest whole code. For V_{REF} = 4.096V and N = 16, k_L = 256 and linearity is defined from code 256 to code 65,535.

Note 3: Digital inputs at 0V or V_{CC}.

Note 4: DC crosstalk is measured with V_{CC} = 5V and V_{REF} = 4.096V, with the measured DAC at mid-scale, unless otherwise noted.

Note 5: R_L = 2kΩ to GND or V_{CC}.

Note 6: Guaranteed by design and not production tested.

Note 7: Inferred from measurement at code 256 (LTC2600), code 64 (LTC2610) or code 16 (LTC2620), and at full-scale.

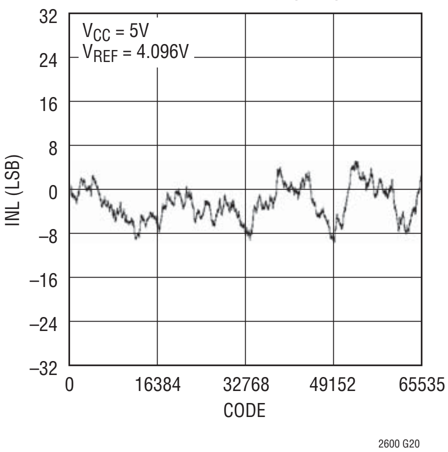
Note 8: V_{CC} = 5V, V_{REF} = 4.096V. DAC is stepped 1/4-scale to 3/4-scale and 3/4-scale to 1/4-scale. Load is 2k in parallel with 200pF to GND.

Note 9: V_{CC} = 5V, V_{REF} = 4.096V. DAC is stepped ±1LSB between half-scale and half-scale – 1. Load is 2k in parallel with 200pF to GND.

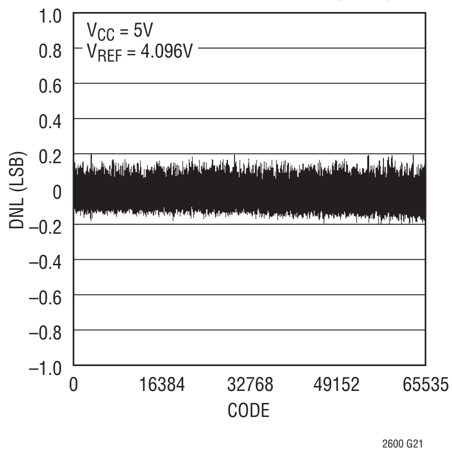
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2600

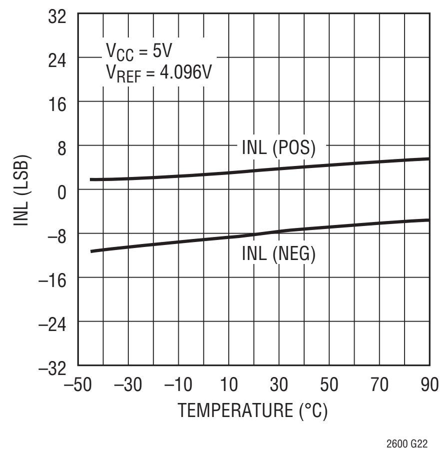
Integral Nonlinearity (INL)



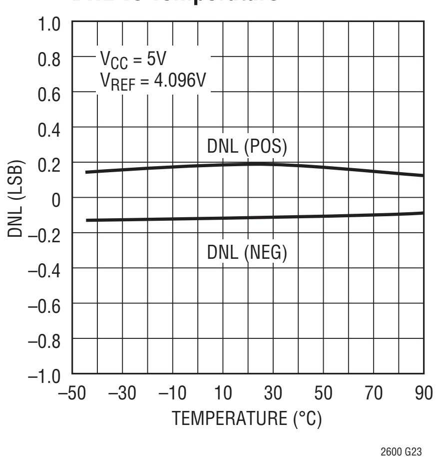
Differential Nonlinearity (DNL)



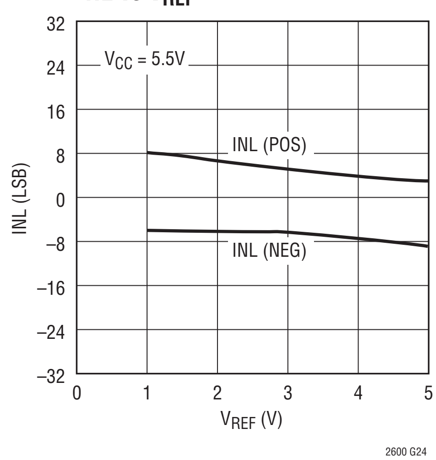
INL vs Temperature



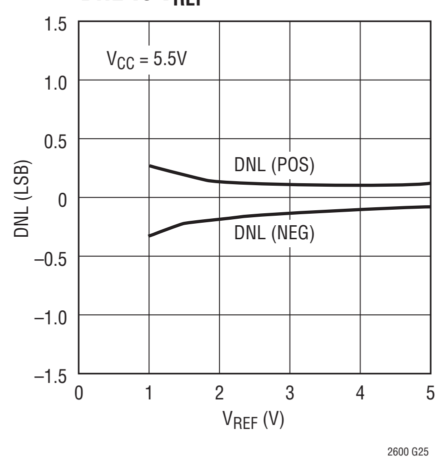
DNL vs Temperature



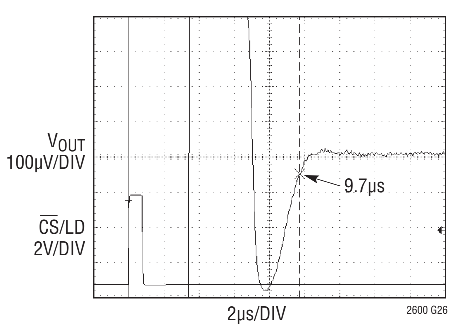
INL vs V_{REF}



DNL vs V_{REF}

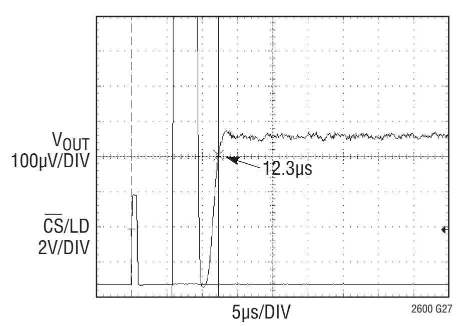


Settling to ±1LSB



V_{CC} = 5V, V_{REF} = 4.096V
1/4-SCALE TO 3/4-SCALE STEP
R_L = 2k, C_L = 200pF
AVERAGE OF 2048 EVENTS

Settling of Full-Scale Step

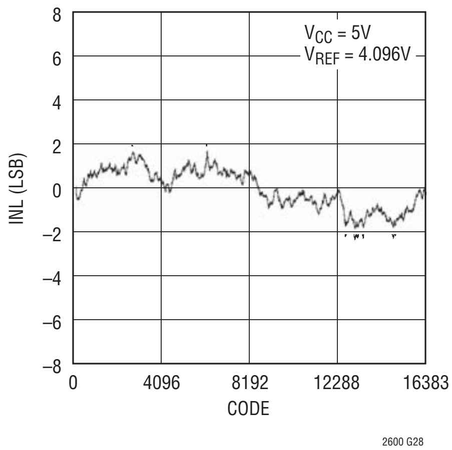


SETTLING TO ±1LSB
V_{CC} = 5V, V_{REF} = 4.096V
CODE 512 TO 65535 STEP
R_L = 2k, C_L = 200pF
AVERAGE OF 2048 EVENTS

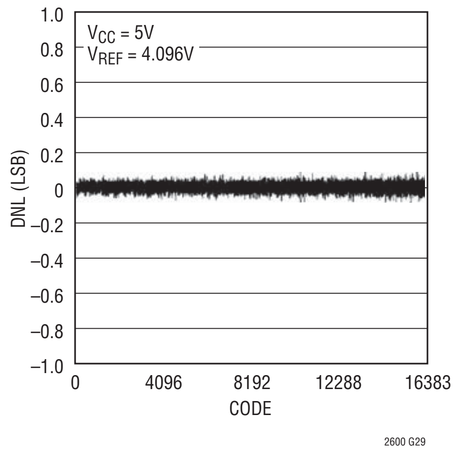
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2610

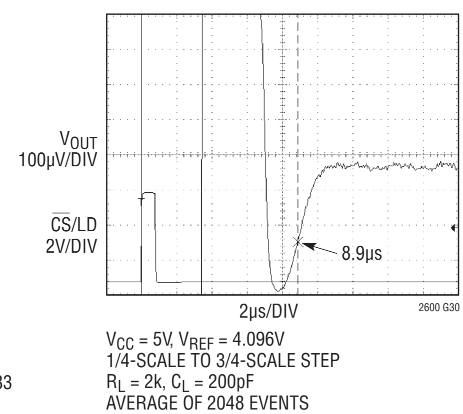
Integral Nonlinearity (INL)



Differential Nonlinearity (DNL)

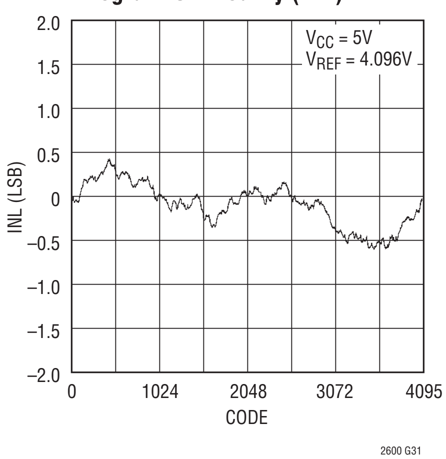


Settling to ±1LSB

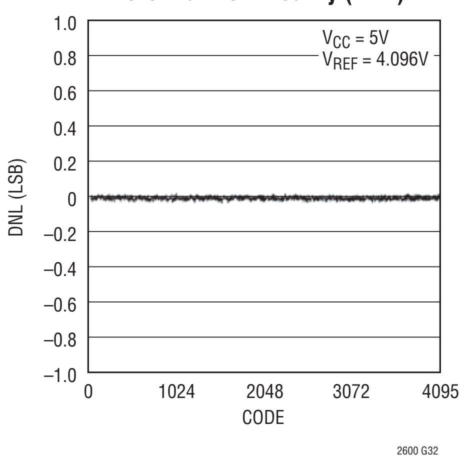


LTC2620

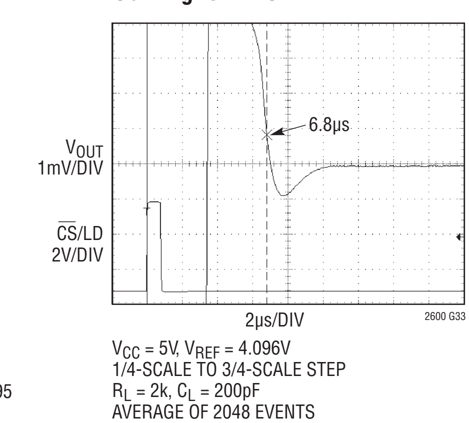
Integral Nonlinearity (INL)



Differential Nonlinearity (DNL)

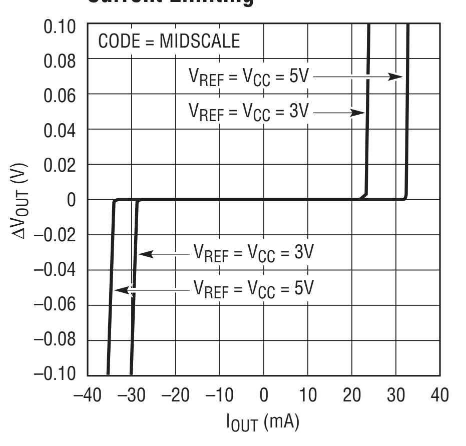


Settling to ±1LSB

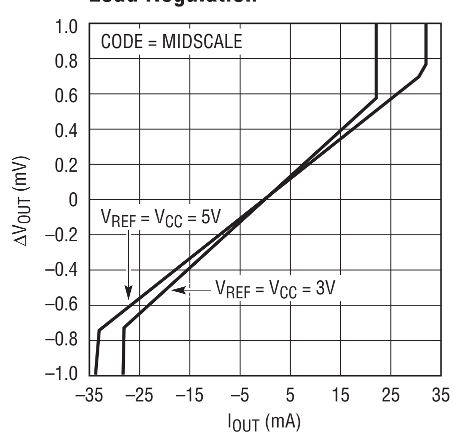


LTC2600/LTC2610/LTC2620

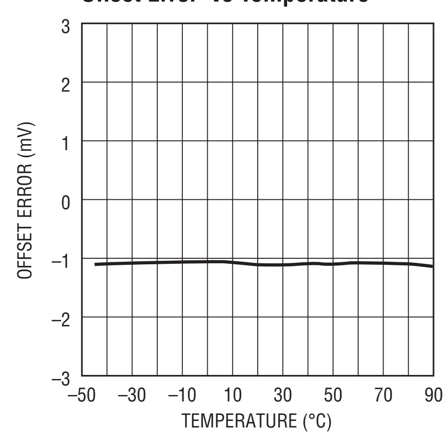
Current Limiting



Load Regulation



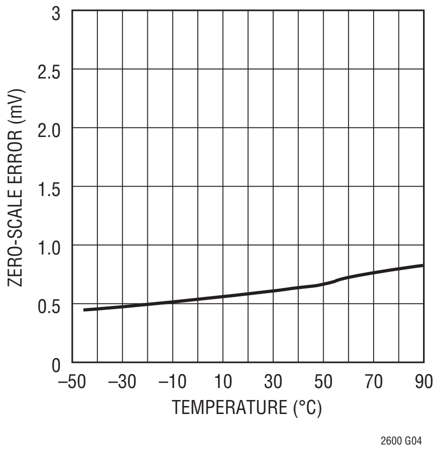
Offset Error vs Temperature



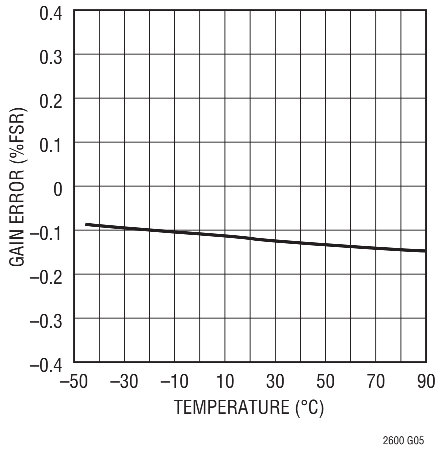
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2600/LTC2610/LTC2620

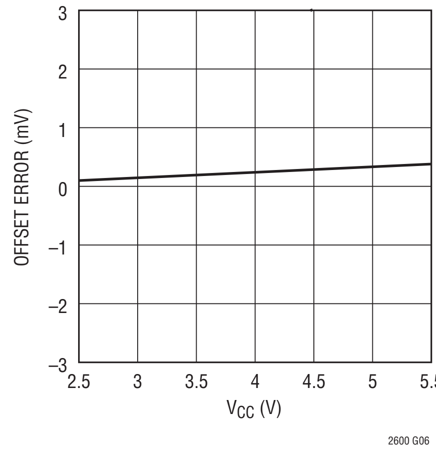
Zero-Scale Error vs Temperature



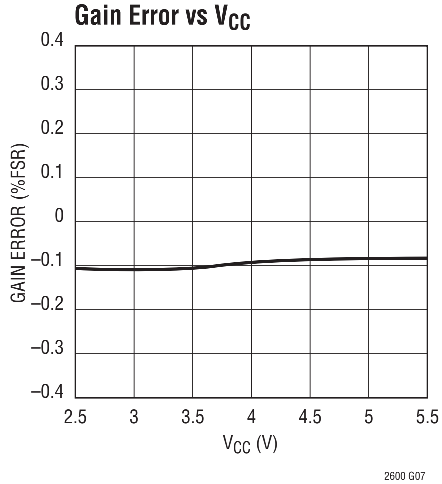
Gain Error vs Temperature



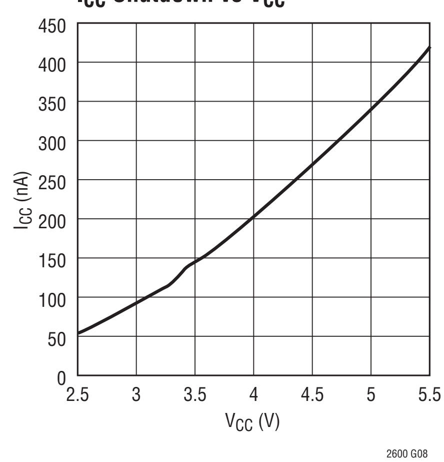
Offset Error vs V_{CC}



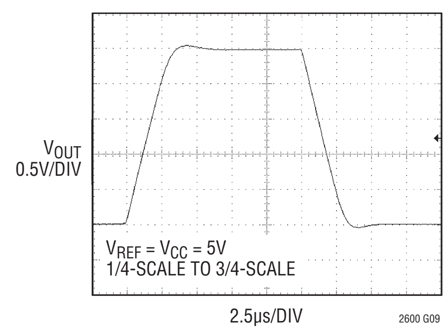
Gain Error vs V_{CC}



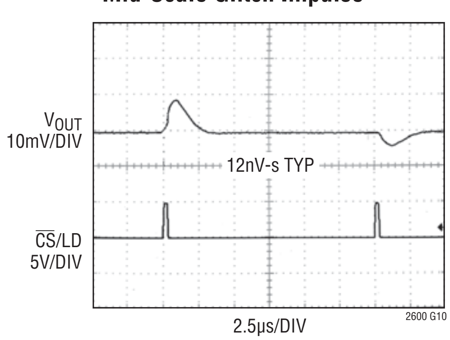
I_{CC} Shutdown vs V_{CC}



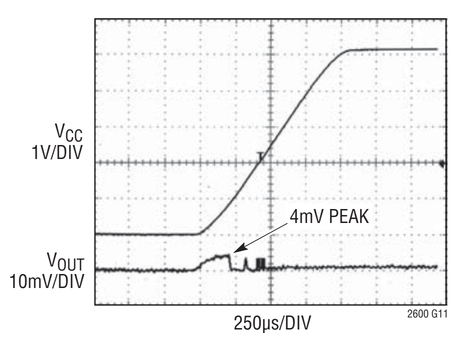
Large-Signal Response



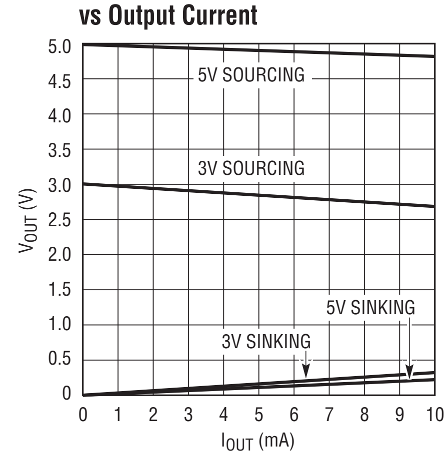
Mid-Scale Glitch Impulse



Power-On Reset Glitch



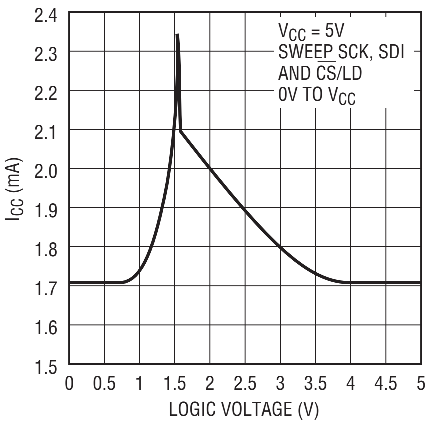
Headroom at Rails vs Output Current



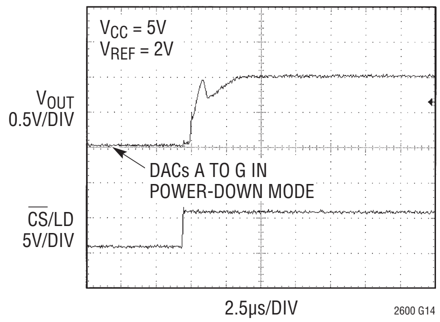
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2600/LTC2610/LTC2620

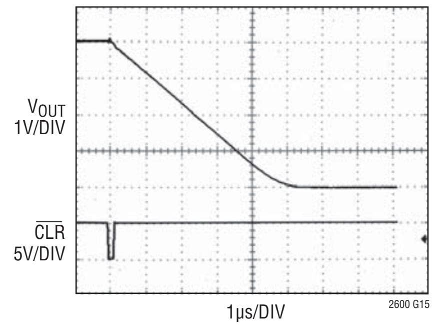
Supply Current vs Logic Voltage



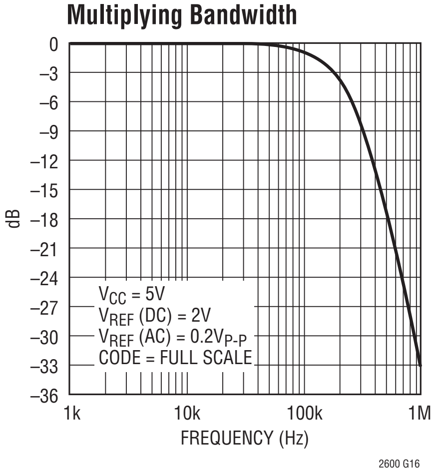
Exiting Power-Down to Mid-Scale



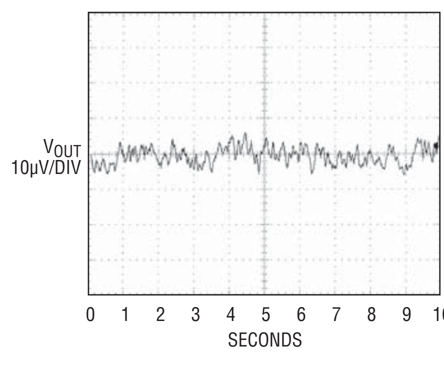
Hardware $\overline{CLR}$



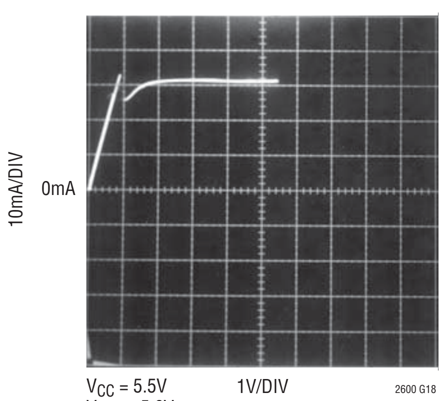
Multiplying Bandwidth



Output Voltage Noise, 0.1Hz to 10Hz

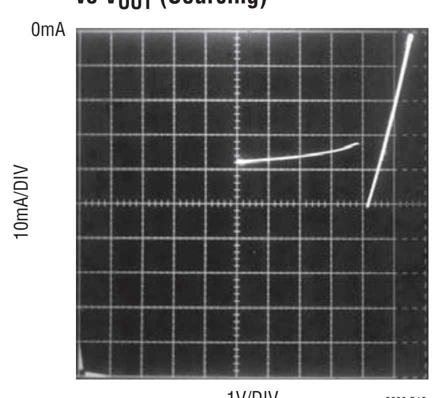


Short-Circuit Output Current vs V_{OUT} (Sinking)



V_{CC} = 5.5V
V_{REF} = 5.6V
CODE = 0
V_{OUT} SWEPT 0V TO V_{CC}

Short-Circuit Output Current vs V_{OUT} (Sourcing)



V_{CC} = 5.5V
V_{REF} = 5.6V
CODE = FULL SCALE
V_{OUT} SWEPT V_{CC} TO 0V

PIN FUNCTIONS (GN/UFD)

GND (Pin 1/Pin 20): Analog Ground.

V_{OUTA} to V_{OUTH} (Pins 2-5 and 12-15/Pins 1-48 and 13-16): DAC Analog Voltage Outputs. The output range is 0 – V_{REF}.

REF (Pin 6/Pin 5): Reference Voltage Input. $0V \le V_{REF} \le V_{CC}$.

$\overline{CS}$/LD (Pin 7/Pin 7): Serial Interface Chip Select/Load Input. When $\overline{CS}$/LD is low, SCK is enabled for shifting data on SDI into the register. When $\overline{CS}$/LD is taken high, SCK is disabled and the specified command (see Table 1) is executed.

SCK (Pin 8/Pin 8): Serial Interface Clock Input. CMOS and TTL compatible.

SDI (Pin 9/Pin 9): Serial Interface Data Input. Data is applied to SDI for transfer to the device at the rising edge of SCK. The LTC2600, LTC2610 and LTC2620 accept input word lengths of either 24 or 32 bits.

SDO (Pin 10/Pin 10): Serial Interface Data Output. This pin is used for daisychain operation. The serial output of the shift register appears at the SDO pin. The data transferred to the device via the SDI pin is delayed 32 SCK rising edges before being output at the next falling edge. SDO is an active output and does not go high impedance, even when $\overline{CS}$/LD is taken to a logic high level.

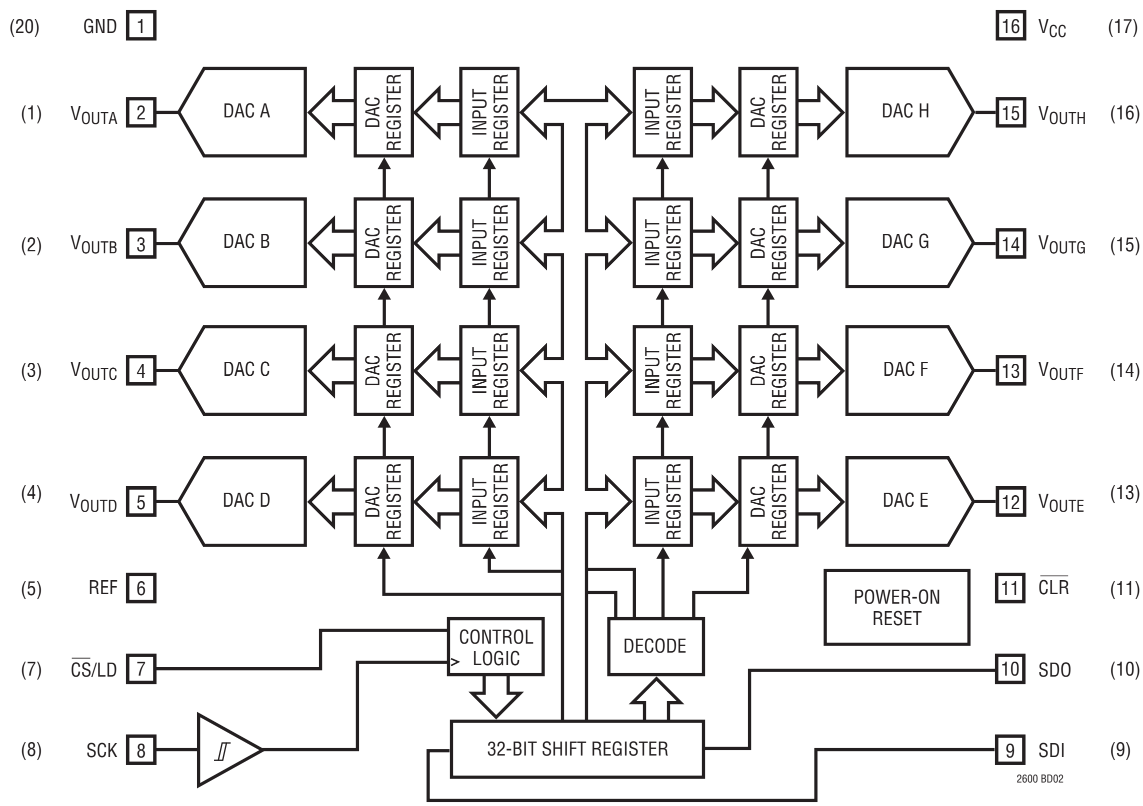
$\overline{CLR}$ (Pin 11/Pin 11): Asynchronous Clear Input. A logic low at this level-triggered input clears all registers and causes the DAC voltage outputs to drop to 0V. CMOS and TTL compatible.

V_{CC} (Pin 16/Pin 17): Supply Voltage Input. $2.5V \le V_{CC} \le 5.5V$.

DNC (Pins 6, 12, 18, 19 UFD Only): Do Not Connect.

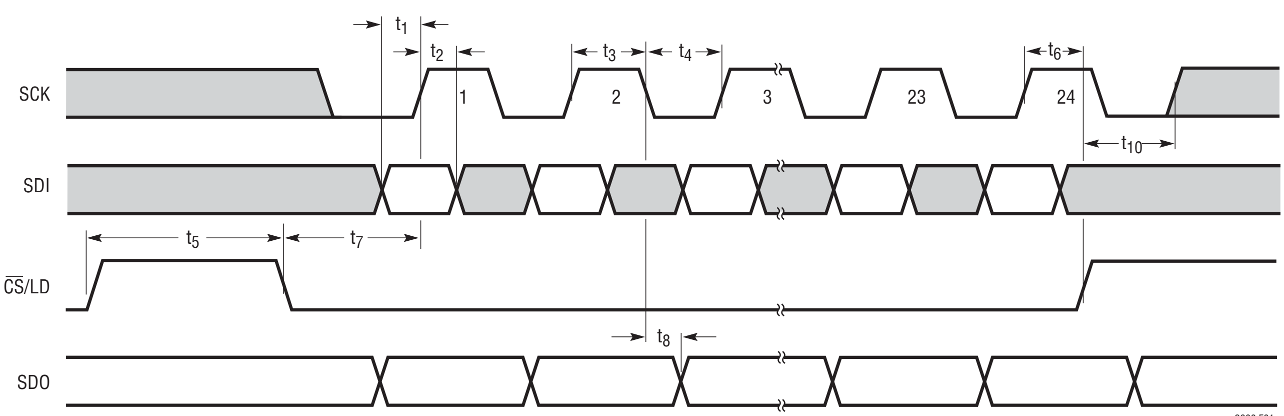
Exposed Pad (Pin 21 UFD Only): Ground. The exposed pad must be soldered to the PCB.

BLOCK DIAGRAM



NOTE: NUMBERS IN PARENTHESIS REFER TO THE UFD PACKAGE

TIMING DIAGRAM



OPERATION

Power-On Reset

The LTC2600/LTC2610/LTC2620 clear the outputs to zero-scale when power is first applied, making system initialization consistent and repeatable.

For some applications, downstream circuits are active during DAC power-up, and may be sensitive to nonzero outputs from the DAC during this time. The LTC2600/2610/2620 contain circuitry to reduce the power-on glitch: the analog outputs typically rise less than 10mV above zero-scale during power on if the power supply is ramped to 5V in 1ms or more. In general, the glitch amplitude decreases as the power supply ramp time is increased. See Power-On Reset Glitch in the Typical Performance Characteristics section.

Power Supply Sequencing

The voltage at REF (Pin 6) should be kept within the range $–0.3V \le V_{REF} \le V_{CC} + 0.3V$ (see Absolute Maximum Ratings). Particular care should be taken to observe these limits during power supply turn-on and turn-off sequences, when the voltage at V_{CC} (Pin 16) is in transition.

Transfer Function

The digital-to-analog transfer function is:

$$V_{OUT(IDEAL)} = \left(\frac{k}{2^N}\right) V_{REF}$$

where k is the decimal equivalent of the binary DAC input code, N is the resolution and V_{REF} is the voltage at REF (Pin 6).

Serial Interface

The $\overline{CS}$/LD input is level triggered. When this input is taken low, it acts as a chip-select signal, powering on the SDI and SCK buffers and enabling the input shift register. Data (SDI input) is transferred at the next 24 rising SCK edges. The 4-bit command, C3-C0, is loaded first; then the 4-bit DAC address, A3-A0; and finally the 16-bit data word. The data word comprises the 16-, 14- or 12-bit input code, ordered MSB-to-LSB, followed by 0, 2 or 4 don't-care bits (LTC2600, LTC2610 and LTC2620 respectively). Data can only be transferred to the device when the $\overline{CS}$/LD signal is low.The rising edge of $\overline{CS}$/LD ends the data transfer and causes the device to carry out the action specified in the 24-bit input word. The complete sequence is shown in Figure 2a.

The command (C3-C0) and address (A3-A0) assignments are shown in Table 1. The first four commands in the table consist of write and update operations. A write operation loads a 16-bit data word from the 32-bit shift register into the input register of the selected DAC, n. An update operation copies the data word from the input register to the DAC register. Once copied into the DAC register, the data word becomes the active 16-, 14- or 12-bit input code, and is converted to an analog voltage at the DAC output. The update operation also powers up the selected DAC if it had been in power-down mode. The data path and registers are shown in the Block Diagram.

While the minimum input word is 24 bits, it may optionally be extended to 32 bits. To use the 32-bit word width, 8 don't-care bits are transferred to the device first, followed by the 24-bit word as just described. Figure 2b shows the

Table 1.

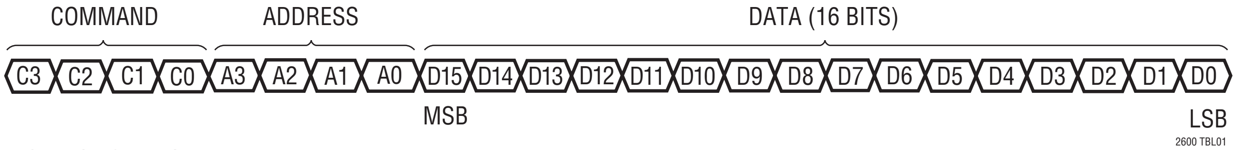
COMMAND*				
C3	C2	C1	C0	
0	0	0	0	Write to Input Register n
0	0	0	1	Update (Power Up) DAC Register n
0	0	1	0	Write to Input Register n, Update (Power Up) All n
0	0	1	1	Write to and Update (Power Up) n
0	1	0	0	Power Down n
1	1	1	1	No Operation

ADDRESS (n)*				
A3	A2	A1	A0	
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	DAC C
0	0	1	1	DAC D
0	1	0	0	DAC E
0	1	0	1	DAC F
0	1	1	0	DAC G
0	1	1	1	DAC H
1	1	1	1	All DACs

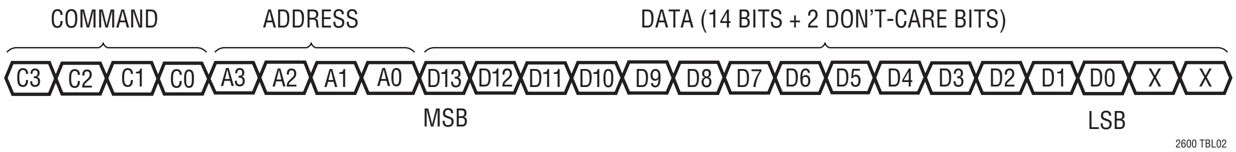
*Command and address codes not shown are reserved and should not be used.

OPERATION

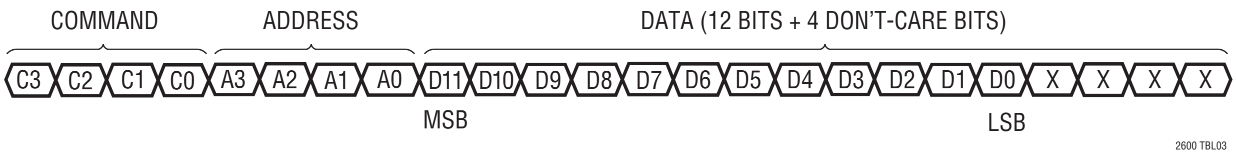
INPUT WORD (LTC2600)



INPUT WORD (LTC2610)



INPUT WORD (LTC2620)



32-bit sequence. The 32-bit word is required for daisychain operation, and is also available to accommodate microprocessors which have a minimum word width of 16 bits (2 bytes).

Daisychain Operation

The serial output of the shift register appears at the SDO pin. Data transferred to the device from the SDI input is delayed 32 SCK rising edges before being output at the next SCK falling edge.

The SDO output can be used to facilitate control of multiple serial devices from a single 3-wire serial port (i.e., SCK, SDI and $\overline{CS}$/LD). Such a "daisychain" series is configured by connecting SDO of each upstream device to SDI of the next device in the chain. The shift registers of the devices are thus connected in series, effectively forming a single input shift register which extends through the entire chain. Because of this, the devices can be addressed and controlled individually by simply concatenating their input words; the first instruction addresses the last device in the chain and so forth. The SCK and $\overline{CS}$/LD signals are common to all devices in the series.

In use, $\overline{CS}$/LD is first taken low. Then the concatenated input data is transferred to the chain, using SDI of the first device as the data input. When the data transfer is complete, $\overline{CS}$/LD is taken high, completing the instruction sequence for all devices simultaneously. A single device can be controlled by using the no-operation command (1111) for the other devices in the chain.

OPERATION

Power-Down Mode

For power-constrained applications, power-down mode can be used to reduce the supply current whenever less than eight outputs are needed. When in power-down, the buffer amplifiers and reference inputs are disabled, and draw essentially zero current. The DAC outputs are put into a high impedance state, and the output pins are passively pulled to ground through individual 90k resistors. When all eight DACs are powered down, the master bias generation circuit is also disabled. Input- and DAC-register contents are not disturbed during power-down.

Any channel or combination of channels can be put into power-down mode by using command 0100b in combination with the appropriate DAC address, (n). The 16-bit data word is ignored. The supply and reference currents are reduced by approximately 1/8 for each DAC powered down; the effective resistance at REF (Pin 6) rises accordingly, becoming a high impedance input (typically > 1GΩ) when all eight DACs are powered down.

Normal operation can be resumed by executing any command which includes a DAC update, as shown in Table 1. The selected DAC is powered up as its voltage output is updated.

There is an initial delay as the DAC powers up before it begins its usual settling behavior. If less than eight DACs are in a powered-down state prior to the update command, the power-up delay is 5μs. If, on the other hand, all eight DACs are powered down, then the master bias generation circuit is also disabled and must be restarted. In this case, the power-up delay is greater: 12μs for V_{CC} = 5V, 30μs for V_{CC} = 3V.

Voltage Outputs

Each of the 8 rail-to-rail amplifiers contained in these parts has guaranteed load regulation when sourcing or sinking up to 15mA at 5V (7.5mA at 3V).

Load regulation is a measure of the amplifier's ability to maintain the rated voltage accuracy over a wide range of load conditions. The measured change in output voltage per milliampere of forced load current change is expressed in LSB/mA.

DC output impedance is equivalent to load regulation, and may be derived from it by simply calculating a change in units from LSB/mA to Ohms. The amplifiers' DC output impedance is 0.025Ω when driving a load well away from the rails.

When drawing a load current from either rail, the output voltage headroom with respect to that rail is limited by the 25Ω typical channel resistance of the output devices; e.g., when sinking 1mA, the minimum output voltage = 25Ω • 1mA = 25mV. See the graph Headroom at Rails vs Output Current in the Typical Performance Characteristics section.

The amplifiers are stable driving capacitive loads of up to 1000pF.

Board Layout

The excellent load regulation and DC crosstalk performance of these devices is achieved in part by keeping "signal" and "power" grounds separated internally and by reducing shared internal resistance to just 0.005Ω.

OPERATION

The GND pin functions both as the node to which the reference and output voltages are referred and as a return path for power currents in the device. Because of this, careful thought should be given to the grounding scheme and board layout in order to ensure rated performance.

The PC board should have separate areas for the analog and digital sections of the circuit. This keeps digital signals away from sensitive analog signals and facilitates the use of separate digital and analog ground planes which have minimal capacitive and resistive interaction with each other.

Digital and analog ground planes should be joined at only one point, establishing a system star ground as close to the device's ground pin as possible. Ideally, the analog ground plane should be located on the component side of the board, and should be allowed to run under the part to shield it from noise. Analog ground should be a continuous and uninterrupted plane, except for necessary lead pads and vias, with signal traces on another layer.

The GND pin of the part should be connected to analog ground. Resistance from the GND pin to system star ground should be as low as possible. Resistance here will add directly to the effective DC output impedance of the device (typically 0.025Ω), and will degrade DC crosstalk. Note that the LTC2600/LTC2610/LTC2620 are no more susceptible to these effects than other parts of their type; on the contrary, they allow layout-based performance improvements to shine rather than limiting attainable performance with excessive internal resistance.

Rail-to-Rail Output Considerations

In any rail-to-rail voltage output device, the output is limited to voltages within the supply range.

Since the analog outputs of the device cannot go below ground, they may limit for the lowest codes as shown in Figure 3b. Similarly, limiting can occur near full scale when the REF pin is tied to V_{CC}. If $V_{REF} = V_{CC}$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC} as shown in Figure 3c. No full-scale limiting can occur if V_{REF} is less than V_{CC} – FSE.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

OPERATION

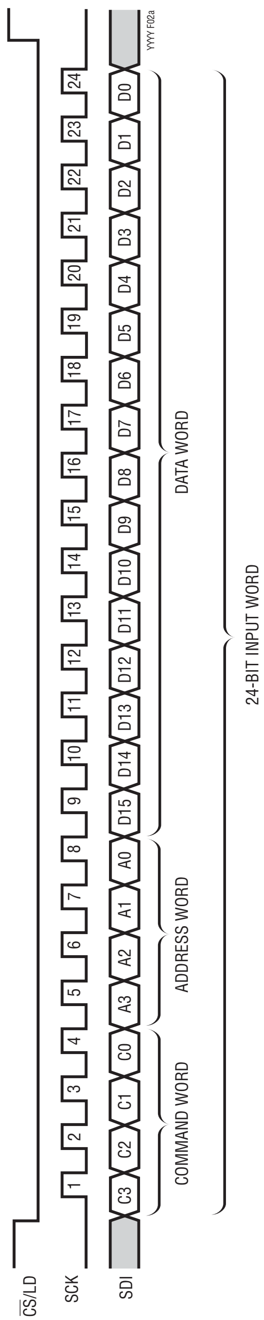


Figure 2a. LTC2600 24-Bit Load Sequence (Minimum Input Word). LTC2610 SDI Data Word: 14-Bit Input Code + 2 Don't-Care Bits; LTC2620 SDI Data Word: 12-Bit Input Code + 4 Don't-Care Bits

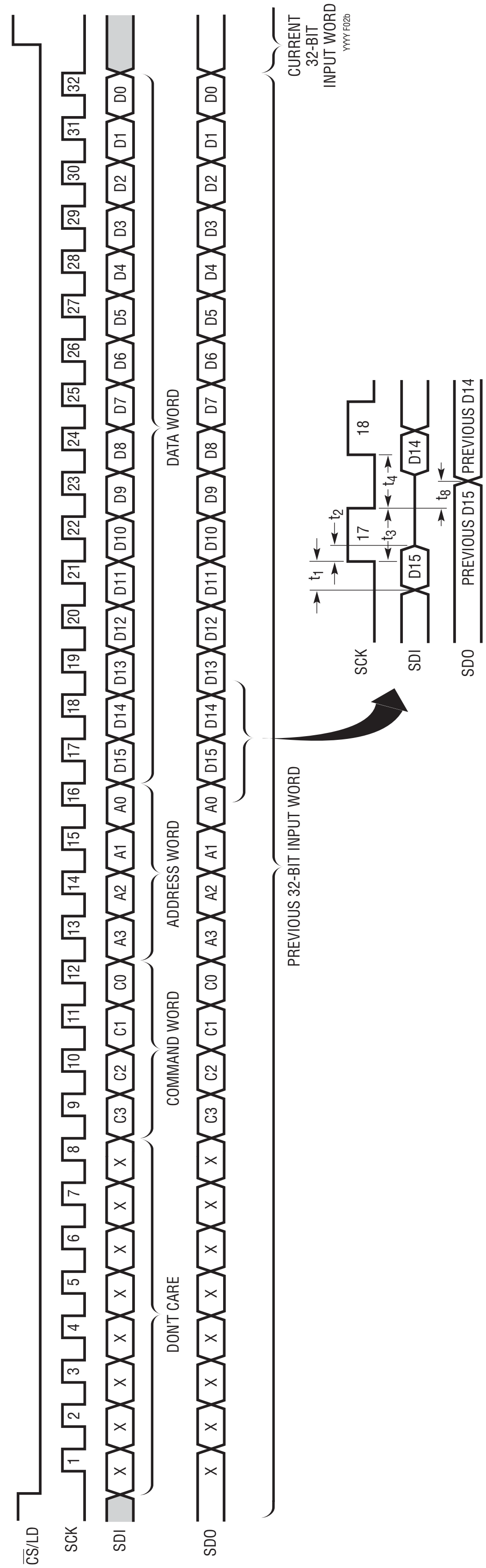


Figure 2b. LTC2600 32-Bit Load Sequence (Required for Daisy-Chain Operation). LTC2610 SDI/SDO Data Word: 14-Bit Input Code + 2 Don't-Care Bits; LTC2620 SDI/SDO Data Word: 12-Bit Input Code + 4 Don't-Care Bits

OPERATION

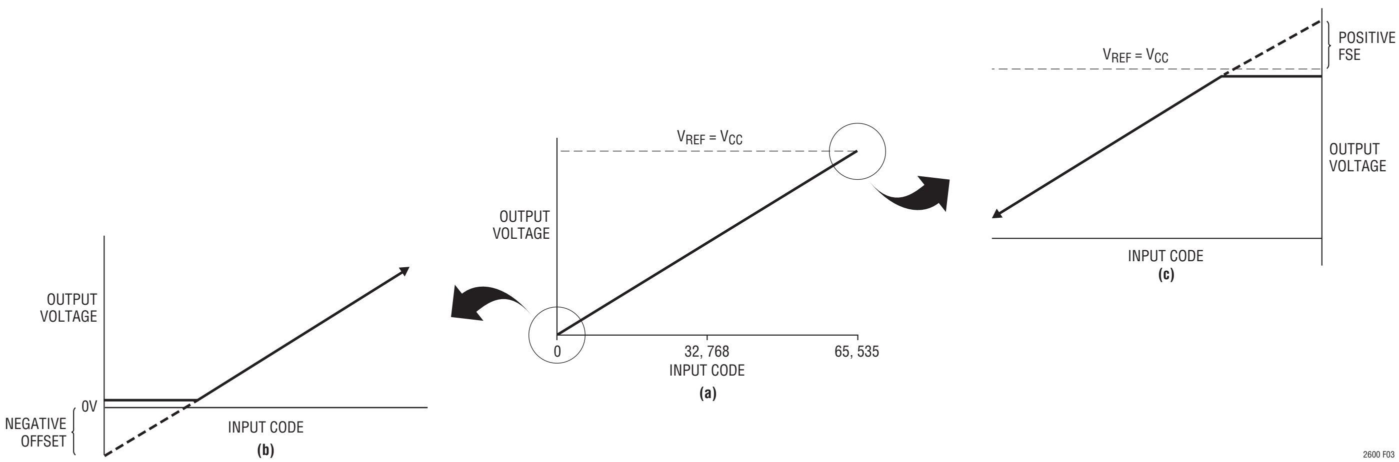
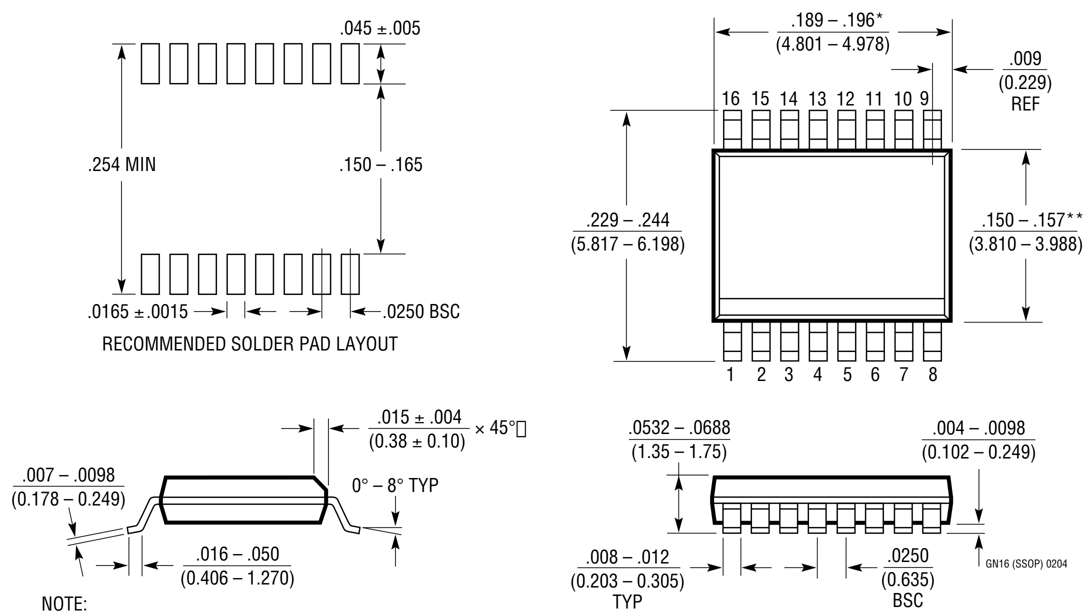


Figure 3. Effects of Rail-to-Rail Operation On a DAC Transfer Curve. (a) Overall Transfer Function (b) Effect of Negative Offset for Codes Near Zero-Scale (c) Effect of Positive Full-Scale Error for Codes Near Full Scale

PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



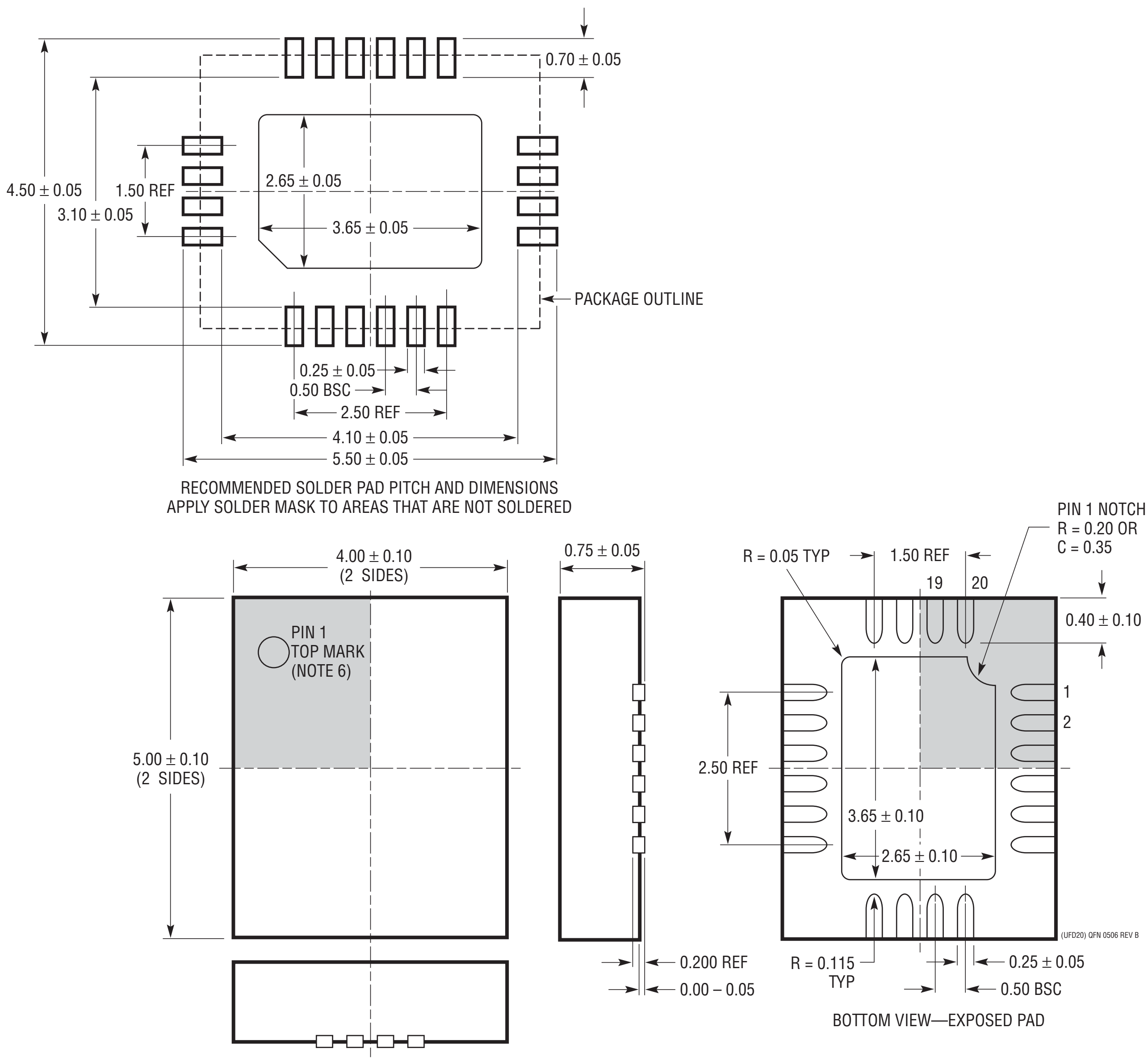
NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

UFD Package
20-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1711 Rev B)



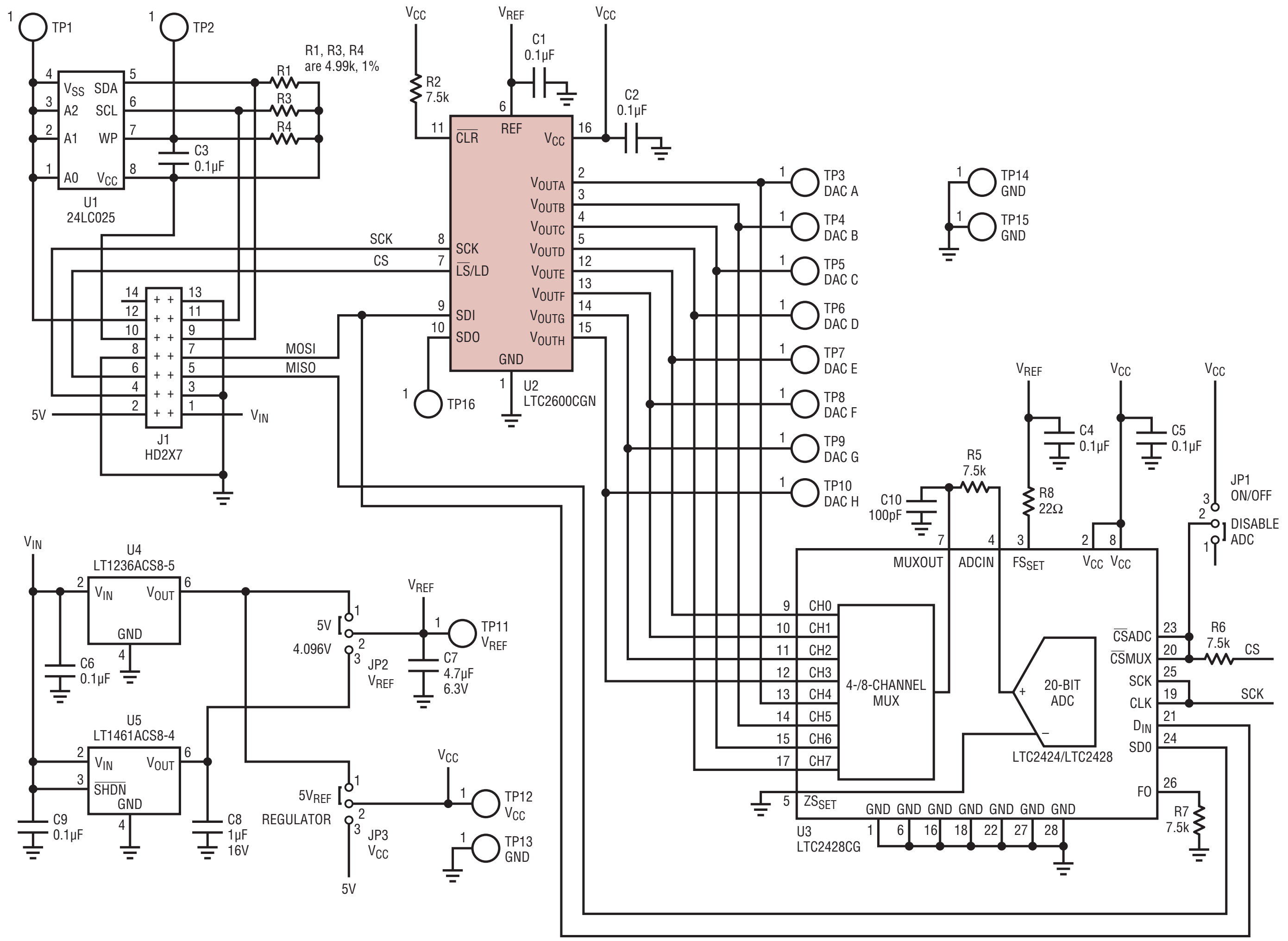
NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev D)

REV	DATE	DESCRIPTION	PAGE NUMBER
D	03/10	Revise GN Part Markings in Order Information	2
E	05/10	Changed “No Connect” pins to “Do Not Connect” in Pin Configuration and Pin Functions sections	2, 10

TYPICAL APPLICATION

Schematic for LTC2600 Demonstration Circuit DC579. The Outputs Are Measured by an Onboard LTC2428



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1458/LTC1458L	Quad 12-Bit Rail-to-Rail Output DACs with Added Functionality	LTC1458: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.096V LTC1458L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1654	Dual 14-Bit Rail-to-Rail V_{OUT} DAC	Programmable Speed/Power, 3.5µs/750µA, 8µs/450µA
LTC1655/LTC1655L	Single 16-Bit V_{OUT} DAC with Serial Interface in SO-8	V_{CC} = 5V(3V), Low Power, Deglitched
LTC1657/LTC1657L	Parrallel 5V/3V 16-Bit V_{OUT} DAC	Low Power, Deglitched, Rail-to-Rail V_{OUT}
LTC1660/LTC1665	Octal 10/8-Bit V_{OUT} DAC in 16-Pin Narrow SSOP	V_{CC} = 2.7V to 5.5V, Micropower, Rail-to-Rail Output
LTC1821	Parallel 16-Bit Voltage Output DAC	Precision 16-Bit Settling in 2µs for 10V Step

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