Dual 16-/14-/12-Bit Rail-to-Rail DACs in 8-Lead MSOP

FEATURES

- **Smallest Pin-Compatible Dual DACs:**
  - **LTC2602: 16-Bits**
  - **LTC2612: 14-Bits**
  - **LTC2622: 12-Bits**
- **Guaranteed 16-Bit Monotonic Over Temperature**
- Wide 2.5V to 5.5V Supply Range
- Low Power Operation: 300μA per DAC at 3V
- Individual Channel Power-Down to 1μA, Max
- Ultralow Crosstalk between DACs (30μV)
- High Rail-to-Rail Output Drive (±15mA)
- Double-Buffered Data Latches
- Pin-Compatible 10-Bit Version (LTC1661)
- Tiny 8-Lead MSOP Package

APPLICATIONS

- Mobile Communications
- Process Control and Industrial Automation
- Instrumentation
- Automatic Test Equipment

DESCRIPTION

The LTC®2602/LTC2612/LTC2622 are dual 16-,14- and 12-bit, 2.5V-to-5.5V rail-to-rail voltage-output DACs, in a tiny 8-lead MSOP package. They have built-in high performance output buffers and are guaranteed monotonic.

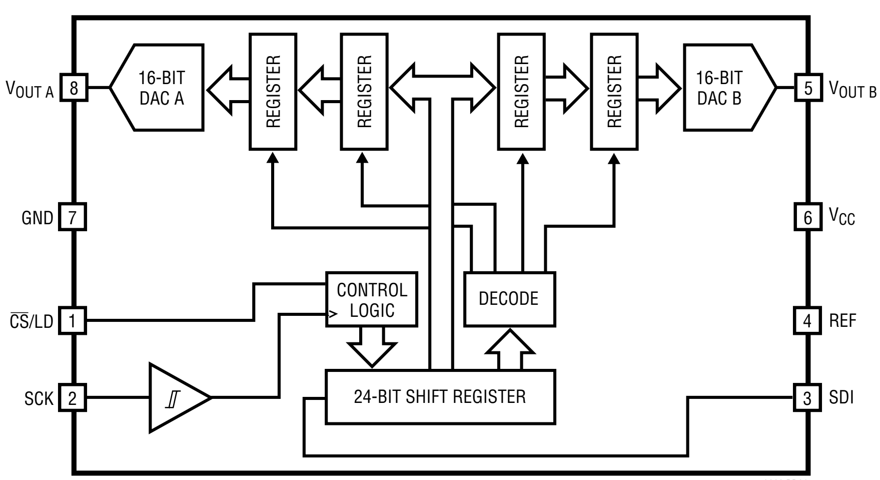
These parts establish advanced performance standards for output drive, crosstalk and load regulation in single-supply, voltage output multiples.

The parts use a simple SPI/MICROWIRE™ compatible 3-wire serial interface which can be operated at clock rates up to 50MHz.

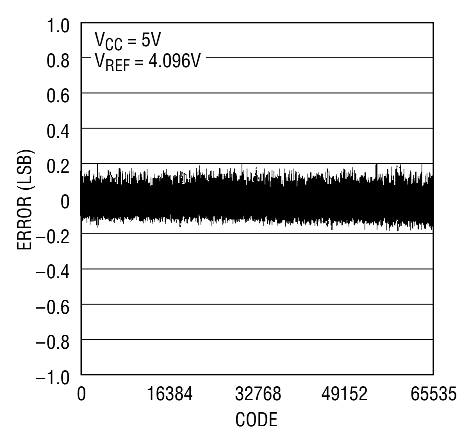
The LTC2602/LTC2612/LTC2622 incorporate a power-on reset circuit. During power-up, the voltage outputs rise less than 10mV above zero scale, and after power-up, they stay at zero scale until a valid write and update take place.

BLOCK DIAGRAM

LTC2602



Differential Nonlinearity (DNL)(LTC2602)



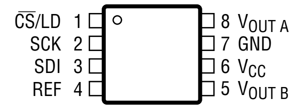
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Any Pin to GND .... –0.3V to 6V
Any Pin to V_{CC} .... –6V to 0.3V
Maximum Junction Temperature .... 125°C
Operating Temperature Range
  LTC2602C/LTC2612C/LTC2622C .... 0°C to 70°C
  LTC2602I/LTC2612I/LTC2622I .... –40°C to 85°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 300°C/W

ORDER PART NUMBER	MS8 PART MARKING
LTC2602CMS8	LTACX
LTC2602IMS8	LTACY
LTC2612CMS8	LTACZ
LTC2612IMS8	LTADA
LTC2622CMS8	LTADB
LTC2622IMS8	LTADC

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.5V to 5.5V, $V_{REF} \le V_{CC}$, V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC2622 MIN	LTC2622 TYP	LTC2622 MAX	LTC2612 MIN	LTC2612 TYP	LTC2612 MAX	LTC2602 MIN	LTC2602 TYP	LTC2602 MAX	UNITS
DC Performance													
	Resolution		●	12			14			16			Bits
	Monotonicity	V_{CC} = 5V, V_{REF} = 4.096V (Note 2)	●	12			14			16			Bits
DNL	Differential Nonlinearity	V_{CC} = 5V, V_{REF} = 4.096V (Note 2)	●			±0.5			±1			±1	LSB
INL	Integral Nonlinearity	V_{CC} = 5V, V_{REF} = 4.096V (Note 2)	●		±0.75	±4		±3	±16		±12	±64	LSB
	Load Regulation	V_{REF} = V_{CC} = 5V, Midscale											
		I_{OUT} = 0mA to 15mA Sourcing	●		0.025	0.125		0.1	0.5		0.4	2	LSB/mA
		I_{OUT} = 0mA to 15mA Sinking	●		0.05	0.125		0.2	0.5		0.65	2	LSB/mA
		V_{REF} = V_{CC} = 2.5V, Midscale											
		I_{OUT} = 0mA to 7.5mA Sourcing	●		0.05	0.25		0.2	1		0.9	4	LSB/mA
		I_{OUT} = 0mA to 7.5mA Sinking	●		0.1	0.25		0.4	1		1.3	4	LSB/mA
ZSE	Zero-Scale Error	V_{CC} = 5V, V_{REF} = 4.096V Code = 0	●		1	9		1	9		1	9	mV
V_{OS}	Offset Error	V_{CC} = 5V, V_{REF} = 4.096V (Note 7)	●		±1	±9		±1	±9		±1	±9	mV
	V_{OS} Temperature Coefficient				±5			±5			±5		µV/°C
GE	Gain Error	V_{CC} = 5V, V_{REF} = 4.096V	●		±0.1	±0.7		±0.1	±0.7		±0.1	±0.7	%FSR
	Gain Temperature Coefficient				±3			±3			±3		ppm/°C

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.5V to 5.5V, $V_{REF} \le V_{CC}$, V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC2602/LTC2612/LTC2622 MIN	TYP	MAX	UNITS
PSRR	Power Supply Rejection Ratio	V_{CC} = 5V ±10%			–80		dB
R_{OUT}	DC Output Impedance	V_{REF} = V_{CC} = 5V, Midscale; –15mA ≤ I_{OUT} ≤ 15mA V_{REF} = V_{CC} = 2.5V, Midscale; –7.5mA ≤ I_{OUT} ≤ 7.5mA	● ●		0.05 0.05	0.15 0.15	Ω Ω
	DC Crosstalk (Note 4)	Due to Full Scale Output Change (Note 5) Due to Load Current Change Due to Powering Down (per Channel)			±30 ±16 ±4		µV µV/mA µV
I_{SC}	Short-Circuit Output Current	V_{CC} = 5.5V, V_{REF} = 5.5V Code: Zero Scale; Forcing Output to V_{CC} Code: Full Scale; Forcing Output to GND	 ● ●	 15 15	 34 38	 60 60	 mA mA
		V_{CC} = 2.5V, V_{REF} = 2.5V Code: Zero Scale; Forcing Output to V_{CC} Code: Full Scale; Forcing Output to GND	 ● ●	 7.5 7.5	 20 28	 50 50	 mA mA
Reference Input							
	Input Voltage Range		●	0		V_{CC}	V
	Resistance	Normal Mode	●	44	64	80	kΩ
	Capacitance				23		pF
I_{REF}	Reference Current, Power Down Mode	All DACs Powered Down	●		0.001	1	µA
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	2.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5V (Note 3) V_{CC} = 3V (Note 3) All DACs Powered Down (Note 3) V_{CC} = 5V All DACs Powered Down (Note 3) V_{CC} = 3V	● ● ● ●		0.7 0.6 0.35 0.10	1.3 1 1 1	mA mA µA µA
Digital I/O							
V_{IH}	Digital Input High Voltage	V_{CC} = 2.5V to 5.5V V_{CC} = 2.5V to 3.6V	● ●	2.4 2.0			V V
V_{IL}	Digital Input Low Voltage	V_{CC} = 4.5V to 5.5V V_{CC} = 2.7V to 5.5V V_{CC} = 2.5V to 5.5V	● ● ●			0.8 0.6 0.5	V V V
I_{LK}	Digital Input Leakage	V_{IN} = GND to V_{CC}	●			±1	µA
C_{IN}	Digital Input Capacitance	(Note 6)	●			8	pF

SYMBOL	PARAMETER	CONDITIONS	LTC2622 MIN	TYP	MAX	LTC2612 MIN	TYP	MAX	LTC2602 MIN	TYP	MAX	UNITS
AC Performance												
t_S	Settling Time (Note 8)	±0.024% (±1LSB at 12 Bits) ±0.006% (±1LSB at 14 Bits) ±0.0015% (±1LSB at 16 Bits)		7			7 9			7 9 10		µs µs µs
	Settling Time for 1LSB Step (Note 9)	±0.024% (±1LSB at 12 Bits) ±0.006% (±1LSB at 14 Bits) ±0.0015% (±1LSB at 16 Bits)		2.7			2.7 4.8			2.7 4.8 5.2		µs µs µs
	Voltage Output Slew Rate			0.80			0.80			0.80		V/µs
	Capacitive Load Driving			1000			1000			1000		pF
	Glitch Impulse	At Midscale Transition		12			12			12		nV • s
	Multiplying Bandwidth			180			180			180		kHz
e_n	Output Voltage Noise Density	At f = 1kHz At f = 10kHz		120 100			120 100			120 100		nV/√Hz nV/√Hz
	Output Voltage Noise	0.1Hz to 10Hz		15			15			15		μV_{P-P}

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (See Figure 1) (Note 6)

SYMBOL	PARAMETER	CONDITIONS		LTC2602/LTC2612/LTC2622 MIN	TYP	MAX	UNITS
V_{CC} = 2.5V to 5.5V							
t_1	SDI Valid to SCK Setup		●	4			ns
t_2	SDI Valid to SCK Hold		●	4			ns
t_3	SCK High Time		●	9			ns
t_4	SCK Low Time		●	9			ns
t_5	$\overline{CS}$/LD Pulse Width		●	10			ns
t_6	LSB SCK High to $\overline{CS}$/LD High		●	7			ns
t_7	$\overline{CS}$/LD Low to SCK High		●	7			ns
t_{10}	$\overline{CS}$/LD High to SCK Positive Edge		●	7			ns
	SCK Frequency	50% Duty Cycle	●			50	MHz

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: Linearity and monotonicity are defined from code k_L to code $2^N - 1$, where N is the resolution and k_L is given by $k_L = 0.016(2^N/V_{REF})$, rounded to the nearest whole code. For V_{REF} = 4.096V and N = 16, k_L = 256 and linearity is defined from code 256 to code 65,535.

Note 3: Digital inputs at 0V or V_{CC}.

Note 4: DC crosstalk is measured with V_{CC} = 5V and V_{REF} = 4.096V, with the measured DAC at midscale, unless otherwise noted.

Note 5: R_L = 2kΩ to GND or V_{CC} at the output of the DAC not being tested.

Note 6: Guaranteed by design and not production tested.

Note 7: Inferred from measurement at code 256 (LTC2602), code 64 (LTC2612) or code 16 (LTC2622), and at fullscale.

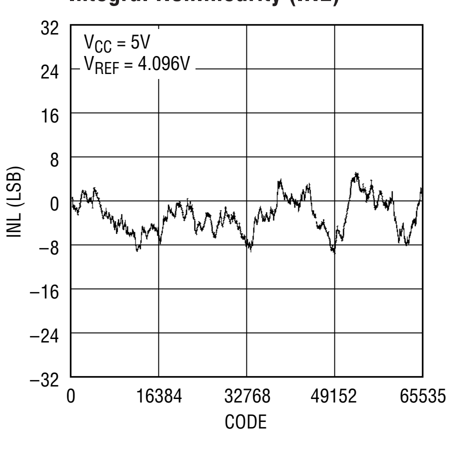
Note 8: V_{CC} = 5V, V_{REF} = 4.096V. DAC is stepped 1/4 scale to 3/4 scale and 3/4 scate to 1/4 scale. Load is 2k in parallel with 200pF to GND.

Note 9: V_{CC} = 5V, V_{REF} = 4.096V. DAC is stepped ±LBS between half scale and half scale –1. Load is 2k in parallel with 200pF to GND.

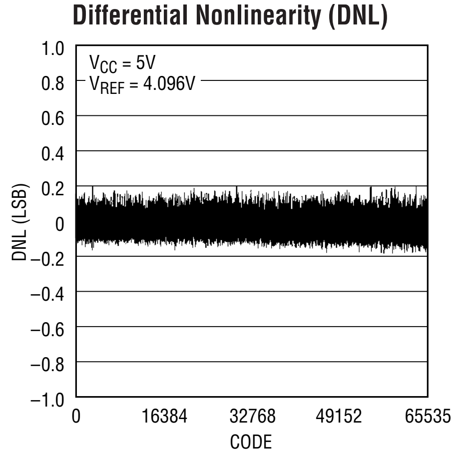
TYPICAL PERFORMANCE CHARACTERISTICS

(LTC2602)

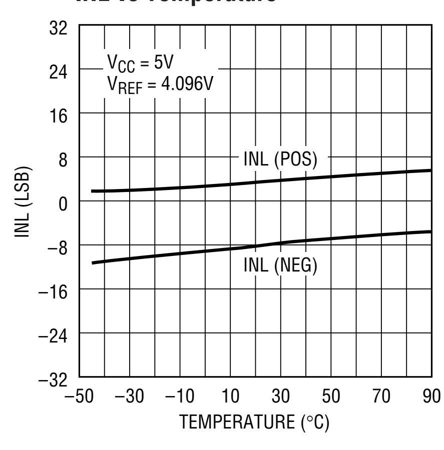
Integral Nonlinearity (INL)



Differential Nonlinearity (DNL)



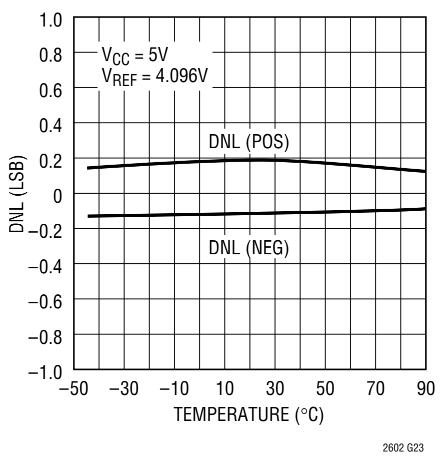
INL vs Temperature



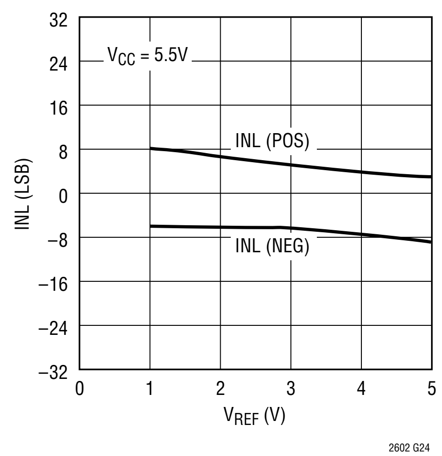
TYPICAL PERFORMANCE CHARACTERISTICS

(LTC2602)

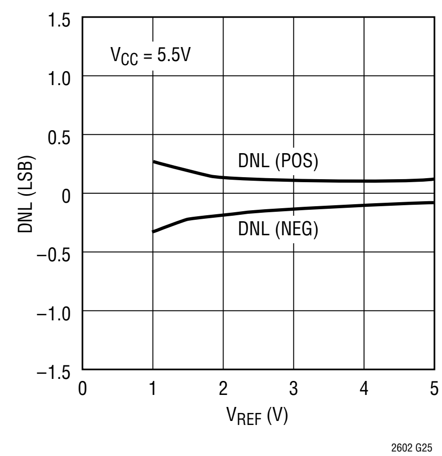
DNL vs Temperature



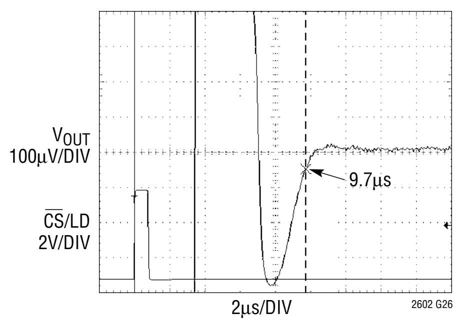
INL vs V_{REF}



DNL vs V_{REF}

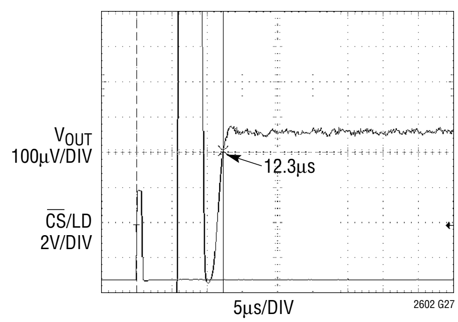


Settling to ±1LSB



V_{CC} = 5V, V_{REF} = 4.096V
1/4-SCALE TO 3/4-SCALE STEP
R_L = 2k, C_L = 200pF
AVERAGE OF 2048 EVENTS

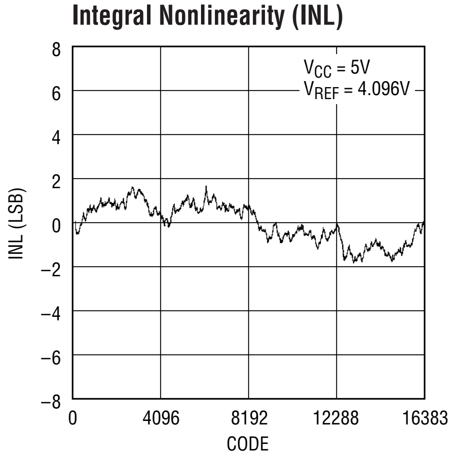
Settling of Full-Scale Step



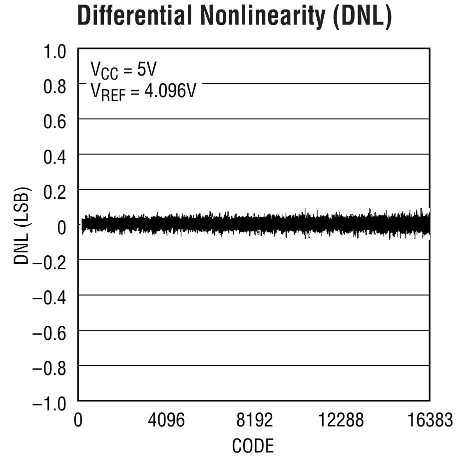
V_{CC} = 5V, V_{REF} = 4.096V
CODE 512 TO 65535 STEP
AVERAGE OF 2048 EVENTS
SETTLING TO ±1LSB

(LTC2612)

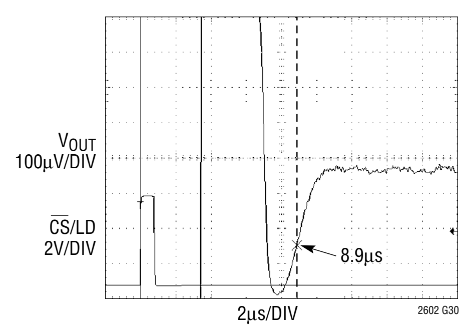
Integral Nonlinearity (INL)



Differential Nonlinearity (DNL)



Settling to ±1LSB

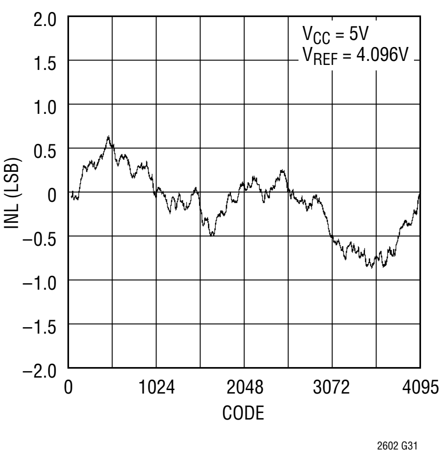


V_{CC} = 5V, V_{REF} = 4.096V
1/4-SCALE TO 3/4-SCALE STEP
R_L = 2k, C_L = 200pF
AVERAGE OF 2048 EVENTS

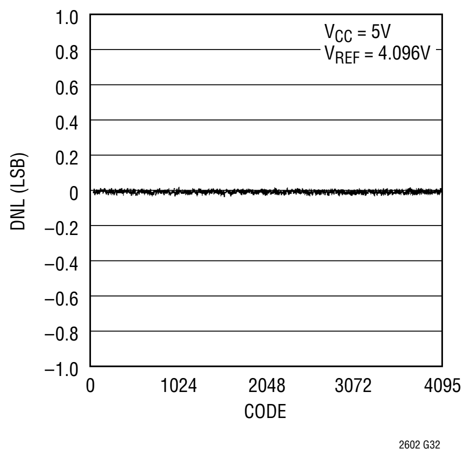
TYPICAL PERFORMANCE CHARACTERISTICS

(LTC2622)

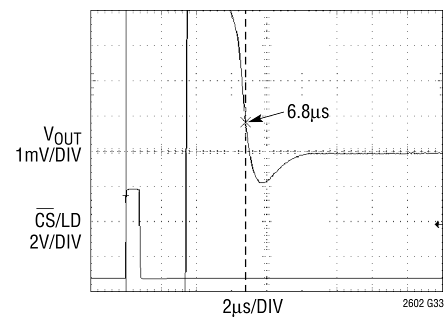
Integral Nonlinearity (INL)



Differential Nonlinearity (DNL)



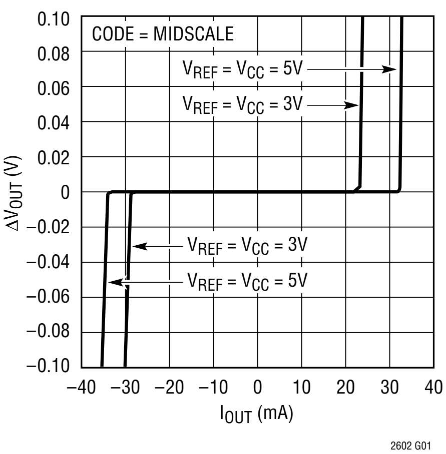
Settling to ±1LSB



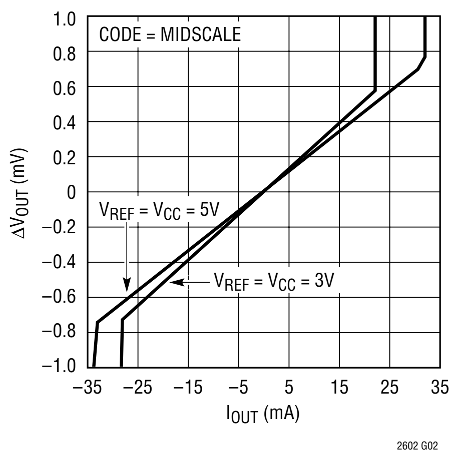
V_{CC} = 5V, V_{REF} = 4.096V
1/4-SCALE TO 3/4-SCALE STEP
R_L = 2k, C_L = 200pF
AVERAGE OF 2048 EVENTS

(LTC2602/LTC2612/LTC2622)

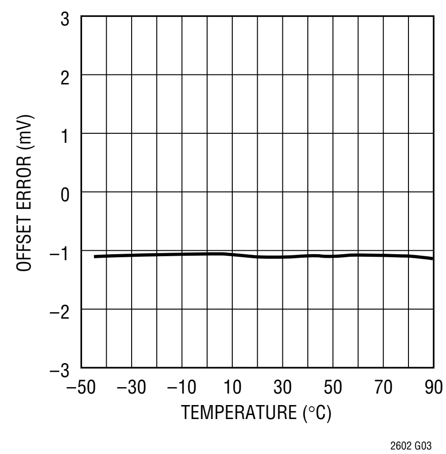
Current Limiting



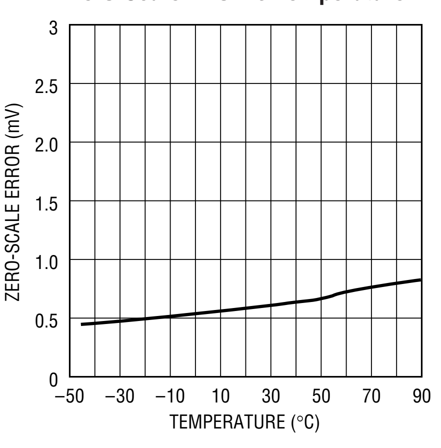
Load Regulation



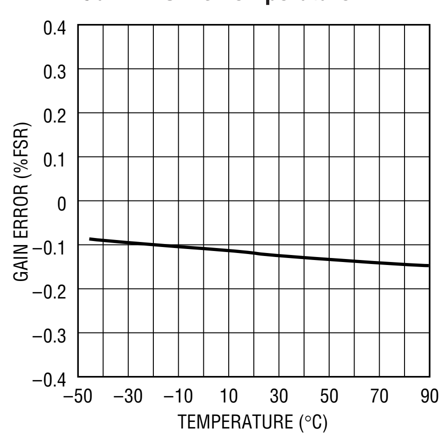
Offset Error vs Temperature



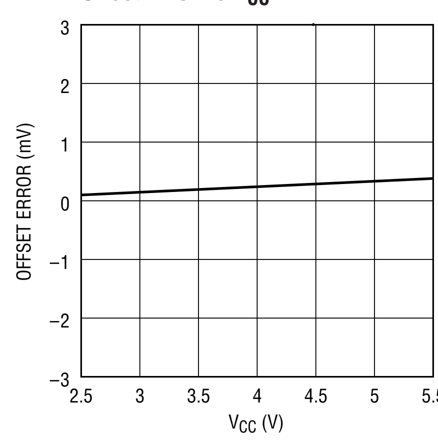
Zero-Scale Error vs Temperature



Gain Error vs Temperature



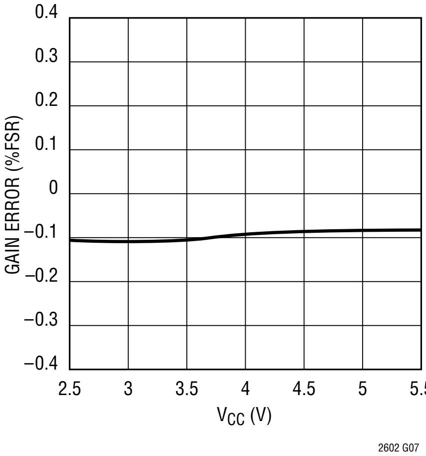
Offset Error vs V_{CC}



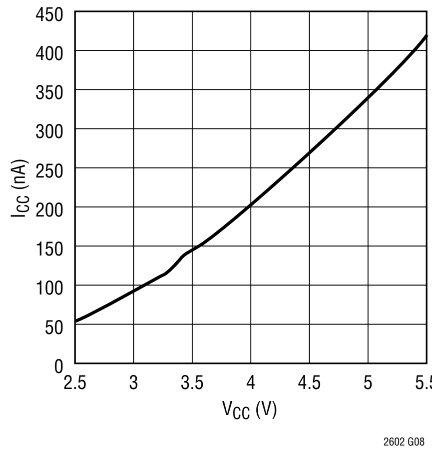
TYPICAL PERFORMANCE CHARACTERISTICS

(LTC2602/LTC2612/LTC2622)

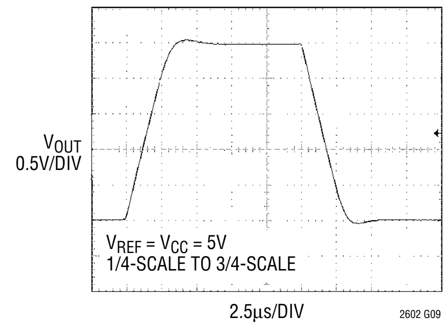
Gain Error vs V_{CC}



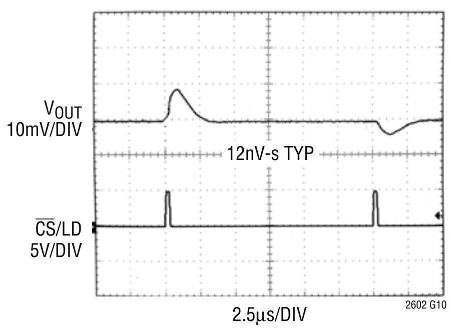
I_{CC} Shutdown vs V_{CC}



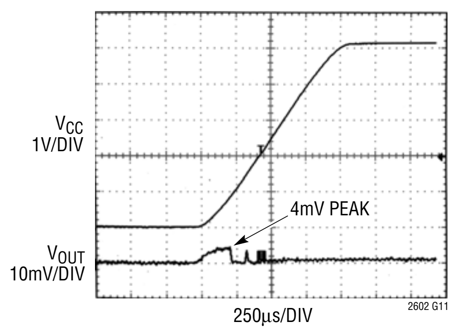
Large-Signal Settling



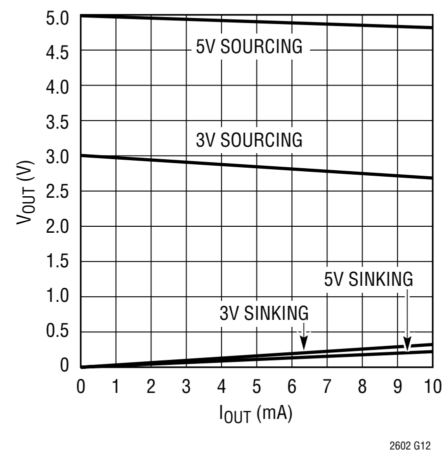
Midscale Glitch Impulse



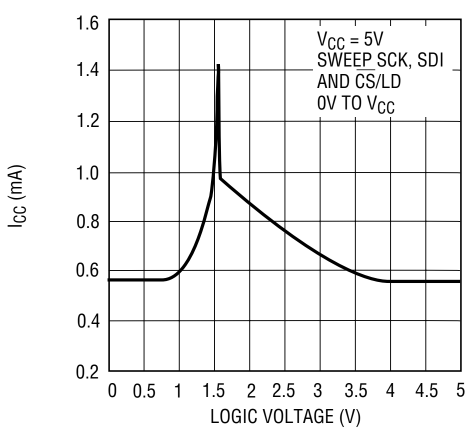
Power-On Reset Glitch



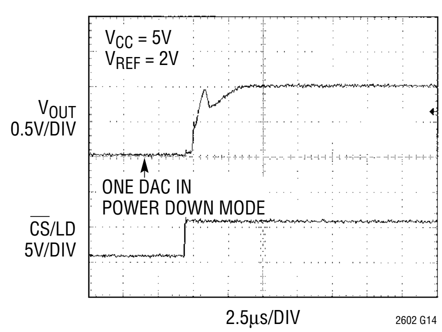
Headroom at Rails vs Output Current



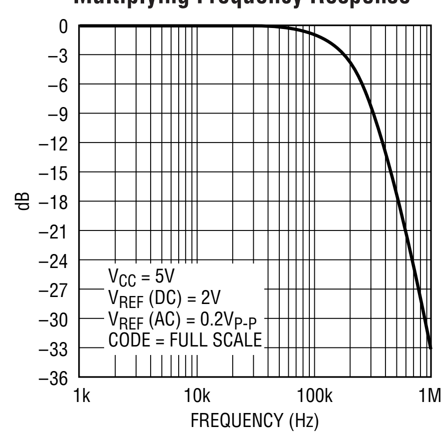
Supply Current vs Logic Voltage



Exiting Power-Down to Midscale



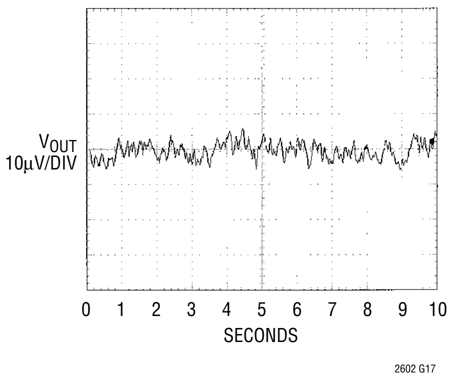
Multiplying Frequency Response



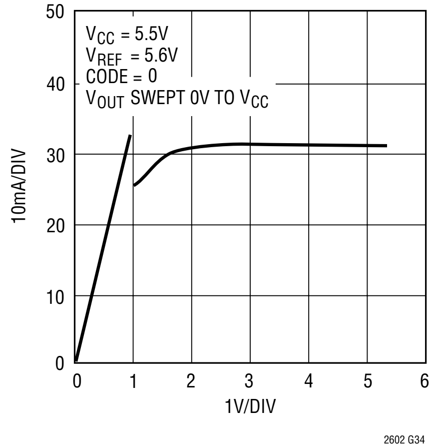
TYPICAL PERFORMANCE CHARACTERISTICS

(LTC2602/LTC2612/LTC2622)

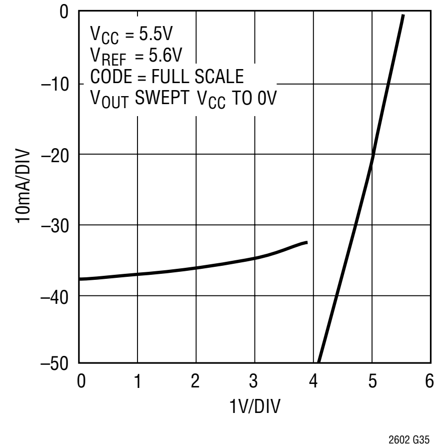
Output Voltage Noise, 0.1Hz to 10Hz



Short-Circuit Output Current vs V_{OUT} (Sinking)



Short-Circuit Output Current vs V_{OUT} (Sourcing)



PIN FUNCTIONS

$\overline{CS}$/LD (Pin 1): Serial Interface Chip Select/Load Input. When $\overline{CS}$/LD is low, SCK is enabled for shifting data on SDI into the register. When $\overline{CS}$/LD is taken high, SCK is disabled and the specified command (see Table 1) is executed.

SCK (Pin 2): Serial Interface Clock Input. CMOS and TTL compatible.

SDI (Pin 3): Serial Interface Data Input. Data is applied to SDI for transfer to the device at the rising edge of SCK. The LTC2602/LTC2612/LTC2622 accept input word lengths of either 24 or 32 bits.

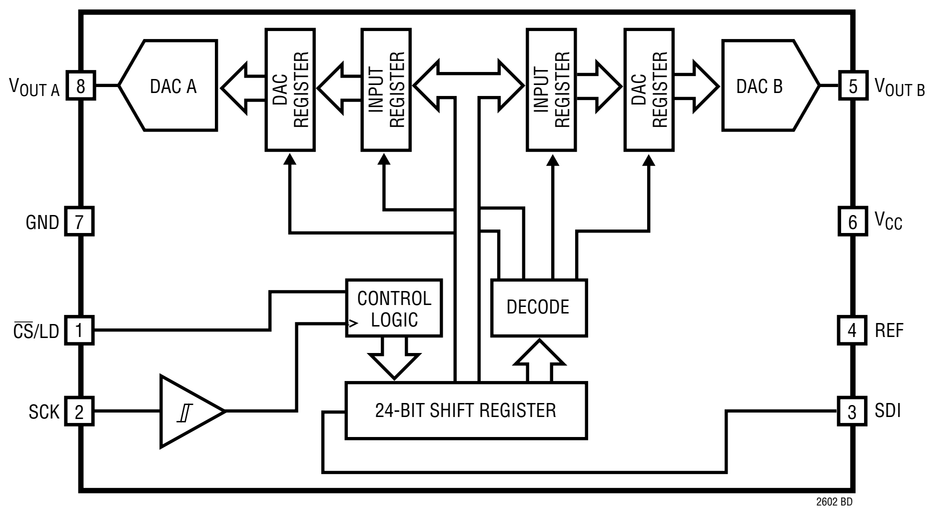
REF (Pin 4): Reference Voltage Input. $0V \leq V_{REF} \leq V_{CC}$.

$V_{OUT\ B}$ and $V_{OUT\ A}$ (Pins 5 and 8): DAC Analog Voltage Outputs. The output range is $0 – V_{REF}$.

V_{CC} (Pin 6): Supply Voltage Input. $2.5V \leq V_{CC} \leq 5.5V$.

GND (Pin 7): Analog Ground.

BLOCK DIAGRAM



TIMING DIAGRAM

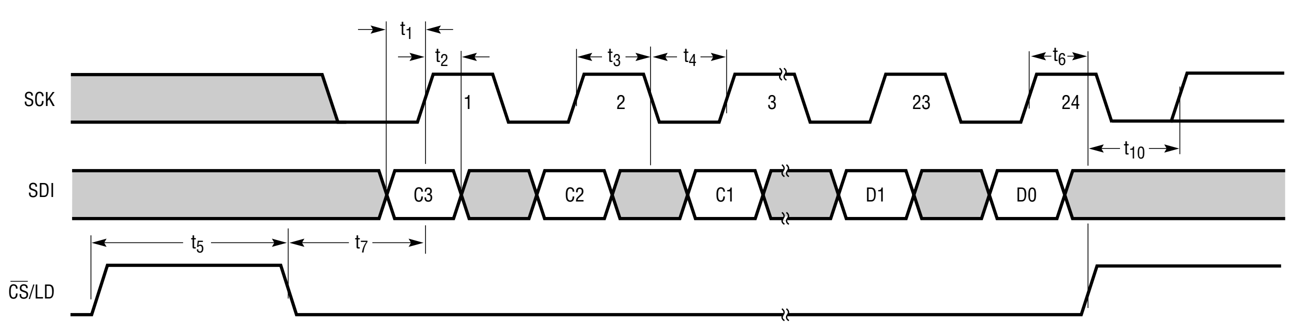


Figure 1

OPERATION

Power-On Reset

The LTC2602/LTC2612/LTC2622 clear the outputs to zero scale when power is first applied, making system initialization consistent and repeatable.

For some applications, downstream circuits are active during DAC power-up, and may be sensitive to nonzero outputs from the DAC during this time. The LTC2602/LTC2612/LTC2622 contain circuitry to reduce the power-on glitch; furthermore, the glitch amplitude can be made smaller by reducing the ramp rate of the power supply. For example, if the power supply is ramped to 5V in 1ms, the analog outputs rise less than 10mV above ground (typ) during power-on. See Power-On Reset Glitch in the Typical Performance Characteristics section.

Power Supply Sequencing

The voltage at REF (Pin 4) should be kept within the range $-0.3V \le V_{REF} \le V_{CC} + 0.3V$ (see Absolute Maximum Ratings). Particular care should be taken to observe these limits during power supply turn-on and turn-off sequences, when the voltage at V_{CC} (Pin 6) is in transition.

Transfer Function

The digital-to-analog transfer function is

$$V_{OUT(IDEAL)} = \left(\frac{k}{2^N}\right)V_{REF}$$

where k is the decimal equivalent of the binary DAC input code, N is the resolution and V_{REF} is the voltage at REF (Pin 4).

Table 1.

COMMAND*				
C3	**C2**	**C1**	**C0**	
0	0	0	0	Write to Input Register n
0	0	0	1	Update (Power Up) DAC Register n
0	0	1	0	Write to Input Register n, Update (Power Up) All n
0	0	1	1	Write to and Update (Power Up) n
0	1	0	0	Power Down n
1	1	1	1	No Operation
ADDRESS (n)*				
A3	**A2**	**A1**	**A0**	
0	0	0	0	DAC A
0	0	0	1	DAC B
1	1	1	1	All DACs

*Command and address codes not shown are reserved and should not be used.

Serial Interface

The $\overline{CS}$/LD input is level triggered. When this input is taken low, it acts as a chip-select signal, activating the SDI and SCK buffers and enabling the input shift register. Data (SDI input) is transferred at the next 24 rising SCK edges. The 4-bit command, C3-C0, is loaded first; then the 4-bit DAC address, A3-A0; and finally the 16-bit data word. The data word comprises the 16-, 14- or 12-bit input code, ordered MSB-to-LSB, followed by 0, 2 or 4 don't-care bits (LTC2602, LTC2612 and LTC2622 respectively). Data can only be transferred to the device when the $\overline{CS}$/LD signal is low.The rising edge of $\overline{CS}$/LD ends the data transfer and causes the device to carry out the action specified in the 24-bit input word. The complete sequence is shown in Figure 2a.

The command (C3-C0) and address (A3-A0) assignments are shown in Table 1. The first four commands in the table consist of write and update operations. A write operation loads a 16-bit data word from the 32-bit shift register into the input register of the selected DAC, n. An update operation copies the data word from the input register to the DAC register. Once copied into the DAC register, the data word becomes the active 16-, 14- or 12-bit input code, and is converted to an analog voltage at the DAC output. The update operation also powers up the selected DAC if it had been in power-down mode. The data path and registers are shown in the block diagram.

While the minimum input word is 24 bits, it may optionally be extended to 32 bits to accommodate microprocessors which have a minimum word width of 16 bits (2 bytes). To use the 32-bit word width, 8 don't-care bits are transferred to the device first, followed by the 24-bit word as just described. Figure 2b shows the 32-bit sequence.

Power-Down Mode

For power-constrained applications, power-down mode can be used to reduce the supply current whenever less than two outputs are needed. When in power-down, the buffer amplifiers, bias circuits and reference inputs are disabled, and draw essentially zero current. The DAC outputs are put into a high-impedance state, and the

OPERATION

INPUT WORD (LTC2602)

COMMAND				ADDRESS				DATA (16 BITS)															
C3	C2	C1	C0	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								MSB															LSB

2602 TBL01

INPUT WORD (LTC2612)

COMMAND				ADDRESS				DATA (14 BITS + 2 DON'T-CARE BITS)															
C3	C2	C1	C0	A3	A2	A1	A0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X
								MSB													LSB		

2602 TBL02

INPUT WORD (LTC2622)

COMMAND				ADDRESS				DATA (12 BITS + 4 DON'T-CARE BITS)															
C3	C2	C1	C0	A3	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X
								MSB											LSB				

2602 TBL03

output pins are passively pulled to ground through individual 90kΩ resistors. Input- and DAC-register contents are not disturbed during power-down.

Either channel or both channels can be put into power-down mode by using command 0100_b in combination with the appropriate DAC address, (n). The 16-bit data word is ignored. The supply and reference currents are reduced by approximately 50% for each DAC powered down; the effective resistance at REF (pin 4) rises accordingly, becoming a high-impedance input (typically > 1GΩ) when both DACs are powered down.

Normal operation can be resumed by executing any command which includes a DAC update, as shown in Table 1. The selected DAC is powered up as its voltage output is updated. When a DAC which is in a powered-down state is powered up and updated, normal settling is delayed. If one of the two DACs is in a powered-down state prior to the update command, the power-up delay is 5µs. If, on the other hand, both DACs are powered down, then the main bias generation circuit block has been automatically shut down in addition to the individual DAC amplifiers and reference inputs. In this case, the power up delay time is 12µs (for V_{CC} = 5V) or 30µs (for V_{CC} = 3V).

Voltage Outputs

Each of the two rail-to-rail amplifiers contained in these parts has guaranteed load regulation when sourcing or sinking up to 15mA at 5V (7.5mA at 3V).

Load regulation is a measure of the amplifier's ability to maintain the rated voltage accuracy over a wide range of load conditions. The measured change in output voltage per milliampere of forced load current change is expressed in LSB/mA.

DC output impedance is equivalent to load regulation, and may be derived from it by simply calculating a change in units from LSB/mA to Ohms. The amplifiers' DC output impedance is 0.050Ω when driving a load well away from the rails.

When drawing a load current from either rail, the output voltage headroom with respect to that rail is limited by the 25Ω typical channel resistance of the output devices; e.g., when sinking 1mA, the minimum output voltage = 25Ω • 1mA = 25mV. See the graph Headroom at Rails vs Output Current in the Typical Performance Characteristics section.

The amplifiers are stable driving capacitive loads of up to 1000pF.

OPERATION

Board Layout

The excellent load regulation and DC crosstalk performance of these devices is achieved in part by keeping "signal" and "power" grounds separated internally and by reducing shared internal resistance.

The GND pin functions both as the node to which the reference and output voltages are referred and as a return path for power currents in the device. Because of this, careful thought should be given to the grounding scheme and board layout in order to ensure rated performance.

The PC board should have separate areas for the analog and digital sections of the circuit. This keeps digital signals away from sensitive analog signals and facilitates the use of separate digital and analog ground planes which have minimal capacitive and resistive interaction with each other.

Digital and analog ground planes should be joined at only one point, establishing a system star ground as close to the device's ground pin as possible. Ideally, the analog ground plane should be located on the component side of the board, and should be allowed to run under the part to shield it from noise. Analog ground should be a continuous and uninterrupted plane, except for necessary lead pads and vias, with signal traces on another layer.

The GND pin of the part should be connected to analog ground. Resistance from the GND pin to system star ground should be as low as possible. Resistance here will add directly to the effective DC output impedance of the device (typically 0.050Ω), and will degrade DC crosstalk. Note that the LTC2602/LTC2612/LTC2622 are no more susceptible to these effects than other parts of their type; on the contrary, they allow layout-based performance improvements to shine rather than limiting attainable performance with excessive internal resistance.

Rail-to-Rail Output Considerations

In any rail-to-rail voltage output device, the output is limited to voltages within the supply range.

Since the analog outputs of the device cannot go below ground, they may limit for the lowest codes as shown in Figure 3b. Similarly, limiting can occur near full scale when the REF pin is tied to V_{CC}. If $V_{REF} = V_{CC}$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC} as shown in Figure 3c. No full-scale limiting can occur if V_{REF} is less than V_{CC} – FSE.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

OPERATION

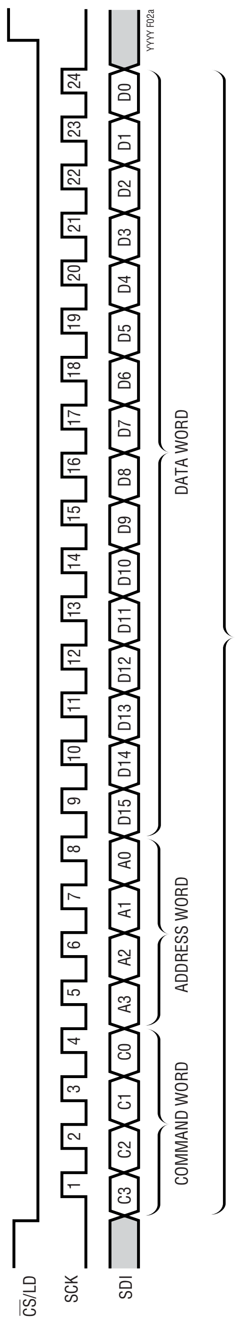


**Figure 2a. LTC2602 24-Bit Load Sequence (Minimum Input Word)
LTC2612 SDI Data Word 14-Bit Input Code + 2 Don't Care Bits
LTC2622 SDI Data Word 12-Bit Input Code + 4 Don't Care Bits**

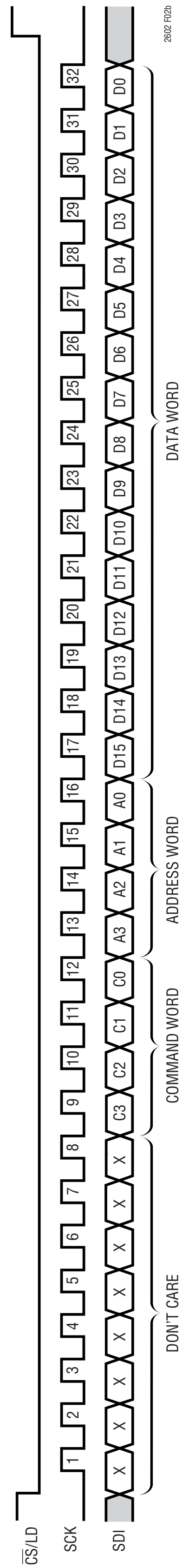


**Figure 2b. LTC2602 32-Bit Load Sequence
LTC2612 SDI Data Word 14-Bit Input Code + 2 Don't Care Bits
LTC2622 SDI Data Word 12-Bit Input Code + 4 Don't Care Bits**

OPERATION

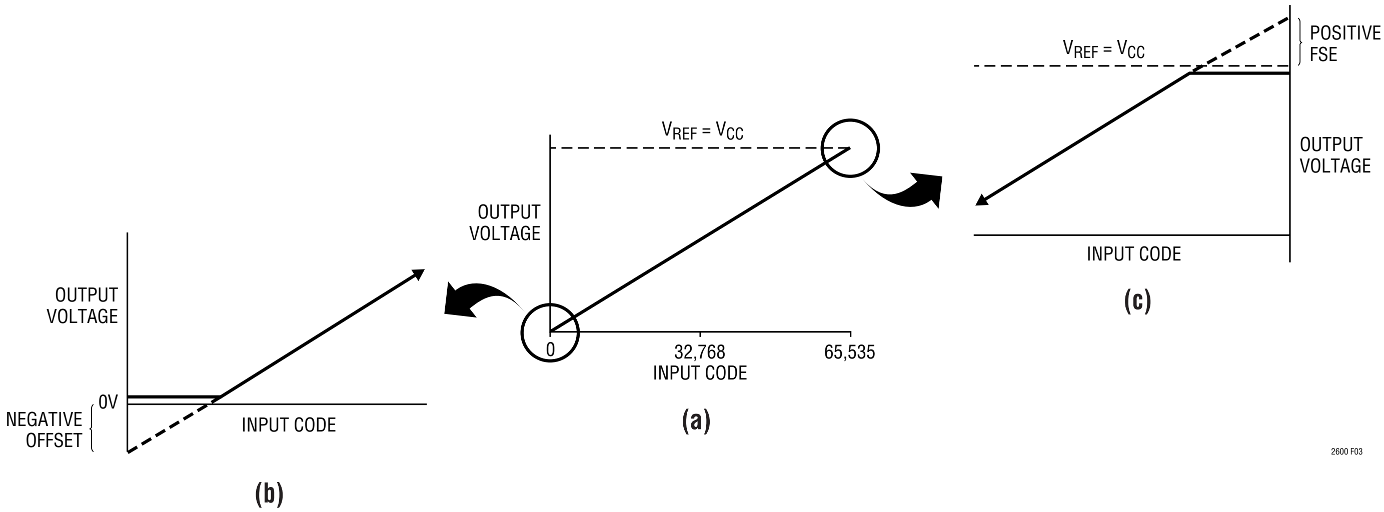
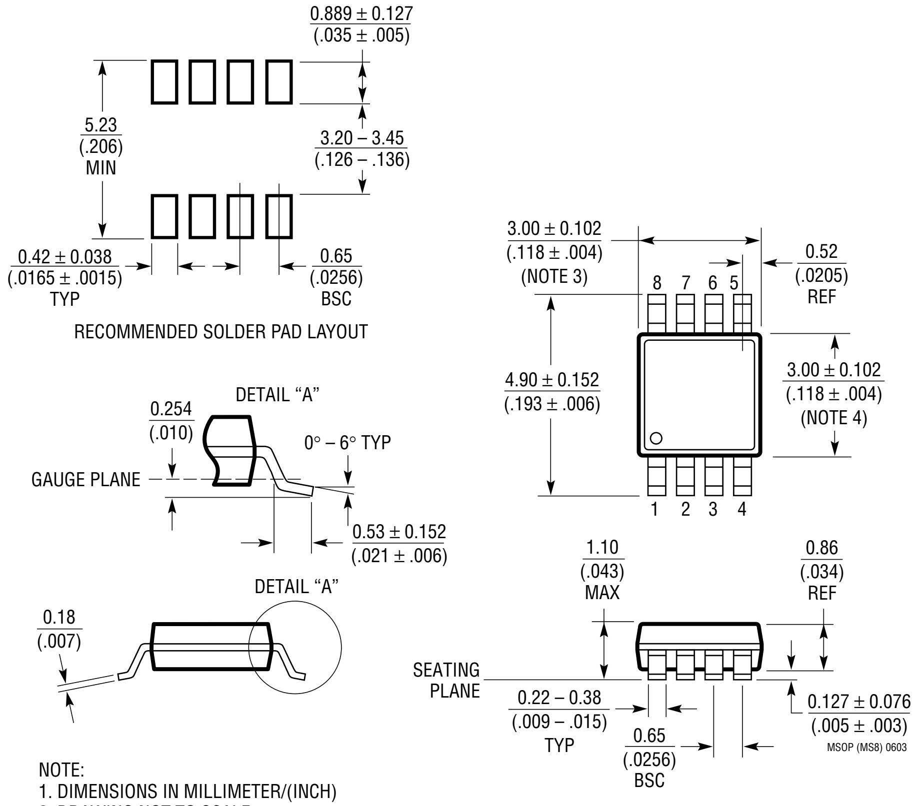


Figure 3. Effects of Rail-to-Rail Operation On a DAC Transfer Curve. (a) Overall Transfer Function (b) Effect of Negative Offset for Codes Near Zero Scale (c) Effect of Positive Full-Scale Error for Codes Near Full Scale

PACKAGE DESCRIPTION

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1458/LTC1458L	Quad 12-Bit Rail-to-Rail Output DACs with Added Functionality	LTC1458: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.096V LTC1458L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1654	Dual 14-Bit Rail-to-Rail V_{OUT} DAC	Programmable Speed/Power, 3.5µs/750µA, 8µs/450µA
LTC1655/LTC1655L	Single 16-Bit V_{OUT} DAC with Serial Interface in SO-8	V_{CC} = 5V(3V), Low Power, Deglitched
LTC1657/LTC1657L	Parrallel 5V/3V 16-Bit V_{OUT} DAC	Low Power, Deglitched, Rail-to-Rail V_{OUT}
LTC1660/LTC1665	Octal 10/8-Bit V_{OUT} DAC in 16-Pin Narrow SSOP	V_{CC} = 2.7V to 5.5V, Micropower, Rail-to-Rail Output
LTC1661	Dual 10-Bit V_{OUT} DAC in 8-Lead MSOP Package	V_{CC} = 2.7V to 5.5V, 60µA per DAC, Rail-to-Rail Output
LTC1821	Parallel 16-Bit Voltage Output DAC	Precision 16-Bit Settling in 2µs for 10V Step
LTC2600/LTC2610/ LTC2620	Octal 16/14/12-Bit Rail-to-Rail DACs in 16-Lead SSOP	250µA per DAC, 2.5V to 5.5V Supply Range Rail-to-Rail Output

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