18V, 5A Synchronous Buck-Boost DC/DC Converter

FEATURES

- **Input Voltage Range: 2.5V to 18V**
- **Runs Down to V_{IN} = 250mV After Start-Up**
- **Output Voltage Range: 0.8V to 18V**
- **5A Output Current in Buck Mode, V_{IN} > 6V**
- **3A Output Current for V_{IN} = 3.6V, V_{OUT} = 5V**
- Programmable Switching Frequency: 400kHz to 2MHz
- Synchronizable with an External Clock Up to 2MHz
- Accurate Run Comparator Threshold
- Burst Mode® Operation, No-Load I_Q = 35µA
- Ultralow Noise Buck-Boost PWM
- Current Mode Control
- Maximum Power Point Control
- Power Good Indicator
- Internal Soft-Start
- 28-Lead 4mm × 5mm QFN and TSSOP Packages

APPLICATIONS

- Wide Input Range Power Supplies
- 1- to 4-Cell Lithium Battery Powered Products
- RF Power Supplies
- Solar Battery Chargers
- System Backup Power Supplies
- Lead Acid to 12V Regulator

DESCRIPTION

The LTC®3119 is a high efficiency 18V monolithic buck-boost converter that can deliver up to 5A of continuous output current. Extensive feature integration and very low resistance internal power switches minimize the total solution footprint for even the most demanding applications. A proprietary 4-switch PWM architecture provides seamless low noise operation from input voltages above, equal to, or below the output voltage.

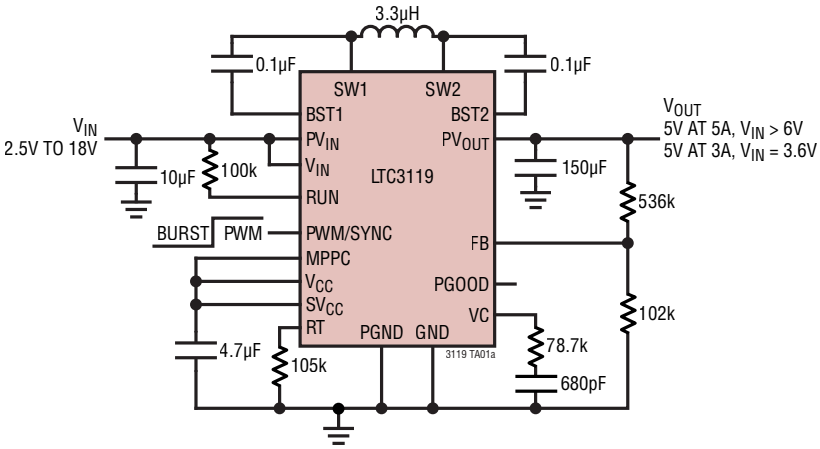
External frequency programming as well as synchronization using an internal PLL enable operation over a wide switching frequency range of 400kHz to 2MHz. The wide 2.5V to 18V input range is well suited for operation from unregulated power sources including battery stacks and backup capacitors. After start-up, operation is possible with input voltages as low as 250mV.

Other features include: output short-circuit protection, thermal overload protection, less than 3µA shutdown current, power good indicator, Burst Mode operation, and maximum power point control.

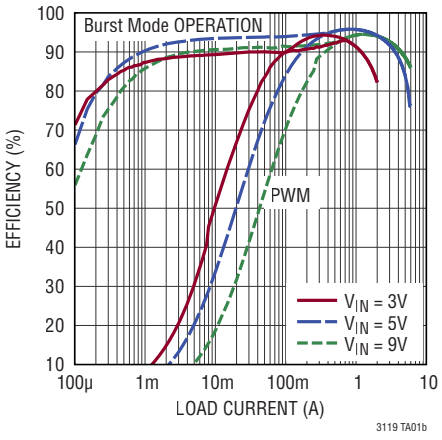
The LTC3119 is offered in thermally enhanced 28-lead 4mm × 5mm QFN and TSSOP packages.

TYPICAL APPLICATION

Wide Input Range 5V Regulator



Efficiency

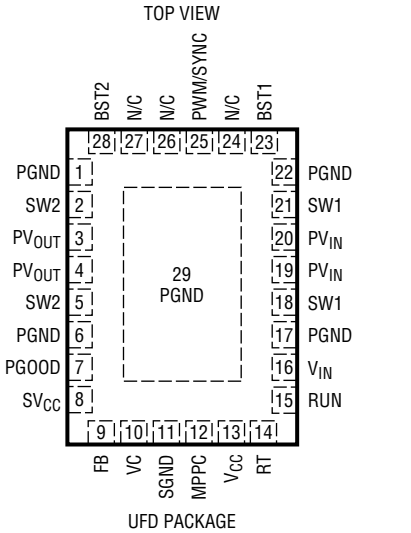


ABSOLUTE MAXIMUM RATINGS (Note 1)

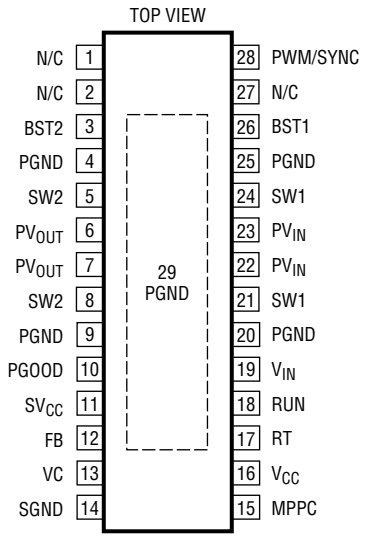
V_{IN}, PV_{IN}, PV_{OUT}, RUN, PGOOD ..... –0.3V to 19V
FB, VC, RT, SYNC, MPPC, V_{CC}, SV_{CC} ..... –0.3V to 6V
BST1 Voltage ..... (SW1 – 0.3V) to (SW1 + 6V)
BST2 Voltage ..... (SW2 – 0.3V) to (SW2 + 6V)

Operating Junction Temperature (Notes 2, 3)
LTC3119E/LTC3119I ..... –40°C to 125°C
LTC3119H ..... –40°C to 150°C
LTC3119MP ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
FE ..... 300°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 22°C/W
EXPOSED PAD (PIN 29) IS PGND, MUST BE SOLDERED TO PCB



FE PACKAGE
28-LEAD PLASTIC TSSOP
T_{JMAX} = 150°C, θ_{JA} = 21°C/W
EXPOSED PAD (PIN 29) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC3119#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3119EUFD#PBF	LTC3119EUFD#TRPBF	3119	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3119IUFD#PBF	LTC3119IUFD#TRPBF	3119	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3119EFE#PBF	LTC3119EFE#TRPBF	3119	28-Lead Plastic Enhanced TSSOP	–40°C to 125°C
LTC3119IFE#PBF	LTC3119IFE#TRPBF	3119	28-Lead Plastic Enhanced TSSOP	–40°C to 125°C
LTC3119HFE#PBF	LTC3119HFE#TRPBF	3119	28-Lead Plastic Enhanced TSSOP	–40°C to 150°C
LTC3119MPFE#PBF	LTC3119MPFE#TRPBF	3119	28-Lead Plastic Enhanced TSSOP	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = PV_{IN} = 12V, PV_{OUT} = 5V, R_T = 76.8k unless otherwise stated.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Operating Voltage	 After Start-Up (Note 4)	● ●	2.5 0.25		18 18	V V
Output Operating Voltage		●	0.8		18	V
V_{CC} Undervoltage Lockout Threshold	V_{CC} Rising V_{CC} Falling	● ●	 2.18	2.35 2.25	2.4	V V
V_{CC} Undervoltage Lockout Hysteresis				60		mV
Input Current in Shutdown	RUN = 0V				3	µA
Input Current in Sleep	FB = 0.9V			31		µA
Oscillator Frequency		●	900	1000	1100	kHz
Oscillator Operating Frequency		●	400		2000	kHz
PWM/SYNC Frequency Range		●	400		2000	kHz
PWM/SYNC Logic Threshold		●	0.3	0.7	1.1	V
PWM/SYNC Pulse Width	Minimum Low or High Duration		100			ns
PWM/SYNC Pin Current				1	50	nA
Soft-Start Duration				6		ms
Feedback Voltage	 	 ●	787 779	795 795	803 811	mV mV
Feedback Pin Current				1	50	nA
Error Amplifier Transconductance				120		µS
RUN Pin Logic Threshold		●	0.3	0.8	1	V
RUN Pin Comparator Threshold	V_{RUN} Rising	●	1.17	1.205	1.24	V
RUN Pin Hysteresis Current				0.25		µA
RUN Pin Hysteresis Voltage				90		mV
PGOOD Threshold	Percentage of FB Voltage Falling	●	–9.5	–8	–6.5	%
PGOOD Hysteresis	Percentage of FB Voltage			1.2		%
PGOOD Pull Down Resistance				700	2000	Ω
PGOOD Leakage	V_{PGOOD} = 18V			1	40	nA
MPPC Pin Threshold		●	774	798	822	mV
MPPC Pin Current				1	50	nA
Inductor Current Limit	(Note 3)	●	7	8		A
Burst Mode Operation Inductor Current Limit	V_{IN} > V_{OUT} (Note 3)			0.6		A
Maximum Duty Cycle	Percentage of Period SW2 is Low in Boost Mode	●	90	92		%
Minimum Duty Cycle	Percentage of Period SW1 is High in Buck Mode	●	0			%
SW1, SW2 Minimum Low Time				90		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = PV_{IN} = 12V, PV_{OUT} = 5V, R_T = 76.8k unless otherwise stated.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
N-Channel Switch Resistance	Switch A (PV_{IN} to SW1) Switch B (SW1 to PGND) Switch C (SW2 to PGND) Switch D (SW2 to PV_{OUT})			30 30 30 30		mΩ mΩ mΩ mΩ
N-Channel Switch Leakage	PV_{IN} = PV_{OUT} = 18V, SW1 = SW2 = 0V, 18V			1	10	µA
V_{CC} Regulation Voltage		●	3.55	3.70	3.85	V
V_{CC} Dropout Voltage	V_{CC} Current = 50mA, V_{IN} = 3V			90		mV
V_{CC} Current Limit			180			mA
V_{CC} Reverse Current	V_{CC} = 5V, V_{IN} = 3V			5		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3119 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3119E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specification over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3119I specifications are guaranteed over the –40°C to 125°C operating junction temperature range. The LTC3119H specifications are guaranteed over the –40°C to 150°C operating junction temperature range. The LTC3119MP specifications are guaranteed and tested over the –55°C to 150°C operating junction temperature range. High temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C.

Note 3: Current measurements are performed when the LTC3119 is not switching. The current limit values measured in operation will be somewhat higher due to the propagation delay of the comparators.

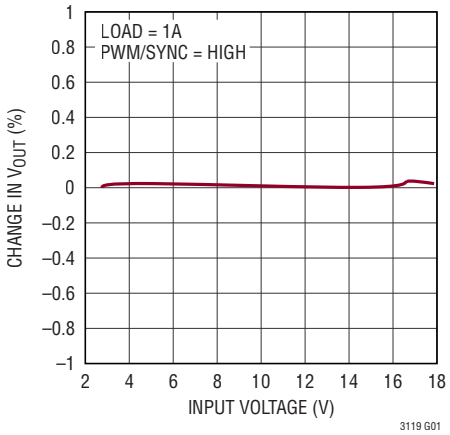
Note 4: Minimum input voltage is governed by the V_{CC} UVLO threshold. If V_{CC} is maintained though external bootstrapping, the part will continue to operate until power transfer to the output is no longer possible.

Note 5: Switch timing measurements are made in an open-loop test configuration. Timing in the application may vary somewhat from these values due to differences in the switch pin voltage during the non-overlap durations when switch pin voltage is influenced by the magnitude and direction of the inductor current.

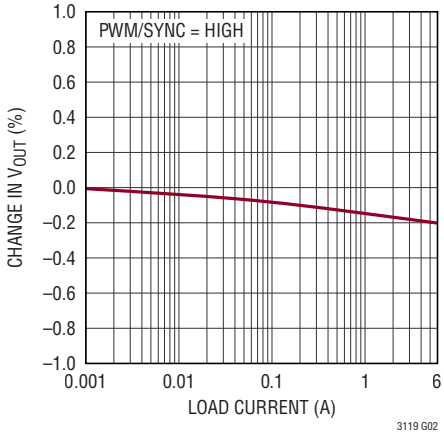
Note 6: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

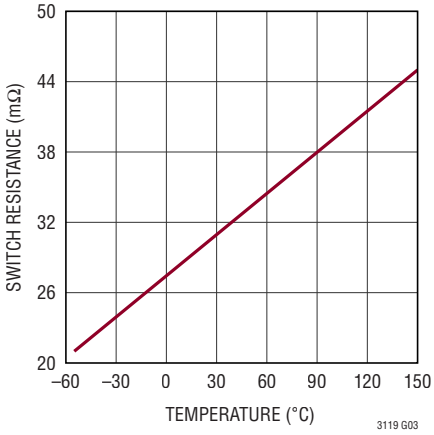
Output Voltage Line Regulation



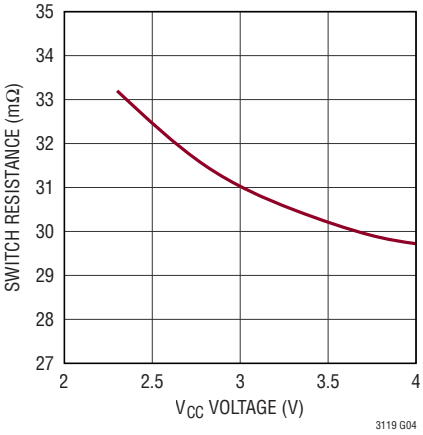
Output Voltage Load Regulation



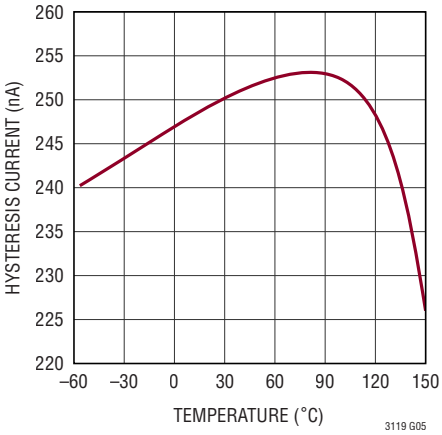
Power Switch Resistance vs Temperature



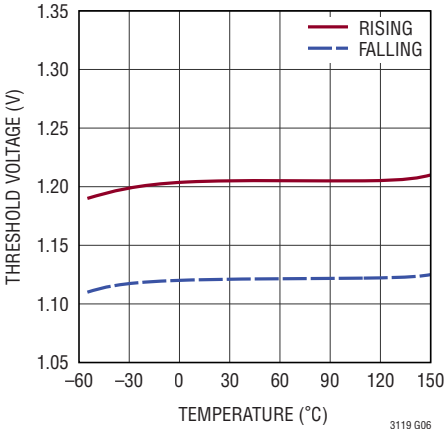
Power Switch Resistance vs V_{CC}



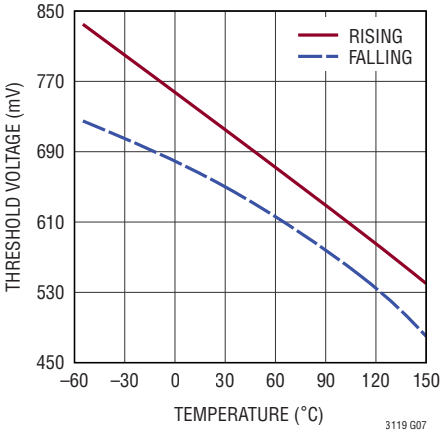
Run Pin Hysteresis Current vs Temperature



Run Pin Comparator Threshold vs Temperature

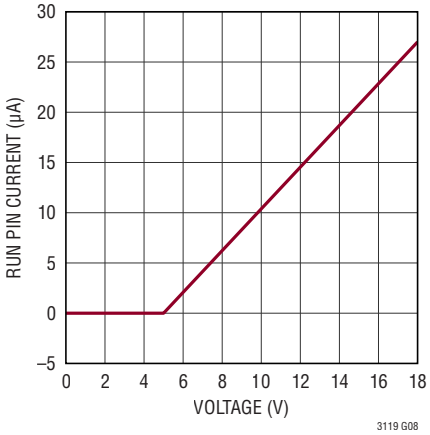


Run Pin Logic Threshold vs Temperature

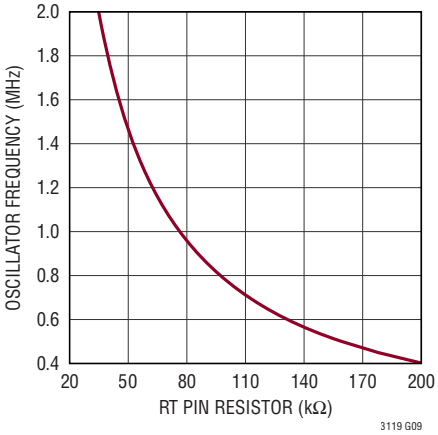


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

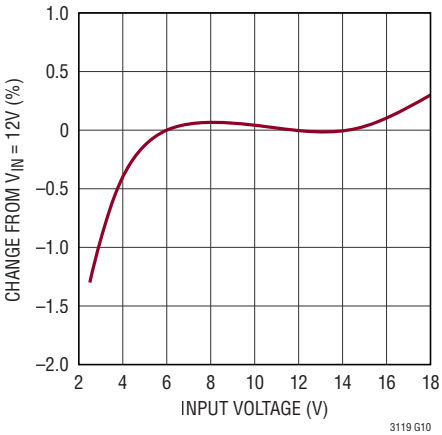
Run Pin Current vs Run Pin Voltage



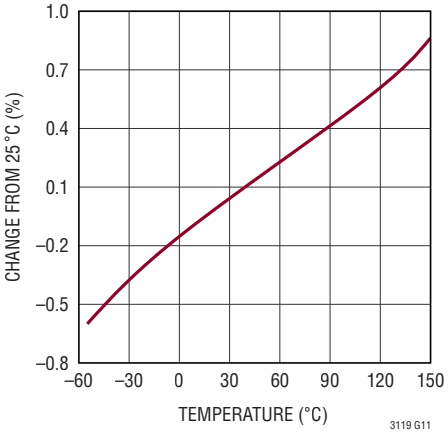
Oscillator Frequency vs RT



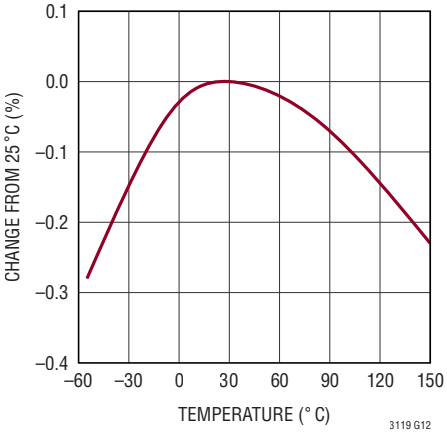
Oscillator Frequency vs V_{IN}



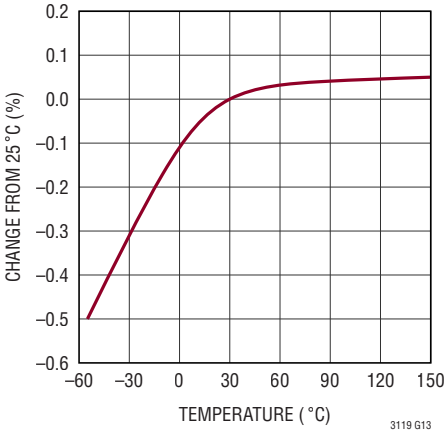
Oscillator Frequency vs Temperature



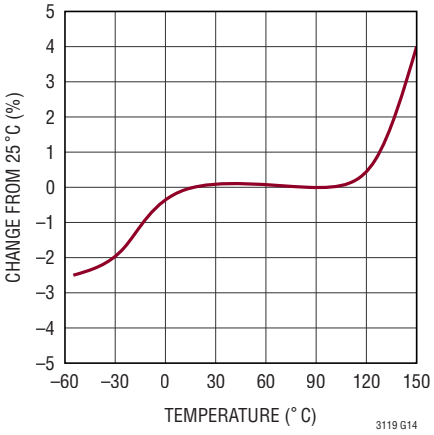
FB Voltage vs Temperature



MPPC Pin Voltage vs Temperature

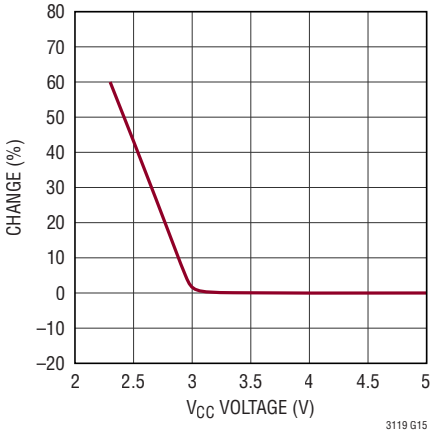


SW1, SW2 Minimum Low Time vs Temperature

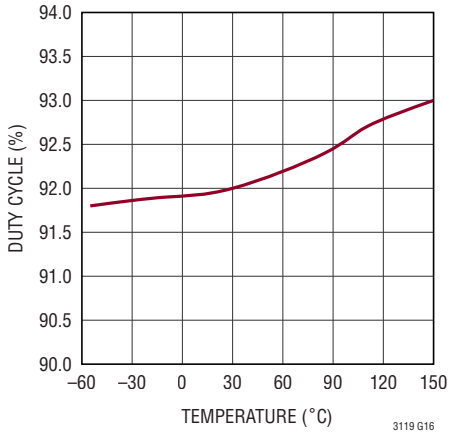


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

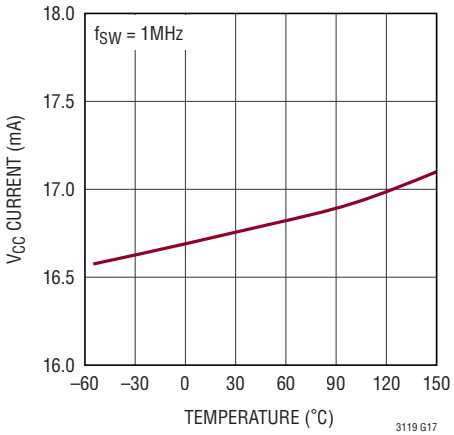
SW1, SW2 Minimum Low Time vs V_{CC}



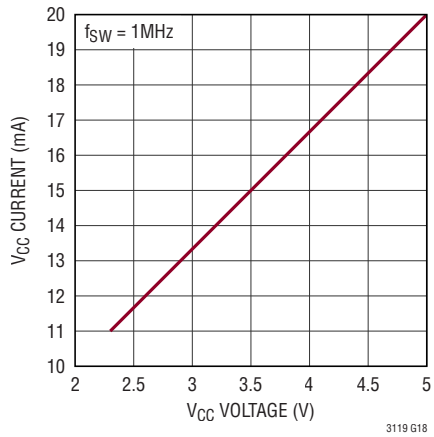
SW2 Maximum Duty Cycle vs Temperature



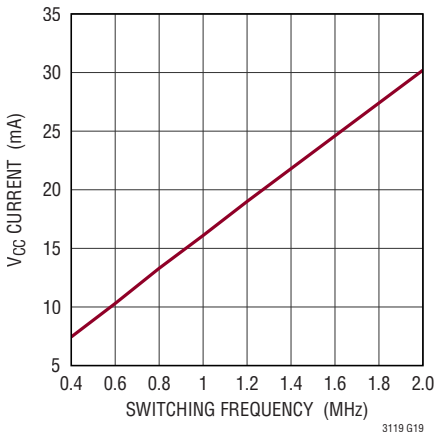
V_{CC} Current vs Temperature



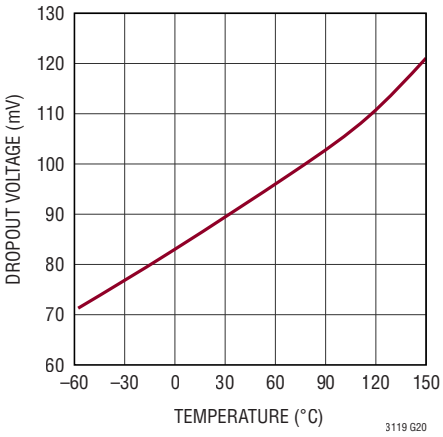
V_{CC} Current vs V_{CC}



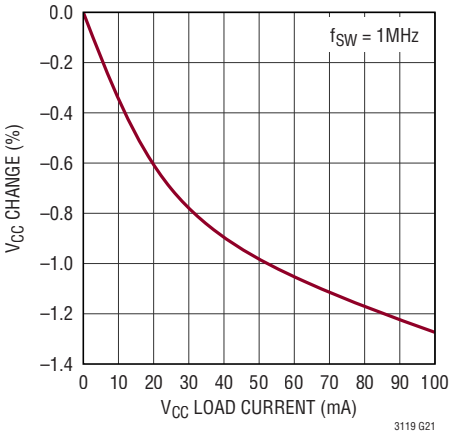
V_{CC} Current vs Switching Frequency



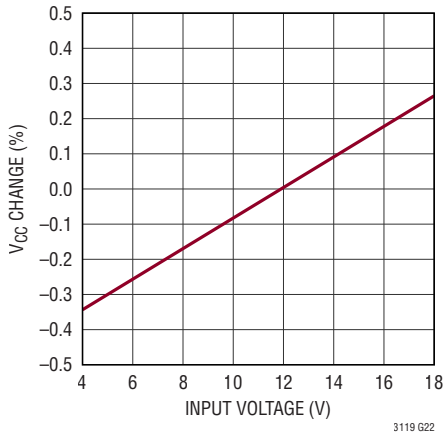
V_{CC} Dropout Voltage vs Temperature



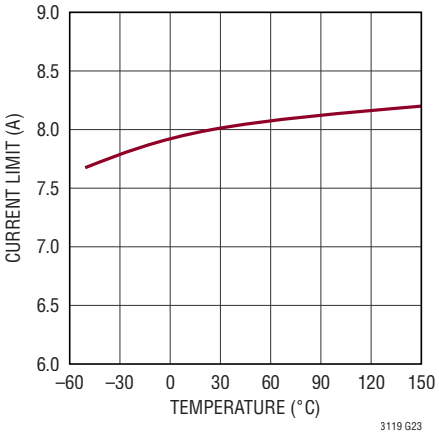
V_{CC} Load Regulation



V_{CC} Line Regulation

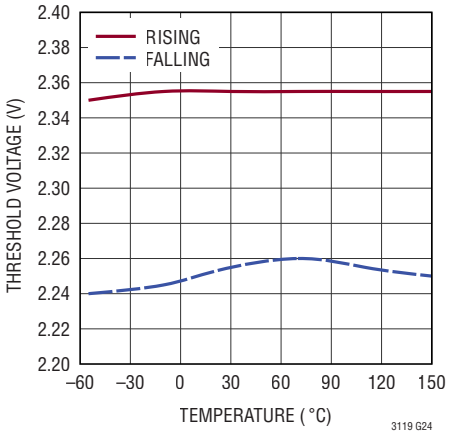


Inductor Current Limit vs Temperature

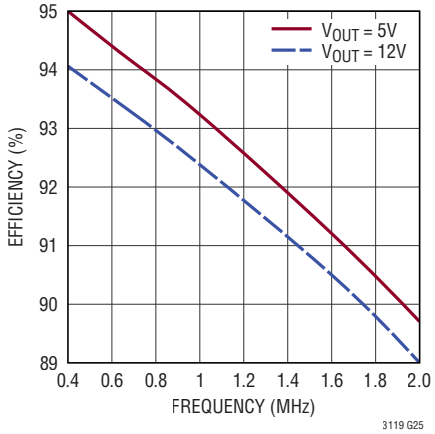


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

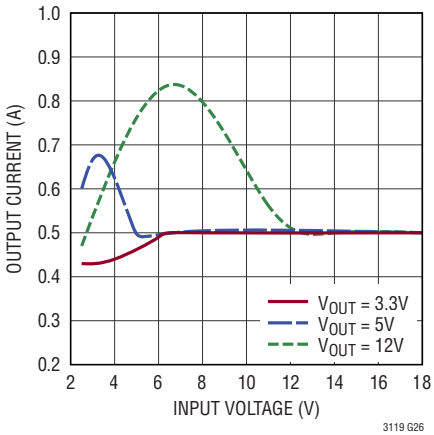
V_{CC} UVLO Threshold vs Temperature



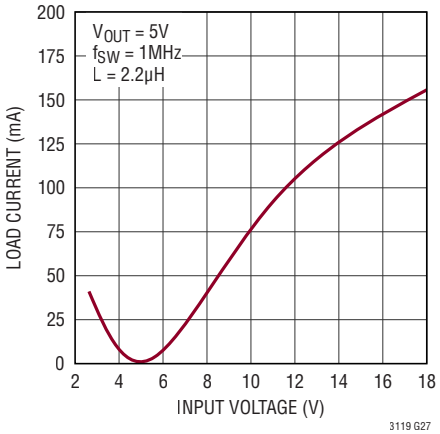
Efficiency vs Switching Frequency



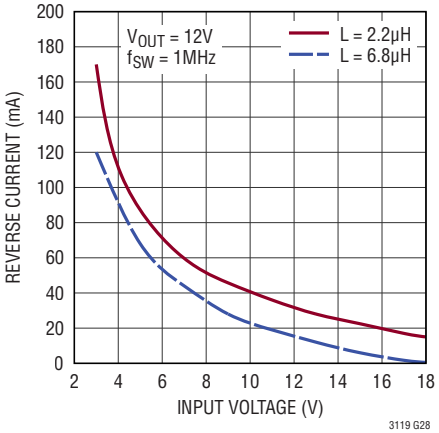
Burst Mode Operation Threshold



Minimum Current to Avoid Pulse Skipping

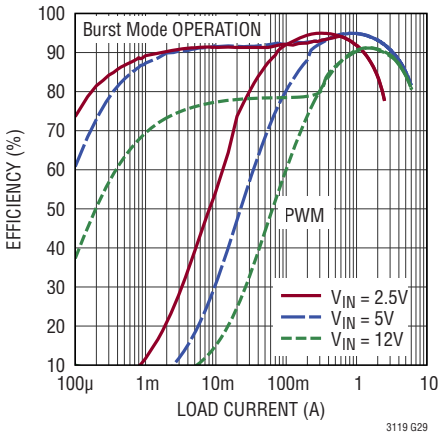


Maximum Reverse Current During MPPC Control (V_{MPPC} < 0.86)

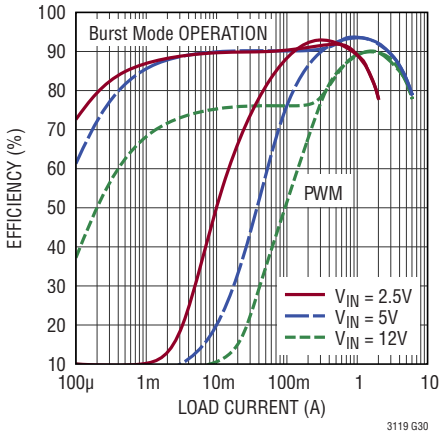


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

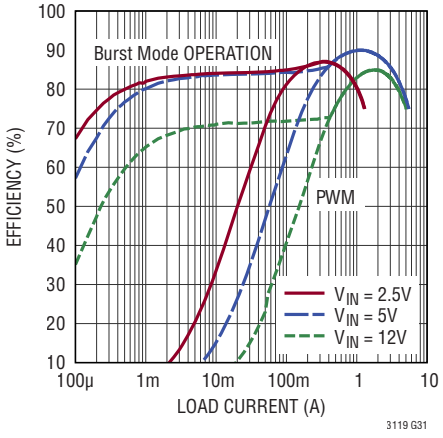
Efficiency, V_{OUT} = 3.3V
f_{SW} = 500kHz



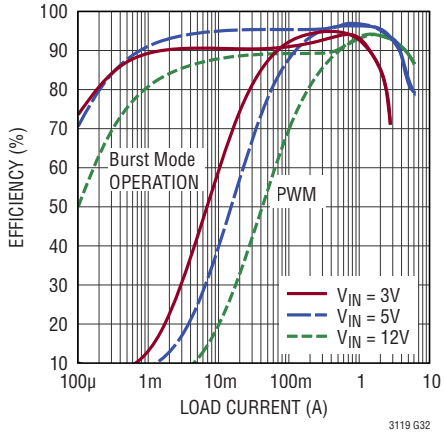
Efficiency, V_{OUT} = 3.3V
f_{SW} = 1MHz



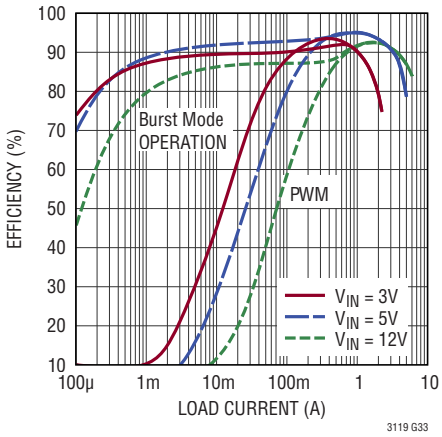
Efficiency, V_{OUT} = 3.3V
f_{SW} = 2MHz



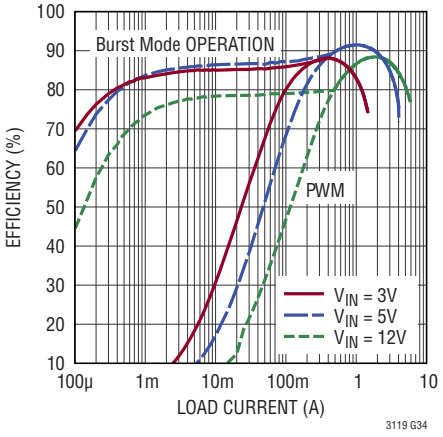
Efficiency, V_{OUT} = 5V
f_{SW} = 500kHz



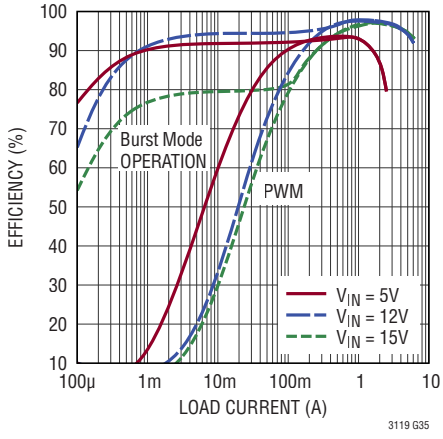
Efficiency, V_{OUT} = 5V
f_{SW} = 1MHz



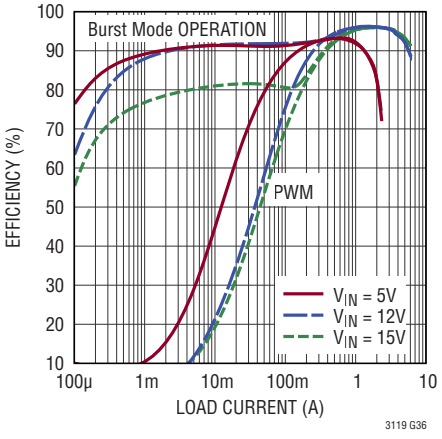
Efficiency, V_{OUT} = 5V
f_{SW} = 2MHz



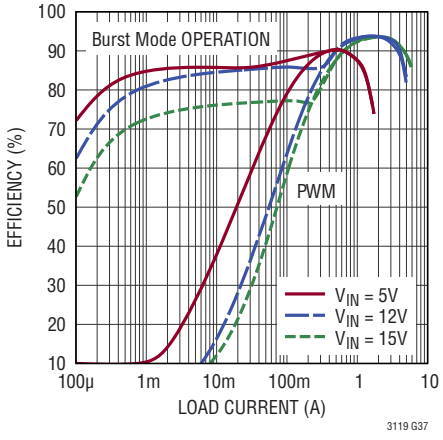
Efficiency, V_{OUT} = 12V
f_{SW} = 500kHz



Efficiency, V_{OUT} = 12V
f_{SW} = 1MHz

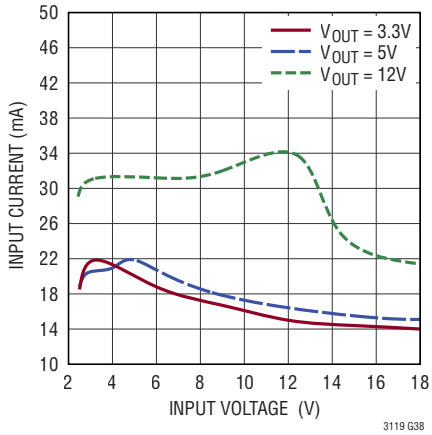


Efficiency, V_{OUT} = 12V
f_{SW} = 2MHz

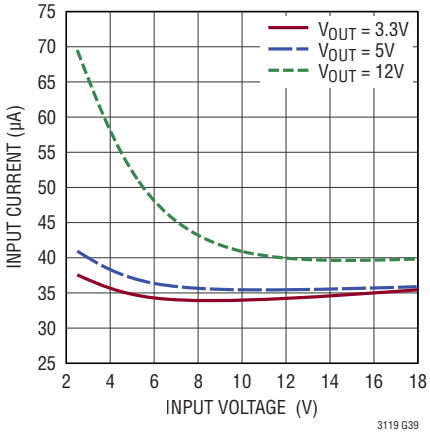


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

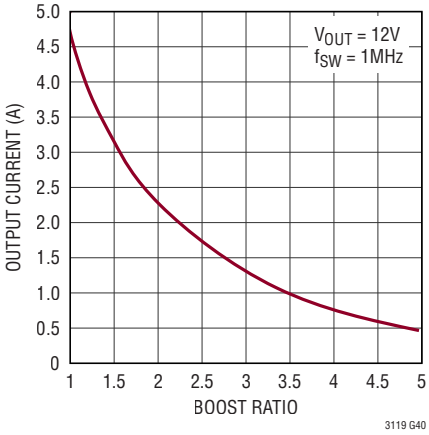
PWM Mode No-Load Input Current



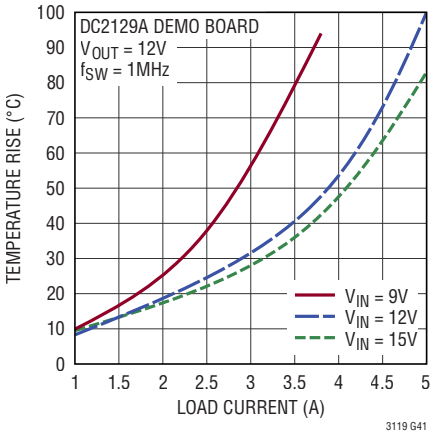
Burst Mode Operation No–Load Input Current



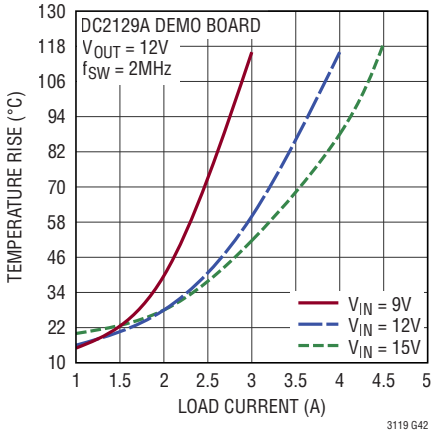
Maximum Output Current vs Boost Ratio



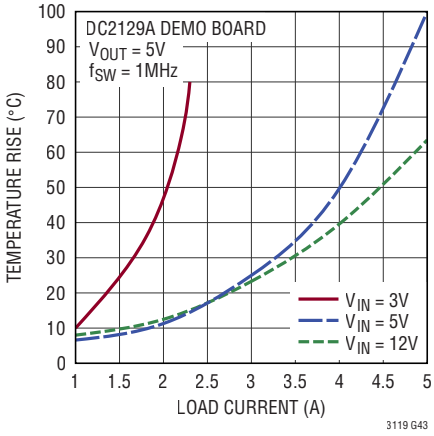
Temperature Rise vs Load Current



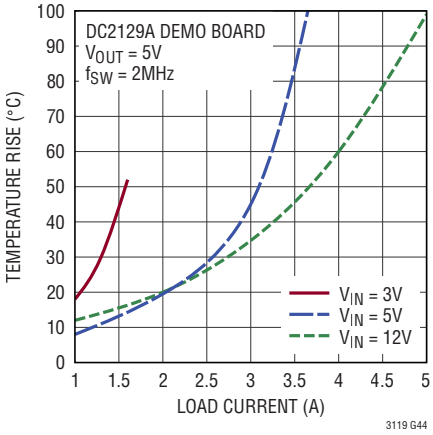
Temperature Rise vs Load Current



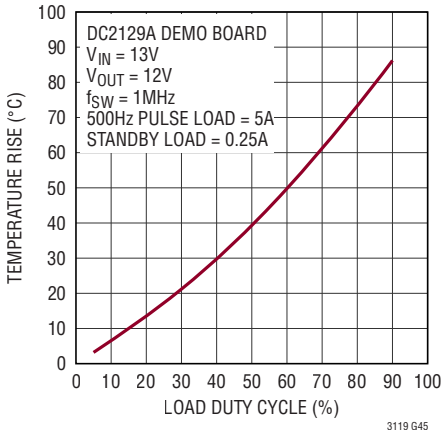
Temperature Rise vs Load Current



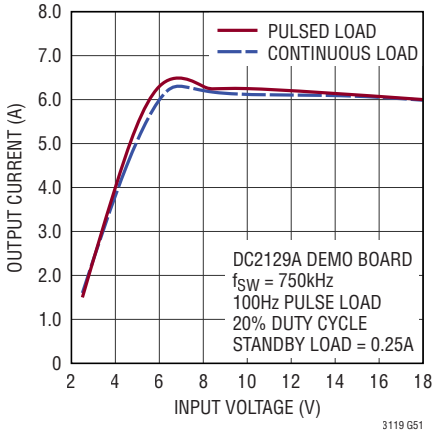
Temperature Rise vs Load Current



Temperature Rise vs Pulsed Load Duty Cycle

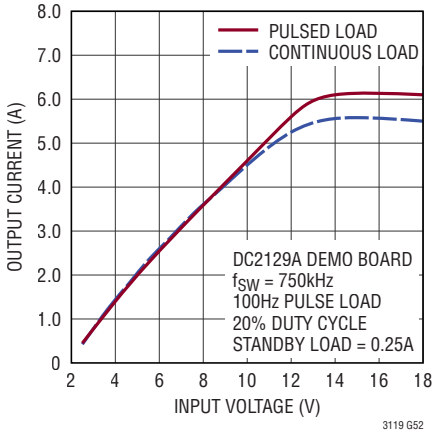


Maximum Output Current V_{OUT} = 5V

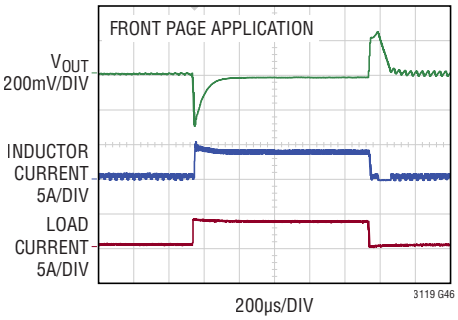


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

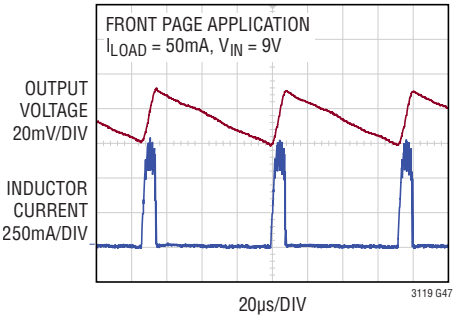
Maximum Output Current
V_{OUT} = 12V



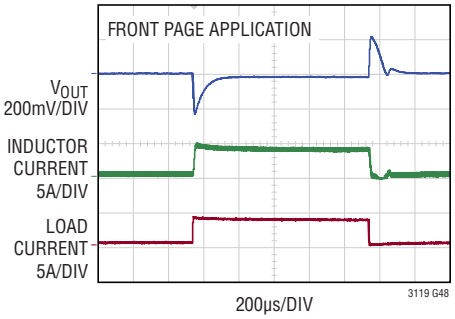
Burst Mode Operation Load Step
400mA to 4A, V_{IN} = 9V



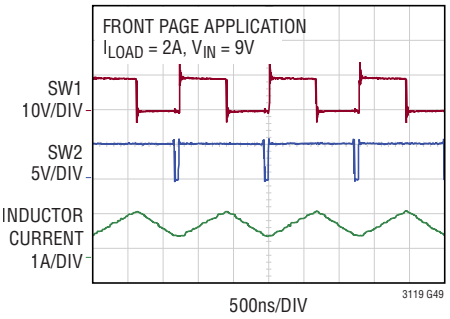
Burst Mode Operation
V_{OUT} Ripple



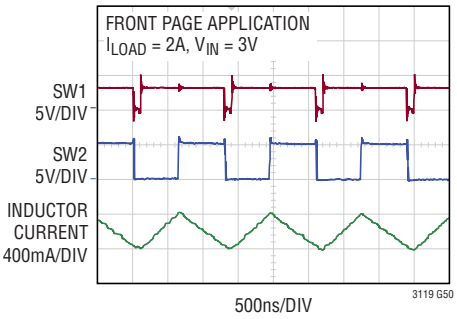
PWM Mode Load Step 400mA to
4A, V_{IN} = 9V



Switching Waveforms, Buck
Mode Operation



Switching Waveforms, Boost
Mode Operation



PIN FUNCTIONS (QFN/TSSOP)

PGND (Pins 1, 6, 17, 22, Exposed Pad Pin 29/Pins 4, 9, 20, 25, Exposed Pad Pin 29): Power Ground Connection. These pins should be connected to the power ground using the shortest and widest connections possible. The exposed pad must be soldered to the PCB and electrically connected to ground through the shortest and lowest impedance path possible and to the PCB ground plane for rated thermal performance.

SW2 (Pins 2, 5/Pins 5, 8): Buck-Boost Converter Power Switch Pin. These pins should be connected to one side of the Buck-Boost inductor.

PV_{OUT} (Pins 3, 4/Pins 6, 7): Output Voltage Power Connection. These pins is connected to switch D of the buck-boost converter. Connect a low ESR 10µF or larger capacitor between this pin and ground using the lowest impedance path possible.

PGOOD (Pin 7/Pin 10): Open drain output that pulls to ground when FB drops too far below its regulated voltage. Connect a pull-up resistor from this pin to a positive supply. Refer to the Operation section of the data sheet for more detail.

SV_{CC} (Pin 8/Pin 11): Supplies voltage to internal circuits used for production test. This pin must be tied to V_{CC}.

PIN FUNCTIONS (QFN/TSSOP)

FB (Pin 9/Pin 12): Feedback Voltage Input. A resistor divider connected to this pin sets the output voltage for the buck-boost converter.

VC (Pin 10/Pin 13): Error Amplifier Output. A frequency compensation network must be connected between this pin and SGND to stabilize the voltage control loop.

SGND (Pin 11/Pin 14): Signal Ground. This pin is the ground connection for the control circuitry of the IC and must be tied to ground in the application.

MPPC (Pin 12/Pin 15): Maximum Power Point Control Setpoint. Connect this pin to a resistive divider from V_{IN} to GND to set the input regulation voltage. The MPPC pin should be tied to V_{CC} to disable MPPC operation.

V_{CC} (Pin 13/Pin 16): Internal Regulator Output Voltage and Supply Rail for Control Circuits. This pin is the output of the internal low voltage linear regulator used to supply the control circuitry. The V_{CC} output may also be used to power external loads of up to 10mA. A 4.7µF capacitor should be connected between this pin and GND using the shortest trace possible.

RT (Pin 14/ Pin 17): Oscillator Frequency Programming Input. Connect a resistor between this pin and GND to set the buck-boost converter switching frequency.

RUN (Pin 15/Pin 18): Input to Enable and Disable the IC and Set Custom Input UVLO Threshold. The RUN pin can be driven by external logic signals to enable and disable the IC. In addition, the voltage on this pin can be set by a resistor divider connected to the input voltage to provide an accurate undervoltage lockout threshold. The IC is enabled if the RUN pin voltage exceeds 1.205V nominally. Once enabled, a 250nA current is sourced from this pin to provide additional hysteresis.

V_{IN} (Pin 16/Pin 19): Input Voltage Pin for Internal V_{CC} Regulator.

PV_{IN} (Pins 19, 20/Pins 22, 23): Input Voltage Power Connection. These pins is connected to switch A of the buck-boost converter. Connect a 10µF or larger capacitor between this pin and GND using the lowest impedance path possible.

SW1 (Pins 18, 21/Pins 21, 24): Buck-Boost Converter Power Switch Pin. These pins should be connected to one side of the Buck-Boost inductor.

BST1 (Pin 23/Pin 26): Power Rail for SWA Driver. This pin must be connected to SW1 through a 0.1µF capacitor. This pin is used to generate the gate drive rail for power switch A.

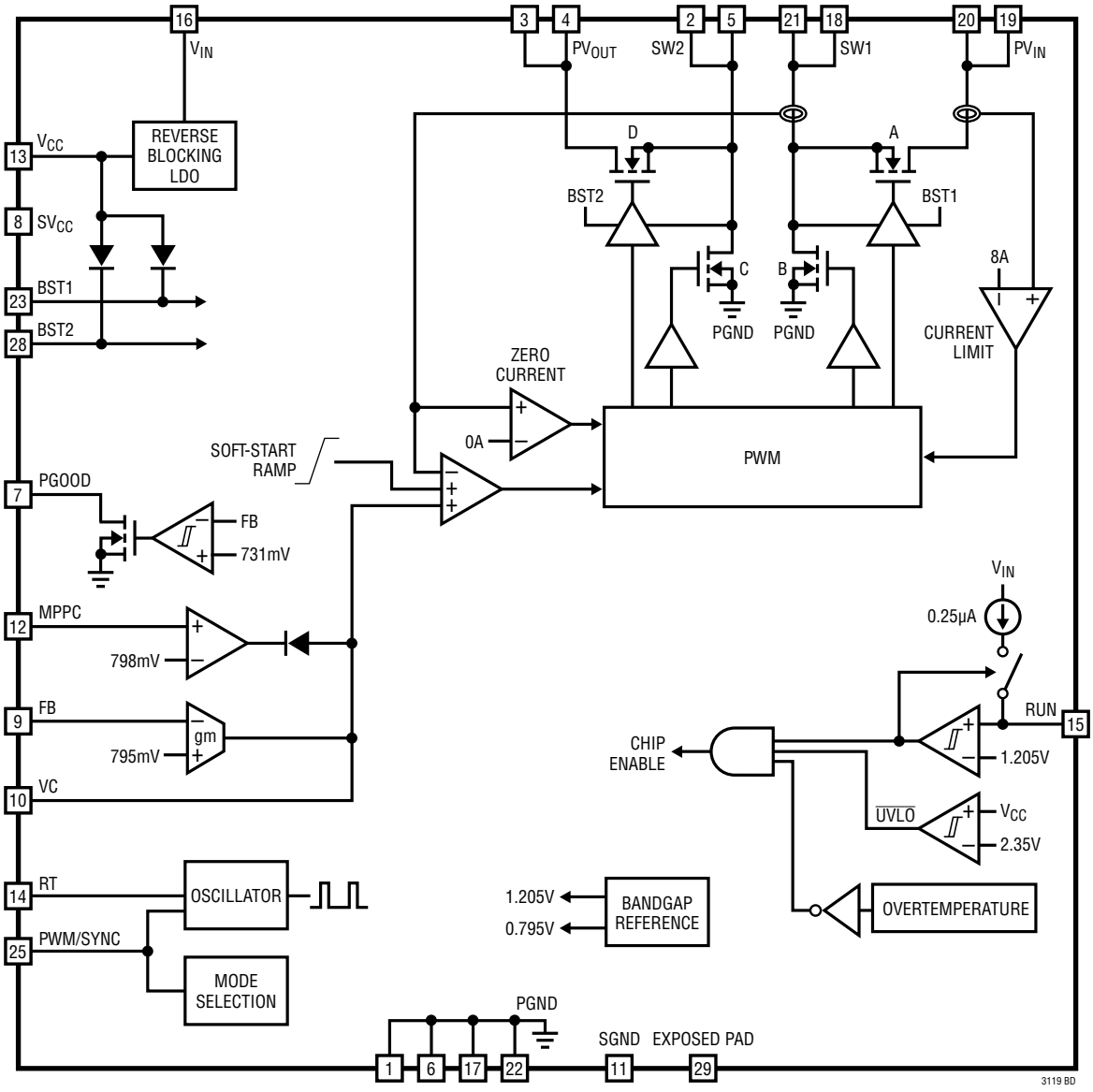
N/C (Pins 24, 26, 27/Pins 1, 2, 27): No Connection. Can be connected to ground or left open. This pin does not connect to any internal circuitry.

PWM/SYNC (Pin 25/Pin 28): Automatic Burst Mode Operation/PWM Mode Control Pin and Synchronization Input. Forcing this pin high causes the IC to operate in fixed frequency PWM mode at all loads using the internal oscillator at the frequency set by the RT Pin. Forcing this pin low causes the IC to enable Burst Mode operation at light loads to maximize efficiency. Clocking this pin will cause the part to synchronize to the clock for frequencies higher than the frequency programmed by the RT Pin. When using this pin for synchronization, a minimum input pulse width of 100ns should be used.

BST2 (Pin 28/Pin 3): Power Rail for SWD Driver. This pin must be connected to SW2 through a 0.1µF capacitor. This pin is used to generate the gate drive rail for power switch D.

BLOCK DIAGRAM

Pin numbers are shown for UFD package only.



OPERATION

INTRODUCTION

The LTC3119 is a 5A monolithic Buck-Boost DC/DC converter that can operate over a wide range of 2.5V to 18V on V_{IN} and 0.8V to 18V on V_{OUT}. Integrated low $R_{DS(ON)}$ N-Channel DMOS power switches reduce solution complexity and maximize conversion efficiency. Internal high side power switch drivers require only two small external capacitors and further simplify application circuit design. The LTC3119 incorporates many additional features to allow for maximum flexibility when designing application solutions, including an accurate RUN pin comparator, wide operating frequency range of 400kHz to 2MHz, external clock synchronization, power good indicator, and Maximum Power Point Control (MPPC) of the input voltage for operation from current limited sources such as photovoltaic arrays.

High side drive and sense circuitry allow for operation to 0V on the output while maintaining current control and synchronous switch operation. Operation to voltages below 2.5V on the input is also possible when bootstrapping the V_{CC} pin from V_{OUT}, or other alternate sources, allowing for maximum extraction of power from energy storage devices such as supercapacitors.

A proprietary ultralow noise PWM switching algorithm maintains output regulation with input voltages that are below, equal to, or above the output voltage. Transitions between buck and boost operating modes occur seamlessly without transients or subharmonic switching. The LTC3119 has an internal oscillator that can be configured to operate over a wide range of frequencies. Using a single programming resistor, the operating frequency can be configure between 400kHz and 2MHz allowing for flexibility when optimizing for board area and efficiency. The internal oscillator can also be synchronized to an external clock applied to the PWM/SYNC pin in noise sensitive applications.

Burst Mode operation allows for high efficiency operation at light loads while automatically transitioning to PWM mode at heavier loads. At low output currents, Burst Mode operation is enabled, with a current of only 31µA (typical). In shutdown the total supply current is further reduced to 3µA (maximum).

PWM MODE OPERATION

If the PWM/SYNC pin is held high, or the load current on the converter is high enough to command PWM mode operation with the PWM/SYNC pin held low, the LTC3119 operates in a fixed frequency PWM mode. The operating frequency is defined by the resistance on the RT pin as described in the Applications section of this data sheet. PWM mode minimizes output voltage ripple and yields a low noise switching frequency spectrum. A proprietary switching algorithm provides seamless transitions between operating modes and eliminates discontinuities in the average inductor current, inductor ripple current and loop transfer function throughout all modes of operation. These advantages result in increased efficiency, improved loop stability and lower output voltage ripple in comparison to a traditional buck-boost converter. Figure 1 shows the topology of the LTC3119 power stage which is comprised of four N-channel DMOS switches and their associated gate drivers.

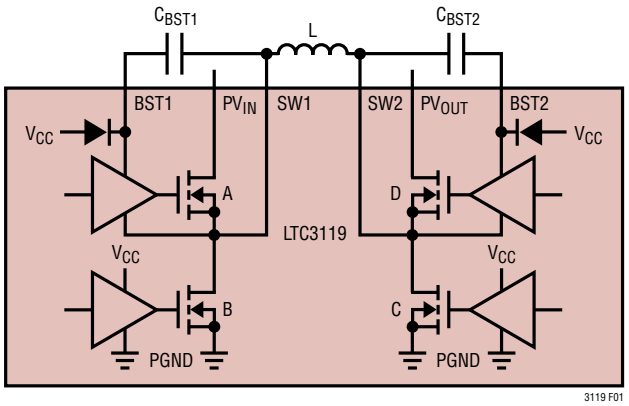


Figure 1. Power Stage Schematic

In PWM mode operation both switch pins transition on every cycle independent of the input and output voltages. The internal average current control loop commands the pulse width modulator to generate the appropriate switch duty cycle to maintain regulation of the output voltage.

Oscillator and Phase-Locked Loop

The LTC3119 operates from an internal oscillator with a switching frequency that is configured by a single external resistor between the RT pin and GND. For noise sensitive applications, an internal phase-locked loop allows the

OPERATION

LTC3119 to be synchronized to an external clock signal applied to the PWM/SYNC pin. The phase-locked loop is only able to increase the frequency of the internal oscillator to obtain synchronization. Therefore, the resistor R_T must be chosen to program the internal oscillator to a lower frequency than the frequency of the clock applied to the PWM/SYNC pin. Sufficient margin must be included to account for the frequency variation of the external synchronization clock as well as the worst-case variation in frequency of the internal oscillator. Whether operating from its internal oscillator or synchronized to an external clock signal, the LTC3119 is able to operate with a switching frequency from 400kHz to 2MHz, providing the ability to trade-off small solution size and optimum power conversion efficiency.

RUN Pin Comparator

In addition to serving as a logic-level input to enable the IC, the RUN pin features an accurate internal comparator allowing it to be used to set custom rising and falling input undervoltage lockout thresholds with the addition of an external resistor divider. When the RUN pin is driven above its logic threshold (typically 0.8V) the V_{CC} regulator is enabled which provides power to the internal control circuitry of the IC and the accurate RUN pin comparator is enabled. If the RUN pin voltage is increased further so that it exceeds the RUN comparator threshold (1.205V nominal), the buck-boost converter will be enabled. If the RUN pin is brought below the RUN comparator threshold, the buck-boost converter will inhibit switching, but the V_{CC} regulator and control circuitry will remain powered unless the RUN pin is brought below its logic threshold. Therefore, in order to place the part in shutdown and reduce the input current to its minimum level (3µA) it is necessary to ensure that the RUN pin is brought below the worst-case logic threshold (0.3V).The RUN pin is a high voltage input and can be connected directly to V_{IN} to continuously enable the part when the input supply is present. If the RUN pin is forced above approximately 5V it will sink a small current as given by the following equation:

$$I_{RUN} = \frac{(V_{RUN} - 5V)}{5M\Omega}$$

With the addition of an external resistor divider as shown in Figure 2, the RUN pin can be used to establish a custom input under voltage lockout threshold. The buck-boost converter is enabled when the RUN pin reaches 1.205V which allows the rising UVLO threshold to be set via the resistor divider ratio. Once the RUN pin reaches the threshold voltage, the comparator switches and the buck-boost converter is enabled. When the part is enabled an internal 0.25µA (typical) current source is enabled which sources current out of the RUN pin raising the RUN pin voltage away from the threshold.

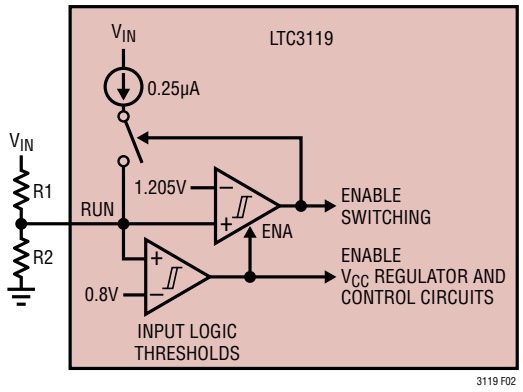


Figure 2. Accurate Run Pin Comparator

In order to disable the part, V_{IN} must be reduced sufficiently to overcome the hysteresis generated by this current as well as the 90mV hysteresis of the RUN comparator. As a result, the amount of hysteresis can be independently programmed without affecting the rising UVLO threshold by scaling the values of both resistors.

V_{CC} REGULATOR

An internal low dropout regulator generates the 3.7V (nominal) V_{CC} rail from V_{IN}. The V_{CC} rail powers the internal control circuitry and power device gate drivers of the LTC3119. In addition to powering the internal circuitry of the LTC3119, the V_{CC} regulator can also support an external load of 10mA. The V_{CC} regulator is disabled when the RUN pin is below its logic threshold to reduce quiescent current and is enabled when the RUN pin is above its logic threshold. The V_{CC} regulator includes current limit protection to safeguard against short circuiting and overload conditions. For applications where the output voltage is

OPERATION

set to 5V, V_{CC} can be driven from the output rail through a Schottky diode. Bootstrapping in this manner can provide a significant efficiency improvement, particularly at large voltage step down ratios, and also allows operation down to lower input voltages. The maximum operating voltage for the V_{CC} pin is 5.5V and care must be taken to ensure that this limit is not exceeded when driving V_{CC} externally.

CURRENT MODE CONTROL

The LTC3119 utilizes an average current mode control scheme. Current mode control provides simplified loop compensation, rapid response to load transients and inherent line voltage rejection. The voltage on the VC pin defines the commanded average inductor current, and is adjusted by the error amplifiers to maintain regulation of the active control loop (FB or MPPC).

The internal current mode control loop error amplifier compares the sensed average inductor current and the commanded average inductor current level to modulate the SW1 and SW2 pins on a cycle-by-cycle basis.

The average current mode control technique is similar to peak current mode control except that the average current amplifier, by virtue of its configuration as an integrator, controls average current instead of the peak current. This difference eliminates the peak to average current error of peak current mode control, while maintaining most of the advantages inherent to peak current mode control. Compensation of the inner current loop is accomplished by an internal compensation network that is optimized to provide high bandwidth and low regulation error under all operating conditions.

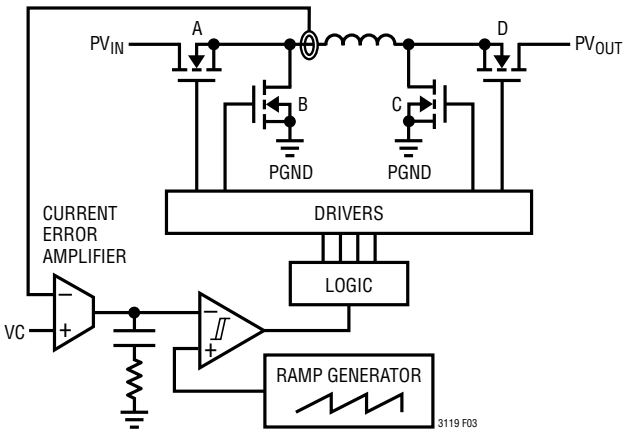


Figure 3. Inner Average Current Loop Diagram

ERROR AMPLIFIERS

Integrated into the LTC3119 are two separate error amplifiers to control the input to the inner current mode control loop. These amplifiers monitor voltages at the FB and MPPC pins. The outputs from these amplifiers are summed together and used as the commanded current level for the inner current mode control loop. To ensure stability, a compensation network must be connected between the output of the error amplifiers (VC pin) and GND. A Type II compensation network, as shown in Figure 4, is recommended for most applications since it provides the flexibility to optimize converter response while minimizing DC errors in the output voltage.

While the FB error amplifier is the only amplifier with the ability to increase the commanded current level, both amplifiers can reduce the commanded current to maintain regulation for their associated control loop (see Block Diagram). At any given time, only one control loop is active while the other is inactive. Priority is given to the MPPC control loop, which can override the voltage loop and reduce the commanded current level. When under control of the MPPC error amplifier, the compensation network of the VC pin is ignored.

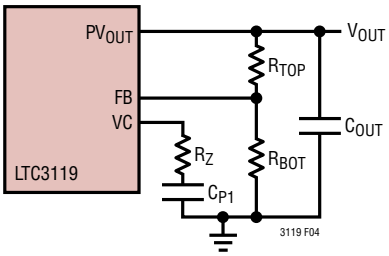


Figure 4. FB and VC Pin Configuration

CURRENT LIMIT AND ZERO CURRENT DETECTION

The LTC3119 incorporates limits for both the maximum peak and maximum average inductor current. Using the current sense information, if the inductor current reaches a peak level of 11A (typical), switch A is immediately turned off to ensure that the inductor current remains controlled.

OPERATION

The average current mode control loop also clamps the maximum average current in the inductor to 8A (typical). These two current limits help to ensure a smooth transition into regulation as well as protecting against current conditions beyond the capability of the IC.

The LTC3119 incorporates dedicated zero current detection comparators to minimize reverse current during switching and provide discontinuous mode operation. The zero current detection thresholds are adjusted based on operating conditions to avoid subharmonic switching and may result in small amounts of negative current under some conditions. When the part is being controlled by the MPPC control loop, the zero cross comparators are set to approximately 150mA to help prevent any reverse current from discharging the output storage element.

SOFT-START

The LTC3119 soft-start circuit minimizes input current transients and output voltage overshoot on initial power-up. The required timing components for soft-start are internal to the LTC3119 and produce a typical soft-start duration of 6ms. The internal soft-start circuit slowly ramps the command signal to the current mode control loop (VC pin voltage). In doing so, the inductor current is also slowly increased, starting from zero. Soft-start is reset by the V_{CC} UVLO, the RUN pin accurate enable comparator, and thermal shutdown.

MAXIMUM POWER POINT CONTROL (MPPC)

The MPPC input of the LTC3119 can be used with an optional external voltage divider to dynamically adjust the commanded inductor current in order to maintain a minimum input voltage. This is primarily useful when using resistive sources, such as photovoltaic panels, to maximize input power transfer and prevent V_{IN} from dropping too low under load. Referring to Figure 5, the MPPC pin is internally connected to the noninverting input of a transconductance amplifier. If the MPPC pin voltage falls below the reference voltage, the output of the amplifier reduces the commanded average inductor current (VC pin voltage) to reduce the input current and regulate V_{IN} to the programmed minimum voltage.

External compensation may also be required and is generally provided by a series resistor and capacitor connected between the MPPC pin and GND. This compensation network is in parallel with the lower resistor of the V_{IN} voltage divider network.

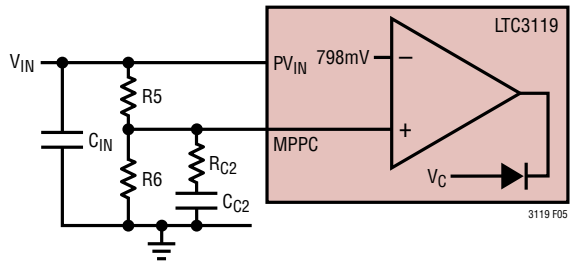


Figure 5. MPPC Pin Configuration

BURST MODE OPERATION

When the PWM/SYNC pin is held low, the LTC3119 is configured for Burst Mode operation. As a result, the buck-boost DC/DC converter will operate with continuous PWM switching until the output current drops to low levels at which point the converter will automatically transition to power saving Burst Mode operation at lower output currents. When operating in Burst Mode operation, the LTC3119 will go into a sleep state when the output voltage achieves its nominal regulation level. The sleep state halts PWM switching and powers down all nonessential functions of the IC, reducing the quiescent current of the LTC3119 to just 31µA (typical). This greatly improves overall power conversion efficiency for light loads. Since the converter is not switching in sleep, the output voltage will slowly decay at a rate determined by the output load resistance and the output capacitor value. When the output voltage has decayed by a small amount, the LTC3119 will wake and initiate PWM switching operation until the output voltage on V_{OUT} is restored to the previous level. If the load is very light, the LTC3119 may only need to switch for a few cycles to restore V_{OUT} and will sleep for extended periods of time, significantly improving efficiency. If the load is suddenly increased above the burst transition threshold, the part will automatically enter continuous PWM operation until the load is once again reduced. Note that Burst Mode operation is inhibited until soft-start is completed and V_{OUT} has reached regulation. Burst Mode operation is also inhibited when the MPPC loop is in control.

OPERATION

POWER GOOD INDICATOR

The LTC3119 provides an open-drain PGOOD output that pulls low if V_{OUT} falls more than 8% (typical) below its programmed value. When V_{OUT} rises to within 6.5% (typical) of its programmed value, the internal PGOOD pull-down will turn off and PGOOD will go high if an external pull-up resistor has been provided. An internal filter prevents nuisance trips of PGOOD due to short transients on V_{OUT}. Note that PGOOD can be pulled up to any voltage, as long as the absolute maximum rating of 19V is not exceeded. The PGOOD function is active when the RUN pin voltage is above the logic enable threshold of 0.8V (typical). When the RUN pin voltage is below 0.8V (typical) and the V_{CC} supply is still present, the PGOOD pull-down will be enabled.

THERMAL CONSIDERATIONS

The power switches in the LTC3119 are designed to operate continuously with currents up to the internal current limit thresholds. Operating at high current levels results in significant heat generated within the IC. In addition, in many applications the V_{CC} regulator is operated with large input-to-output voltage differentials resulting in significant additional power dissipation in the pass element. As a result, careful consideration must be given to the thermal environment of the IC in order to optimize efficiency and ensure that the LTC3119 is able to provide its full-rated output current. Specifically, the exposed die attach pad of both the QFN and TSSOP packages must be soldered to the PC board. The PC board should be designed to maximize the conduction of heat out of the IC package, utilizing multiple vias from the die attach pad connection to a large area of exposed copper. If the die temperature exceeds approximately 165°C, the IC will enter overtemperature shutdown and all switching will be inhibited. The part will remain disabled until the die cools by approximately 10°C. The soft-start circuit is re-initialized in over temperature shutdown to provide a smooth recovery when the fault condition is removed.

APPLICATIONS INFORMATION

V_{CC} Capacitor Selection

The V_{CC} output on the LTC3119 is generated from the input voltage by an internal low dropout regulator. The V_{CC} regulator has been designed for stable operation with a wide range of output capacitors. For most applications, a 4.7µF low ESR ceramic capacitor is a good choice. The capacitor should connect to the V_{CC} pin and ground through the shortest traces possible.

Bootstrapping the V_{CC} Regulator

For output voltages between 4.5V and 6V, the V_{CC} regulator can be held up using a diode from V_{OUT} to V_{CC} as shown in Figure 6. The appropriate diode should be selected to ensure that the output voltage, less the diode forward voltage, is within the acceptable external forcing voltage of 4.2V to 5.5V. This may be accomplished through the use of Schottky diodes or silicon diodes. In either case,

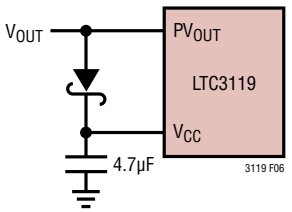


Figure 6. Bootstrapping V_{CC} to V_{OUT}

the diode should have sufficient current handling capability to drive the V_{CC} pin.

For applications that use an output voltage that is beyond the maximum ratings for the V_{CC} pin (i.e. V_{OUT} = 7V), a diode-OR can be used between the input voltage and output voltage to power the internal V_{CC} regulator. This is accomplished by tying the diode-OR node to the V_{IN} pin and connecting the PV_{IN} pins to the input source. In this configuration, an additional bypass capacitor is required

APPLICATIONS INFORMATION

between the V_{IN} pin and GND in addition to the bypass capacitor located between PV_{IN} and GND. This configuration is shown in Figure 7.

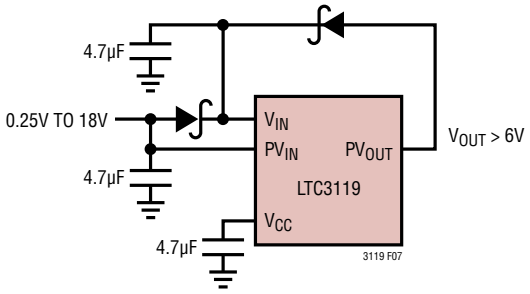


Figure 7. Diode-OR of Input Supply and V_{OUT} Powers V_{CC} Regulator

Programming Custom V_{IN} UVLO Thresholds

With the addition of an external resistive divider connected to V_{IN} as shown in Figure 8, the RUN pin can be used to program the input voltage at which the LTC3119 is enabled and disabled.

For a rising input voltage, the LTC3119 is enabled when V_{IN} reaches a threshold given by the following equation, where R1 and R2 are the values of the resistor divider resistors:

$$V_{TH(RISING)} = 1.205V\left(\frac{R1+R2}{R2}\right)$$

To ensure robust operation in the presence of noise, the RUN pin has two forms of hysteresis. A fixed 90mV hysteresis within the RUN pin comparator provides hysteresis equal to 7.5% of the input turn-on voltage independent of the resistor divider values. In addition, an internal hysteresis current that is sourced from the RUN pin during operation generates an additive level of hysteresis which can be programmed by the value of R1 to increase the overall hysteresis to suit the requirements of specific applications.

Once the IC is enabled, it will remain enabled until the input voltage drops below the comparator threshold by the hysteresis voltage, V_{HYST}, as given by the following equation where R1 and R2 are the values of the voltage divider:

$$V_{HYST} = R1 \bullet 0.25\mu A + \left(\frac{R1+R2}{R2}\right) \bullet 0.09V$$

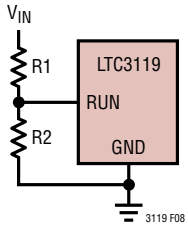


Figure 8. Setting the Input UVLO and Hysteresis

Therefore, the rising UVLO threshold and the amount of hysteresis can be independently programmed via appropriate selection of resistors R1 and R2. For high levels of hysteresis the value of R1 can become larger than is desirable in a practical implementation. In such cases, the amount of hysteresis can be increased further through the addition of an additional resistor R_H, as shown in Figure 9.

When using the additional R_H resistor, the rising RUN pin threshold remains as given by the original equation and the hysteresis is given by the following expression:

$$V_{HYST} = \left(\frac{R_H R2 + R_H R1 + R1R2}{R2}\right)0.25\mu A + \left(\frac{R1+R2}{R2}\right)0.09V$$

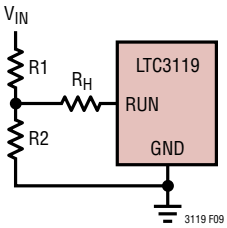


Figure 9. Increasing Input UVLO hysteresis

To improve the noise robustness and accuracy of the UVLO threshold, the RUN pin input can be filtered by adding a 470pF capacitor from RUN to GND. Larger valued capacitors should not be utilized because they could interfere with operation of the hysteresis.

Switching Frequency Selection

The switching frequency is set by the value of a resistor connected between the RT pin and ground. The switching frequency is related to the resistor value by the following equation where R_T is the resistance:

$$f_{SW} = \frac{100MHz}{8 + (1.2 \bullet R_T / k\Omega)}$$

APPLICATIONS INFORMATION

Higher switching frequencies facilitate the use of smaller inductors as well as smaller input and output filter capacitors which results in a smaller solution size and reduced component height. However, higher switching frequencies also generally reduce conversion efficiency due to the increased switching losses.

Output Capacitor Selection

A low ESR output capacitor should be utilized at the buck-boost converter output in order to minimize output voltage ripple. Multilayer ceramic capacitors are an excellent option as they have low ESR and are available in small footprints. The capacitor value should be chosen large enough to reduce the output voltage ripple to acceptable levels. Neglecting the capacitor ESR and ESL, the peak-to-peak output voltage ripple can be calculated by the following formulas, where f_{SW} is the switching frequency, C_{OUT} is the output capacitance, t_{LOW} is the switch pin minimum low time, and I_{LOAD} is the output current. Curves for the value of t_{LOW} as a function of V_{CC} voltage and temperature can be found in Typical Performance Characteristics section of this data sheet.

$$\Delta V_{P-P(BUCK)} \cong \frac{I_{LOAD} t_{LOW}}{C_{OUT}}$$

$$\Delta V_{P-P(BOOST)} \cong \frac{I_{LOAD}}{f_{SW} C_{OUT}} \left(\frac{V_{OUT} - V_{IN} + t_{LOW} f_{SW} V_{IN}}{V_{OUT}} \right)$$

The output voltage ripple increases with load current and is generally higher in boost mode than in buck mode. These expressions only take into account the output voltage ripple that results from the output current being discontinuous. They provide a good approximation to the ripple at any significant load current but underestimate the output voltage ripple at very light loads where output voltage ripple is dominated by the inductor current ripple.

In addition to output voltage ripple generated across the output capacitance, there is also output voltage ripple produced across the internal resistance of the output capacitor. The ESR-generated output voltage ripple is proportional to the series resistance of the output capacitor and is given by the following expressions where R_{ESR} is the series resistance of the output capacitor and all other terms are as previously defined.

$$\Delta V_{P-P(BUCK)} \cong \frac{I_{LOAD} R_{ESR}}{1 - t_{LOW} f_{SW}} \cong I_{LOAD} R_{ESR}$$

$$\Delta V_{P-P(BOOST)} \cong \frac{I_{LOAD} R_{ESR} V_{OUT}}{V_{IN}(1 - t_{LOW} f_{SW})} \cong I_{LOAD} R_{ESR} \left(\frac{V_{OUT}}{V_{IN}} \right)$$

Input Capacitor Selection

The PV_{IN} pin carries the full inductor current and provides power to internal control circuits in the IC. To minimize input voltage ripple and ensure proper operation of the IC, a low ESR bypass capacitor with a value of at least 10µF should be located as close to this pin as possible. The traces connecting this capacitor to PV_{IN} and the ground plane should be made as short as possible. The V_{IN} pin provides power to the V_{CC} regulator and other internal circuitry. If the PCB trace connecting V_{IN} to PV_{IN} is long, it may be necessary to add an additional small value bypass capacitor near the V_{IN} pin.

When powered through long leads or from a high ESR power source, a larger value bulk input capacitor may be required. In such applications, a 47µF to 100µF electrolytic capacitor in parallel with a 1µF ceramic capacitor generally yields a high performance, low cost solution.

When powered through an inductive connection such as a long cable, the inductance of the power source and the input bypass capacitor form a high-Q resonant LC filter. In such applications, hot-plugging into a powered source can lead to a significant voltage overshoot, even up to twice the nominal input source voltage. Care must be taken in such situations to ensure that the absolute maximum input voltage rating of the LTC3119 is not violated. See Linear Technology Application Note 88 for solutions to increase damping in the input filter and minimize this voltage overshoot.

Inductor Selection

The choice of inductor used in LTC3119 application circuits influences the maximum deliverable output current, the converter bandwidth, the magnitude of the inductor current ripple and the overall converter efficiency. The inductor must have a low DC series resistance, when compared to the

APPLICATIONS INFORMATION

internal switch resistance (30mΩ), or output current capability and efficiency will be compromised. Larger inductor values reduce inductor current ripple but may not increase output current capability as is the case with peak current mode control as described in the Maximum Output Current section. Larger value inductors also tend to have a higher DC series resistance for a given case size, which will have a negative impact on efficiency. Larger values of inductance will also lower the right half plane zero (RHPZ) frequency when operating in boost mode, which can compromise loop stability. Nearly all LTC3119 application circuits deliver the best performance with an inductor value between 1.5µH and 15µH. Buck mode only applications can use the larger inductor values as they are unaffected by the RHPZ, while mostly boost applications generally require inductance on the lower end of this range depending on how large the step-up ratio is. Regardless of inductor value, the saturation current rating should be selected such that it is greater than the worst case average inductor current plus half of the ripple current.

The peak-to-peak inductor current ripple for each operational mode can be calculated from the following formula, where f_{SW} is the programmed switching frequency, L is the inductance and t_{LOW} is the switch pin minimum low time, typically 90ns.

$$\Delta I_{L(P-P)(BUCK)} \cong \frac{V_{OUT}}{L}\left(\frac{V_{IN}-V_{OUT}}{V_{IN}}\right)\left(\frac{1}{f_{SW}}-t_{LOW}\right)$$

$$\Delta I_{L(P-P)(BOOST)} \cong \frac{V_{IN}}{L}\left(\frac{V_{OUT}-V_{IN}}{V_{OUT}}\right)\left(\frac{1}{f_{SW}}-t_{LOW}\right)$$

It should be noted that the worst-case peak-to-peak inductor ripple current occurs when the duty cycle in buck mode is minimum (highest V_{IN}) and in boost mode when the duty cycle is 50% ($V_{OUT} \cong 2 \bullet V_{IN}$).

As an example, if V_{IN} (minimum) = 2.5V and V_{IN} (maximum) = 15V, V_{OUT} = 5V, f_{SW} = 1MHz and L = 4.7µH, the peak-to-peak inductor ripples at the voltage extremes (15V V_{IN} for buck and 2.5V V_{IN} for boost) are:

$$\Delta I_{L(P-P)(BUCK)} \cong \frac{5}{4.7\mu H}\left(\frac{15-5}{15}\right) \bullet 910ns = 645mA$$

$$\Delta I_{L(P-P)(BOOST)} \cong \frac{2.5}{4.7\mu H}\left(\frac{5-2.5}{5}\right) \bullet 910ns = 242mA$$

One half of this inductor ripple current must be added to the highest expected average inductor current in order to select the proper saturation current rating for the inductor.

Programming the Output Voltage

The output voltage is set via the external resistive divider comprised of resistors R_{TOP} and R_{BOT} as shown in Figure 4. The resistor divider values determine the output regulation voltage according to:

$$V_{OUT} = 0.795V \bullet \left(1+\frac{R_{TOP}}{R_{BOT}}\right)$$

Programming the MPPC Voltage

The LTC3119 includes an MPPC function to optimize performance when operating from current limited input sources. Using an external voltage divider from V_{IN} (refer to Figure 5), the MPPC function takes control of the average inductor current when necessary to maintain a minimum input voltage V_{MPPC}, as programmed by the user.

$$V_{MPPC} = 0.798V \bullet \left(1+\frac{R5}{R6}\right)$$

This is useful for such applications as photovoltaic powered converters, since the maximum power transfer point occurs when the photovoltaic panel is operated at approximately 75% of its open-circuit voltage. For example, when operating from a photovoltaic panel with an open-circuit voltage of 10V, the maximum power transfer point will be when the panel is loaded such that its output voltage is about 7.5V.

When using the MPPC function, the input capacitor should be sized between 100µF and 470µF. Resistor R6 should be chosen between 50k and 250k. Lower values will result in smaller undershoot of the MPPC tracking point during line and load transient conditions, but will draw more current from the input supply. For this example, a value of 100k will be used.

$$R5 = \left(\frac{V_{MPPC}}{0.798V}-1\right) \bullet R6 = \left(\frac{7.5}{0.798}-1\right) \bullet 100k\Omega$$
$$= 838k\Omega \cong 845k\Omega$$

APPLICATIONS INFORMATION

Using these resistor values, the MPPC function is programmed to control the maximum input current so as to maintain V_{IN} at a minimum of 7.56V. Note that if the photovoltaic panel can provide more power than the LTC3119 can draw or the load requires, the input voltage will rise above the programmed MPPC point. Higher input voltages do not present a problem so long as the input voltage does not exceed the maximum operating input voltage. For photovoltaic panel applications, it may be also desirable to use the programmable RUN feature to disable the part when V_{IN} drops too low due to lack of sufficient light. Using the RUN pin provides a well controlled behavior when the input power source is dropping out. Preventing switching while under these conditions is important to minimize discharging of the output storage element due to switching while the input source is dropping out. This custom input UVLO voltage should be programmed to be below the MPPC tracking voltage with sufficient margin to ensure the part does not disable under transient conditions.

The MPPC loop requires compensation to maintain stability of the input voltage regulation loop. This can be accomplished by means of a pole-zero pair on the MPPC pin created with a series RC network in parallel with the lower MPPC resistor R6.

The pole and zero locations should be selected to create a low frequency pole at or below approximately 360Hz and a zero at a frequency that is scaled based on the size of the input capacitor. The equations for determining the values for the compensation capacitor CC2, and zero resistor RC2 are:

$$C_{C2} = \frac{1}{2\pi \bullet R_6 \bullet 360Hz}$$

$$R_{C2} = \frac{C_{IN}}{2\pi \bullet C_{C2}}$$

Using the divider values determined previously, and a 220µF input capacitor, the following compensation values are obtained:

$$C_{C2} = \frac{1}{2\pi \bullet 100k\Omega \bullet 360Hz} = 4.42nF \cong 4.7nF$$

$$R_{C2} = \frac{220\mu F}{2\pi \bullet 4.7nF} = 7.45k\Omega \cong 7.50k\Omega$$

Compensation of the Buck-Boost Converter

The LTC3119 incorporates an average current mode control architecture which consists of two control loops. Both the inner average current mode control loop and outer control loop require compensation to maintain stability. The inner current mode control loop is internally compensated to maintain wide bandwidth and good transient response. For many applications, the inner current loop can be treated like a voltage controlled current source (VCCS). This current source is commanded by the voltage error amplifier to regulate the output load formed primarily by the load resistance (R_{LOAD}) and output capacitor (C_{OUT}). This simplified version is illustrated in Figure 10, showing the key components that need to be considered when compensating the converter.

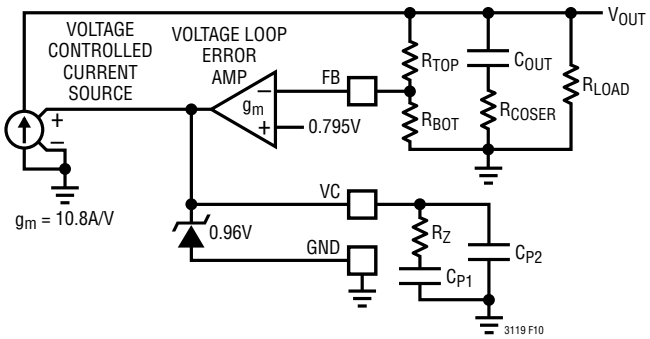


Figure 10. Simplified Representation of Control Loop Components

The bandwidth of the output voltage control loop should be set low enough to avoid the small signal effects of the inner current loop. The maximum loop bandwidth is determined using the inductor value to be approximately:

$$F_{VLOOP} \leq \frac{(4.7\mu H \bullet 100kHz)}{10 \bullet L}$$

With a full-scale command on VC, the LTC3119 buck-boost converter will generate an average inductor current of 8A. With a VC voltage range of 220mV to 960mV, the resulting current gain for the inner average current loop is 10.8A/V. Similar to peak current mode control, the inner average current mode control loop effectively turns the inductor into a current source over the frequency range of interest, resulting in a frequency response from the

APPLICATIONS INFORMATION

power stage that exhibits a single pole (–20dB/decade) roll off. The output capacitor (C_{OUT}) and load resistance (R_{LOAD}) form the normally dominant low frequency pole and the effective series resistance of the output capacitor and its capacitance form a zero, usually at a high enough frequency to be ignored. A potentially troublesome right half plane zero (RHPZ) is also encountered if the LTC3119 is operated in boost mode. The RHPZ causes an increase in gain, like a zero, but a decrease in phase, like a pole. This will ultimately limit the maximum converter bandwidth that can be achieved with the LTC3119. The RHPZ is not present when operating in buck mode. The overall open loop gain at DC is the product of the following terms:

Voltage Error Amplifier Gain:

$G_{EA} = g_m \bullet R_{EA} = 120\mu S \bullet 5M\Omega = 600$

Voltage Divider Gain:

$$\frac{V_{FB}}{V_{OUT}} = \frac{0.795V}{V_{OUT}}$$

Current Loop Transconductance:

$$G_{CS} = \frac{8A}{0.74V} = 10.8A/V$$

It is important to note that G_{CS} is the transconductance gain from the control voltage VC to the inductor current level, which equals the output current level in buck mode. In boost mode, the output current level will be reduced by the efficiency divided by the boost ratio. Refer to the typical curves for efficiency information.

$$G_{CS(OUT)} = 10.8A/V \quad \text{(Buck Mode)}$$

$$G_{CS(OUT)} = 10.8A/V \bullet \frac{V_{IN}}{V_{OUT}} \bullet Eff \quad \text{(Boost Mode)}$$

Frequency dependent terms that affect the loop gain include:

Output Load Pole (P1)

$$f_{P1} = \frac{1}{2\pi \bullet R_{LOAD} \bullet C_{OUT}}$$

Error Amplifier Compensation (P2, Z1)

$$f_{P2} = \frac{1}{2\pi \bullet R_{EA} C_{P1}} \text{ Hz (close to DC)}$$

$$f_{Z1} = \frac{1}{2\pi \bullet R_{ZCP1}} \text{ Hz}$$

Right Half Plane Zero (RHPZ)

$$f_{RHPZ} = \frac{V_{IN}^2 \bullet R_{LOAD}}{V_{OUT}^2 \bullet 2\pi \bullet L} \text{ Hz}$$

In some cases it may not be possible to achieve sufficient loop bandwidth and phase margin using a simple RC network connected to the V_C pin. In these cases, additional compensation may be required. This is accomplished by the addition of a feed forward RC network in parallel with the top resistor of the feedback divider. A small feed forward capacitor alone may be sufficient in some applications.

A common situation that may require a feed forward network is when the converter is operating in boost mode and the closed loop crossover frequency (f_{CC}) is close the Right Half Plane Zero (RHPZ). This may be done in order to reduce output capacitance requirements by increasing the loop bandwidth. Due to the phase additions of the RHPZ, a simple compensator on the V_C pin may not be able to provide sufficient phase boost to stabilize the loop.

Compensation Example

This section will demonstrate how to derive and select the compensation components for a 5V output supplying 2A from an input voltage as low as 3V. Designing compensation for most other applications is simply a matter of substituting in different values to the equations given in the example and reviewing the resulting Bode Plot, adjusting as needed. Since the compensation design procedure uses a simplified model of the LTC3119, results should be checked using time domain step response tests to validate the effectiveness of the compensation chosen. It is assumed that values and types for capacitors and the inductor will be selected based on the guidance given elsewhere in this data sheet. Particular attention should

APPLICATIONS INFORMATION

be paid to voltage biasing effects on capacitors used for input and output bypassing. Similarly, it is assumed that inductor values and current ratings are selected based on application requirements.

Example Operating Conditions:

$V_{IN} = 3V$ to $15V$

$V_{OUT} = 5V$

$I_{LOAD(MAX)} = 2A$

$C_{OUT} = 150\mu F$

$L = 3.3\mu H$

$f_{SW} = 1MHz$

First it is necessary to determine the lowest frequency for f_{RHPZ}. This will determine the maximum bandwidth that can safely be configured for the converter while operating in boost mode.

$$f_{RHPZ} = \frac{V_{IN}^2 \bullet R_{LOAD}}{V_{OUT}^2 \bullet 2\pi \bullet L} = 43.4kHz$$

In order to ensure sufficient safety margin, a closed loop crossover frequency (f_{CC}) should be sufficiently below the RHPZ frequency to account for variability of the internal components of the IC as well as variability of external influences on the converter response at the cost of possibly higher loop bandwidth. If sufficient phase margin exists at the crossover frequency, a higher loop bandwidth may be realizable while still maintaining stability and good transient response. In this example, we will use cross over frequency equal to one sixth of the RHPZ frequency.

$$f_{CC} = \frac{f_{RHPZ}}{6} \cong 7.24kHz$$

The RHPZ will have a negligible effect on the gain at the loop crossover, however it will have a phase contribution that must be considered.

$$\varphi_{RHPZ} = \tan^{-1}\left(\frac{fcc}{f_{RHPZ}}\right) = \tan^{-1}\left(\frac{1}{6}\right) = 9.5^{o}$$

Since the converter will be operating in boost mode, the G_{CS} term must be scaled to represent the commanded output current.

Looking in the Typical Curves section, we find the efficiency to be roughly 77%. Using this information, the effective output current gain can be calculated.

$$G_{CS(OUT)} = \left(G_{CS} \bullet \frac{V_{IN}}{V_{OUT}} \bullet Eff\right) = 4.99\,{}^{A}/_{V}$$

Using this information, the gain and phase contributions from the output filter are calculated.

$$G_{OUT} = G_{CS(OUT)} \bullet \sqrt{\frac{R_{LOAD}^2}{\left({}^{f_{CC}}/_{f_{P1}}\right)^2 + 1}} = 0.729$$

$$\varphi_{P1} = \tan^{-1}\left(\frac{fcc}{f_{P1}}\right) = \tan^{-1}\left(\frac{7240}{424}\right) = 86.5^{\circ}$$

Choosing a phase margin of 50 degrees, the required phase boost from the compensation network is determined by summing together the phase contributions that were calculated above. A phase contribution of 90° is assumed for P2.

$$\varphi_{Z1} = 50 + \varphi_{P2} + \varphi_{P1} + \varphi_{RHPZ} - 180 = 56^{\circ}$$

The compensation network gain is used to adjust the loop gain to crossover at the desired frequency. Using the feedback divider gain and output gain, the compensation network gain is calculated.

$$G_{COMP} = \left(\frac{V_{REF}}{V_{OUT}} \bullet G_{OUT}\right)^{-1} = 8.57$$

The compensation network resistor is then found using the error amplifier transconductance and the required compensation gain found above.

$$R_Z = \frac{G_{COMP}}{g_m} = \frac{8.57}{120\mu s} = 71.4k\Omega$$

APPLICATIONS INFORMATION

With the value of R_Z now known, the compensation capacitor can be chosen to place the zero Z1 in the correct location.

$$C_{P1} = \frac{\tan(\varphi_{Z1})}{2\pi \bullet f_{CC} \bullet R_Z} = 455pF$$

Selecting standard value components, values of R_Z = 71.5kΩ and C_{P1} = 470pF are used.

PCB Layout Considerations

The LTC3119 buck-boost converter switches large currents at high frequencies. Special attention should be paid to the PC board layout to ensure a stable, noise-free and efficient application circuit. Figures 11 and 12 show a representative PCB layout for each package option to outline some of the primary considerations. A few key guidelines are provided below:

1. The parasitic inductance and resistance of all circulating high current paths should be minimized. This can be accomplished by keeping the routes to all bold components in Figures 11 and 12 as short and as wide as possible. Capacitor ground connections should via down to the ground plane by way of the shortest route possible. The bypass capacitors on PV_{IN}, PV_{OUT} and V_{CC} should be placed as close to the IC as possible and should have the shortest possible paths to ground.
2. The exposed pad is the electrical ground connection for the LTC3119. Multiple vias should connect the back pad directly to the ground plane. In addition, maximization of the metallization connected to the back pad will improve the thermal environment and improve the power handling capabilities of the IC in both the FE and UFD packages.
3. There should be an uninterrupted ground plane under the entire converter in order to minimize the cross-sectional area of the high frequency current loops. This minimizes EMI and reduces the inductive drops in these loops thereby minimizing SW pin overshoot and ringing.
4. Connections to all of the components shown in bold should be made as wide as possible to reduce the series resistance. This will improve efficiency and maximize the output current capability of the buck-boost converter.
5. To prevent large circulating currents in the ground plane from disrupting operation of the LTC3119, all small-signal grounds should return directly to GND by way of a dedicated Kelvin route. This includes the ground connection for the RT pin resistor, and the ground connection for the feedback network as shown in Figures 11 and 12.
6. Keep the routes connecting to the high impedance, noise sensitive inputs FB and RT as short as possible to reduce noise pick-up.

APPLICATIONS INFORMATION

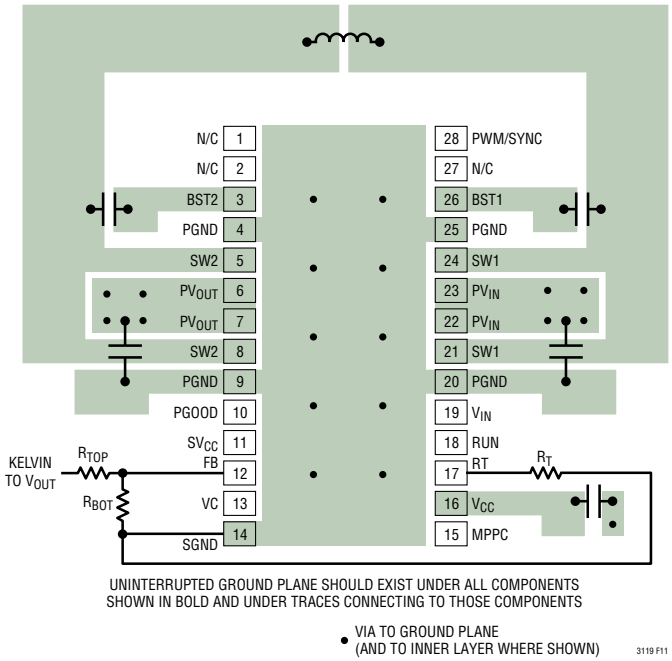


Figure 11. PCB Layout Recommended for the FE Package

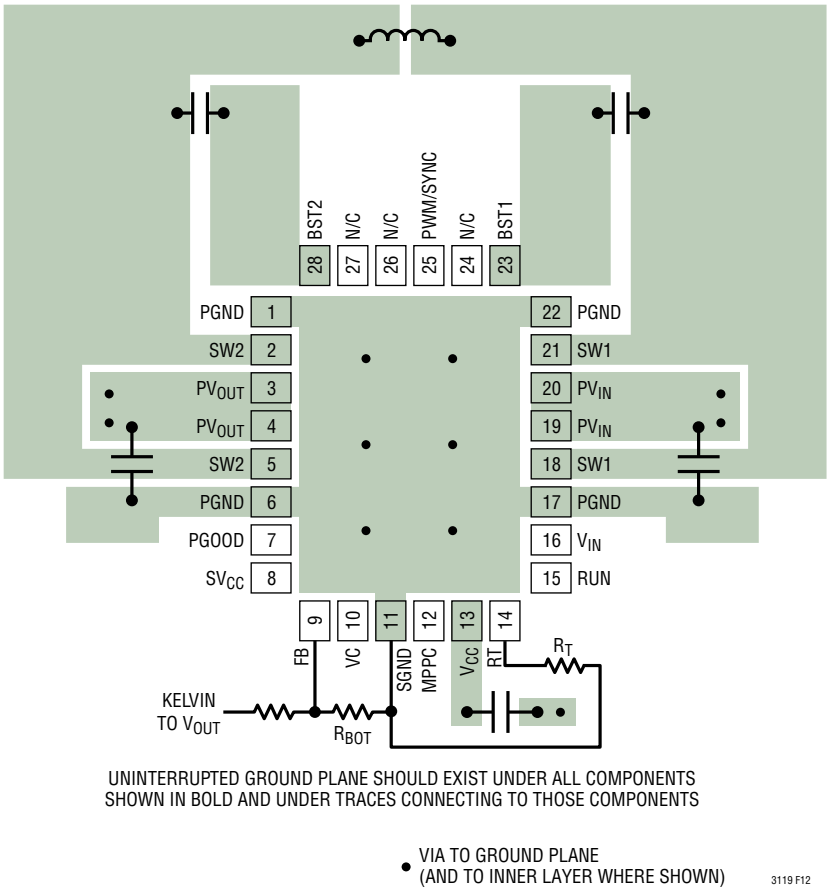
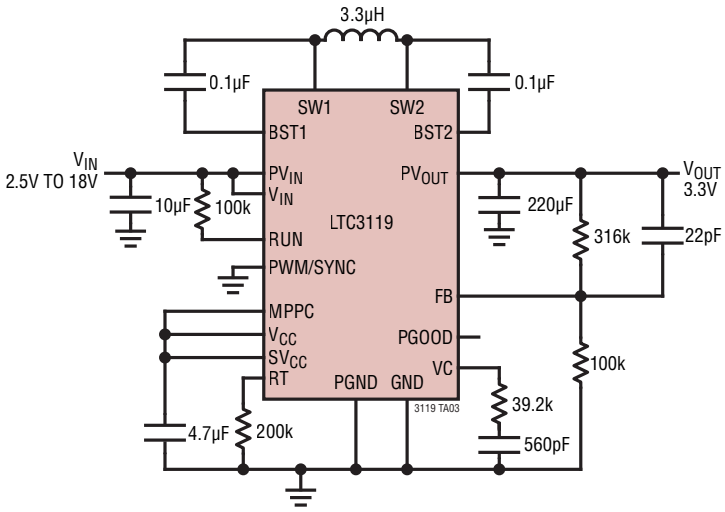


Figure 12. PCB Layout Recommended for the UFD Package

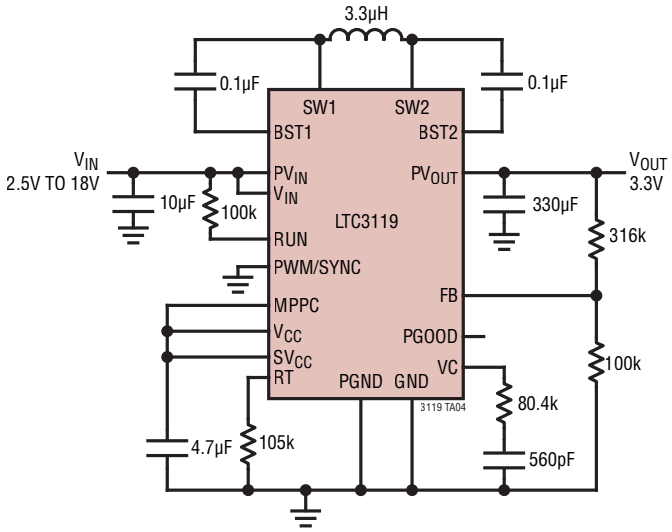
TYPICAL APPLICATIONS

3.3V, 400kHz Wide Input Regulator



V_{IN} = 2.5; I_{OUT} = 2.4A; EFFICIENCY = 78%
V_{IN} = 5.0; I_{OUT} = 5A; EFFICIENCY = 84%

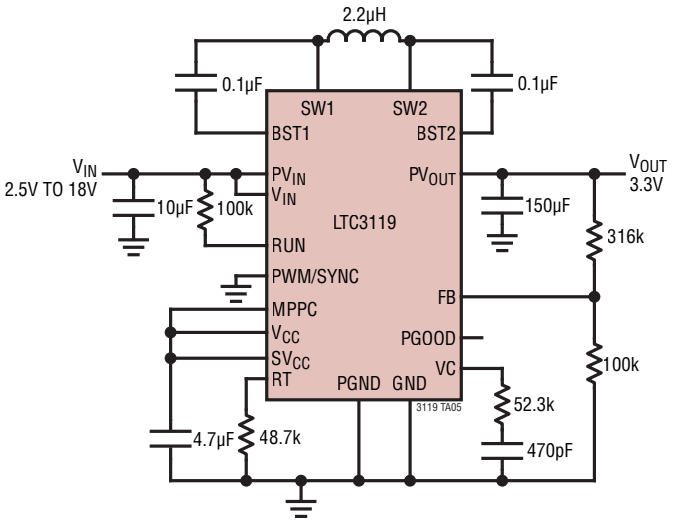
3.3V, 750kHz Wide Input Regulator



V_{IN} = 2.5; I_{OUT} = 2A; EFFICIENCY = 78%
V_{IN} = 5.0; I_{OUT} = 5A; EFFICIENCY = 82%

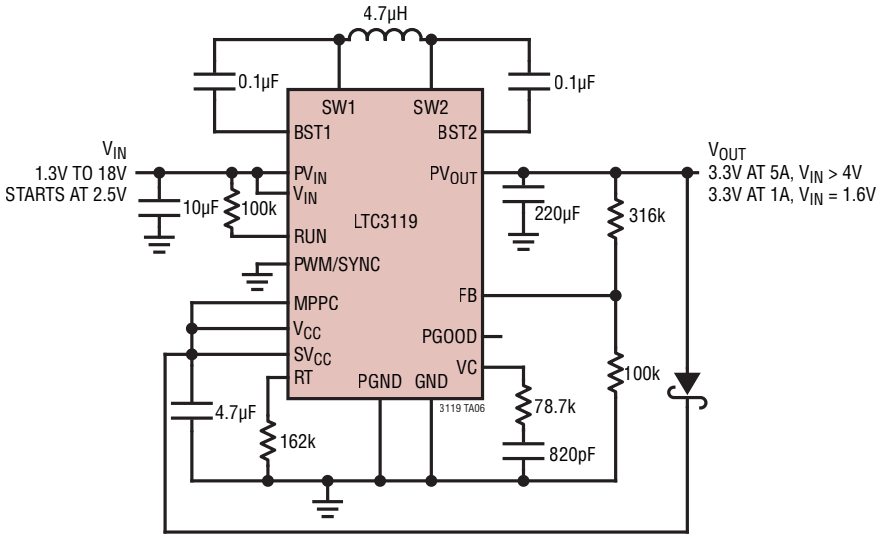
TYPICAL APPLICATIONS

3.3V, 1.5MHz Wide Input Regulator



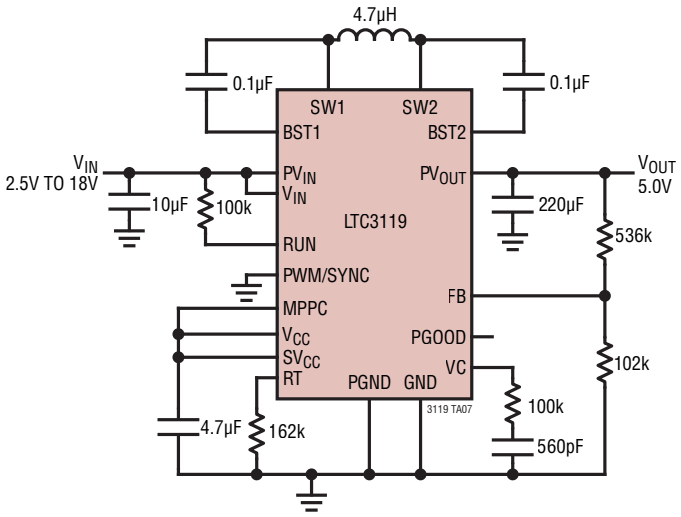
V_{IN} = 2.5; I_{OUT} = 1.75A; EFFICIENCY = 73%
V_{IN} = 5.0; I_{OUT} = 5A; EFFICIENCY = 80%

3.3V, 500kHz Wide Input Regulator



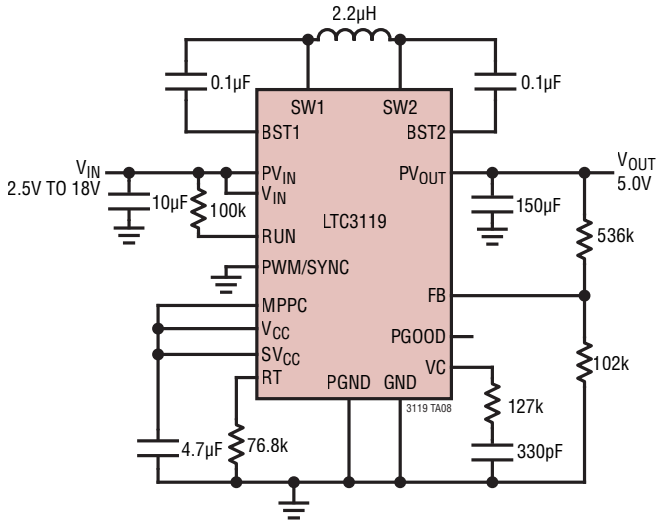
TYPICAL APPLICATIONS

5V, 500kHz Wide Input Regulator



V_{IN} = 2.5; I_{OUT} = 1.5A; EFFICIENCY = 78%
V_{IN} = 6.0; I_{OUT} = 5A; EFFICIENCY = 88%

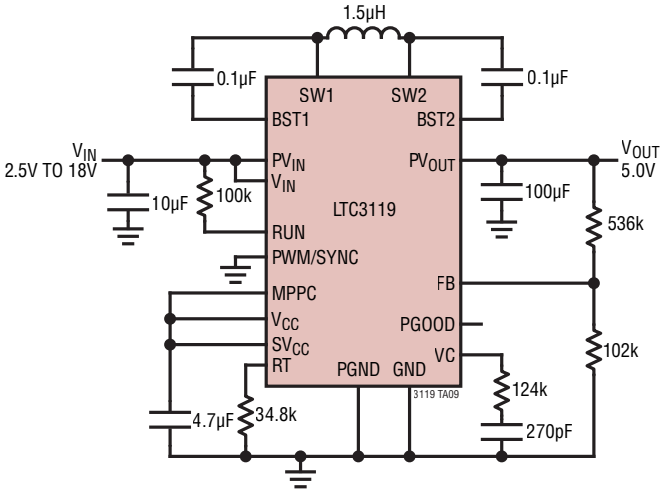
5V, 1MHz Wide Input Regulator



V_{IN} =2.5; I_{OUT} = 1.2A; EFFICIENCY = 73%
V_{IN} =6.0; I_{OUT} = 5A; EFFICIENCY = 83%

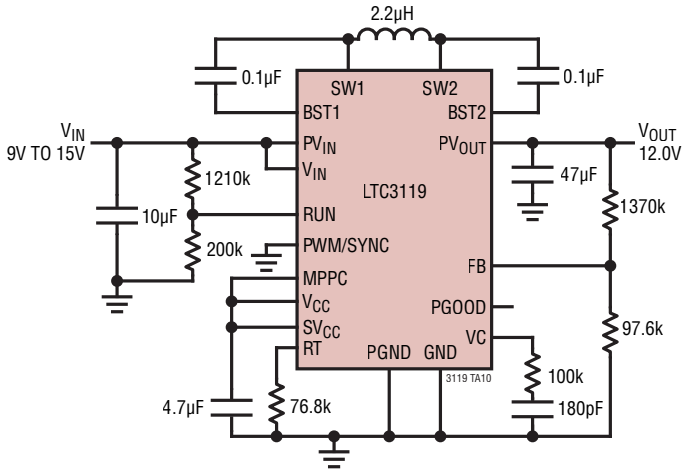
TYPICAL APPLICATIONS

5V, 2MHz Wide Input Regulator



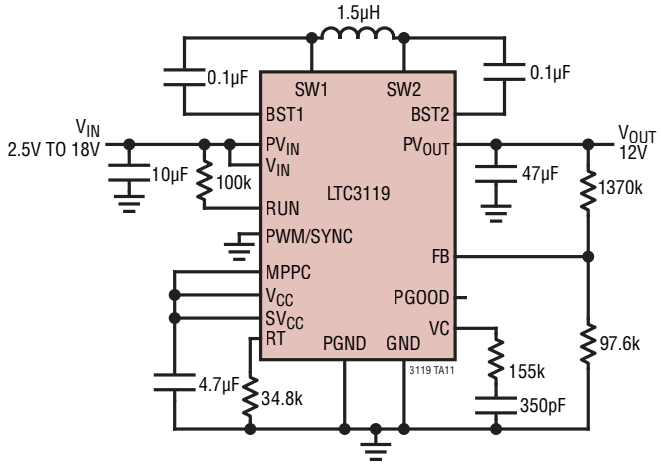
V_{IN} = 2.5; I_{OUT} = 1A; EFFICIENCY = 70%
V_{IN} = 6.0; I_{OUT} = 4.5A; EFFICIENCY = 80%

12V to 12V, 1MHz Line Conditioner with 8.5V Undervoltage Lockout Threshold

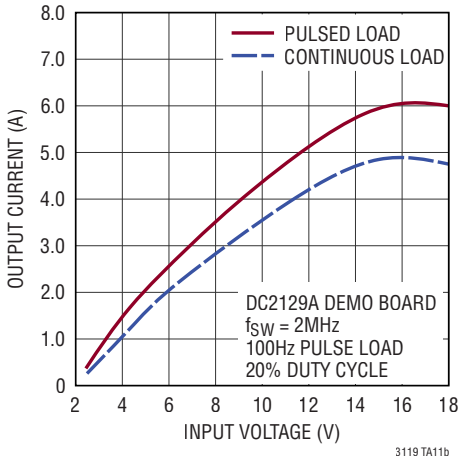


V_{IN} = 9; I_{OUT} =3A; EFFICIENCY = 92.5%
V_{IN} = 13; I_{OUT} =5A; EFFICIENCY = 93.5%
ENABLE AT V_{IN} > 8.5V

12V, 2MHz Wide Input Regulator

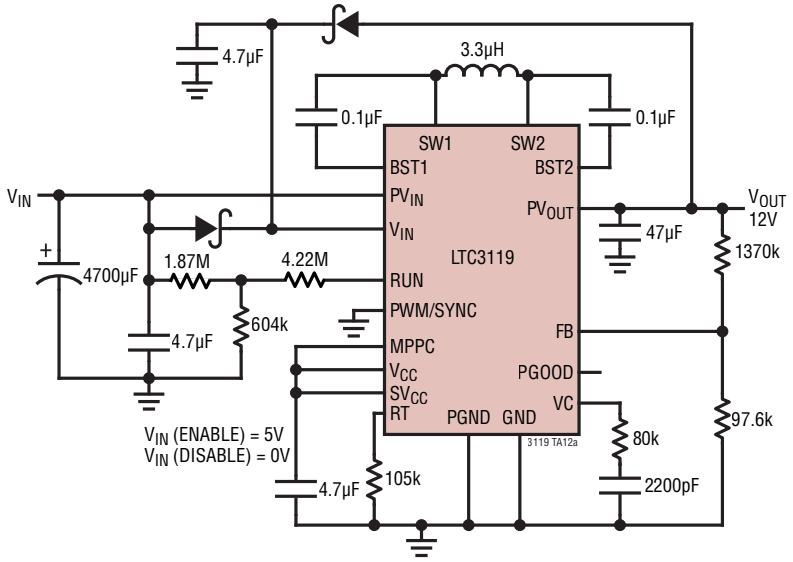


Maximum Output Current V_{OUT} = 12V

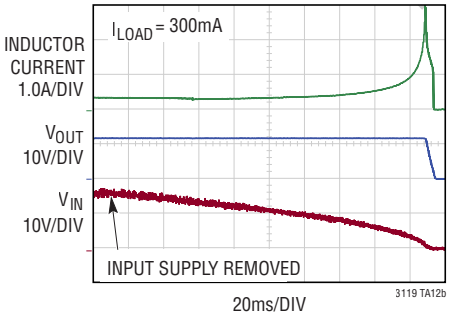


TYPICAL APPLICATIONS

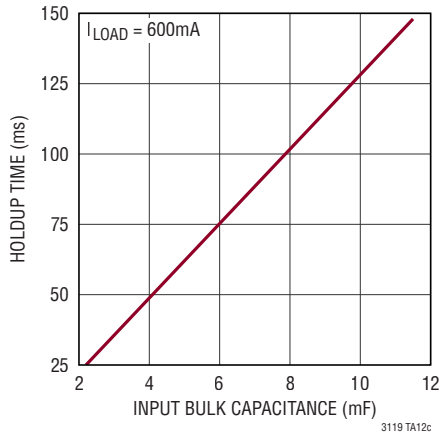
12V, 750kHz Regulator with Input Supply Rundown



Rundown Behavior After Input Disconnect

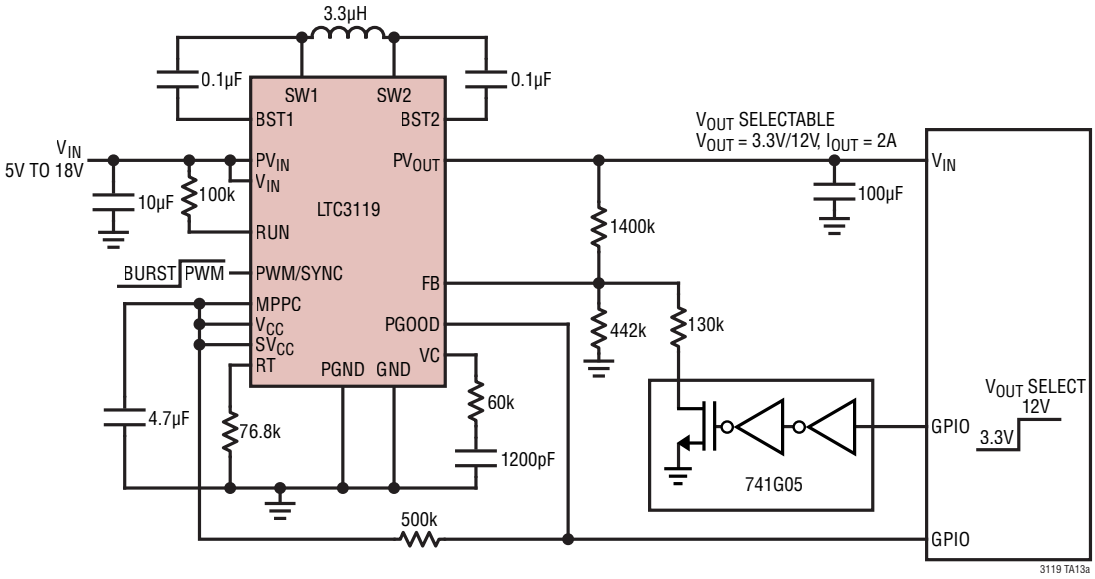


Output Holdup Time vs Input Bulk Capacitor Size

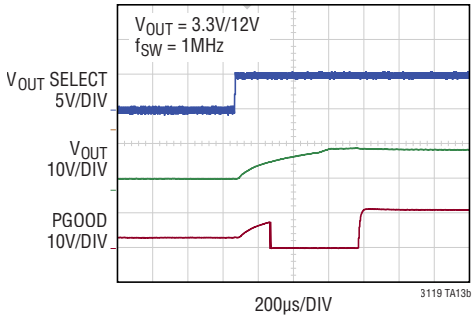


TYPICAL APPLICATIONS

Selectable 12V or 3.3V Output, 1MHz Regulator



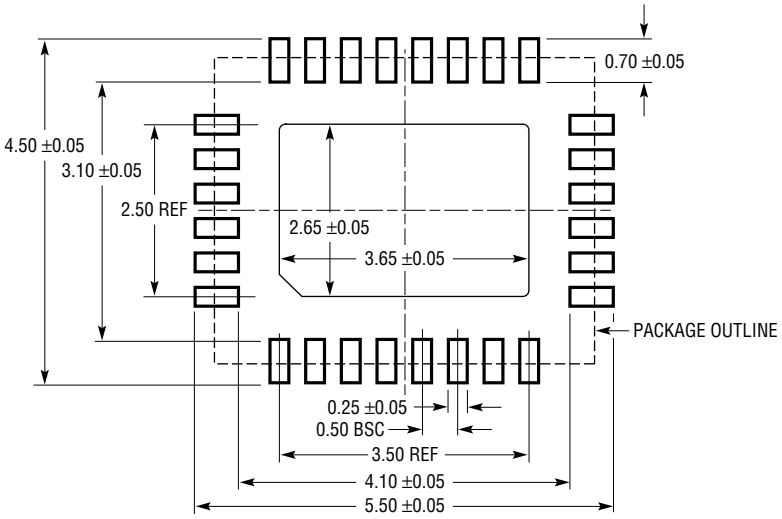
Output Voltage Transition
3.3V to 12V



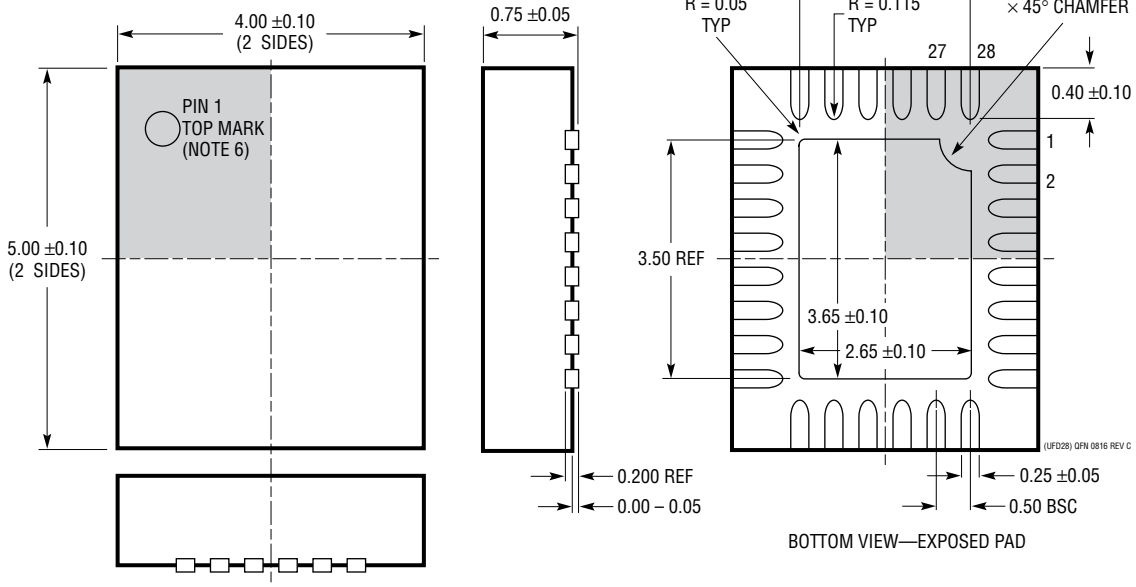
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3119#packaging for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



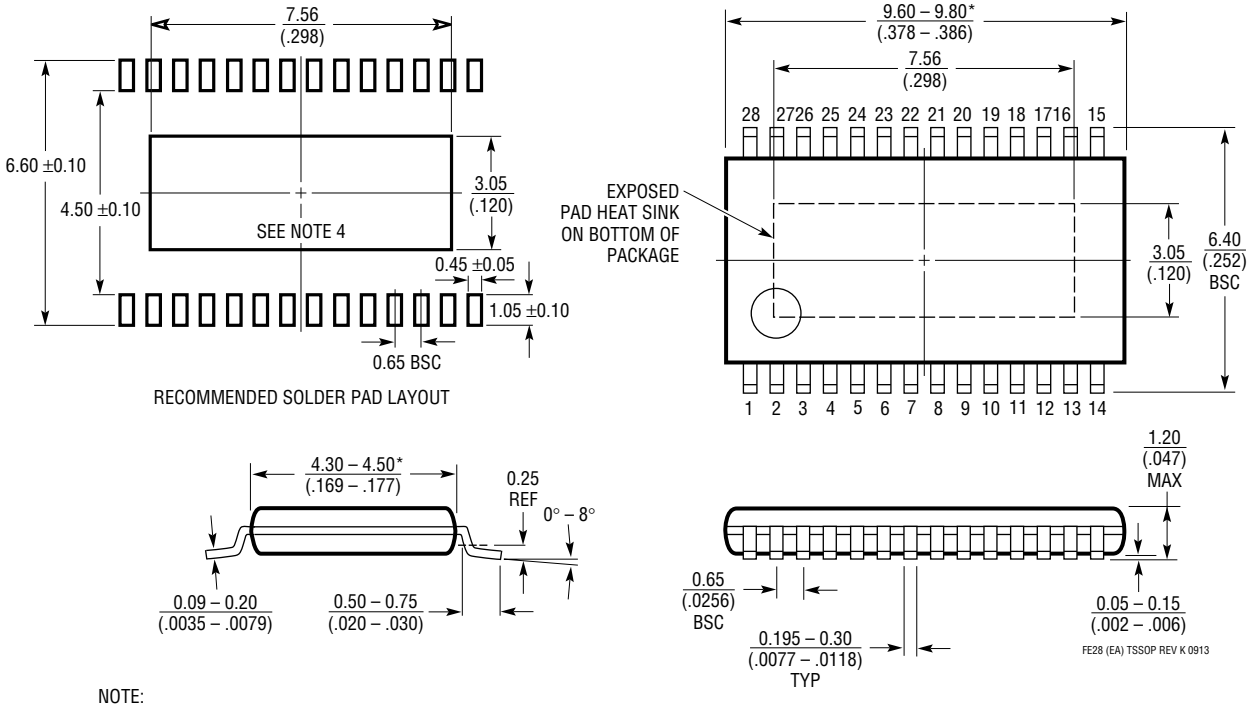
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGHD-3).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3119#packaging for the most recent package drawings.

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev K)
Exposed Pad Variation EA



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

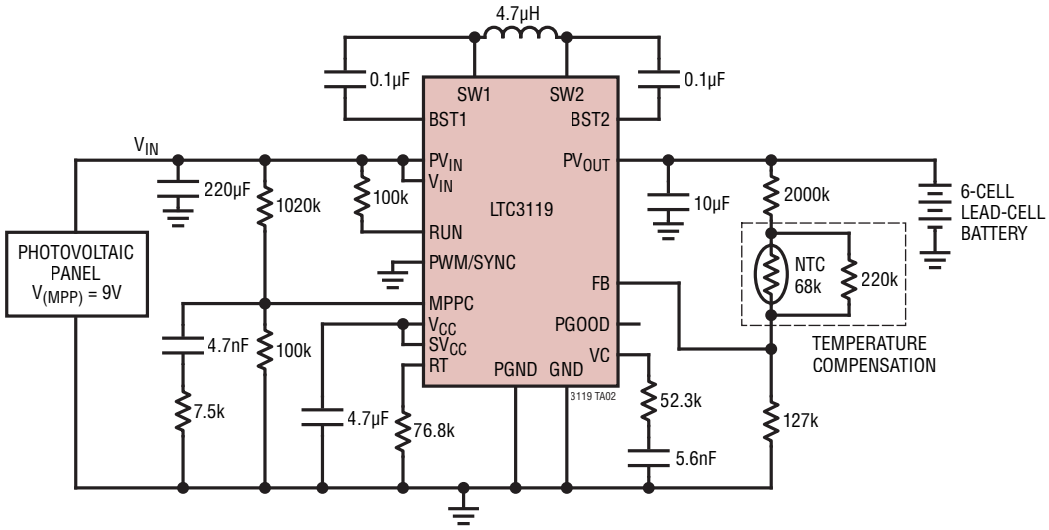
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	02/17	Added Maximum Output Current Curves	10, 11, 30
		Modified Schematic	32, 36
B	03/17	Modified BST2 pin description	12
		Output Capacitor Selection, changed switching frequency to V_{CC} voltage	20
		Modified Voltage Error Amplifier Gain equation	23

TYPICAL APPLICATION

Photovoltaic Panel Input Lead-Acid Charger with Temperature Correction (1MHz)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3113	5V, 3A Synchronous Buck-Boost	V_{IN} = 1.8V to 5.5V, V_{OUT} = 1.8V to 5.25V, I_Q = 30µA, I_{SD} < 1µA, DFN and TSSOP Packages
LTC3129/ LTC3129-1	15V, 200mA Synchronous Buck-Boost with 1.3µA I_Q	V_{IN} = 2.42V to 15V, V_{OUT} = 2.5V to 14V, I_Q = 1.3µA, I_{SD} = 10nA, QFN and MSOP Packages
LTC3112	15V, 2.5A Synchronous Buck-Boost	V_{IN} = 2.7V to 15V, V_{OUT} = 2.5V to 14V, I_Q = 40µA, I_{SD} < 1µA, DFN and TSSOP Packages
LTC3118	18V, 2A Dual Input PowerPath™ Buck-Boost Converter	V_{IN} = 2.2V to 18V, V_{OUT} = 2V to 14V, I_Q = 50µA, I_{SD} < 2µA, QFN and TSSOP Packages
LTC3130/ LTC3130-1	25V, 600mA Synchronous Buck-Boost Converter	V_{IN} = 2.4V to 25V, V_{OUT} = 1V to 25V, I_Q = 1.2µA, I_{SD} = 500nA QFN and MSOP Packages
LTC3114-1	40V, 1A Synchronous Buck-Boost	V_{IN} = 2.2V to 40V, V_{OUT} = 2.7V to 15V, I_Q = 30µA, I_{SD} < 3µA, DFN and TSSOP Packages
LTC3115-1/ LTC3115-2	40V, 2A Synchronous Buck-Boost	V_{IN} = 2.7V to 40V, V_{OUT} = 2.7V to 40V, I_Q = 30µA, I_{SD} < 3µA, DFN and TSSOP Packages
LTC3785	10V, High Efficiency, Synchronous, No R_{SENSE}™ Buck-Boost Controller	V_{IN} = 2.7V to 10V, V_{OUT} = 2.7V to 10V, I_Q = 86µA, I_{SD} < 15µA, QFN Package
LTC3789	38V, High Efficiency, Synchronous, 4-Switch Buck-Boost Controller	V_{IN} = 4V to 38V, V_{OUT} = 0.8V to 38V, I_Q = 3mA, I_{SD} < 60µA, SSOP-28, QFN-28 Packages
LT3790	60V, Synchronous, 4-Switch Buck-Boost Controller	V_{IN} = 4.7V to 60V, V_{OUT} = 1.2V to 60V, I_Q = 3mA, I_{SD} < 1µA, TSSOP Package

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